# Development of low-mass, high-density, hybrid for the silicon microstrip sensors in very high radiation environment

Y. Ikegami, T. Kohriki, S. Terada Y. Unno (KEK), K. Hara (Univ. of Tsukuba)
A. Clark, D. Ferrere, M. Weber, S. G. Sevilla (Univ. of Geneva)

## INTORDUCTION

Recent silicon microstrip detectors are designed to incorporate VLSI chips on the detector to readout the signals and to communicate with the outside data acquisition system. The hybrid, the base for the VLSI chips and related circuit components, is required to be low mass to reduce multiple coulomb scattering effects for precision tracking. The proposed silicon strip detector at the super LHC experiment includes a short strip silicon detector system in order to cope with the high track density. The system has about 10,000,000 readout channels. The thermal property of the hybrid is also a critical issue to efficiently dissipate the heat generated in the highly condensed readout chips and also in the silicon detector after receiving an enormous amount of radiation. We designed and fabricated a new hybrid, applying a technology of copper-polyimide flexible circuit board and carbon-carbon reinforce material which have been developed and adopted for the present LHC ATLAS silicon detector.

## CIRCUIT DIAGRAM OF THE HYBRID

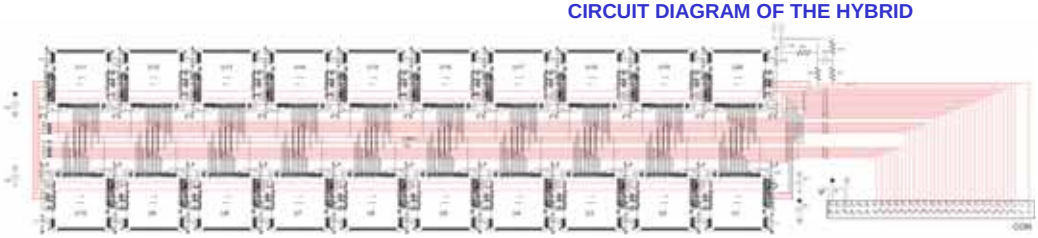


Fig.1: Circuit diagram of the hybrid.
The hybrid (dimensions: 136x28x0.165~0.260 mm) is loaded with 20 FE ASICs (ABCnext), each having 128 readout channels. This hybrid provides the full specifications operation of ABCnext chips, including the functions such as a redundancy operation and selection of various serial powering schemes.

## LAYOUT OF THE HYBRID LAYERS

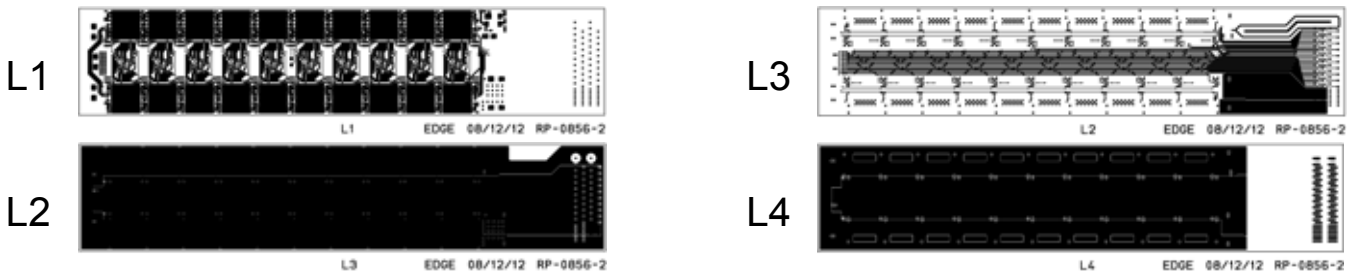
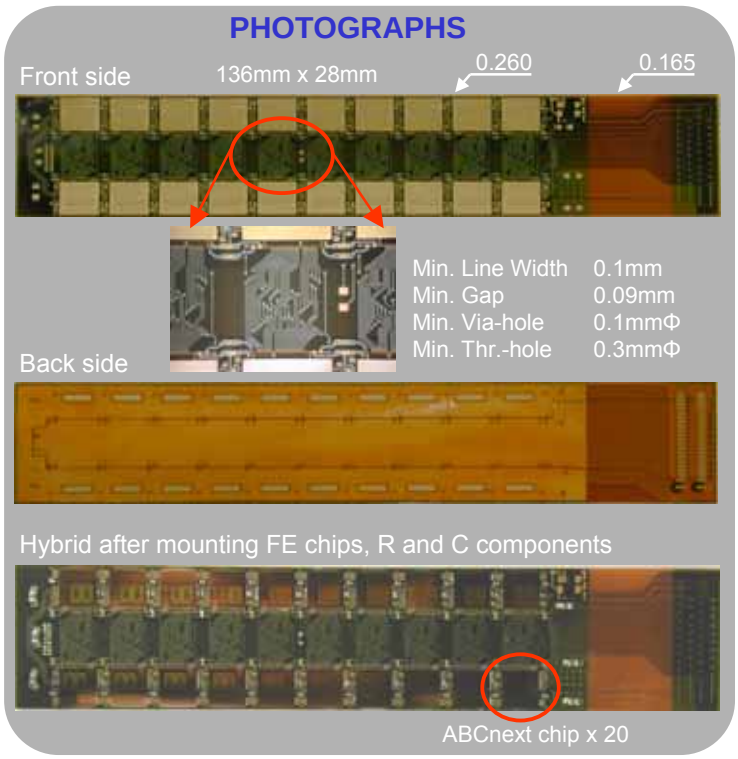



Fig.2: Layout of the hybrid layers.
The hybrid is composed of two double-sided flexible polyimide sheets, having four circuit layers, L1 to L4. The polyimide sheet is 25 μm thick having 12 μm thick laminated Cu on both surfaces. L1 includes the main circuit patterns for ASICs with redundancy lines incorporated in L2. L3 and L4 are mainly for the power distribution and grounding, respectively. The two layers on the same sheet are connectable by via-holes of 100 μm diameter. The two layers are inter-connectable by laser drilled through-holes of 300 μm diameter which are filled with Cu. A 0.8mm pitch miniature connector will be mounted at the right end.

## CONSTRUCTION

The total weight of bare FPC is 1.91g. The weight considerably decreased to 1.91g from 3.09g by pads-only plating, also called button plating or spot plating, limiting an area of the via- and through-hole plating. The hybrid backed with a 400 mm thick and 110 mm wide carbon-carbon sheet is designed to bridge over the silicon sensor avoiding any interference to the sensor surface. The carbon-carbon bridge having large heat conductivity of 1,400 W/mK transfers the generated heat to the heat sink located at the legs of the bridge. The total weight (excluding electrical components) is 4.25 g, having 0.00425 X0 equivalent radiation lengths.

## PHOTOGRAPHS




## Electrical Tests Results

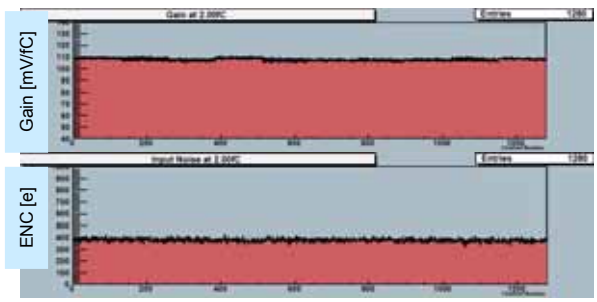



Fig. 3. Gain and ENC uniformity.
Fig. 3 shows the distribution of gain and Equivalent Noise Charge (ENC) for 10 ASIC chips (=1280 channels =one link). The average gain is about 110mV/fC and the average ENC is about 390e. Quite uniform distributions were obtained.

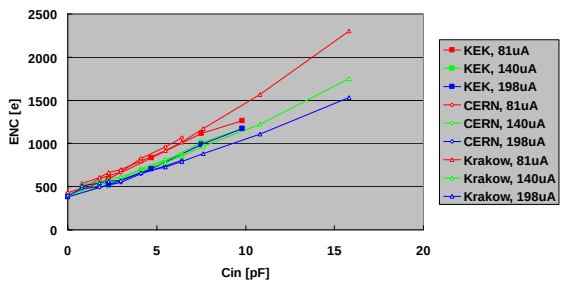



Fig. 4. ENC vs. input capacitance.
In order to investigate a change of ENC with a detector capacitance, we connected external capacitances with the input of amplifiers, and measured ENC. The current of the first stage of amplifier was changed into 81 (red),140 (green) and198uA (blue). ENC measurements were performed at three sites independently and the results were in agreement. The detector capacitance is between 2.5 and 10pF, according to the distance from the colliding point.

## Summary

We have fabricated a low-mass, high-density, hybrid which provides the full functionality of the ABCnext full chips. The electrical tests on the hybrid level are completed mostly. The module tests are planned to start soon.