Master thesis

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Active Pixel Sensors based on High Voltage CMOS Technology

- Laboratory Characterization -

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Abstract

Active Pixel Sensors based on High-Voltage Complementary Metal Oxide Semiconductor Technology – Laboratory Characterization –

The luminosity of the LHC will be increased during the Long Shutdown of 2022 and 2023 (LS3) in order to increase the sensitivity of its experiments. A completely new inner detector for the ATLAS experiment needs to be developed to cope with the extremely harsh environment of the upgraded LHC, called High Luminosity-LHC (HL-LHC). In HL-LHC, assuming a bunch spacing of 25 ns, about 140 proton-proton interactions per bunch crossing are expected, as well as fluences in the innermost layers of the tracker detector beyond $10^{16} \, \mathrm{n_{eq}/cm^2}$ [1]. Therefore, radiation hardness, low occupancy and excellent performance in high pile-up environment are mandatory requirements.

A new silicon detector concept which uses commercial high voltage and full CMOS processes as active sensor for pixel and strip layers has garnered high attention, as it provides high radiation hardness and at the same time a reduced price due to the commercial processing.

Laboratory characterization results, including tuning procedures, temperature dependency, and parameter studies are presented.

Keywords: pixel detector, particle physics, silicon detector, HV-CMOS, CCPD.



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Introduction

1.1 Context

1.1.1 High energy physics

At the European Organization for Nuclear Research (CERN), physicists are probing the fundamental structure of the universe. Protons and nuclei are made to collide with each other at close to the speed of light. The collisions give the physicists clues about how the particles interact, and provide insight into the fundamental laws of nature. The instruments used at CERN are purpose-built particle accelerators and detectors. Accelerators boost beams of particles to high energies before the beams are made to collide with each other or with stationary targets. Detectors observe and record the traces of these collisions. Founded in 1954, the CERN laboratory sits on the Franco-Swiss border near Geneva.

Since the 1970s, particle physicists have described the fundamental structure of matter using a series of equations called the Standard Model. The model describes how phenomenon we observe in the universe is made from a few basic "elements" called fundamental particles. Physicists at CERN use powerful particle accelerators and detectors to test the predictions and limits of the Standard Model. Over the years they explained many experimental results and precisely predicted a range of phenomena, such that today the standard model is considered a well-tested physics theory. This model, however, only describes 4% of the known universe, does not take into account the gravity force, and questions remain unresolved. Will we see a unification of forces at the high energies of the Large Hadron Collider (LHC)? Why is gravity so weak? Why is there more matter than antimatter in the universe? Is there new physics waiting to be discovered at higher energies? Will we discover evidence for a theory called supersymmetry at the LHC? [2].

1.1.2 ATLAS experiment

ATLAS (A Toroidal LHC ApparatuS) is one of the two general-purpose detectors at the LHC. It investigates a wide range of physics, from the search for the Higgs boson to extra dimensions and particles that could make up dark matter. Although it has the same scientific goals as the CMS experiment, it uses different concept for particle measurement and a different magnet-system design.

Beams of particles from the LHC collide at the centre of the ATLAS detector making collision debris in the form of new particles, which fly out from the collision point in all directions. Different detecting subsystems arranged in layers around the collision point record the paths, momentum, and energy of the particles, allowing them to be individually identified. A huge magnet system bends the paths of charged particles so that their momenta can be measured. The interactions in the ATLAS detectors create an enormous flow of data. To select the data, ATLAS uses an advanced "trigger" system to tell the detector which events to record and which to ignore. The designed collision rate is typically around 40Mhz, which means 1 billion collisions per second (assuming 25 proton-proton interactions per bunch crossing), and so the timing of detectors is a very important factor. Complex data-acquisition and computing systems are then used to analyse the recorded collision events. With 46 metres long, 25 metres high and 25 metres wide, the 7000-tonne ATLAS detector is one of the largest volume particle detector ever constructed. It sits in a cavern 100 metres below ground near the main CERN site, close to the village of Meyrin in Switzerland. More than 3000 scientists from 174 institutes in 38 countries work on the ATLAS experiment (February 2012). The figure 1.1 shows a 3D view of the entire ATLAS detector, [2].

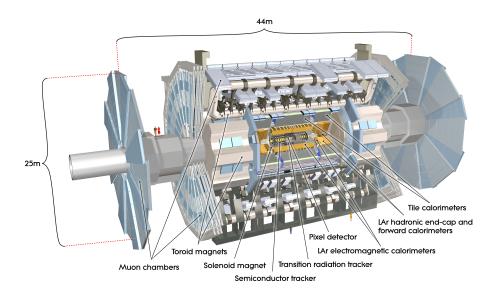


Figure 1.1: Computer generated image of the ATLAS detector. Picture taken from [2].

The ATLAS detector consists of four major components which are described below.

1.1.2.1 Magnet system

The ATLAS detector uses two large superconducting magnet systems (inner solenoid magnet and outer toroidal magnets) to bend charged particles so that their momenta can be measured. High-momentum charged particles curve very little, while low-momentum particles curve significantly. The amount of curvature can be measured and the particle momentum can be determined from this value.

The inner solenoid produces a two Tesla magnetic field surrounding the inner detector. This high magnetic field even allows very energetic particles to curve enough for their momentum to be determined, and its nearly uniform direction and strength allow measurements to be made very precisely.

The outer toroidal magnetic field is produced by eight very large air-core superconducting barrel and two end-cap air toroidal magnets, all situated outside the calorimeters and within the muon system.

1.1.2.2 Muon spectrometer

Muons are charged leptons like electrons, but 200 times heavier. They are the only detectable particles that can go through all the calorimeter absorbers without being stopped. The muon spectrometer surrounds the calorimeter and measures muon paths to determine their momenta with high precision. It consists of thousands of charged particle sensors placed in the magnetic field produced by large superconducting toroidal coils.

1.1.2.3 Calorimeters

There are two types of calorimeters: electromagnetic and hadronic. Electromagnetic calorimeters measure the energies of electrons and photons while hadronic calorimeters the energy of hadrons. They consist of metal plates (absorbers) and sensing elements. Interactions in the absorbers transform the incident energy into a "shower" of particles that are detected by the sensing elements. In the inner sections of the calorimeter, the sensing element is liquid argon. The showers ionize the argon and create an electron and an ion that are collected and recorded. The collection time of ions is very high compared to electrons, therefore electrons contribute mostly to the charge collection. In the outer sections, the sensors are tiles of scintillating plastic. The showers cause the plastic to emit light which is detected and recorded.

1.1.2.4 Inner detector

The last subsystem of ATLAS is the inner detector. Because the present master thesis is about silicon chips used in the inner detector, a more detailed description is given in the next subsection.

1.1.2.5 Particle detection overview

An overview of different particle detections (muons, protons, neutrons, electrons, and photons) in the ATLAS detector is shown on figure 1.2. The view is a slice in the middle of ATLAS detector, and is perpendicular to the beam direction.

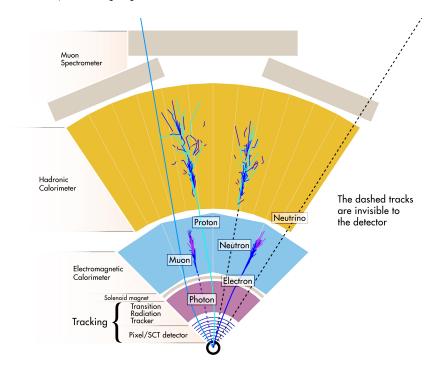


Figure 1.2: Particle detection through different ATLAS sub-detectors. The muon spectrometer is colored in grey, the hadronic calorimeter in orange, the electromagnetic calorimeter in blue and the Transition Radiation Tracker (TRT) in purple. Pixel/Semiconductor Tracker (SCT) detectors are situated very close to the beam and are represented by blue lines. Picture taken from [2].

1.1.3 Inner detector

The ATLAS inner detector combines high-resolution detectors at the inner radii with continuous tracking elements at the outer radii, all contained in the Central Solenoid, which provides a nominal field of 2 T. A 3D view is shown on figure 1.3a. Three main parts can be distinguished:

- Transition Radiation Tracker (TRT)
- Semiconductor Tracker (SCT)
- Pixel detectors

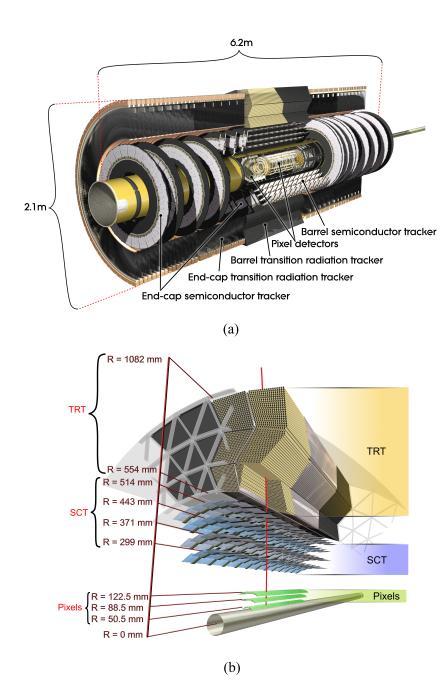


Figure 1.3: Computer generated images of the inner detectors. (a) Barrel and end-caps, (b) zoom of the barrel. Pictures taken from [2].

The highest granularity is achieved around the vertex region using semiconductor pixel detectors followed by a silicon microstrip detector. The outer radius of the inner detector is 1.15 metres, and the total length 7 metres. In the barrel region the high-precision detectors are arranged in concentric cylinders around the beam axis, while the

end-cap detectors are mounted on disks perpendicular to the beam axis. All end-cap tracking elements are located in disks perpendicular to the beam direction.

1.2 Purpose of this study

This present master thesis is part of the HV-CMOS research and development (R&D) project led in the ATLAS group, Nuclear and Particle Physics department (DPNC) of the University of Geneva.

The luminosity of the LHC will be increased during the Long Shutdown of 2022 and 2023 (LS3) in order to increase the sensitivity of its experiments. A completely new inner detector for the ATLAS experiment needs to be developed to cope with the extremely harsh environment of the upgraded LHC, called High Luminosity-LHC (HL-LHC). Assuming a bunch spacing of 25 nanoseconds, about 140 proton-proton interactions (pileup) per bunch crossing are expected (compared to the 27 measured on the $7^{\rm th}$ June, 2015). The innermost sub-detectors (Pixel Detector, Semiconductor Tracker and TRT) will face fluences beyond $10^{16}~\rm n_{eq}/cm^2$ [1], so that radiation hardness, low occupancy and excellent performance in high pile-up environment are mandatory requirements.

The main purpose of this work consists in characterizing a new silicon detector concept which has recently attracted attention because of its reduced price due to a commercial processing and a alternative gluing method. This silicon detector concerns the ATLAS inner detector and more precisely the pixel layers, see figure 1.3b.

Laboratory characterization results, including tuning procedure, temperature dependency, and parameter studies are presented here.

Theoretical background

2.1 Semiconductor basics

Semiconductors are materials with special electrical properties widely used nowadays and are the foundation of modern electronic components such as transistors, diodes, etc... A semiconductor material has an electrical conductivity between that of a conductor and an insulator. Silicon and germanium are the most commonly used elements in the preparation of semiconducting materials.

The electrical conductivity of a semiconductor increases when the temperature is raised, which is a behavior opposite to that of a metal. Semiconductor devices can display a range of useful properties such as passing current more easily in one direction than the other (diode), showing variable resistance, and sensitivity to light or heat. Because the electrical properties of semiconductors can be modified by controlled addition of impurities, or by the application of electrical fields or light, devices made from semiconductors can be used for amplification, switching, and energy conversion.

The transport of current in a semiconductor occurs through the movement of free electrons (negative) and holes ("positive"), known as charge carriers. Adding impurities to a semiconducting material, known as "doping", changes the number of avalanche charge carriers while keeping it neutral. When a doped semiconductor contains mostly free holes it is called p-type, and when it contains mostly free electrons it is known as n-type. The semiconductor materials used in electronic devices are doped under precise conditions to control the concentration and regions of p-type and n-type dopants. A single semiconductor crystal can have many p- and n-type regions; the P-N junctions between these regions are responsible for the electronic behavior of the crystal, which can be used for several useful applications.

In order to introduce semiconductor detectors, a quick look at basic and general theories behind them is necessary. Because this report does not have the ambition to give a detailed explanation of those theories, only brief explanations are presented below. This section is mainly derived from W.A. Harrison's and D.A. Neamon's books, [3][4].

2.1.1 Band theory

In solid-state physics, band theory describes ranges of energy that an electron within the solid may have (energy bands) and ranges of energy that it may not have (called band gaps). Band theory highlights these bands and band gaps by examining the allowed quantum mechanical wave functions for an electron in a large, periodic lattice of atoms, in other words a crystal.

In the case of an isolated atom (figure 2.1a), energy of electrons has only discrete and well-determined values (atomic orbitals). Now, if we combine this atom with another one (figure 2.1b), their outer electrons probability densities overlap to form a molecular orbital; in this way the outer electrons of both atoms have permitted energy bands slightly shifted due to Pauli exclusion principle. If we continue this exercise with a large number of atoms (solid), a band structure appears as shown on figure 2.1c. The Fermi level E_f describes the top of the collection of electron energy levels at absolute zero temperature. This concept comes from Fermi-Dirac statistics. Electrons are fermions and by the Pauli exclusion principle cannot exist in identical energy states. So at absolute zero temperature they pack into the lowest available energy states and build up a "Fermi sea" of electron energy states. The Fermi level is the highest possible energy occupied by those electrons.

Electrons from the valence band contribute to the local cohesion of the solid and so cannot participate to the electrical conduction. Only electrons of the conduction band are not localized and so contribute to the conduction phenomena. A schematic representation of valence and conduction bands for different material is shown in figure 2.2. For a metal, the conduction and valence band overlap, for a insulator, the band gap is so large that the conversion of a valence electron to a conduction electron is very hard.

Finally, the case of a semiconductor is in between a metal and a insulator. For an intrinsic semiconductor the band gap is very small. For a n-type semiconductor (negatively doped), the Fermi level is shifted to a higher value, this is due to the fact that we add electrons to the solid, so logically the Fermi level gets higher. Conversely, the Fermi level of a p-type semiconductor (positively doped) decreases.

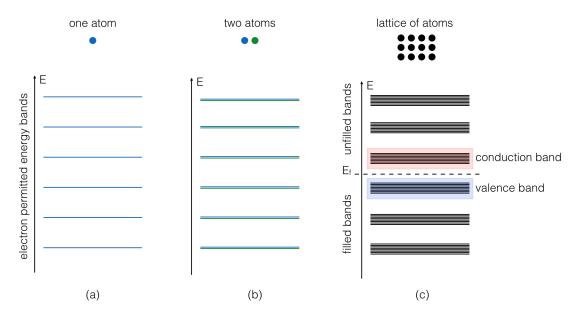


Figure 2.1: Schematic representation of band structures. (a) one atom, (b) two atoms joined (c) lattice of atoms, in other words a solid. Here, the vertical axis represents the energy of electrons, while E_f is the Fermi level.

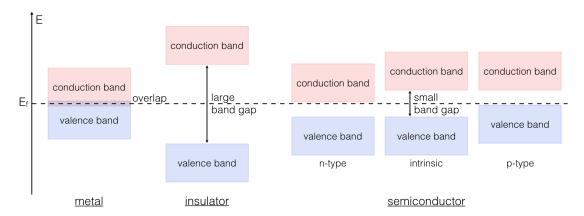


Figure 2.2: Schematic representation of valence and conduction bands for metals, insulators, and different types of semiconductor.

The real electrical interest of semiconductors occurs when two semiconductors of different doping (n-type and p-type for example) are joined together. The junction between those different semiconductors is called the "P-N junction".

2.1.2 P-N junction

A P-N junction is defined as the interface between two types of semiconductor material, p-type and n-type, inside a single crystal of semiconductor. The P-N junction has interesting properties that have useful applications in modern electronics.

To understand the particular feature of the P-N junction, we must consider two mechanisms that create an electric current: diffusion and drift.

Diffusion mechanism One way to understand the diffusion mechanism is to imagine two sets of different colored particles concentrated in two distinct zones. Particles are free to moves in all directions. Their random motion tends to equalize their concentration in the whole volume. Diffusion is the physical mechanism which gives rise to free particles trying to occupy the maximum possible volume.

Drift mechanism The drift mechanism is a movement caused by an electric field (Lorentz's force). This electric field makes the holes ("positive" charge carriers) moves in one direction and the electrons (negative charge carriers) in the other. If there is an electric field in a region of space, there will be an electrical potential associated with it. The potential decreases in the direction in which the electric field points.

After joining p-type and n-type semiconductors, electrons from the n-region near the P-N interface tend to diffuse into the p-region. As electrons diffuse, they leave positively charged ions (donors) in the n-region. Likewise, holes from the p-type region near the P-N interface begin to diffuse into the n-type region, leaving fixed ions (acceptors) with negative charge. The region nearby the P-N interfaces loses its neutrality and become charged, forming the space charge region (or depletion region). An electric field is created inside this depletion region and its associated potential acts like a barrier, preventing the diffusion process for both electrons and holes, see figure 2.3. Equilibrium is reached when the diffusion current equals the drift current.

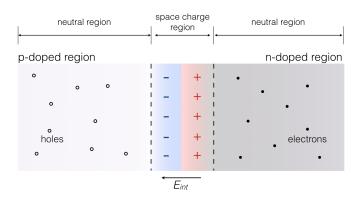


Figure 2.3: Schematic representation of a P-N junction at equilibrium with zero-bias voltage applied. \vec{E}_{int} is the intrinsic electric field.

P-N junctions are commonly used as diodes: circuit elements that allow an electric current in one direction but not in the other. Bias is the application of a voltage (forward or reverse) across a P-N junction.

2.1.3 Forward and reverse bias

2.1.3.1 Forward bias

Connecting the p-type region to a positive voltage, and the n-type to negative voltage is called forward biasing. With a voltage connected this way, the holes in the p-type region and the electrons in the n-type region are pushed toward the junction. This reduces the width of the depletion zone and so the electrical potential is reduced. A reduced potential cannot prevent electrons and holes from diffusing across the structure, see figure 2.4.

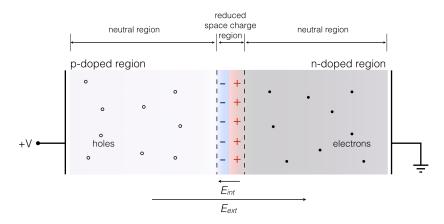


Figure 2.4: Schematic representation of a P-N junction with a forward bias voltage applied. \vec{E}_{int} is the intrinsic electric field while \vec{E}_{ext} is the applied external electric field.

The positive potential applied to the p-type material repels the holes, while the negative potential applied to the n-type material repels the electrons. With increasing forward bias voltage, the depletion zone eventually becomes thin enough that the potential associated to the intrinsic electric field cannot counteract charge carrier motion across the P-N junction. An electric current appears in the junction due to the diffusion mechanism.

2.1.3.2 Reverse bias

Connecting the p-type region to a negative voltage, and the n-type to positive voltage is called reverse biasing. With a voltage connected this way, the direction of the external electric field applied is inverted with respect to the forward bias. In this way, the holes in the p-type region and the electrons in the n-type region are pushed pulled away from the junction. Therefore, the depletion region widens, and does so increasingly with

increasing reverse-bias voltage. The electric potential increases causing a high resistance to the flow of charge carriers, thus allowing minimal electric current to cross the junction. This results in the junction behaving as an insulator.

The strength of the depletion zone electric field increases as the reverse-bias voltage increases. Once the electric field intensity increases beyond a critical level, the P-N junction depletion zone breaks down and current begins to flow, usually by either the Zener or the avalanche breakdown processes. Both of these breakdown processes are non-destructive and are reversible, as long as the amount of current flowing does not reach levels that cause the semiconductor material to overheat and cause thermal damage.

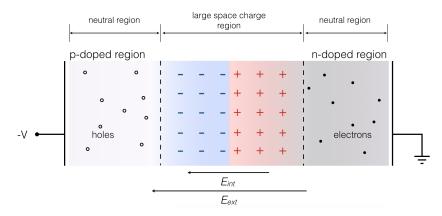


Figure 2.5: Schematic representation of a P-N junction with a reverse bias voltage applied. \vec{E}_{int} is the intrinsic electric field while \vec{E}_{ext} is the external electric field applied.

2.1.4 Carrier generation and recombination

Carrier generation and recombination are processes by which mobile charge carriers (electrons and holes) are created and eliminated. The electron-hole pair is the fundamental unit of generation and recombination, corresponding to an electron transitioning between the valence band and the conduction band.

Carrier generation Carrier generation occurs when an electron from the valence band absorbs enough energy (radiations, electrical/thermal energy, electron collision, etc...) to move to the conduction band.

Recombination Any electron which exists in the conduction band is in a meta-stable state and will eventually stabilize to a lower energy position in the valence band. When this occurs, it must move into an empty valence band state. Therefore, when the electron stabilizes back down into the valence band, it also effectively removes a hole. This process is called recombination. There are three basic types of recombination in the bulk of a single-crystal semiconductor: radiative recombination, Auger recombination, and Shockley-Read-Hall recombination.

2.2 Semiconductor detectors

A semiconductor detector is a device that uses a semiconductor material to measure the effect of incident particles or photons.

Ionizing particles produce free electrons and holes inside the depletion zone. The number of electron-hole pairs is proportional to the energy of the particle. Under the influence of the external electric field, electrons and holes travel to the electrodes, where they result in a pulse that can be measured in an outer circuit, as described by the Shockley-Ramo theorem [5]. As the amount of energy required to create an electron-hole pair is known, and is independent of the energy of the incident radiation, measuring the number of electron-hole pairs allows the intensity of the incident radiation to be determined [4]. A schematic representation of a semiconductor detector is shown in figure 2.6.

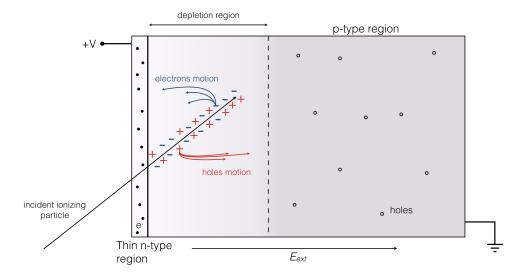


Figure 2.6: Schematic representation of a semiconductor detector with a reverse bias voltage applied.

The energy required to produce electron-hole-pairs is very low compared to the energy required to produce paired ions in a gas detector. Consequently, in semiconductor detectors the statistical variation of the pulse height is smaller and the energy resolution is higher. As the electrons travel fast, the time resolution is also very good, and is dependent upon rise time.

2.2.1 Energy deposition in matter

Fast charged particles moving through matter interact with electrons and atoms in the material. This leads to an energy loss of the traveling particle. The mean rate of

energy loss by moderately relativistic (0.1 $\lesssim \beta \gamma \lesssim 1000$) charged heavy particles is welldescribed by the Bethe formula [6]:

$$-\left\langle \frac{dE}{dx} \right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta \gamma^2 T_{\text{max}}}{I^2} - \beta - \frac{\delta(\beta \gamma)}{2} \right]$$
 (2.1)

with the quantities: $K = 4\pi N_A r_e^2 m_e c^2 = 0.307074 \,\text{MeV} \,\text{mol}^{-1} \,\text{cm}^2$ T_{max} is the maximum energy transfer in a single collision. $T_{\text{max}} = \frac{2m_e c^2 \beta \gamma^2}{\left(1 + 2\gamma \frac{m_e}{M} + \left(\frac{m_e}{M}\right)^2\right)}$

z: charge of incident particle

M: mass of incident particle

Z: charge number of medium

A: atomic mass of medium

I: mean excitation energy of medium δ : density correction

 N_A : Avogadro's number

 r_e : classical electron radius

 m_e : electron mass

 $\beta = \frac{v}{c}$: relativistic velocity $\gamma = \frac{1}{\sqrt{1 - \frac{v^2}{c^2}}}$: Lorentz factor

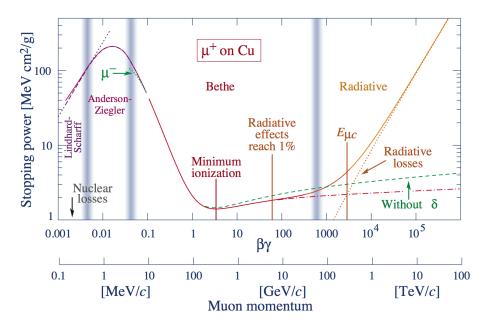


Figure 2.7: Stopping power $\left(-\left\langle \frac{dE}{dx}\right\rangle\right)$ for positive muons in copper as function of $\beta\gamma$ $(=\frac{p}{Mc})$. The solid curve indicates the total stopping power. Graphic taken from [6].

The statistical nature of the ionizing process during the crossing of a fast charge particle through matter results in a large fluctuations of the energy loss (Δ) in absorber. The number of electron-hole pairs (J) is related to Δ by the expression $J = \Delta/P$, where P is the energy to create an electron-hole pair, for the silicon equals to $\sim 3.6\,\mathrm{eV}$. The probability function $f(\Delta)$ is usually called energy loss distribution or straggling function. The straggling function in silicon for 500 MeV pions and the most probable energy loss in silicon are shown in figure 2.8.

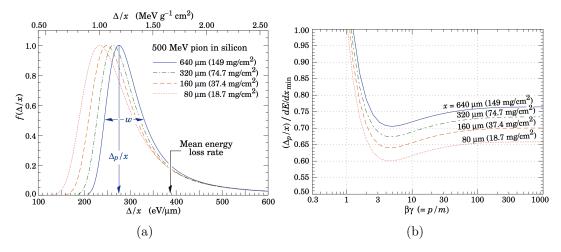


Figure 2.8: (a) Straggling functions in silicon for 500 MeV pions, normalized to unity at the most probable value Δ_p/x . The width w is the full width at half maximum. (b) Most probable energy loss in silicon, scaled to the mean loss of a minimum ionizing particle, $388 \text{ eV}/\mu\text{m}$ (1.66 MeV g⁻¹ cm²). Graphics taken from [6].

The sensor design needs to make sure to detect the Minimum Ionizing Particle (MIP) with a significant signal/noise ratio. The mean loss of a minimum ionizing particle in silicon is $388\,\text{eV}/\mu\text{m}$. J then equals to $388/3.6 \simeq 108$ electron-hole pairs per μm . For a silicon detector with a depletion of 10 μm the signal amplitude (in term of generated electrons) of the mean loss of a MIP is approximately 1000 electrons. However, some caution needs to be taken because according to [7], the Landau distribution fails at some point to describe energy loss in very thin absorbers such as silicon detectors. In the scope of this project, however, the description given by the Landau distribution is good enough to have a global comprehension of the system. In the case of thin silicon layers ($< 50\,\mu\text{m}$), it is common to assume that a MIP generates 80 electrons/ μ m.

2.2.2 Shockley-Ramo theorem

The Shockley–Ramo theorem allows the instantaneous electric current induced by a charge moving nearby an electrode to be calculated. It is based on the fact that the current induced in the electrode is due to the instantaneous change of electrostatic flux lines which end on the electrode. We first consider the general situation described by the figure 2.9.

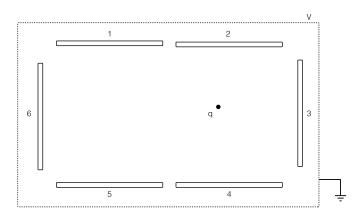


Figure 2.9: Electrodes are numbered from 1 to 6, q is the charge at an initial position $\vec{x_0}$. V is a very large volume which includes the system.

 $\phi(\vec{x})$ is the potential induced by the charge q, where all electrodes are connected to the ground $(U_i = 0)$.

 $\phi_i(\vec{x})$ is the potential induced by the electrode *i* with a voltage U_i applied, while others equal zero.

The boundary conditions are set as:

$$\begin{cases} \phi_i(x) = U_i & \text{on the surface of i} \\ \phi_i(x) = 0 & \text{on the surface of V} \\ \phi(x) = 0 & \text{on the surface of V} \end{cases}$$
(2.2)

The Gauss law equation for the electric field is:

$$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\varepsilon_0} \tag{2.3}$$

where ρ is the electric charge density, \vec{E} the electric field, ε_0 the permittivity of free space, and $\vec{\nabla}$ is the nabla operator.

The relation between the electric field and its potential is given by:

$$\vec{E} = -\vec{\nabla}\phi \tag{2.4}$$

Replacing \vec{E} in (2.3) by (2.4), we obtain :

$$\begin{cases} \Delta \phi_i(x) = 0\\ \Delta \phi(x) = -q \frac{1}{\varepsilon_0} \delta(\vec{x_0}) \end{cases}$$
 (2.5)

where Δ is the Laplace operator.

The Gauss theorem gives:

$$\oint_{S(V)} \vec{E} \cdot \vec{n} \, d\sigma = \int_{V} \vec{\nabla} \cdot \vec{E} \, d^{3}x = \frac{1}{\varepsilon_{0}} \int_{V} \rho \, d^{3}x$$
 (2.6)

where V is a volume containing charge density ρ and S(V) is the surface of V. The Green's second formula, for all functions ϕ and ψ , is:

$$\int_{V} (\phi \Delta \psi - \psi \Delta \phi) d^{3}x = \oint_{S(V)} \left(\phi \left(\vec{\nabla} \psi \cdot \vec{n} \right) - \psi \left(\vec{\nabla} \phi \cdot \vec{n} \right) \right) d\sigma$$
 (2.7)

Starting with (2.5) and using (2.6) and (2.7) we obtain the Shockley-Ramo's formula for a general case:

$$I_i(t) = -\frac{q}{U_i} \vec{E}_i \left(\vec{x_o}(t) \right) \cdot \vec{v}(t)$$
(2.8)

 $I_i(t)$ is the induced current in the electrode i as a function of time, $\vec{v}(t)$ is the drift velocity of the charge q, keeping in mind that $v_h \ll v_e$.

We apply now the Shockley-Ramo's formula to a simplified detector in which a single electron has been ionized, as shown on figure 2.10.

The electric field is $\vec{E}(x) = \frac{U}{d}\vec{e_x}$, the velocity of q is $v(t) = \mu E$ and the Shockley-Ramo's formula gives (on the anode) $I(t) = -\frac{q}{U}E(x)v_{drift}(t)$. The induced current on the cathode is given by $I_{cathode}(t) = -I_{anode}(t)$.

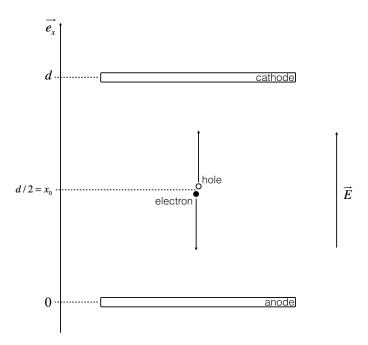


Figure 2.10: Schematic repressation of a simplified detector. x_0 is the initial position of the electron-hole pair. We assume here that holes behave the same way as an ions.

The time can be divided in four parts: before the ionization (t < 0), during the drift mechanism of the electron $(0 < t < t_e)$, during the drift mechanism of the hole $(t_e < t < t_h)$ after the charge collection $(t_h < t)$. The induced charge is given by $Q(t) = \int_0^t I(t') dt'$.

We can now compute the induced current and induced charge in the different time intervals:

$$\begin{cases} t < 0: & I(t) = 0 \\ 0 < t < t_e: & I(t) = -\frac{q}{d}(v_e + v_h) & Q(t) = -\frac{q}{d}(v_e + v_h)t \\ t_e < t < t_h: & I(t) = -\frac{q}{d}v_h & Q(t) = -\frac{q}{d}v_ht + x_0 \\ t_h < t: & I(t) = 0 & Q(t) = -\frac{q}{d}(d - x_0 + x_0) = -q \end{cases}$$

$$(2.9)$$

The induced current and charge given in equations 2.9 are plotted in the figure 2.11.

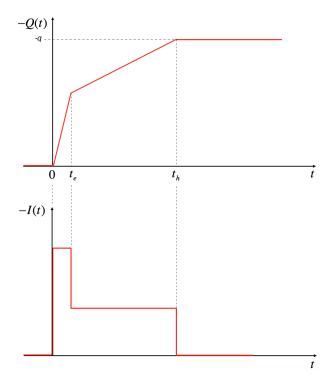


Figure 2.11: Induced charge and induced current in function of time.

2.2.3 Other characteristics

2.2.3.1 Leakage current

When operating a semiconductor detector in reverse bias, the current measured between the two doped regions is never perfectly equal to zero (leakage). The leakage current of a semiconductor device is a phenomenon where an electron in the valence band moves to the conduction band. This phenomenon is mostly due to thermal effects. The leakage current decreases as temperature decreases. Radiation damages to the silicon material also increase the leakage current (see section 2.2.3.3).

2.2.3.2 Breakdown voltage

When a reverse voltage applied to a semiconductor device is high enough, a phenomenon called "breakdown" occurs. The free electrons move fast enough due to strong drift mechanism and ionize other electrons in the silicon, creating more free electron-hole pairs, then the device become suddenly electrically conductive. This mechanism is called avalanche breakdown, and is the main contribution for silicon detectors. No signal from a ionizing particle can be measured in these conditions. A semiconductor detector is generally operated at a voltage level just below this breakdown voltage in order to maximize the depletion region, keeping the current as low as possible. Another breakdown type is the Zener effect. A sufficiently strong electric field enables tunneling of electrons from the valence to the conduction band leading to a large number of free charge carriers. This sudden generation of carriers rapidly increases the reverse current and gives rise to a breakdown.

2.2.3.3 Radiation damage

Very high levels of radiation are produced in the LHC experimental underground areas and in the accelerator tunnel during operations. Environments with high levels of ionizing radiation create special design challenges for physicists. High energy radiations and particles can introduce operation errors and even permanent damages to the semiconductor devices.

Radiation damage in silicon detectors can roughly be divided in surface and bulk damage. The bulk damage is the limiting factor for the use of silicon detectors in the intense radiation fields close to the interaction point of high energy physics experiments. The bulk damage produced in silicon particle detectors by hadrons (neutrons, protons, pions and others) or higher energetic leptons is caused primarily by displacing a primary knock on atom (PKA) out of its lattice site resulting in a silicon interstitial and a loft over vacancy (Frenkel pair) as shown on figure 2.12. Both can migrate through the lattice and may finally form point defects with impurity atoms being resident in the silicon. Ionization losses do not lead to any changes in the silicon lattice. The surface damage is not the limiting factor for silicon detectors but few precautions are needed in the detector design. The term surface damage summarizes all defects in the overlaid dielectrics, i.e. the silicon oxide, and the interface between the silicon and the dielectric. The surface damage affects interface properties and can increase the noise in electronics. A way to avoid surface damage is to create a specific detector design, for example the transistors with enclosed gate [8].

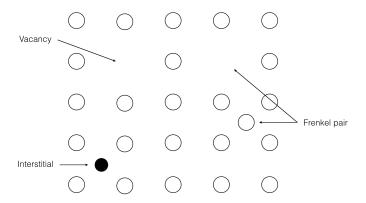


Figure 2.12: Schematic illustration of defects in a mono-atomic solid.

On a macroscopic scale, damage in solid state detectors causes:

- An increase of a leakage current translating into an increase in noise. Defects with deep energy levels in the middle of the forbidden gap act as recombination/generation centers and are hence responsible for an increase of the leakage current.
- A change in material resistivity. The removal of dopants by formation of complex defects as well as the generation of charged centers changes the effective doping concentration.
- The reduction in the amount of collected charge. The trapping mechanism of charge carriers is due to the different time constants of the electron capture and emission processes. Traps are mostly unoccupied in the depletion region due to the lack of free charge carriers and can hold or trap parts of the signal charge for a longer time than the charge collection time and so the signal height is reduced.

Technology description

3.1 HV-CMOS technology

The high-voltage CMOS (Complementary Metal Oxide Semiconductor) technologies are originally used to design the electronic chips that drive automotive or industrial devices by means of high-voltage signals. The high-voltage technologies allow combination of the standard low-voltage CMOS transistors, used to implement internal electronics of the chip, and the high-voltage devices used in output drivers. In order to ease the interface between the low-voltage and the high-voltage circuits, most of the commercial high-voltage technologies offer the so-called "floating logic". The basic idea for a monolithic detector in high-voltage technology is to use the floating logic structure to implement a pixel detector for high-energy particles with 100% fill-factor. The first introduction of HV-CMOS technology for particle physics detection is described in Ivan Peric's paper [9]. A simplified cross section of an HV-CMOS sensor (also referred as "capacitively coupled pixel detector" (CCPD)) is shown in figure 3.1.

Due to the full CMOS functionality, the sensor could integrate the full analog readout logic, such as an Charge Sensitive Amplifier (CSA) and discriminator. It could then take benefit of interconnection to a dedicated, purely digital readout chip. The possibility of analog as well as simple digital readout logic inside the sensor layer has the potential to relax the requirements of the interconnection technique. For example, if the first amplification stage and hit processing logic are implemented inside the sensor, the resulting signal is large enough to be capacitively coupled to the readout chip.

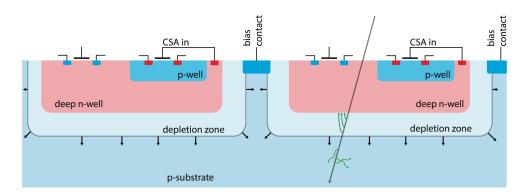


Figure 3.1: Simplified cross section of an HV-CMOS sensor. A reverse bias is applied. A highly sensitive depletion zone is then growing from the deep n-well implants that shield the electronics sitting on the surface of the chip from the high voltage in the bulk. A ionizing particle deposits energy in the depletion zone and creates electron-hole pairs. Due to the electric field and to the drift mechanism, charge carriers are collected in the deep n-well. Picture taken from [10].

Current pixel sensors are usually bump bonded to a dedicated readout chip forming a hybrid detector. Due to the complex photolithography this process is expensive, but can be avoided by coupling the sensor capacitively to the readout chip simply by gluing. Although capacitive coupling is in principle possible for passive sensors, the signal amplitude is usually not sufficient for the attached readout chip. CMOS sensors allow to choose the output amplitude due to the on chip electronics, delivering a good signal to noise ratio for the readout chips. A sketch of a capacitively coupled HV-CMOS sensor to a readout chip (FE-I4) is shown in figure 3.2.

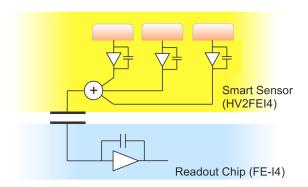


Figure 3.2: Sketch of a capacitively coupled HV-CMOS sensor (also referred as CCPD or HV2FEI4). Three subpixels (CCPD) are connected to one readout electrode that is forming a capacitor with its counterpart on the readout chip. Figure taken from [10].

The list below summarizes the HV-CMOS sensor characteristics and advantages for the use as a tracking detector [11]:

- With a substrate resistivity of about $20 \,\mathrm{Ohm} \cdot \mathrm{cm}$ and a maximum allowed bias voltage of $80 \,\mathrm{V}$, the depletion zone extends between $10 \,\mathrm{to} \,20 \,\mu\mathrm{m}$ into the substrate. The expected charge collected by drift is therefore between $800 \,\mathrm{and} \,1600$ electrons. This relatively low signal can still be easily detected and readout thanks to the direct in-pixel amplification. The thin depletion zone allows a very fast charge collection that leads to low sensitivity to charge trapping at lattice defects. Since charge trapping is the main reason for sensor degradation, a high bulk radiation hardness is therefore expected.
- Deep sub-micron CMOS electronics can be designed to be relatively resistant to ionizing radiation. Therefore high radiation hardness of the electronics is also achieved.
- On-sensor signal amplification makes it possible to use AC-coupling to the readout chip. Instead of the highly complex, mechanically sensitive and expensive bump bonding, the sensor chip can be simply glued onto the readout chip. This is referred to as "capacitively coupled pixel detector" (CCPD).
- Current prototypes are designed to be used with the existing ATLAS pixel readout chip, so-called FE-I4. No development of a new readout ASIC is needed.
- The very thin depletion zone allows for thinning of the sensor to $50 \,\mu\mathrm{m}$ and below. This leads to low material budget compared to other hybrid detectors.
- The pixel size can be made smaller because there is no size restriction from metal bumps. From the electronics side, pixel sizes down to $25 \times 25 \,\mu\text{m}^2$ can be realized. Smaller pixel size leads to smaller pixel capacitance and noise, better particle position detection and lower pile-up. The latter is especially important for high luminosity detectors.
- The HV-CMOS process is a standard electronic production process and therefore cheap and widely available compared to customized processes. This is an attractive feature for large area detectors.

3.2 FE-I4 readout chip

The FE-I4 readout chip has been designed for the Insertable B-Layer (IBL). The ATLAS collaboration has recently upgraded its semiconductor pixel tracking detector few years from now with a new layer between the existing pixel detector and the vacuum pipe of the LHC. The extreme operating conditions at this location have required the development of new radiation hard pixel sensor technologies and a new front-end readout chip, called the FE-I4. The main motivation of the IBL is to provide increased tracking robustness as the instantaneous luminosity of the LHC increases beyond the design luminosity of $10^{34} \, \mathrm{cm}^{-2} \, \mathrm{s}^{-1}$ and the integrated radiation deteriorates the performance of the inner pixel layers. The IBL has been installed in the ATLAS experiment during the LHC

shut-down in 2013-14. Figure 3.3 shows a photograph of the first full scale prototype, the FE-I4A, fabricated in the summer of 2010. The superimposed photograph of the FE-I3 integrated circuit emphasizes the size. The FE-I4 has been developed with a pixel size of $250 \times 50 \,\mu\text{m}^2$ in a 130 nm feature size CMOS process, while FE-I3 was developed in a 250 nm process.

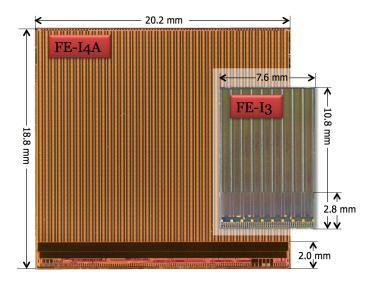


Figure 3.3: Picture of the FE-I4A IC in comparison with FE-I3 (previous ATLAS pixel readout chip.)

It is the basic element of all IBL prototype modules tested during 2011. Each pixel consists of an independent analog section with continuous reset, amplifying the collected charge from the bump-bonded sensor. In the analog section, hits are discriminated at the level of a tunable comparator with an adjustable threshold, and charge is translated to Time over Threshold (ToT) with a proportionality factor that the user can tune by changing the return to baseline behavior of the pixel. More information on FE-I4 can be found in [12].

3.3 Assembly

The prototypes investigated in this project were built in the Austria MicroSystems (AMS) 180 nm high-voltage process. The bare HV-CMOS sensor is connected to a FE-I4 by precision gluing protocol, the epoxy glue used is approximately 5 μ m thick. Finally, both HV-CMOS and FE-I4 are then wirebonded to a PCB (Printed Circuit Board), see figure 3.4. Figure 3.5a shows a bare version 4 through a microscope while figure 3.5b shows an overview of the PCB.

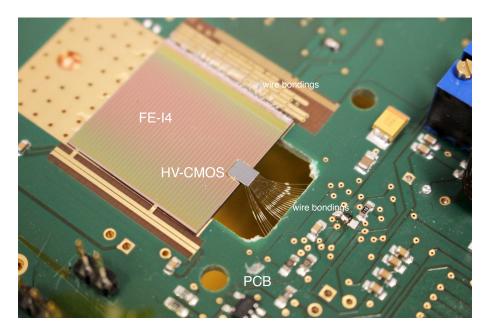


Figure 3.4: Assembly photograph. Both HV-CMOS and FE-I4 are wire bonded to the PCB. To give a scale reference, the FE-I4 is approximately 2 cm wide.

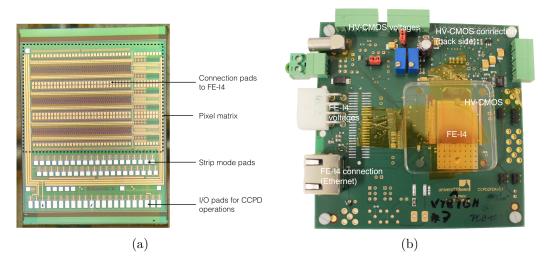


Figure 3.5: (a) Bare sensor (version 4) photograph through a microscope. (b) Full assembly photograph.

3.4 Electronics details

Transistors shown in the figure 3.6 are placed in a lowly doped deep N-well. The PMOS transistors are placed directly in the N-well, while the NMOS transistors are in the P-wells which are inside the deep N-well. It is possible to bias the deep N-well with a high

voltage with respect to the P-substrate. All transistors inside the N-well have only low voltages between their electrodes, which allows the use of small transistors.

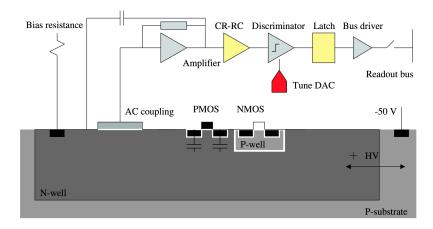


Figure 3.6: Block scheme of one pixel. Picture taken from [9].

The pixel electronics comprises a CSA which is capacitive coupled to sensor, continuous reset, passive CR-RC filter, discriminator, and a 4-bit threshold-tune Digital to Analog Converter (DAC). The large deep N-well plays two roles. First, it is the substrate for the PMOS transistors and P-wells. Second, the deep N-well is the cathode of the sensor diode.

The HV-CMOS chip is designed in such a way that a signal from the sensor can be "simulated" through an injection capacitor. The signal goes through the electronics implemented on the pixel and can be read out after the output stage. The figure 3.7 gives a simplified picture of the most relevant electronic components for this study.

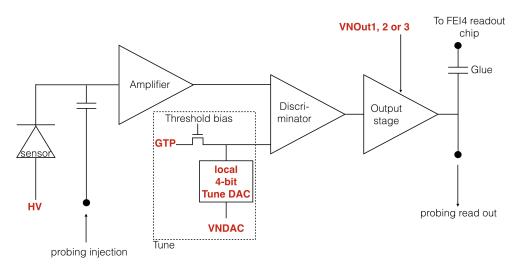


Figure 3.7: Simplified electronic scheme for one HV-CMOS pixel.

- HV (High Voltage) is applied to the sensor. Typically around -80 V.
- GTP (Global Threshold Parameter) is a global voltage which controls the discriminator level.
- Tune DAC (or TDAC) is a local 4-bit digital to analog converter and allows the GTP to be adjusted locally (pixel by pixel). The TDAC value is an integer in between 0 and 15. For sensors version 2, the effective threshold applied to the discriminator gets higher when the TDAC value is higher. For version 4, it is the other way round (see figures 4.22 and 4.23).
- VNDAC, which is a global 6-bit digital to analog converter, is the dynamic range of the TDAC. The higher the VNDAC, the wider the range of the TDAC, but the higher the steps between two TDAC values. The VNDAC value is an integer in between 0 and 63.
- VNOut1, 2 and 3 are three global parameters to choose how many columns of the pixel matrix are powered. Three HV-CMOS pixels are connected to one FE-I4 pixel (3 HV-CMOS pixels \iff 1 FE-I4 pixel), as explained on figure 3.2. VNDAC parameter allows to control the connection between HV-CMOS pixels and FE-I4 pixels. For example, if only VNOut1 is not equal to zero, only the first column will be connected to the associated FE-I4 column, which means: 1 HV-CMOS pixels \iff 1 FE-I4 pixel.

3.5 CCPD versions

Several CCPD versions have been developed so far. Each new version integrates the modifications that have been learned from the previous versions. This work is focused on unirradiated version 2 and 4 CCPD.

3.5.1 Version 2

The version 2 CCPD sensor is composed of 3 pixel types, all of a size of $125 \times 33.3 \,\mu\text{m}^2$.

- "Radiation-hard" pixels: Radiations causes detrimental effects on the characteristics of CMOS devices and circuit. Radiation hard pixels are designed in a way that reduces the impact of radiations on transistors (gate-enclosing). This represents 24×12 pixels
- "Standard" pixels: Pixel designed as shown on figure 3.7. This represents 24×36 pixels.
- "Simple" pixels have a simplified circuitry compared to standard type and represent 24×12 pixels.

Three HV-CMOS pixels are connected to one FE-I4 pixel by following a chess pattern, as shown on figure 3.9a. The focus of the laboratory characterization has been on standard pixel type.

3.5.2 Version 4

The version 4 HV-CMOS sensor is composed of 4 pixels flavors:

- SAmp pixels: Standard pixels in current mode amplitude coding. This represents 12×24 pixels with a size of $125 \times 33.3 \,\mu\text{m}^2$.
- STime pixels: Standard pixels in voltage mode amplitude coding or pulse length coding. This represents 12×24 pixels with a size of $125 \times 33.3 \,\mu\text{m}^2$.
- "New" pixels: Very similar to STime pixels but they have an alternative electronic design. The pixel size is $125 \times 25 \,\mu\text{m}^2$.
- Analog pixels: Only the amplifier is implemented.

The connection of SAmp and STime pixels is slightly different from version 2, as shown on figure 3.9b. This is no more a chess but a linear pattern. The focus of the laboratory characterization has been on the STime pixel type.

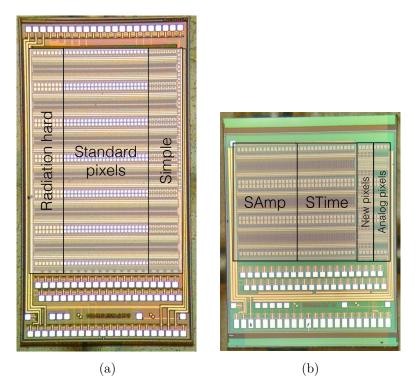


Figure 3.8: Bare sensors with different pixel types. (a) version 2 (b) version 4.

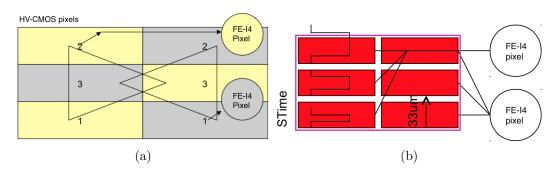


Figure 3.9: (a) Version 2 HV-CMOS to FE-I4 connection chess pattern. (b) Version 4 HV-CMOS to FE-I4 connection linear pattern for STime pixel type.

Laboratory characterization

4.1 Experimental setups

4.1.1 I-V setup

In order to check the behavior of the bare HV-CMOS sensors, the very first step in the laboratory is to measure the current of the sensor as a function of the voltage applied (I-V curve). This measurement is done in a clean room at University of Geneva with a dedicated probe station and software. The figure 4.1 describes the procedure. The current is measured with a Keithley® Electrometer 7517A. A python script using pyVisa library was written during this project in order to automatize the procedure. A detailed procedure to take I-V curve measurements for HV-CMOS version 2 and 4 is described in the appendix 1.

Once we observe the expected behavior (break down voltage around $-90\,\mathrm{V}$), as shown on figure 4.2, the sensor is named, glued to a FE-I4 and wire-bonded to a PCB, as described in section 3.3.

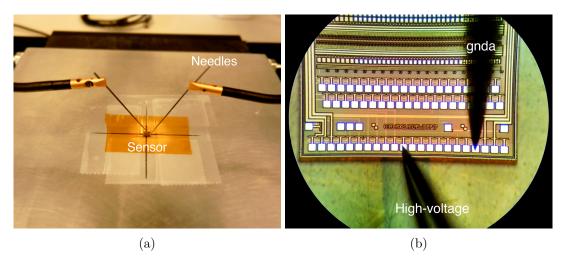


Figure 4.1: (a) Photograph of the probe station. (b) Photograph through the microscope of the bare version 2 sensor (on the left) being probed.

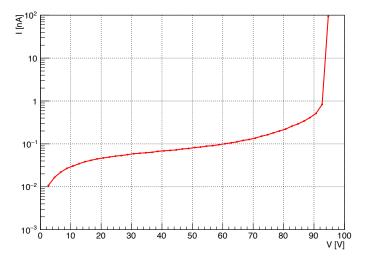


Figure 4.2: Typical I-V curve of a bare version 4 sensor, showing a breakdown at approximately -94V.

4.1.2 Characterization and tuning setup

Once the CCPD and FE-I4 are glued together and wire-bonded to the PCB, as shown on figure 3.5b, the assembly is powered on. Eight power supplies are necessary to power the assembly: six for the CCPD including one high voltage, one low voltage for the FE-I4, and one low voltage for the PCB components. All details on power supply voltages and cable scheme are given in figure 4.3 and table 4.1.

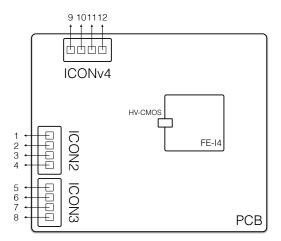


Figure 4.3: Schematic drawing of CCPD electrical connections (PCB version 5).

Voltages [V]					
Input	Name	CCPD v2	CCPD v4	Current [mA]	
ICON2_1	VDDD	1.95	1.8	10	
$ICON2_2$	ThPLow	not used	not used	-	
$ICON2_3$	gate	2.2	2.2	< 3	
$ICON2_4$	SUB/HV	0 to -93	0 to -93	< 1 (unirradiated)	
ICON3_5	$\stackrel{\circ}{\mathrm{GND}}$	0	0	-	
ICON3_6	VDDA	1.95	1.8	10	
ICON3_7	VSSA	1.5	1.5	1 to 15	
ICON3_8	VDD	3.3	3.3	< 150	
$ICONv4_9$	Vminus1	-	0 to 1	< 10	
ICONv4_10	Vminus0	-	0 to 1	< 10	
ICONv4_11	Vplus	-	0 to 1.8, usually 0.3	< 10	
ICONv4_12	GND N/C	-	-	-	
FE-I4	_		2.2	~ 500	

Table 4.1: Voltages corresponding to figure 4.3.

The PCB is connected to a Uxibo board via a flat cable on the board backside, which communicate with the computer via USB. The FE-I4 is connected via RJ45 cable to a UsbPix board which communicate with the computer via USB as well, see figure 4.4. Uxibo and UsbPix boards contain a FPGA (Field-Programmable Gate Array) and act like a bridge between the computer and the CCPD/FE-I4.

The CCPD is controlled by a basic and limited C++ software and the FE-I4 by a software developed by the University of Bonn for the ATLAS pixel project, the so-called "ST Control". Both software are completely independent of each other and cannot communicate or interact.

The setup is situated in a clean room and includes a climate chamber for low temperature measurements (minimum $\sim -30^{\circ}{\rm C}$), see figure 4.5.

Several python scripts have been written all along this thesis in order to analyze and extract all relevant information from the basic outputs of the HV-CMOS software.

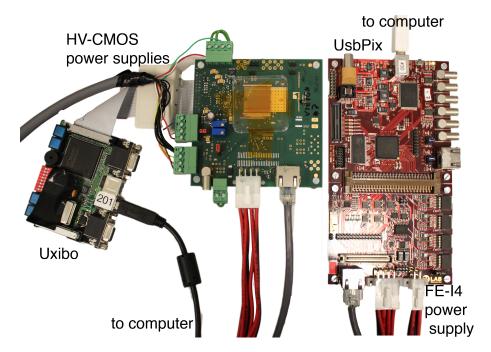


Figure 4.4: Photograph of the setup.

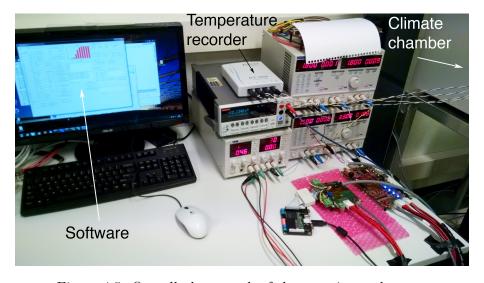


Figure 4.5: Overall photograph of the experimental setup.

4.2 S-curve definition

The threshold value for a pixel is a crucial point which has to be fully understood. As described in section 3.4, a signal can be "simulated" with an injection capacitor. Then, this signal goes through the electronic implemented on the pixel and is read out after the output stage. If the injected signal has a too small amplitude, or the electronic devices (amplifier and discriminator) are not set properly, the injected pulse might not be read out. In addition, the amplifier and the discriminator induce a noise which has to be characterized.

The way to understand the electronic devices behavior is to probe "simulated" signals of different amplitude several times (in our case 128 times). It is clear that if no signal is sent, no readout pulse should be counted up unless the pixel electronics is noisy. Conversely, if the signal amplitude is very high, even with electronics not tuned, a readout pulse should be seen. The "probing efficiency" $\left(=\frac{\# \operatorname{read} \operatorname{out} \operatorname{pulses}}{\# \operatorname{injected} \operatorname{pulses}}\right)$ as a function of the injection signal amplitude in generated electrons unit is called an "S-curve". In a perfect case, i.e. without any signal noise, the S-curve would be a step function centered on the discriminator level. In reality, noise is coming from the amplifier, discriminator and silicon sensor. So instead of having a step function, the S-curve looks like an error function, as shown on figure 4.6a. A "threshold scan" defines a measurement where an S-curve is measured for every pixels. A threshold scan takes typically several hours, depending on the CCPD version and the number of pixels to probe. The time plays an important role and must be taken into account when a tuning procedure is developed.

Threshold: The threshold of a pixel is defined as the injection value (in electrons) for which the probing efficiency is 50%, as shown on figure 4.6a. If the S-curve was a step function, the threshold should be situated at the step value. The threshold differs a lot from one pixel to another. The main goal of the tuning procedure is to make it as uniform as possible and as small as possible, without entering in the noise region.

Sigma: Sigma is the parameter used to characterize the signal noise. It quantifies the interval of the S-curve slope. The higher sigma is, the higher the noise and vice versa. The impact of sigma is represented schematically in figure 4.6b. Another noise characteristic but inaccessible with sigma is when the threshold of a pixel is set too low (GTP and/or TDAC set too low), the signal noise fluctuation can be high enough to fake a signal pulse without injecting. This results in an S-curve measurement where some pulses will be readout even without injecting.

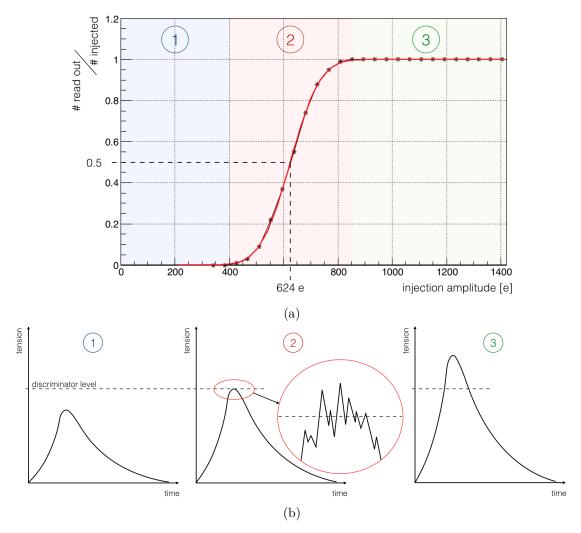


Figure 4.6: (a) Typical S-curve of one pixel. The threshold here is 624 electrons. (b) Schematic representation of signal probing in 3 different region of the S-curve.

Theoretical approach: The error function (also called Gauss error function) is the convolution product of a Gaussian function (in our case the noise) and a step function (discriminator). This function is plotted in figure 4.7.

$$\operatorname{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt$$
 (4.1)

We can write also:

$$\operatorname{erf}\left(\frac{x-\mu}{\sigma\sqrt{2}}\right) = \frac{2}{\sqrt{\pi}} \int_0^{\frac{x-\mu}{\sigma\sqrt{2}}} e^{-t^2} dt \tag{4.2}$$

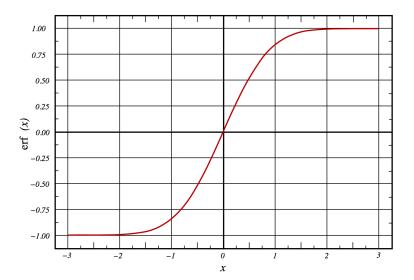


Figure 4.7: Plot of the error function of equation (4.1).

By doing a variable change $t = \frac{v - \mu}{\sigma \sqrt{2}}$, we obtain:

$$v = \sigma\sqrt{2}t + \mu \quad \to \quad dt = \frac{dv}{\sigma\sqrt{2}}$$

The new integration interval is:

$$t = 0 \rightarrow v = \mu$$
 $t = \frac{x - \mu}{\sigma\sqrt{2}} \rightarrow v = x$

Finally, we obtain:

$$a + b \cdot \operatorname{erf}\left(\frac{x - \mu}{\sigma\sqrt{2}}\right) = a + b \cdot 2 \int_{\mu}^{x} G(v) \,dv$$
 (4.3)

where G(v) is a Gaussian function and equals to $G(v) = \frac{1}{\sigma\sqrt{2\pi}}e^{-\frac{(x-\mu)^2}{2\sigma^2}}$. The step function equals to zero from $-\infty$ to μ and to one from μ to $+\infty$.

To conclude, the threshold μ is equal to the mean of the Gaussian function G(v), b is the amplitude, a is the ordinate which corresponds to the threshold μ , and σ is the standard deviation of the noise Gaussian function. The higher the sigma, the flatter the error function curve will be.

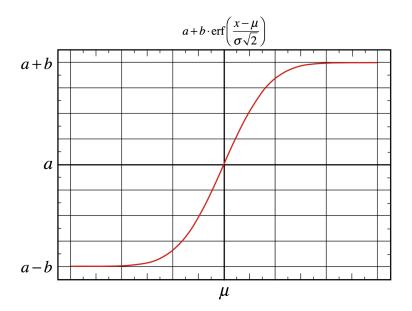


Figure 4.8: Plot of the error function with variable changed of equation (4.3).

4.3 Noise occupancy scans

An other characteristic of the noise inaccessible with sigma appears when the threshold of a pixel is set too low, the noise fluctuation can be high enough to fake a signal pulse without injecting. This noise can be measured on the FE-I4 level itself by doing a noise occupancy scan. The scan reads out randomly if pixels have fired of not over a chosen number of triggers (usually 10 millions in our case). The main reason why this measurement is done on the FE-I4 level is that it can scans all pixels at the same time, while on the HV-CMOS side it can be measured only pixel by pixel. The noise rate requirement for ATLAS experiment is 10^{-6} for each pixel (IBL requirement). As described in section 3.4, in usual settings, 3 HV-CMOS pixels are connected to 1 FE-I4 pixel. This can change to 2 HV-CMOS pixels \iff 1 FE-I4 pixel, or 1 HV-CMOS pixels \iff 1 FE-I4 pixel by changing parameters VNOut 1, 2, and 3, see figure 3.7.

4.4 Tuning methods

As described in section 4.2, the threshold differs a lot from a pixel to another. The main goal of the tuning procedure is to make the threshold as uniform as possible and as small as possible, without entering in the noise region. With a depletion region between 10 and $20\,\mu\text{m}$, a typical signal from a MIP (see section 3.1) is expected to be between 800 and 1600 electrons. In this section, different tuning methods developed during this work are presented.

4.4.1 GTP optimal value

The starting point of any tuning procedure is the selection of an optimal GTP value (see figure 3.7). The developed method consists to set all pixel TDAC at 7, to be sure to be in the middle of the TDAC range. Then without injecting, we measure the noise (noise occupancy scan with the FE-I4) by scanning the GTP to lower values until we reach the noise edge, as shown on figure 4.9a. The "optimized value" (or noise edge) is the GTP value for which the studied pixel is not noisy. This selection criterion is usually set to a noise rate $\left(=\frac{\#read\ out}{\#probing}\right)$ of 10^{-6} but can varies on the user's needs.

If we do this step for every pixels, we can plot the noise edge histogram, as shown on figure 4.9b. Then, the optimized global GTP is simply the mean of this distribution, in this case: 0.8329 V.

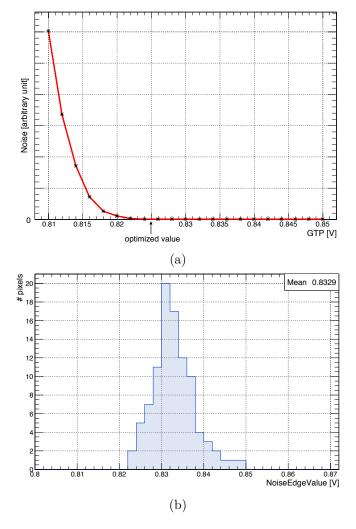


Figure 4.9: (a) Noise in arbitrary unit in function of the GTP for one pixel. (b) Histogram of the noise edge found as described on figure 4.9a.

4.4.2 Interpolation tuning

4.4.2.1 Description

The first tuning procedure developed during this work is called "interpolation tuning". It has been developed initially with version 2 sensors. This method is based on a brutal and basic way: analyze pixels threshold in function of TDAC, while the GTP is fixed.

A step by step description is given below:

- 1. Set the GTP by following the method given above.
- 2. Take several threshold scans where the TDAC configuration is uniform, i.e. all pixels are set to the same TDAC value. The more TDAC value are scanned, the more precise will be the tuning. In general, the time factor limits the number of threshold scans, a good ratio time/tuning quality has to be agreed.
- 3. Plot the threshold versus TDAC value for each pixel, as shown of figure 4.10. In this example, the TDAC values were 2, 4, 6, 9, 11, and 14.
- 4. Target a reasonable threshold, for example 700 electrons is a good value for HV-CMOS version 2.
- 5. Interpolate to find the associated TDAC value.
- 6. Reiterate for all pixels.

Once the tuning is done, the tuned TDAC configuration (figure 4.11b) is uploaded to the sensor. In addition, some tools have been developed in order to better understand the TDAC behavior. For example, the histogram of tuned TDACs can be plotted, see figure 4.11a. The mean and the shape of this histogram allows to know if the GTP was correctly set. Here, the mean is very close to 7, which is the middle of the TDAC range. This means that the GTP was properly set. If the mean is lower than 7, for example 3, the GTP is set too high for CCPD version 2 and too low for CCPD version 4. Conversely, if the mean is higher than 7, the GTP is set too low (version 2) or too high (version 4). The spread of the distribution informs us if the VNDAC is properly chosen. If the distribution is very narrow and no pixels have a TDAC set to 0, 1, 14, or 15, this means that the TDAC range is to high. VNDAC optimization is not obvious and is still under study. The latest results are described in section 4.5.

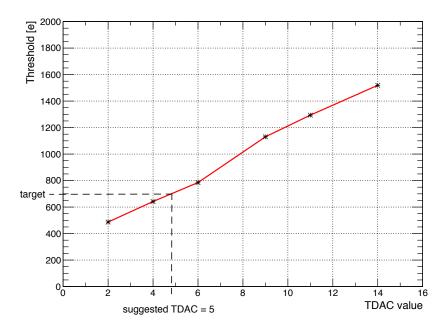


Figure 4.10: Threshold in electrons as a function of TDAC value for one pixel.

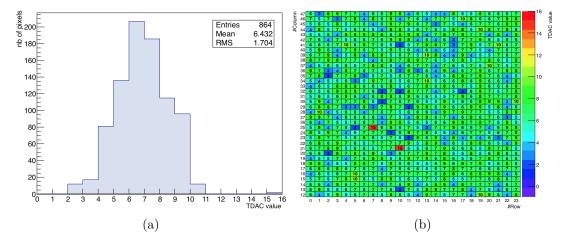


Figure 4.11: Suggested TDAC (a) histogram (b) 2D map, by interpolation tuning.

4.4.2.2 Results

The interpolation tuning method has successfully been tested on several CCPD version 2 and version 4.

The figures 4.12 and 4.12b show the threshold and sigma distributions before and after the tuning for a CCPD version 2 with 700 electrons target, while the figures 4.13a and 4.13a show the result on a sensor version 4 with a target of 400 electrons. As expected, no changes are observed between sigma distributions before and after the

tuning.

The figure 4.14a shows the very strong correlation between the expected threshold distribution and the measured one. Few pixels (less than 1%) are uncorrelated and a secondary fine re-tuning is necessary. Figure 4.14a shows superimposed S-curve of a tuned CCPD threshold scan.

Once the tuning is done on a specific target, another strategy to further decrease the threshold is to reduce the GTP. This strategy has been proven for version 2, as shown on figure 4.15. The distribution for which the sensor has been tuned is blue. The target was 700 electrons and the GTP was set to 0.93 V. In order to better understand the behavior of a tuned sensor, the GTP has been modified by keeping the same tuned TDAC configuration. The result is clear; decreasing the GTP has a direct impact on the distribution. Despite the fact that a fine re-tuning is necessary for some pixels (green peak on figure 4.15), lowering the GTP allows us to reach very low threshold.

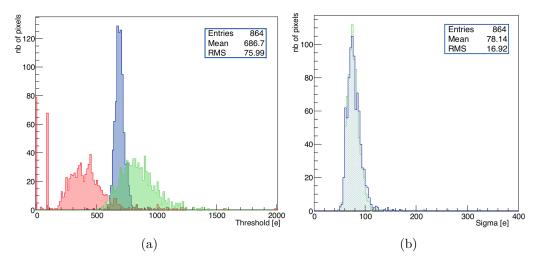


Figure 4.12: (a) Threshold distributions before and after the tuning for a version 2 sensor. The red and green distributions represent a uniform TDAC configuration set at 4 and 9, respectively, while the blue represents a TDAC configuration tuned by the interpolation method. The two red peaks are due to very noisy pixels for which the Scurve measurement failed. The TDAC value was not adapted in those cases. (b) Sigma distributions before and after the tuning. The green curve has been measured with a uniform TDAC configuration of 7, while the blue one is the tuned distribution on the left.

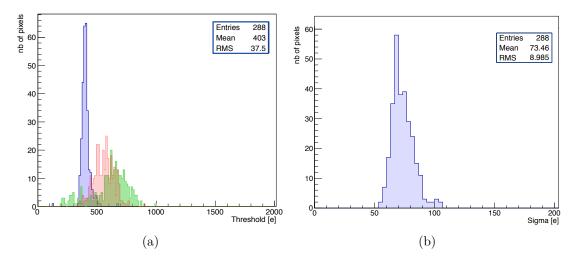


Figure 4.13: (a) Threshold distribution before and after the tuning for a version 4 sensor. The red and green distributions represent a uniform TDAC configuration set at 3 and 9, respectively, while the blue distribution represents a TDAC configuration tuned by the interpolation method. (b) Sigma distribution corresponding to the tuned threshold distribution on the left.

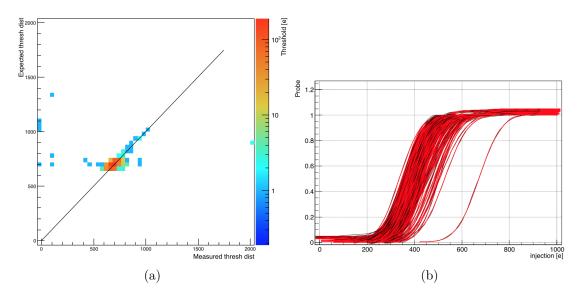


Figure 4.14: (a) Correlation plot between the expected threshold distribution from the tuning shown on figure 4.12 and the measured one. (b) Superimposed S-curves of the tuned threshold distribution on figure 4.13a. The black lines represents the data while the red ones represent the error function fitting.

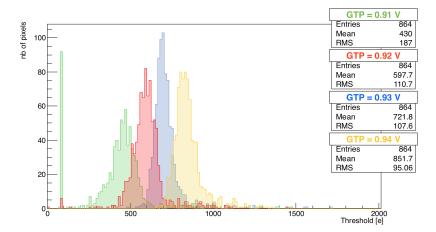


Figure 4.15: Threshold distributions for different GTP values. The sensor was tuned to a target of 700 electrons at an optimal GTP equal to 0.93 V (blue distribution). The green peak near zero represents pixels which are failing the S-curve measurement due to a bad tuning.

4.4.2.3 Noise occupancy scan

Figures 4.16a and 4.16b show a noise occupancy scan measured on a tuned version 4 sensor. The most noisy pixel is situated at column 5, row 156 on the FE-I4 frame. It has a noise rate which does not exceed roughly 10^{-5} . Most of the pixels have a noise rate around 10^{-6} . Only noise occupancy with VNOut 1 is shown in order to compare with the FE noise tuning, see below.

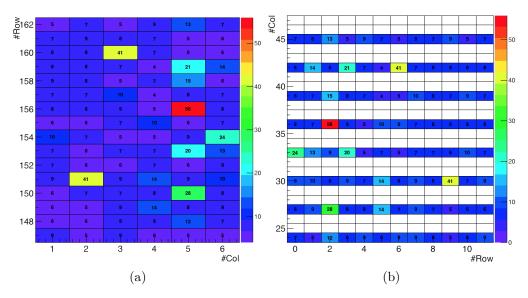


Figure 4.16: Noise occupancy scan of a tuned version 4 sensor with 10 millions triggers and only VNOut 1 enabled. FE-I4 pixel frame (a), CCPD pixel frame (b).

4.4.3 Auto-tune method

4.4.3.1 Description

The auto-tune method has been implemented directly in the C++ HV-CMOS software for sensor version 4 only. The principle is very similar to the interpolation tuning but is in principle faster and more precise if the algorithm is set correctly.

A step by step description is given below:

- 1. Set the GTP as described in section 4.4.1, except that this step is done on the HV-CMOS side.
- 2. Set the injection amplitude at the targeted threshold level. If a pixel is correctly tuned, a probing at the threshold target amplitude should result to 50%.
- 3. Set TDAC to 7 and readout, if the readout is more/less than 50%, increase/decrease (swapped for version 2) the TDAC value.
- 4. Do a binary search until the best TDAC value is found, for which the probing result is the closest to 50%.
- 5. Reiterate for all pixels.

This method is not always stable for low threshold targets and is still under study. Some parameters are not modifiable yet, for example the noise selection for the TDAC value. When the target threshold is set too low, the binary search fails and no tuning is possible.

4.4.3.2 Results

Figure 4.17a shows the threshold distribution after the auto-tune with a target of 389 electrons. Figure 4.17b shows the superimposed S-curves corresponding to the tuned threshold distribution. We can clearly see that despite being very close to each other, some curves are noisy compared to 4.14b.

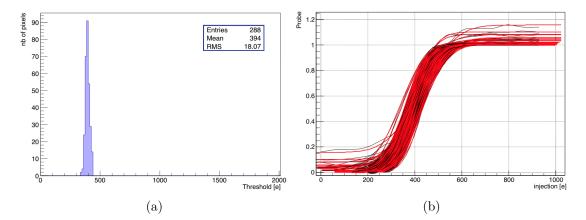


Figure 4.17: (a) Threshold distributions after auto-tune with a target of 400 electrons. (b) Superimposed S-curves corresponding to the tuned threshold distribution. The black lines represents the data while the red ones represents the error function fitting.

4.4.3.3 Noise occupancy scan

Figures 4.18 show a noise occupancy scan measured on a tuned version 4 sensor with auto-tune method. As expected by seeing the figure 4.17b, pixels are a bit noisier compared to noise occupancy with interpolation tuning in figure 4.16, but are still under a noise rate of 10^{-5} .

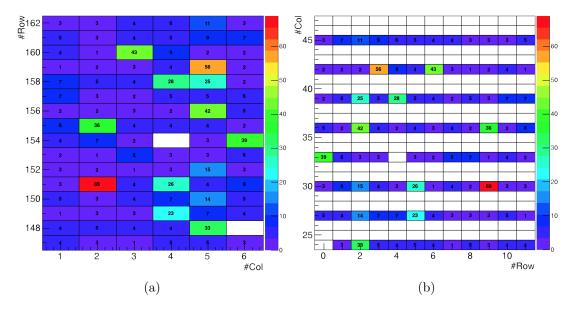


Figure 4.18: Noise occupancy scan of a tuned (auto-tune) version 4 sensor. 10 millions triggers and only VNOut 1 was enabled, the noise rate selection was done on the HV-CMOS side only. FE-I4 pixel frame (a), HV-CMOS pixel frame (b).

4.4.4 FE noise tuning method

4.4.4.1 Description

The "FE noise tuning" method is a tuning done only on the FE-I4 side. The main interest is the gain of time, because S-curve measurements (which take the larger amount of time) are no longer needed with this method. However, as mentioned earlier in the chapter, no interaction between ST control and HV-CMOS software is possible. This means that a user intervention is necessary for each measurements. This method is still under study but results seem encouraging. Once the method is automatized, it will be by far the fastest tuning method developed.

A step by step description is given below:

- 1. Set a uniform TDAC configuration.
- 2. Measure the noise with a noise occupancy scan and note the noise edge position (same principle as finding the optimal GTP value). The most important point here is to have a noise reference point for each pixel (step 2) and to "equalize" them by changing the TDAC (step 7).
- 3. Set another uniform TDAC configuration and redo step 2, see figure 4.19a. If additional TDAC configurations are measured, the tuning will be more precise (low RMS of the threshold distribution).
- 4. The mean of the distribution with a TDAC configuration of 7 gives the optimal GTP (as described above).
- 5. Plot the noise edge in function of TDAC value for each pixels, figure 4.19b.
- 6. Target the optimal GTP.
- 7. Suggest a TDAC value by interpolation for all pixels.

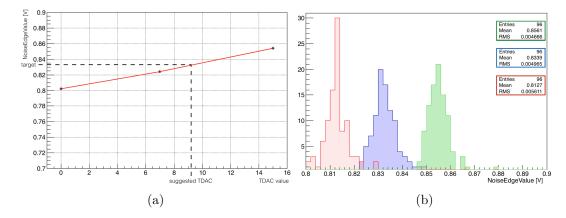


Figure 4.19: (a) Noise edge in function of TDAC value for one pixel. The target here is $GTP = 0.8339\,V$ (b) Histograms of the noise edge values in volts for different TDAC configurations. The red, blue and green distributions have been measured with a uniform TDAC configuration of 0, 7, and 15, respectively.

4.4.4.2 Results

Because this method requires a lot of user intervention and is time consuming, only a first test with VNOut 1 enabled has been done. In these conditions, 96 pixels are studied, which is enough to give an overview of the method. The figure 4.20 shows the threshold distribution with a tuned sensor.

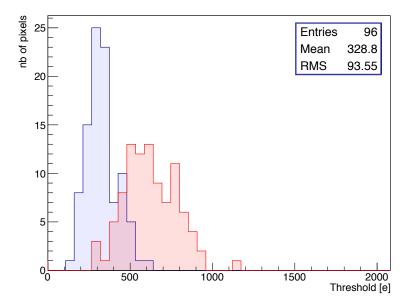


Figure 4.20: Threshold distribution before and after tuning. The red distribution has been measured with a uniform TDAC configuration of 7.

4.4.4.3 Noise occupancy scan

During the tuning, the noise rate selection was set to 10^{-5} . By looking at figure 4.21a, some pixels are above this value, which means a fine re-tuning is necessary. However, most of the pixels respect the criterion, as desired.

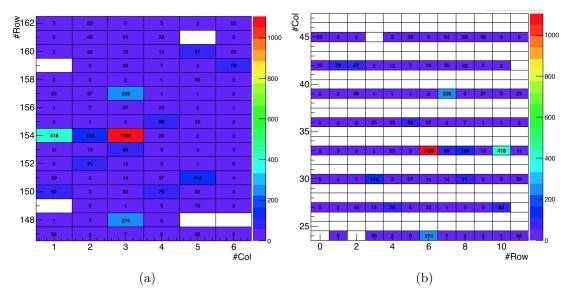


Figure 4.21: Noise occupancy scan of a tuned version 4 sensor. 10 millions triggers and only VNOut 1 was enabled, the noise rate selection was 10^{-5} . FE-I4 pixel frame (a), HV-CMOS pixel frame (b).

4.5 VNDAC parameter study

4.5.1 Motivation

As described in section 3.4, VNDAC is the dynamic range of the TDAC. Some pixels show a unexpected and limited TDAC range, as shown on figure 4.22. As a non-negligible number of pixels are concerned (more than 50%), changing the VNDAC might be worth it. Changing the VNDAC influences all pixels, as it is a global parameter. This study has been done with version 4 only, version 2 is expected to have the same behavior.

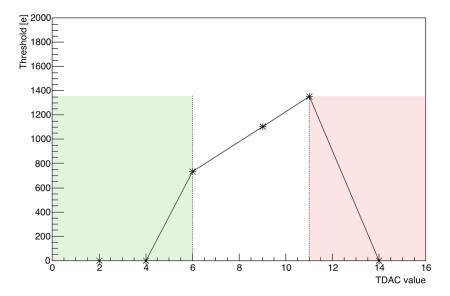


Figure 4.22: Threshold as a function of the TDAC value for one pixel of a version 2 sensor. The green area represents a very noisy region, where the pixel is so noisy that the S-curve measurement fails. The red area represents a region where the pixel has such a high threshold that the S-curve measurement could not reach it, resulting in a failing S-curve. Some pixels are limited only in one region (green or red), not necessary both at the same time (as shown on the figure).

4.5.2 Method

The method is very simple but needs a lot of threshold scans, which is time consuming. This is why the study is focused on a region of interst of 100 pixels, which is enough to have a good overview. An interpolation tuning is done for different VNDAC values, in our case 6, 8, 10, 12, and 14, see figure 4.23. Then, the slope of the threshold as a function of the TDAC is expected to change with respect to the VNDAC. For different VNDAC, a slope distribution is obtained as shown on figure 4.24.

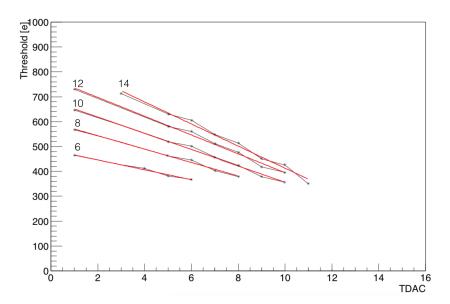


Figure 4.23: Superimposed threshold in function of the TDAC value for different VN-DAC: 6, 8, 10, 12, and 14 for one pixel of a version 4 sensor. Version 4 TDAC values are swapped with respect to version 2, see 3.4.

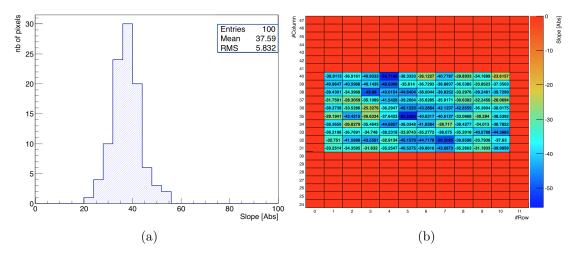


Figure 4.24: (a) Distribution of the slope from the threshold versus TDAC curve (figure 4.23) for a VNDAC value equals to 10. (b) 2D map of all the STime pixels for a VNDAC value of 10. The color scale represents the slope of the threshold as a function of the TDAC value. Pixels in red are not studied.

4.5.3 Results

The figure 4.25 shows the slope distribution mean as a function of the VNDAC value. The error bars are the RMS of the associated distribution. It is clear that the slopes decrease as the VNDAC decrease. Despite that the VNDAC has truly an effect on the TDAC range, it also modifies the threshold value for the same TDAC, i.e. for a same TDAC but different VNDAC, the pixel threshold changes. This is clearly visible on figure 4.23. This last point tends to complicate the tuning of this parameter and is still undergoing research.

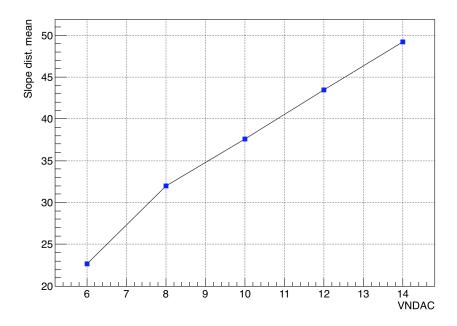


Figure 4.25: Slope distribution mean in function of VNDAC value.

4.6 TDAC linearity

4.6.1 Broken registers

A special TDAC behavior for a few pixels (1%) of version 2 has been noticed, as shown on figure 4.26. A break appears between the TDAC value of 7 and 8. The cause of this is a broken most significant bit (MSB) of TDAC registers, see table 4.2. This issue has been fixed with version 4.

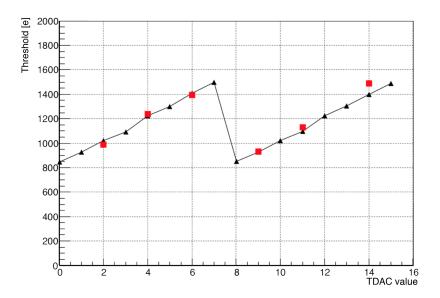


Figure 4.26: Threshold in function of TDAC value for one pixel of a version 2 sensor. The red squares are the original data points while the black triangles are a complementary measurements. The break appears between TDAC of 7 and 8.

Table 4.2: TDAC values converted into bits.

TDAC	0-6	7	8	9-15	
bits	0000-0110	0 111	1 000	1001-1111	

4.6.2 Version 4 TDAC linearity uniformity

Studying VNDAC parameter allows us to understand and quantify the TDAC linearity uniformity, i.e. if the pixels threshold as a function of the TDAC behaves differently from a pixel to another. Figure 4.27 allows us to quantify this.

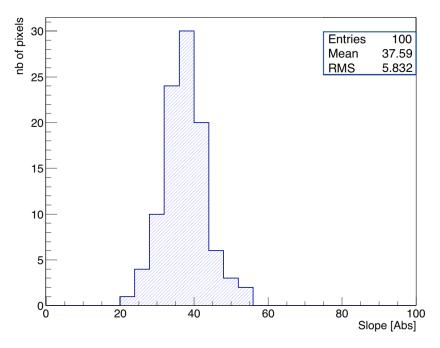


Figure 4.27: Distribution of the slope from threshold versus the TDAC curve for a VNDAC value equals to 10 (default value). Study done on 100 pixels of a version 4 CCPD.

4.7 Temperature dependency

4.7.1 CCPD version 2

Measurements at low temperature have been performed. The results for CCPD version 2 are shown in the figure 4.28. The decrease of the temperature greatly affects the threshold distribution. The mean is reduced by more than 10% at 0°C.

4.7.2 CCPD version 4

More details measurements have been performed on CCPD version 4. The results are shown in figure 4.29. The threshold distribution mean is slightly reduced by a maximum of 6%. The sigma distribution mean tends to decrease with the temperature. This is explained by the fact that the noise contribution from the silicon sensor normally decreases with the temperature. The lower temperature decreases the sigma distribution mean by less than 5%.

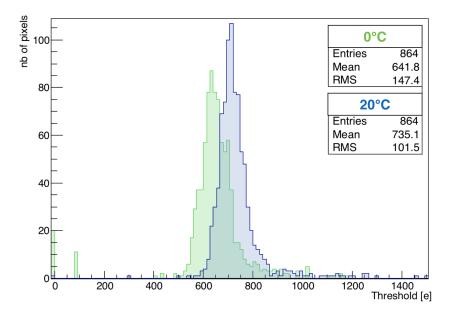


Figure 4.28: Threshold distributions for a tuned version 2 sensor targeted to 700 electrons, with (green) and without (blue) the FE-I4 powered on.

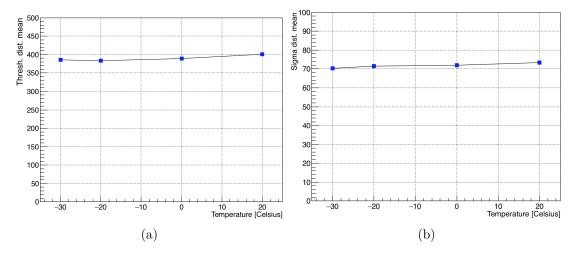


Figure 4.29: The interpolation tuning was done on a version 4 CCPD and targeted at 20°C to 400 electrons. (a) Threshold distribution mean in function of the temperature. (b) Sigma distribution mean as a function of the temperature.

4.8 Power cycles

In order to show the stability of TDAC configuration, full power cycles have been done by changing the power supplies and the setup location. The correlation between tuned threshold distributions before and after a full power cycle is shown on figure 4.30a. Despite that a quick fine re-tuning is necessary for the few pixels outside the correlation, the tuned TDAC configuration is fairly stable. No "hot" points have been found on the 2D map, figure 4.30b, since a power cycle to another, pixels out of the correlation seem to appear randomly in the pixel matrix.

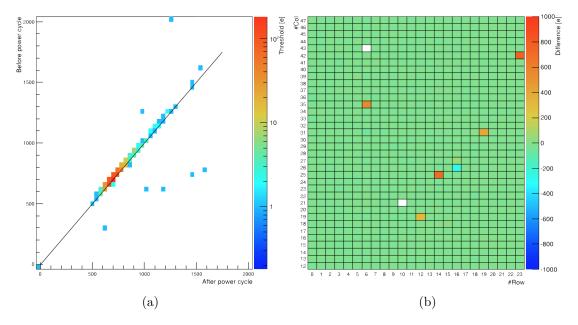


Figure 4.30: (a) Correlation plot between the threshold distribution of a tuned version 2 sensor before and after the power cycle, with the same tuned TDAC configuration. (b) 2D map of the differences from the correlation plot on the left. The z-axis represents the difference in electron unit.

4.9 Test-beam

4.9.1 Test-beam setup

Test-beam studies are performed to analyze prototypes properties such as efficiency. Particles are sent through the prototype (also referred as device under test (DUT)) and are recorded thanks to a telescope designed by the University of Geneva. An overall 3D view of this telescope is shown in figure 4.31. It is composed of six planes (IBL double-chip planar modules), two triggering scintillators (one in the front and the other one at the back), and a movable stage hosting the DUT. The DUT can be cooled down (typically to few Celsius degrees under zero) thanks to an hermetic box and an external chiller. Two planes have been rotated by 90° in order to improve the resolution of the the telescope.

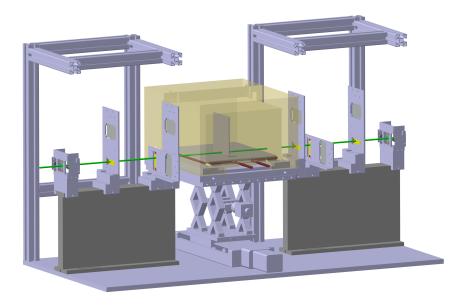


Figure 4.31: Overall 3D view of the telescope. The two telescope arms load three planes each and triggering scintillator plane at both ends. The particle beam is shown in green, the DUT box in dark yellow, and the planar modules in yellow and red. The dark red pipe inside the DUT box represents the chiller cooling pipe. Picture taken from [13].

4.9.2 Results

This master thesis work did not focus on test-beam analysis. The purpose of this section is to show an overview of the latest test-beam studies performed on HV-CMOS sensors. All results presented in this section are taken from [13] and [14].

More than 90 million triggers have been taken at the SPS (Super Proton Synchrotron) in October and November 2014. A summary of studied CCPD devices is shown in table 4.3. Due to a systematic early breakdown, the bias voltage applied could not exceed 12 V and 35 V for the unirradiated and irradiated version 4 CCPD, respectively.

The efficiency maps for unirradiated version 2 (sample C19) and version 4 (sample 402) CCPD are shown in figures 4.32 and 4.33. The C19 efficiency map presents one pixel with less efficiency, this is due to the fact that during data taking, two out of six HV-CMOS pixels have been disabled.

Figure 4.34 shows the efficiency as a function of the GTP value for two version 4 prototypes. The GTP has a great impact on the efficiency. As expected, the efficiency decreases as the GTP increases. This is due to the fact that if the discriminator level is set to high, a small fraction of particles for which the signal was low are missed. Therefore, the tuning of the GTP, in addition of the other parameters, are very important.

Table 4.3: Summary of tested pr	prototypes and their efficiency.
---------------------------------	----------------------------------

Sample	Version	Irradiation $[n_{eq}/cm^2]$	GTP value [V]	Bias voltage [V]	Efficiency [%]
C19	2	-	0.84	90	99.5 ± 0.2
C22	2	10^{15}	0.84	80	95.1 ± 0.4
402	4	-	0.94	12	99.4 ± 0.2
404	4	10^{15}	0.94	35	96.2 ± 0.3

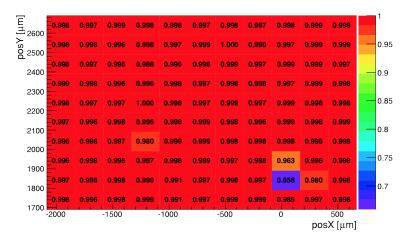


Figure 4.32: Efficiency map of sample of a unirradiated version 2 CCPD (C19).

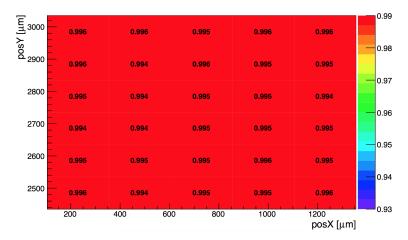


Figure 4.33: Efficiency map of sample of a unirradiated version 4 CCPD (402).

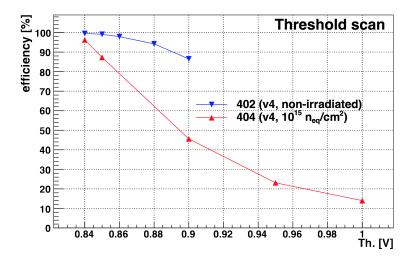


Figure 4.34: Efficiency as a function of the GTP value (also referred as Th.) for two version 4 prototypes.

Discussion and perspectives

5.1 Laboratory characterization

5.1.1 Tuning methods and perspectives

Interpolation tuning The interpolation tuning has been the first (and only) tuning procedure developed for the CCPD version 2. No real and systematic tunings have been done before. Results in section 4.4.2 have proved that the tuning works well for CCPD version 2 and 4. This method is based on the analysis of threshold scans, which is time consuming. To give an order of magnitude, one threshold scan takes approximately five hours for the 864 pixels of CCPD version 2 and three hours for the 288 pixels of CCPD version 4. To perform a precise tuning, the best is to scan at least half of the 15 TDAC possible values, which means 7 times 5 hours = 35 hours of measurements. This is too long and can be very problematic in test-beam conditions, when an "in-situ" tuning is necessary. Fortunately, tuning configurations are fairly stable when changing setup environment, as shown in sections 4.7 and 4.8. So tunings can be performed in the laboratory and used in the test-beam. A more precise tuning could be reached by scanning the 15 TDAC values. This would lead to lower distribution RMS and a more narrow distribution but it would take 15 times 5 hours = 75 hours. The ratio between precision and tuning time has to be optimized and scanning half of the possible TDAC values showed a good ratio between precision and time.

The tools developed with the interpolation tuning allow us understanding of pixels behavior. Figure 5.1 shows the intrinsic limit of some pixels with a given GTP and VNDAC. Three expected threshold distributions with a different threshold target are shown. These distributions share their tails, which means that even by decreasing the

threshold target, the tuning is at some point limited. This tail is mostly due to the intrinsic limitation of some pixels. This problem can be mitigated by modifying the GTP and VNDAC as shown on sections 4.4.2 and 4.5, but some intrinsic limitations will remain.

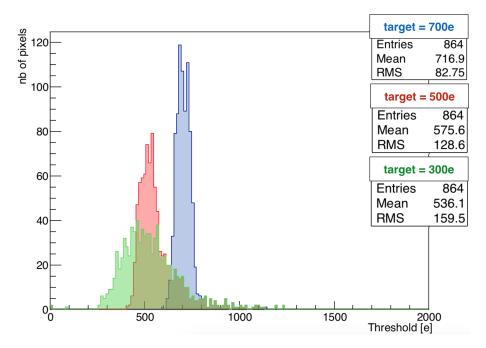


Figure 5.1: Expected threshold distributions with different target using interpolation tuning. Green, red, and blue distributions have respectively a threshold target of 300, 500, and 700 electrons.

Auto-tune The auto-tune method was already implemented in the C++ software for CCPD version 4. As shown in section 4.4.3, the procedure works well. However, the algorithm crashes when the target is set too low, which leads to several "trials" before finding a reasonable threshold target. Furthermore, the algorithm does not manage the noise correctly, as shown on figure 4.17. This procedure uses a binary research, and is the best way to find an optimized TDAC, because all values are scanned very quickly compared to other algorithms. A good precision/time ratio is then observed.

FE noise tuning The FE noise tuning method shown in section 4.4.4 is in a very early stage of development. A study has been done on 96 pixels of a CCPD version 4. The tuning was not optimized at all because only 3 TDAC values have been noise scanned. The best would be to scan the 15 TDAC values but this would take a lot of time. The procedure takes time because a lot of noise occupancy scans have to be measured. In the case discussed in section 4.4.4, 30 noise occupancy scans have been recorded, requiring user action for each of them. When tuning all pixels (VNOut1, 2, and 3 enabled), approximately 60 noise occupancy scans are necessary. In the future,

implementing a binary noise research would be a useful feature. The main point is that the tuning principle fulfills its purpose. It allows all pixels to be tuned quickly and at the same time in an automatized procedure. Furthermore, this method is based on noise occupancy scans, which basically gives the effective noise value to take into account when looking at the ATLAS pixel noise requirements. Once again, when a automatize procedure will be developed, this method will definitely be the best tuning option.

Tuning perspectives Because the development of tuning methods is in a very early stage, the tuning of a CCPD takes a lot of effort and time. The main goal of this work was to understand the sensor behavior, and then tune it. Even though pixels have an intrinsic limit (figure 5.1) and procedures take a long time, this work has proved that a great level of optimization can be reached. The next step in the laboratory is to abandon the Uxibo board and ST Control and use another boards system fully and easily modifiable using python libraries. This system called "Caribou" is under development and will soon be available. This will be a great advantage for laboratory studies. It would allow to communicate with the CCPD and the FE-I4 at the same time, and to automatize the tuning procedures.

5.1.2 VNDAC study

The VNDAC parameter behavior has been studied in section 4.5. Many pixels (approximately 50%) show a limitation at some point in the TDAC range (figure 4.22). The optimization of VNDAC parameter is then necessary. If the VNDAC value is increased, the TDAC range increases but the TDAC suggested value becomes less precise, so the RMS of the threshold distribution increases and the distribution becomes wider. Conversely, if the VNDAC value is decreased, the tuning becomes more precise, but the TDAC range is even more limited. A good ratio between tuning precision and TDAC range is then not obvious at all to find. Currently, the default value seems to be reasonable, but a systematic and automatic procedure to find the best VNDAC value has to be implemented in the future.

5.1.3 TDAC linearity

The TDAC linearity has been studied in section 4.6 using the tools developed for the VNDAC study. The first thing observed was a most significant bit issue with CCPD version 2, as shown on figure 4.26. This issue has been fixed in next the CCPD versions. The TDAC linearity shown on figure 4.27 is not very uniform. A great difference between pixels is observed. This non-uniformity is intrinsic to the pixels and could be in principle optimized with VNDAC parameter.

5.1.4 Temperature effect

Temperature effects have been studied on CCPD version 2 and 4 (section 4.7). A significant improvement of 10% in the threshold distribution of a CCPD version 2 is observed

when the temperature is decreased at 0° C (figure 4.28).

More precise measurements at low temperatures have been performed on a unirradiated version 4 sensor, shown in figure 4.29. No significant improvements in term of threshold distribution are observed. The sigma-distribution mean slightly decreases when the temperature decreases. This could indicate that most of the sigma contribution does not come from the silicon sensor itself, but from the electronics. However, the effect is very small and not relevant during operations. Measurements at low temperatures with irradiated sensors have to be performed in the future, since decreasing the temperature should have a real impact on the leakage current, and therefore on the noise.

Conclusion

The luminosity of the LHC will be increased during the Long Shutdown of 2022 and 2023 (LS3) in order to increase the sensitivity of its experiments during 10 additional years of data taking. A completely new inner detector for the ATLAS experiment needs to be developed to cope with the extremely harsh environment of the HL-LHC. Radiation hardness, low occupancy and excellent performance in high pile-up environment are mandatory requirements.

A new silicon detector concept based on HV-CMOS technologies for pixel and/or strip layers has garnered a lot of attention, as it provides reduced price due to the commercial processing and at the same time high radiation hardness.

The main goal of this work consisted in characterizing different HV-CMOS sensors and understanding all features and behaviors. Tuning procedure algorithms have also been developed during this laboratory characterization.

Although the characterization of the HV-CMOS assemblies is in an early stage, three tuning procedures based on different algorithms have been developed. The two first ones are based on HV-CMOS C++ software. Probing the sensor is time consuming, and can be done only pixel by pixel. The latest procedure is based only on FE-I4 read out chip. This could allows one to use only the FE-I4 and to get rid off the CCPD probing. Thus, the tuning would be very fast. Finally, a good understanding and control of the noise rate and the pixels threshold have been demonstrated in different ways. Despite small fraction of the pixels having an intrinsic limit, a great optimization can be reached. In addition, a good understanding of the sensors behavior, such as TDAC linearity, noise, VNDAC parameter behavior, and temperature effects has been shown.

During test-beams campaigns, the results show a detection efficiency of 99.5% for version 2 unirradiated CCPD and 95.1% for version 2 irradiated at $10^{15}\,\mathrm{n_{eq}/cm^2}$. Regarding version 4, an efficiency of 99.4% and 96.2% is measured for unirradiated and irradiated at $10^{15}\,\mathrm{n_{eq}/cm^2}$, respectively.

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Abbreviations

AMS - Austria MicroSystems

CCPD - Capacitively Coupled Pixel Detector

CERN - European Organization for Nuclear Research

CSA - Charge Sensitive Amplifier

DAC - Digital to Analog Converter

 \mathbf{DUT} - Device Under Test

 $\mathbf{FE}\text{-}\mathbf{I4}$ - Front End I4

HL-LHC - High Luminosity-LHC

HV-CMOS - High-Voltage Complementary Metal Oxide Semiconductor

HV2FEI4 - HV-CMOS to FE-I4, refers to a HV-CMOS assembly

 ${f IBL}$ - Insertable B-Layer

MIP - Minimum Ionizing Particle

 \mathbf{MSB} - Most Significant Bit

PCB - Printed Circuit Board

 $\mathbf{R}\&\mathbf{D}$ - Research & Development

SPS - Super Proton Synchrotron

 \mathbf{TDAC} - Tune DAC

 \mathbf{ToT} - Time over Threshold

Appendix 1: I-V measurement protocol

In order to check the good behavior of the new bare HV-CMOS sensors received from the production, the very first step in the laboratory is to measure the current of the sensor in function of the voltage applied (I-V curve). This measurement is done in a clean room at university of Geneva with a dedicated probing station and software. The figure 5.2 describes the procedure for version 2 while figure 5.2 for version 4. The current is measured with a Keithley® Electrometer 7517A. Results for HV-CMOS version 4 are shown on figure 5.4.

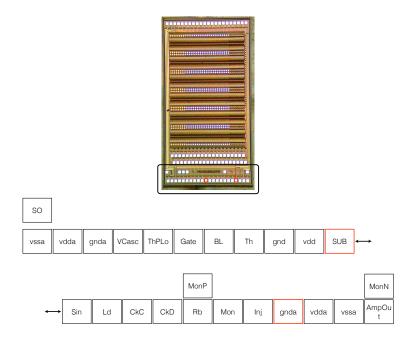


Figure 5.2: Pad scheme for bare HV-CMOS sensor version 2. High-voltage is connected to "SUB" pad while "gnda" to the electrometer ground.

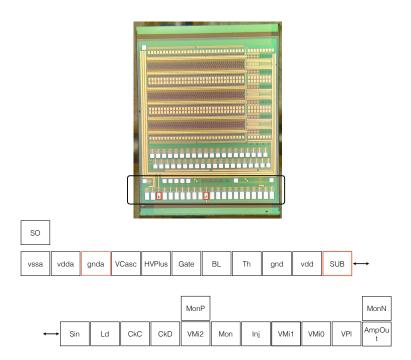


Figure 5.3: Pad scheme for bare HV-CMOS sensor version 4. High-voltage is connected to "SUB" pad while "gnda" to the electrometer ground.

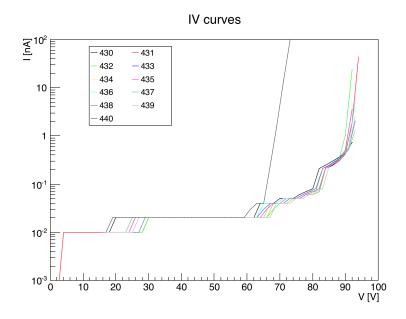


Figure 5.4: I-V curves for several version 4 bare sensors.

Appendix 2: G01 results

Additional results with a version 2 sensor (G01) are shown in this appendix. This unirradiated CCPD is glued with SU8 pillars to control the glue thickness, as shown on figure 5.5. Results show that the interpolation tuning works fine with a different assembly.

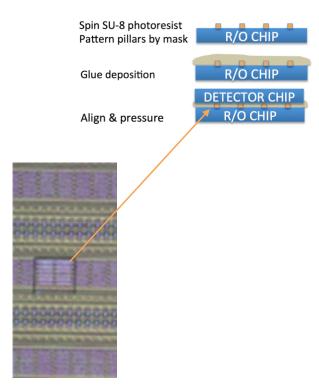


Figure 5.5: G01 is a CCPD version 2 and glued with SU8 pillars in order to control the glue thickness.

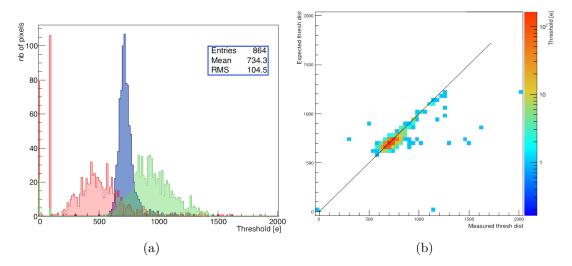


Figure 5.6: (a) Threshold distributions before and after the tuning for a version 2 sensor (G01). The red and green distributions represent a uniform TDAC configuration set at 4 and 9, respectively, while the blue represents a TDAC configuration tuned by the interpolation method. The two red peaks are due to very noisy pixels for which the S-curve measurement failed, the TDAC value was not adapted in those cases. (b) Correlation plot between the expected threshold distribution from the tuning and the measured one.