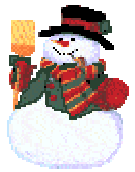
UNIVERSITÉ
DE GENÈVE
FACULTÉ DES SCIENCES
DPNC



# Electronics Highlights 2011

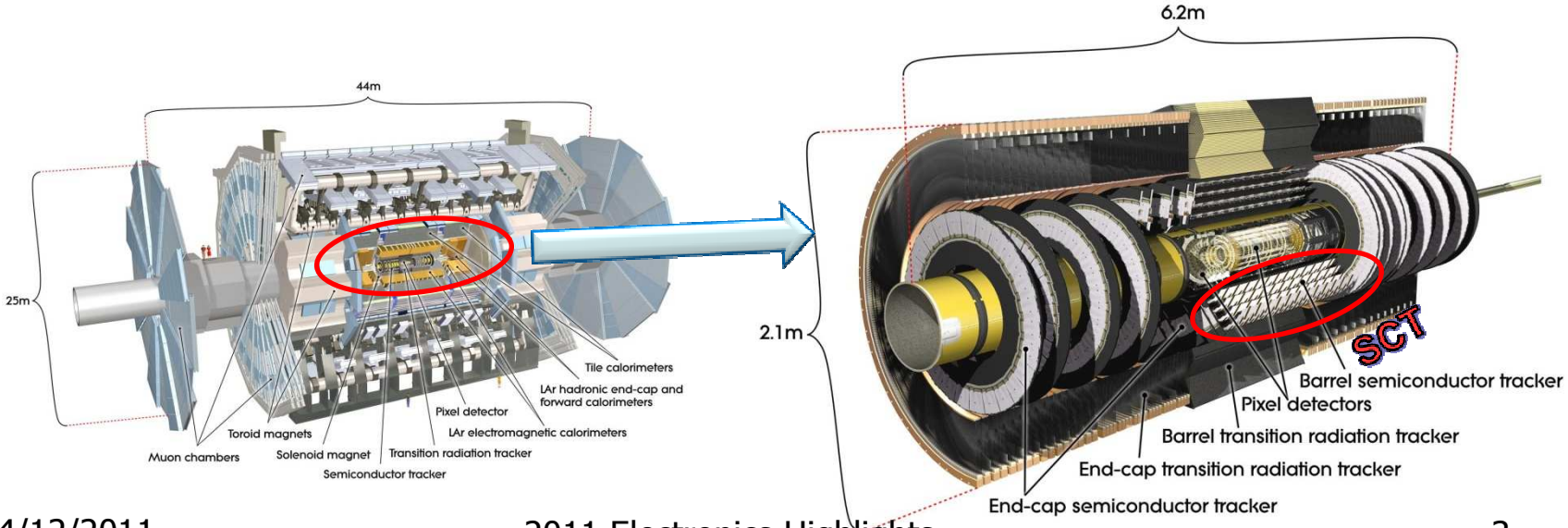
*Yannick FAVRE*

# Electronics group

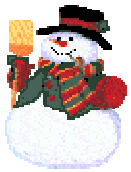
- 3 Engineers
  - Daniel La Marra
  - Stéphane Débieux
  - Yannick Favre
- 2 technical assistants
  - Gabriel Pelleriti
  - Javier Mesa

# **ABCn-130 chip :** Analog Binary Chip

- **Context :**
  - ATLAS Upgrade, Semi-Conductor Tracker detector (SCT)
  - Collaborative team for improvement of the Frond-End chip
  - Verilog programming  (Hardware language similar to VHDL)
  - Planned submission to chip foundry : end of 2012
  - Installed chips : 350,000 (> 2020 integration)
  - Digital blocs development : Daniel La Marra (2011-2012)

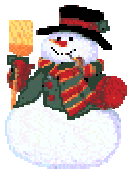


# **ABCn-130 :** Main improvements

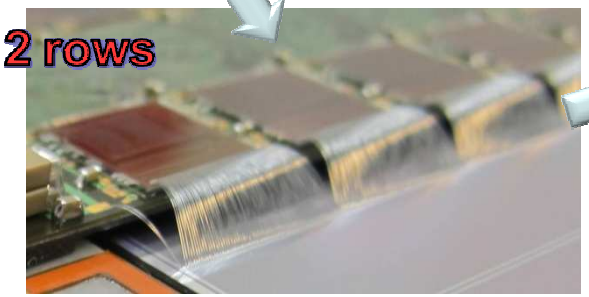


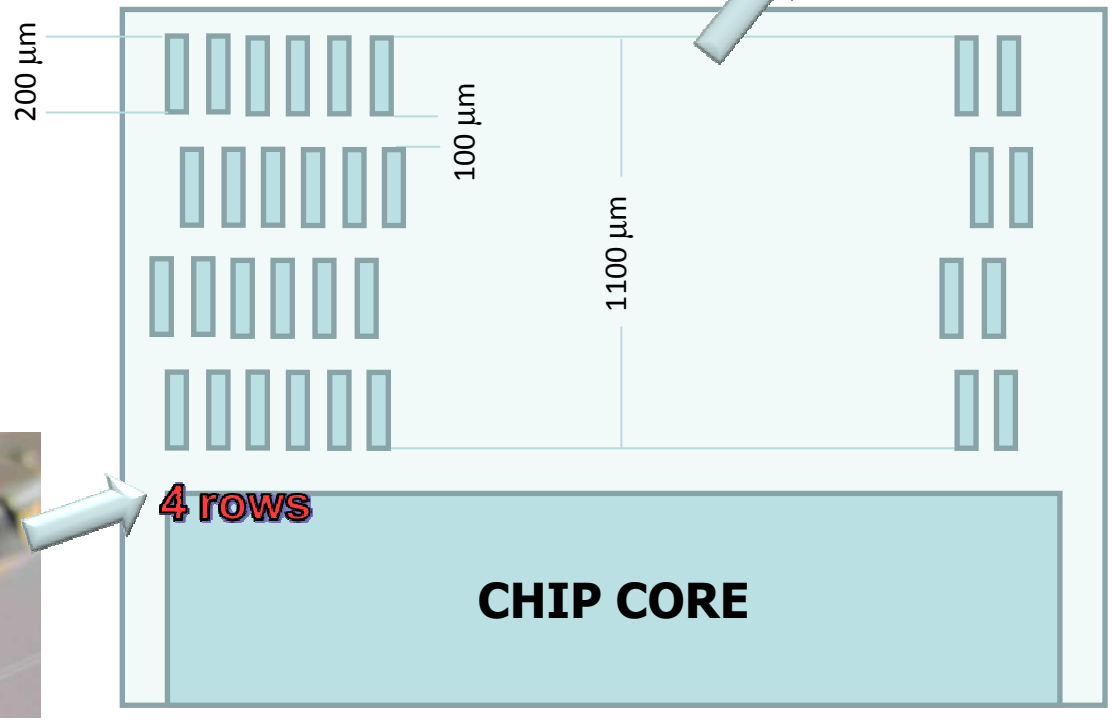

| | **ABCn-250** | **New ABCn-130** |
|---|---|---|
| Technology: | 250nm | 130nm |
| # channels: | 128 | 256 |
| Data rate: | 40 Mbit/s | 80 Mbit/s |
| Data flow : | Variable | Fixed (data rate increase) |
| TX Chain (chip to chip) | Hardware token signal | Software Xon/Xoff (more flexibility) |
| Single Event Upset Protection | none | Configuration choice :<br>- Watchdog or<br>- 3X Flip Flop + vote or<br>- Hamming code |
| # buffer levels: | 1 | 2 (L0 & L1 triggers) |

# **ABCn-130 :** Front-End bonding



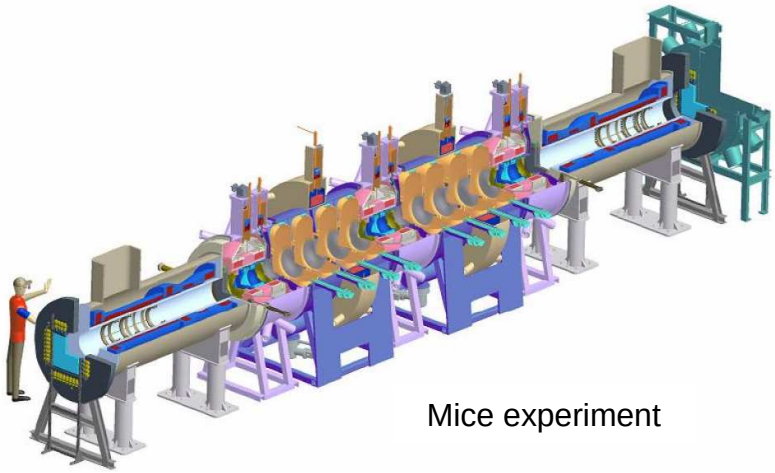
## Challenge for bonding

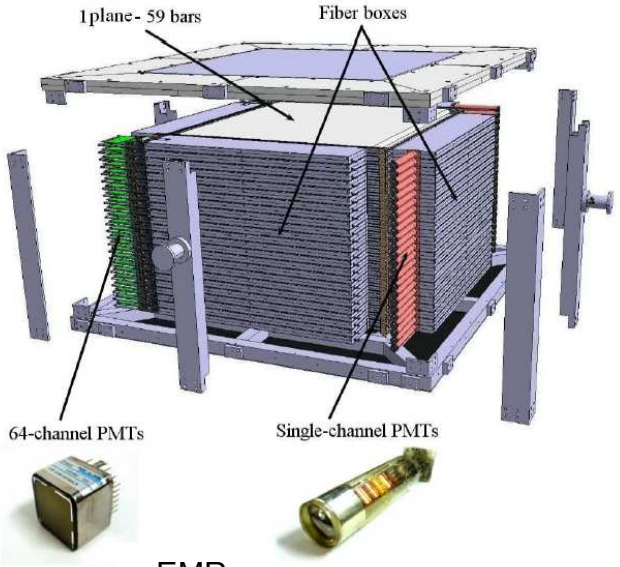



# **DBB :** Digitizer & Buffer Board

- **Context :**
  - MICE experiment (RAL/UK)
  - Electron Muon Ranger detector (EMR)
  - Part of a collaborative team with the Front End Board
  - Board & FPGA design + test : Stéphane Débieux



Mice experiment

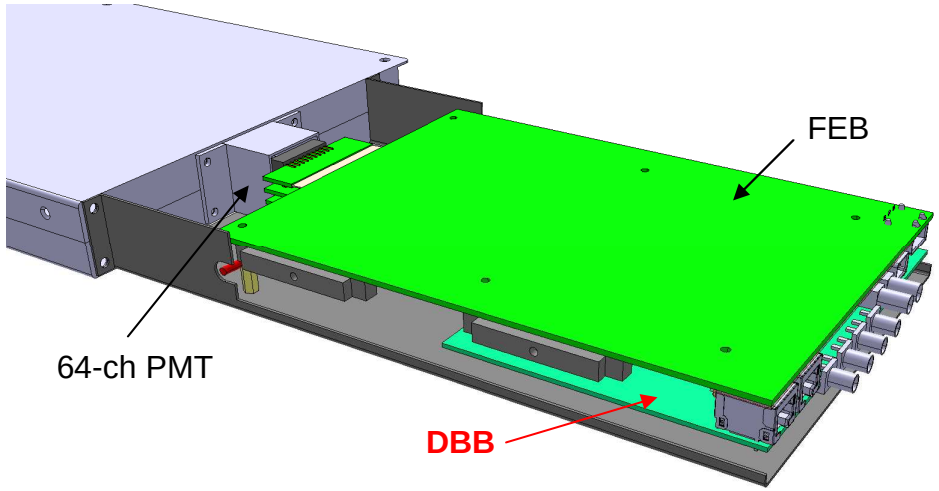



EMR

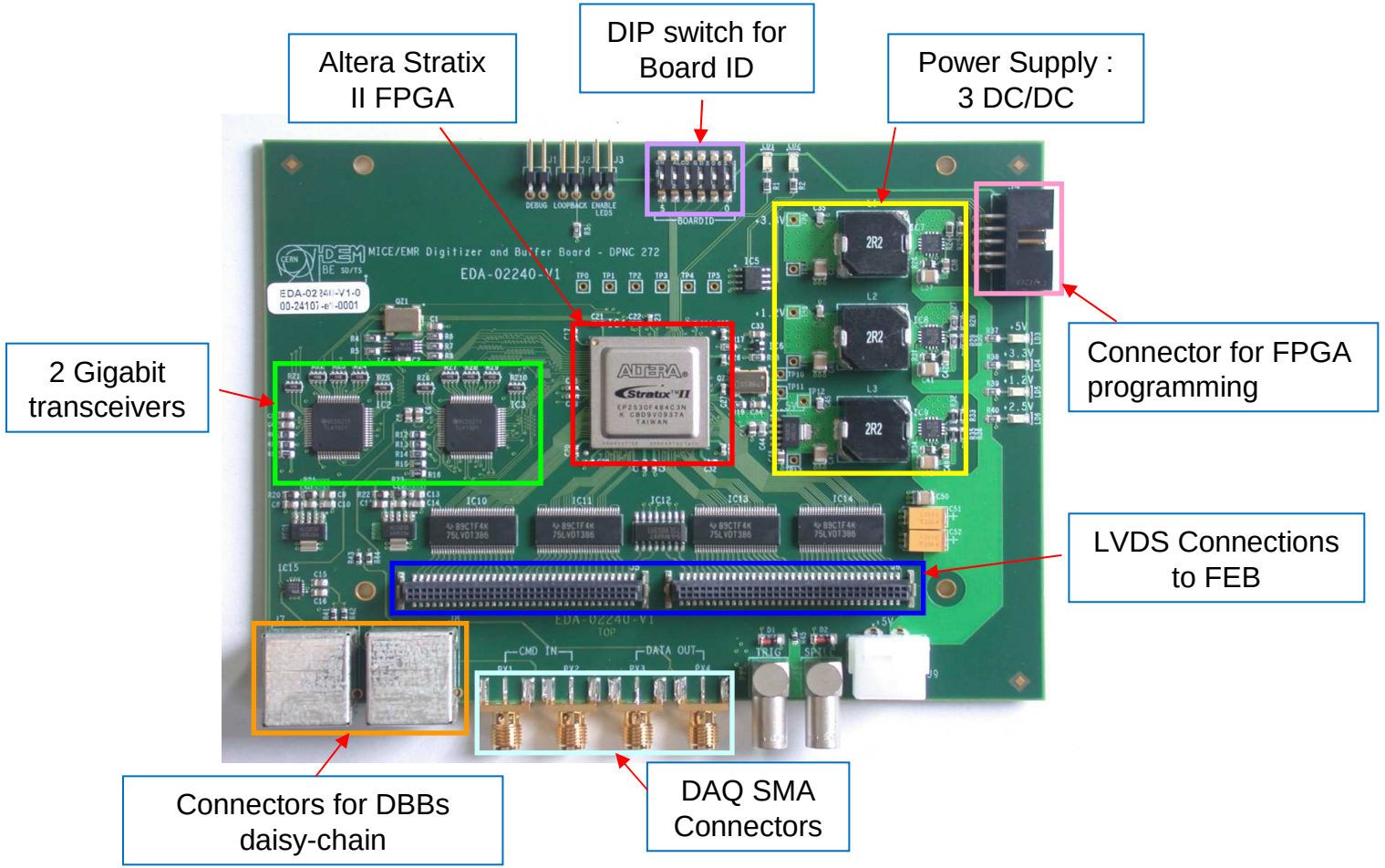
# **DBB :** Main characteristics

**Characteristics :**

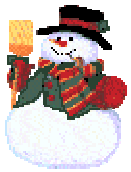
- 64 channels sampling from Front-End Board (FEB) at 400 MHz
- Event data storage and transmission upon request from DAQ over gigabit link
- Implementation of a set of commands according to a simple communication protocol
- 6 daisy-chained DBBs
- Total of 8x6=48 FEB-DBB assemblies



# **DBB :** Overview



# **DBB :** Test setup



PC Software for DAQ configuration

DAQ system on VME crate

FEB signals simulation board
*(D.LaMarra testbench on Altera FPGA)*

DBB with DAQ Gigabit connections to VME

# **DBB :** Current status

- Integrated in the detector with 6 layers at Geneva
- Tested with positive results in June at RAL
- Need further investigation and tests in laboratory to evaluate possible improvements both hardware and firmware
- Planning for volume production required : target May 2012