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Production, integration and commissioning of the ATLAS Insertable B-Layer and test beam studies of new pixel technologies for the HL-LHC

THÈSE

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"Production, Integration and Commissioning of the ATLAS Insertable B-Layer and Test Beam Studies of New Pixel Technologies for the HL-LHC"

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Thèse - 4901 -

Le Doyen

"Men are just beginning to propose questions and find answers, and we may be sure that no matter what question we ask, so long as it is not against the laws of nature, a solution can be found."

Thomas Alva Edison

Acknowledgements

Résumé

Le Grand collisionneur de hadrons (the Large Hadron Collider, LHC) au CERN fournit des collisions proton-proton depuis 2009. Afin d'améliorer les conditions de fonctionnement et les performances de l'accélérateur, ce dernier opère en alternant des périodes bien définies de prise de données pour les différentes expériences physiques, ainsi que des périodes d'arrêt, où des opérations de maintenance et d'améliorations sont conduites en vue d'augmenter l'énergie du faisceau et la luminosité opérationnelle de l'accélérateur. Ces périodes d'arrêt sont également l'occasion pour les différentes expériences de physique de réparer et adapter en conséquence leurs diverses technologies de détection.

Lors du premier arrêt technique du LHC (2012-2014), une nouvelle couche de détection a été installée dans le détecteur à pixels de l'expérience ATLAS, le Insérable B-Layer (IBL). Cette nouvelle couche de détection donne une quatrième mesure pixel, augmentant ainsi la redondance contre la détérioration du détecteur due aux radiations et ainsi permettant d'assurer une reconstruction des traces avec une haute efficacité dans les prochaines années de prise de données. Le détecteur IBL est composé de quatorze supports mécaniques (*staves*) équipés de capteurs au silicium. Dans la première partie de cette thèse, nous décrivons en détail la production et le contrôle qualité des modules et des *staves* IBL. Ces étapes sont suivies par la phase de mise en service et de qualification lors de l'intégration du détecteur ainsi qu'après son l'installation dans l'expérience ATLAS.

Le programme du LHC sera prolongé pour une nouvelle décennie par le LHC à haute luminosité (HL-LHC), dans lequel la luminosité intégrée sera augmentée d'un ordre de grandeur pour atteindre finalement les $300 \, \text{fb}^{-1}$. Dans la phase de R&D en cours pour le HL-LHC, des nouvelles technologies pour des détecteurs résistants aux radiations sont en cours de développement. En particulier, la technologie de capteurs CMOS à haute tension (HV-CMOS), basée sur des procédés de fabrication industrielle, a été développée et étudiée pour la réalisation de détecteurs au silicium hautement résistant aux radiations. Dans le contexte de ces études, un nouveau télescope (appelé "télescope FE-I4") a été conçu et réalisé par l'Université de Genève. Il permet lévaluation de la performance des nouveaux prototypes de détecteurs à pixel lors de l'acquisition de données dans un test faisceau. Dans la deuxième partie de cette thèse, le télescope FE-I4 et les résultats obtenus pendant les tests faisceaux des nouveaux détecteurs HV-CMOS sont présentés.

Abstract

The Large Hadron Collider (LHC) at CERN is providing proton-proton collisions since 2009. The accelerator is alternating a series of periods of physics data-taking of the different experiments and well-defined shut-down periods in which the beam energy and the delivered luminosity are being increased, until reaching the final operating conditions.

During the first long shut-down of the LHC (2012-2014), a new Pixel Detector layer (the Insertable B-Layer, IBL) has been installed in the ATLAS Detector. This new layer will provide a fourth precise measurement from the Pixel detector to add redundancy against radiation damage and to ensure a high-quality tracking over the coming years of data taking. The IBL detector is composed of fourteen mechanical staves equipped with silicon sensors. In the first part of this thesis we describe in detail the production and quality assurance of the IBL modules and staves. We then report on the commissioning phase during the detector integration and after the installation in the ATLAS experiment.

The LHC physics programme will be extended by another decade in the so-called High-Luminosity LHC (HL-LHC), in which the integrated luminosity will be increased by one order of magnitude to reach 300 fb^{-1}. In the current R&D phase for the HL-LHC, new radiation-hard detector technologies are under development. In particular, the High-Voltage CMOS sensor technology based on commercially available manufacturing processes has been developed and studied as a high efficient radiation tolerant detector. In this respect, a new tracking telescope (so-called "FE-I4 telescope") has been designed and produced by the University of Geneva, allowing the evaluation of the performance of new pixel detector prototypes with test-beam data. In the second part of this thesis, the FE-I4 telescope and the test-beam results obtained on the new High-Voltage CMOS detectors are presented.

Contents

Nomenclature

4-PDR	4-Pixel Digital Region
ALICE	A Large Ion Collider Experiment
AMS	Austria Micro Systems
ASIC	Application-Specific Integrated Circuit
ATCA	Advanced Telecommunications Computing Architecture
ATLAS	A Toroidal LHC ApparatuS
BC	Bunch Crossing
CAD	Computer Aided Design
CAN	Controller Area Network
CCA	Connected Component Analysis
CCPD	Capacitive Coupled Pixel Detector
CERN	Conseil Européen pour la Recherche Nucléaire
CIM	Cluster Interconnect Module
CMOS	Complementary Metal Oxide Semiconductor
CMS	Compact Muon Solenoid
CSC	Cathode Strip Chambers
CTE	Coefficients of Thermal Expansion
DAC	Digital to Analog Converter
DC	Double-Chip
DCS	Detector Control System
DM	Dark Matter
DRIE	Deep Reactive Ion Etching
DUT	Device Under Test
EMcal	Electromagnetic Calorimeter
ENC	Equivalent Noise Charge
EoS	End-of-Staves
FE	Front-End
FPGA	Field-Programmable Gate Arrays
FTK	Fast TracKer
GUI	Graphical User Interface
Hcal	Hadronic Calorimeter
HEP	High Energy Physics
HL-LHC	High-Luminosity LHC
HLT	High Level Triggers
HSIO	High Speed Input/Output
HV	High Voltage
HV-CMOS	High-Voltage Complementary Metal Oxide Semiconductor
IBL	Insertable B-Layer
IC	Integrated Circuit
ID	Inner Detector
IPT	Inner Positioning Tube
IST	Inner Support Tube
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LINAC	Linear Particle Accelerator
LS	Long Shut down
LV	Low Voltage
LVDS	Low Voltage Differential Signal
LVTTL	Low Voltage Transistor-Transistor Logic
MAPS	Monolithic Active Pixel Sensors
MC	Monte Carlo
MCC	Module-Control Chip
MIP	Minimum Ionising Particles
MOS	Metal-Oxide-Semiconductor
MTD	Monitored Drift Tubes
NI	National Instrument
NMOS	N-type Metal-Oxide-Semiconductor
NNC	Neural Network Clustering
nSQP	New Service Quarter Panels
NTC	Negative Temperature Coefficient
PCB	Printed Circuit Board
PEEK	Polyether Ether Ketone
PMOS	P-type Metal-Oxide-Semiconductor

PS	Proton Synchrotron		SM	Standard Model
PSB	Proton Synchrotron Booster		SMD	Surface Mounted Device
QA	Quality Assurance		SPS	Super Proton Synchrotron
QCD	Quantum Chromo Dynamics		SUSY	Supersymmetry
RCE	Reconfigurable Cluster Element		TFoM	Thermal Figure of Merit
RF	Radio Frequency		TGC	Thin Gap Chambers
RMS	Root Mean Square		ToT	Time over Threshold
ROI	Region Of Interest		TRT	Transition Radiation Tracker
RPC	Resistive Plate Chambers		VDDA	Voltage Drain Analog
SC	Single-Chip		VDDD	Voltage Drain Digital
SCT	Semiconductor Tracker		WIMP	Weakly interacting massive particles
SDA	Smart Diode Array		*ndof*	Number of degrees of freedom

The Standard Model and Beyond

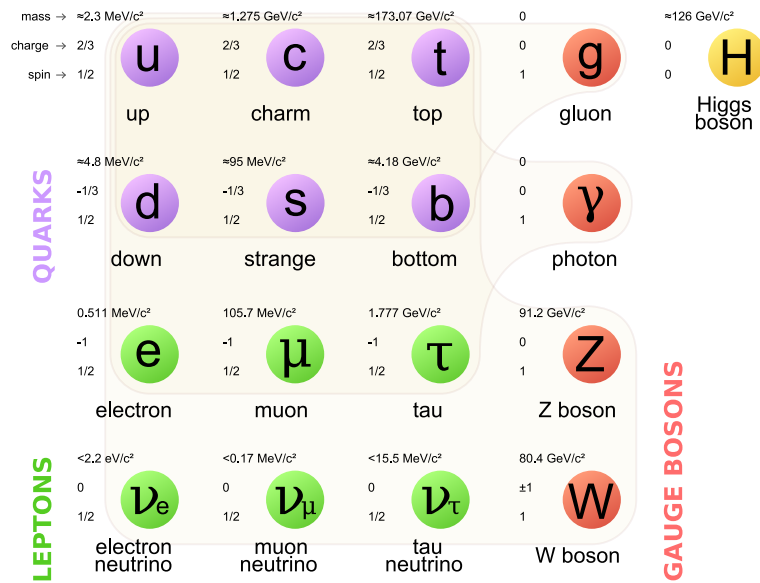## 1.1 The Standard Model of Particle Physics

The "Standard Model" of particle physics, developed in the second half of the 20th century, constitutes our present understanding of all matter, its constituents and their interactions. The Standard Model (SM) gained popularity in the 1970s upon experimental confirmation of the existence of quarks and the discovery of the J/ψ meson[1] [1]. The SM provides a theory framework based on quantum field theory, that incorporates all that is known about subatomic particle interactions through electromagnetic, weak, and strong forces. Furthermore, conservation laws such as energy and electric charge derived from the gauge invariance and symmetries, are intrinsic to the SM and defines the decay modes of unstable particles into more fundamental ones, as observed experimentally.

The SM is composed of the elementary particles of Figure 1.1. They are grouped in families based on their properties and interactions. The SM includes twelve *fermions* with spin 1/2 (and their equivalent 12 antiparticles), composing what we commonly understand as "matter" (and "antimatter"). Additionally to the *fermions*, five *bosons* (defined as particles with integer spin) complete the SM. Vector bosons (i.e. the photon, the Z^0 and the $W^\pm$), are the carriers of the three forces described by the SM. Finally the Higgs boson (with spin zero) completes the SM.

Fermions are grouped evenly in two different families, *leptons* and *quarks*, depending on how they interact.

• *Leptons* are defined as *fermions* that do not undergo strong interactions. In total there are six leptons [2]. Organised in doublets, the first generation comprises the electron (e) and the electron neutrino (ν_e); the second the muon (μ) and muon neutrino (ν_μ); and the third the tau (τ) and the tau neutrino (ν_τ). *Lepton* doublets are organised by their mass, where heavier leptons can decay into lighter charged *fermions* via the weak interaction (Figure 1.2). Indeed *leptons* are subjected to two fundamental interactions: the weak interaction via the weak charge (weak isospin) and gravitation via their mass; additionally, charged leptons (excluding neutrinos which are electrically neutral) are subjected to the electromagnetic via their electric charge.

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[1]Mesons formed by a bound state of a charm quark and a charm anti-quark are generally known as "charmonium"

Figure 1.1 – The elementary particles of the Standard Model with the three generations of matter, the gauge vector bosons and the Higgs boson.

• *Quarks* in addition to the electroweak interaction are subjected to the strong force. The SM comprises of 6 *quarks* organised in doublets and three generations: the up and down (u, d), charm and strange (c, s), and top and bottom (t,b). Quarks can carry three different strong-force charges, named colours (green, red and blue), and therefore interact via the strong force. Colour singlet combinations of three quarks (baryons) or a quark-antiquark pair (meson) constitutes the strong bounded states we observe. Although each of the *quarks* have a fractional electric charge (-1/3, 2/3) and a colour, *hadrons* have always been observed with an integer electric charge and a neutral colour.
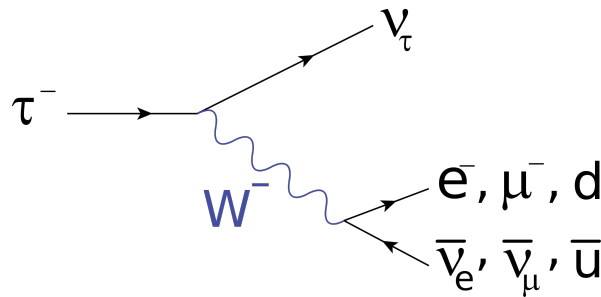
Figure 1.2 – Feynman-Stueckelberg diagram of the electroweak τ decay.

The fermion-to-fermion interactions described above are "transmitted" by the exchange of gauge bosons, which are the spin 1 force carriers.
• **The photon** (γ) is the carrier of the electromagnetic force, exchanged between electrically charged particles. The photon is massless, hence the range of the electromagnetic force is infinite and photons travel at the speed of light.

- **The Z^0 and $W^\pm$-bosons** mediate the weak force. They interact with all fermions (quarks and leptons) via the weak isospin. The vector bosons mediating the weak force, Z^0 and $W^\pm$ have a mass of 91.1876 ± 0.0021 GeV/c^2 and 80.385 ± 0.015 GeV/c^2 respectively [3]. The boson mass, directly responsible for the force reach, introduced an early misconception in the "weak-force" since its coupling constant is much larger than the electromagnetic one, but only accessible at very short distances of the order of (10^{-18} m). Additionally, one of the most relevant features of the weak force is its unique discrimination between matter and antimatter via its charge-parity symmetry violation [4].
- **The gluons** (g) are responsible for the transmission of the strong force between colour-charged particles (i.e. quarks and the gluons themselves). Gluons are massless particles, which exist in eight different colours (as derived from the Gell-Mann matrices in a SU(3) gauge symmetry).

Due to the gluon self-coupling and the strong coupling constant at low energies, the strong field increases with the distance. This particularity of the strong force is responsible for the so-called "colour confinement", i.e. that only colour-singlet particles can be observed. This phenomena can be understood due to the divergency of the energy needed to take apart two colour particles. When both particles are taken away, the energy stored in the field increases until the energy is large enough to create a particle-antiparticle pair out of the vacuum. The recombination of these newly generated particles and the initial ones gives rise to two colour-singlet bound states (hadrons). This process is schematically represented in Figure 1.3. Although gluons are massless bosons and therefore the strong force range should be infinite, due to the colour confinement the strong force can only be observed at small distances.
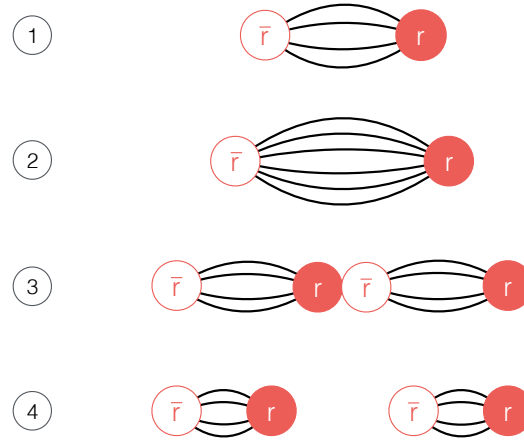
Figure 1.3 – Artistic representation of colour confinement, where a colour singlet is taken apart until a pair of particles is spontaneously created leading to two colour singlets.

For the SM Lagrangian to be gauge invariant for the electroweak force, massless vector-bosons were required [5, 6]. In oder to provide an effective mass to the Z^0 and $W^\pm$, the Higgs mechanism was introduced allowing the spontaneous symmetry breaking of the electro-weak field by the presence of a Higgs field. The Higgs mechanism also predicts the existence of the spin 0 Higgs boson, which was discovered at the Large Hadron Collider in 2012 [7, 8], with a measured mass of 125.09 GeV/c^2 [3]. The Higgs boson was the last missing piece of the Standard Model.

1.2 The Standard Model Limitations

In despite of the success of the SM and its agreement with the experimental observations up to the TeV scale, there are however observations that can not be addressed within the SM. The gravity that has been observed at the macroscopic scale, has not yet been explained by the SM. Although gravity remains very weak at low energies (long distances), it is expected to become strongly coupled at higher energies (close to the Plank scale [9]) and therefore observable at the particle level via the graviton exchange[2]. The coupling of the gravity field being smaller by a factor 10^{16} with respect to the weak force (known as the hierarchy problem), combined with the relatively small Higgs boson mass with respect to the Plank mass [10], requires a delicate cancelation of the quantum corrections of the Higgs mass calculation (fine tuning).

One of the most plausible explanations of the mass hierarchy problem and of the fine tuning may come from a new theory where the relatively small Higgs mass can be protected from the divergent quantum corrections. The hierarchy problem is addressed in an elegant way in Supersymmetry (SUSY) [11], where the divergent terms in the radiative corrections of the Higgs mass can be prevented by the introduction of partner supersymmetric particles. The hierarchy problem can be therefore avoided as long as the supersymmetric particles are light enough [12].

Additionally, from the observation of the dynamics of distant galaxies and the gravitational lensing, it has been postulated that according to our current gravitational models, a mass of the universe significantly larger than the observed one is required [3]. These observations, suggest that only $\sim$16% of the mass in the universe is visible [14, 15], while the remaining 84% is invisible and therefore so-called "Dark Matter" (DM) [16]. Even though many indirect observations of DM at the cosmological scale have been observed since the early 1930's, no direct measurement of DM has been yet performed. Although yet unknown, the most accepted candidate among particle physicists for the DM constituent are the so-called Weakly Interacting Massive Particles (WIMPs)[17]. One of the strength of SUSY is that it provides a WIMP that predicts the correct abundance of dark matter as observed in the Universe.

The search for a direct evidence of new physics, as well as a better measurement of the Standard Model parameters, motivates the continuous effort to explore the boundaries of experimental particle physics.

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[2]The graviton is an hypothetical spin 2 elementary particle that mediates the gravitation in quantum field theory.

[3]Additionally, theoretical models and predictions during the Big Bang nucleosynthesis [13] corroborate the existence of the DM.

The LHC and ATLAS

2.1 The CERN Accelerator Complex

CERN ("Conseil Européen pour la Recherche Nucléaire") is currently the largest particle physics laboratory in the world. Established in 1954, CERN has gradually built and housed large particle accelerators that over time have served as injectors for future accelerators with increased beam collision energies [18]. This historical development can be seen in its accelerator facilities. Figure 2.1 shows the actual CERN accelerator complex. Protons start their acceleration process at a linear accelerator (LINAC), boosting their energies up to 50 MeV in the LINAC 2. At this first acceleration stage, a linear accelerator is used to cope with the protons rapid velocity increase with energy (forcing a custom cavity design over the LINAC length). The LINAC is followed by the Proton Synchrotron Booster (PSB) increasing the energy of the proton beams to 1.4 GeV, after which it is sent to the Proton Synchrotron (PS) to raise its energy to 25 GeV. A larger accelerator of 7 km circumference and 40 m underground, the Super Proton Synchrotron (SPS), boosts the protons energy up to 450 GeV which is the injection energy of the Large Hadron Collider (LHC). With a 27 km circumference and a nominal proton-proton centre of mass energy of 14 TeV, the LHC is currently the largest and most powerful particle collider in the world. The choice for a proton-proton collider (with respect to a lepton collider for example) was motivated by the need to increase the luminosity and energy, that lepton (electrons[1]) colliders can not cope using current technology and facilities.

Protons inside the LHC are accelerated in bunches thanks to radio-frequency (RF) cavities of 2.5 ns length [19]. Given the circumference of the LHC and the RF bunch length, up to 35640 bunches can circulate simultaneously on each of the LHC rings. Although such configuration will allow to achieve very high luminosities (with a theoretical 2.5 ns bunch spacing), due to bunch-to-bunch interaction (cloud effect [20, 21]) and other technical limitations in the LHC and experiments [22], only one out of ten bunches are filled with a final 25 ns "Bunch Crossing" (BC) period. It is important to mention that during Run-I (2008-2013), the LHC has been oper-

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[1]Although lepton collider refers generally to all lepton families, current technology only allows electron colliders. Muon colliders are under study and are particularly interesting for their small synchrotron radiation (proportional to the fourth power of the relativistic gamma factor) but are at present far from a technical realisation.
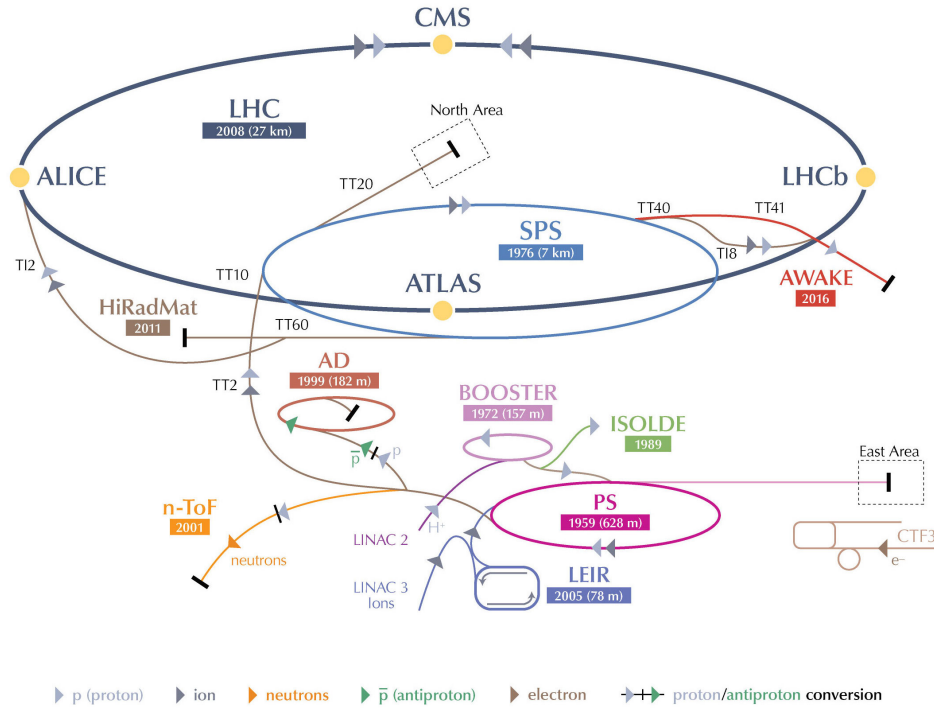
Figure 2.1 – Schematic representation of the CERN accelerator facility and construction date. Additionally to the LHC and its pre-accelerators, other accelerator and decelerator facilities have been developed for Ion acceleration and for other smaller size projects.

ating exceptionally at 50 ns BC due to beam and vacuum instabilities produced by the electron cloud effect [21]. During this period, in order to correct for the instantaneous luminosity decrease without scarifying the final integrated luminosity, more populated proton bunches were circulated. Although these run conditions allowed to increase the luminosity up to $8 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$, they generated a larger number of collisions per bunch-crossing (pileup) and new analysis techniques had to be implemented to correct for the impact of the increased pileup.

The LHC hosts four main experiments: ALICE [23], ATLAS [24], CMS [25] and LHCb [26], located ∼100 m underground in four of the LHC interaction points. While all four experiments look for new physics, ATLAS and CMS were designed to explore a broad range of new possible signatures (so called general purpose detectors) such as the Higgs and beyond the Standard Model scenarios predicted to occur at the TeV energy scale [27]. In addition to such searches, the high luminosity and increased cross-sections at the LHC enable further studies on high precision Quantum Chromo Dynamics (QCD), electroweak interactions, and flavour physics [28, 29]. The increasing cross-section of rare events with the centre of mass energy (Figure 2.2) motivates the quest for higher centre-of-mass energies, where heavier particles are accessible and smaller substructures might arise. The LHC, with a nominal centre-of-mass energy of 14 TeV surpasses by almost an order of magnitude its predecessor (the Tevatron collider at Fermilab) and therefore increases the production of rare events (e.g. Higgs production) increases by a factor of $\sim 10^2$. Unfortunately at the beginning of Run-1, a large power dissipation in the superconducting splices of the cryostat dipoles imposed the choice to run the LHC at a reduced centre-of-mass energy of 8 TeV. During the Long Shut Down 1 (LS1) in 2013-14, all the defective superconducting splices were repaired and in 2015 the LHC resumed with 13 TeV collisions.
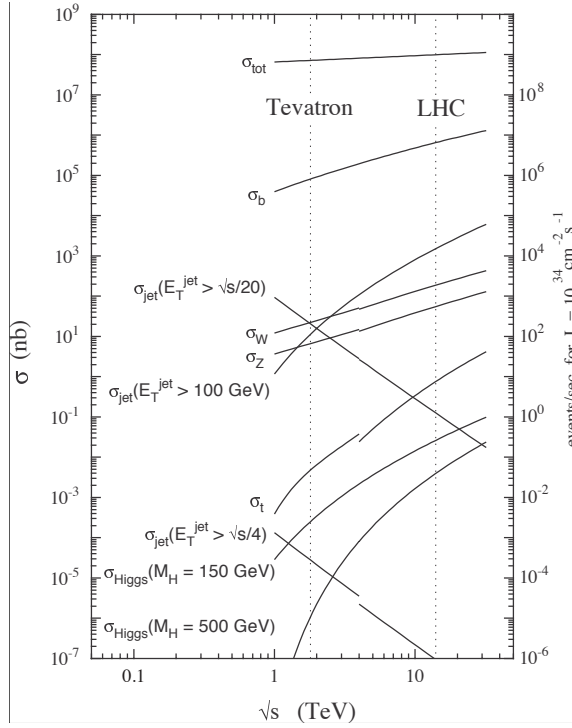
Figure 2.2 – Cross sections for several processes in proton–proton collisions as a function of centre-of-mass energy. [30]

2.2 The LHC Program

The LHC operation program is divided in Runs followed by Long Shut down periods, where maintenance and machine upgrades are performed. Machine upgrades aim to increase the luminosity and energy delivered. Although the schedule is always subject to mid and long term modifications, the current LHC upgrade plan is presented in Figure 2.3. As it can be seen until 2022, every $\sim$3.5 years a Long Shut down is scheduled with a subsequent luminosity increase (accelerator upgrade). In the longer term (2025-2035), a High Luminosity LHC (HL-LHC) is under study [31].

- During Run-I the LHC has been running with an instantaneous luminosity below $8 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$, as shown in Figure 2.4. As it can be observed, the peak luminosity increased during Run-I thanks to the accelerator optimisation, such as beam emittance, increasing the number of particles per bunch and LHC fine tuning. During **LS1**, the 10 000 superconductive soldering between dipole magnets have been repaired in the LHC cryostats in order to prevent quenching at high currents. Additionally, the entire ventilation system for the 628 m circumference PS has been replaced, as well over 100 kilometres of cables on the SPS. This LS1 intervention allowed the LHC to raise its energy to 13 TeV in 2015, since early Run-II. Although a 25 ns BC has been adopted after the LHC commissioning in Run-II, in order to reduce the bunch-to-bunch interactions smaller proton bunches have been circulated reducing significantly the initial peak luminosity as shown in Figure 2.4. Similarly to Run-I, thanks to the fine tuning of the LHC and larger proton bunches, the peak luminosity has increased over Run-II until reaching $5 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$ in December 2015 and targeting $1 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ by end of Run-II.
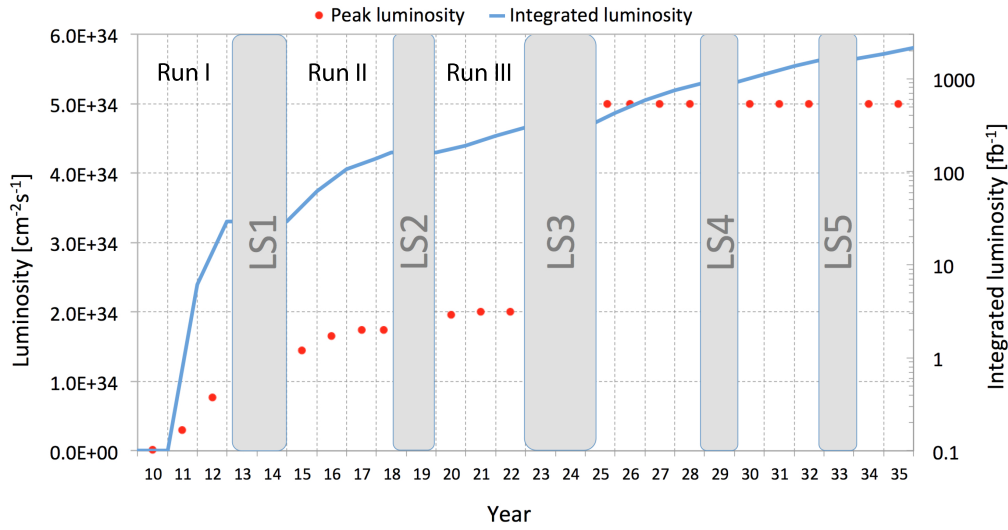
**Figure 2.3 –** LHC schedule and expected peak and integrated luminosity.

- After Run-II and 350 fb^{-1} integrated luminosity, the LHC will undergo a major upgrade to increase its luminosity to 2-3 $\times 10^{34}$cm^{-2}s^{-1} during **LS2** from 2018 to 2019. Two major upgrades are scheduled during **LS2**. Firstly, the commissioning of the LINAC 4 replacing the current LINAC 2 and increasing the brightness of the PSB by a factor two. Additionally, the upgrade of the LHC collimation system, reducing the beam size at the iteration point allowing the luminosity increase.

- A second major machine upgrade is planed during **LS3** in 2023 for about 2 years, to allow the luminosity to increase above 5×10^{34}cm^{-2}s^{-1} (HL-LHC). This significant luminosity upgrade will only be achievable by a major update of the full accelerator chain optics, decreasing the losses and improving the beam focus at collision points. At very high luminosities and energies, due to the proton proton collisions a significant wear of the beam is expected. Therefore, in order to achieve a total integrated luminosity of 3000 fb^{-1} by $\sim$2035, new refill techniques need to be developed [32].

2.3   The ATLAS Experiment

The LHC houses four main experiments, providing hadron collisions at unprecedented center-of-mass energy and luminosity. ATLAS, one of the two general-purpose detectors, was designed to fully exploit the LHC discovery potential. The ATLAS experiment therefore needs to be efficient in the identification of the particles emerging from the proton-proton collisions, by measuring their transverse momentum (p_T), energy and charge. From the fact that the LHC provides proton-proton collisions, the ATLAS detector has to deal with a very dense particle environment, including large multi-jet production, multiple vertices in the same event, etc. Therefore, high precision tracking with vertex identification is needed up to the TeV scale. The LHC energy range represents a challenging environment for the detector operation and design, pushing the frontiers of the available technology.
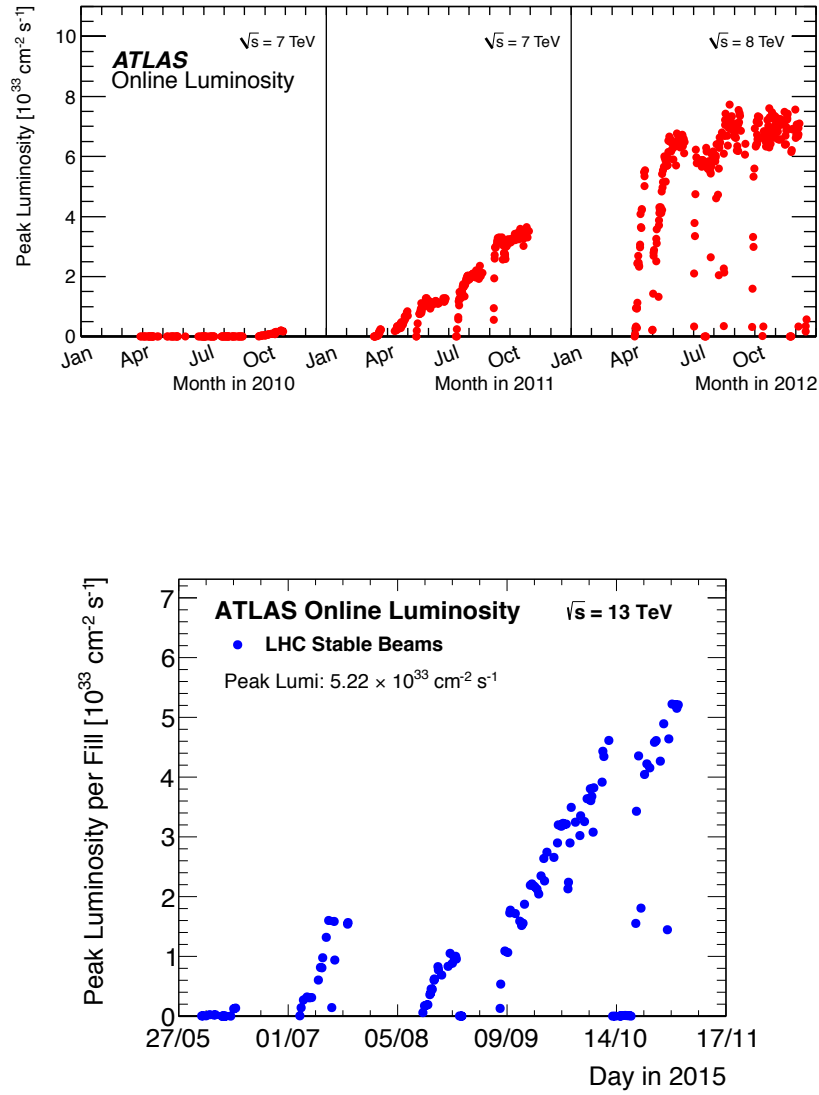
Figure 2.4 – The peak instantaneous luminosity delivered by LHC versus time during the p-p runs of Run-I (top) and ongoing Run-II (bottom). The online luminosity measurement is used for these plots.
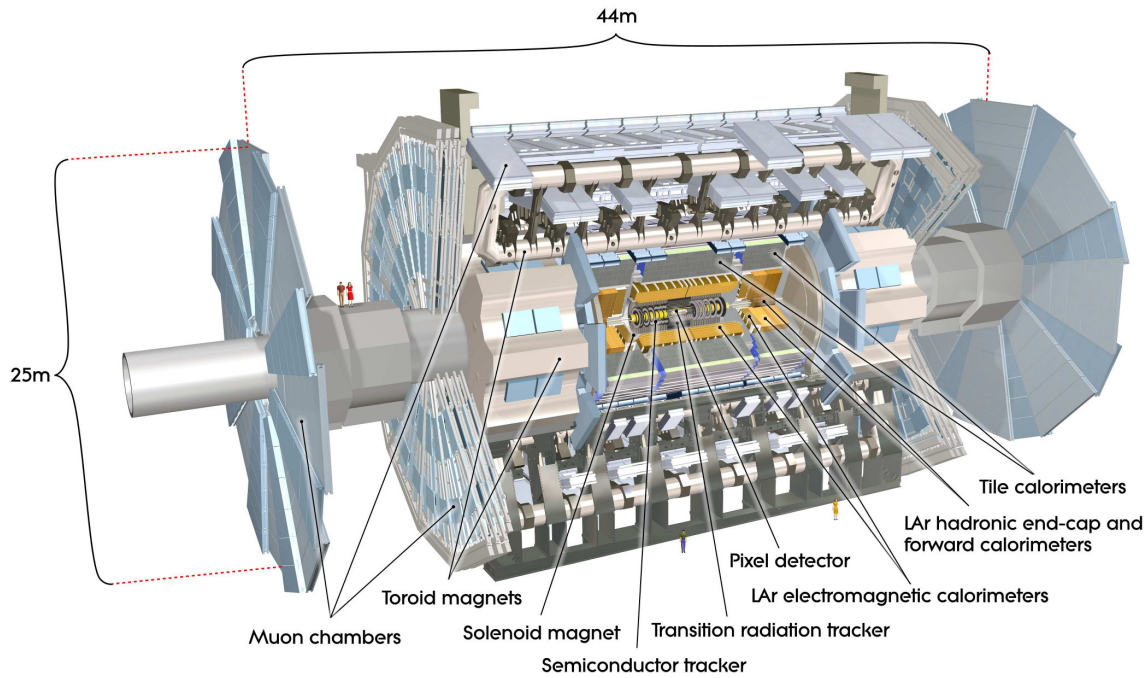
Figure 2.5 – Cut-away view of the ATLAS detector. The dimensions of the detector are 25 m in height and 44 m in length. The overall weight of the detector is approximately 7000 tonnes. [24].

2.3.1 Detector Overview

The ATLAS detector design started 25 years ago and regroups nowadays a very large community of scientists, with more than three thousand physicists and engineers all over the world from 187 institutes. The ATLAS detector, has a cylindrical shape around the beam axis with a "cap" on each extremity for hermiticity. With a radius of 12 m and a length of 44 m and an overall weight of 7000 tonnes, the ATLAS detector is composed of several sub-detectors as shown in Figure 2.5.

The full event reconstruction of a proton-proton collision makes use of all the different sub-detectors. Figure 2.6 shows schematically the different signatures of each particle type. As it can be observed, each sub-detector is responsible for specific measurements and only the combined information from all of them allows the full reconstruction of the event properties. The main ATLAS sub-detectors are briefly described in the following list:

- **Inner Detector (ID)**: it is responsible for the charged-particles track reconstruction, it allows to identify primary and secondary vertices, while at the same time measuring charge particles momentum by their deflection in a 2T solenoidal magnetic field. Additionally, ionisation energy deposition can be also retrieved for particle identification.

- **Electromagnetic Calorimeter (EMcal)**: it is located around the Inner Detector; electrons and photons entering the EMcal produce particle showers due to the electromagnetic interactions and therefore releasing all their energies in the liquid argon of the EMcal cells. Given the segmentation of the calorimeter, electrons, photons and early hadronic showers can be discriminated based on the shape of the energy deposit in the EMcal.
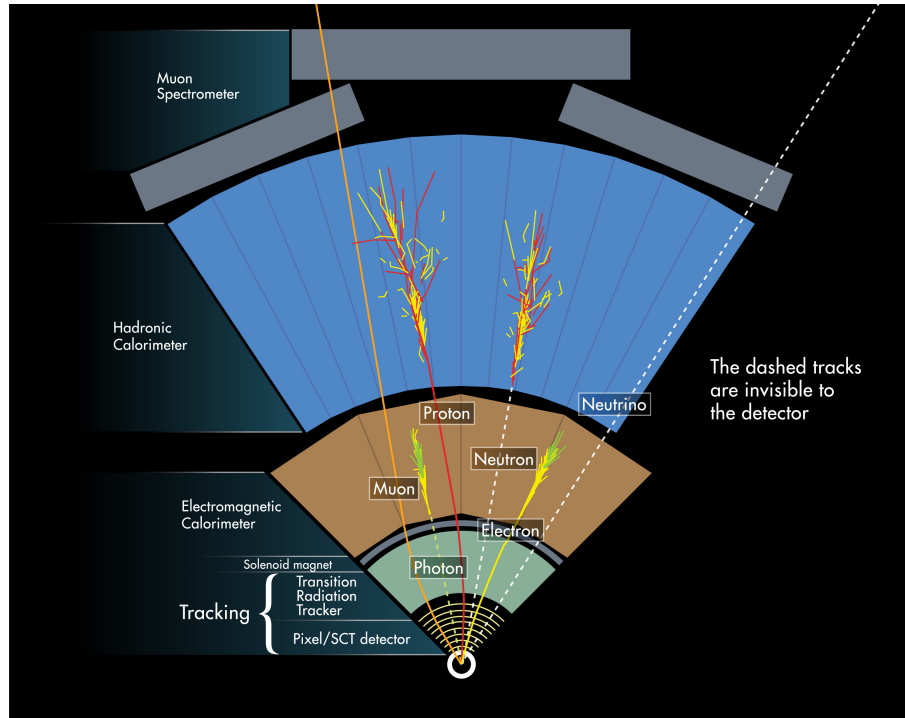
Figure 2.6 – Principle of operation of ATLAS at the LHC. The detection of basic elementary particles emanating from hadron collisions is illustrated: charged hadrons and electrons produce tracks in the Inner Detector; electrons and photons are absorbed and their energy is measured in the electromagnetic calorimeter; hadrons deposit a small fraction of their energy in the electromagnetic calorimeter and are totally absorbed in the hadronic calorimeter, where their energy is measured; finally, muons are the only charged particles that escape both calorimeters and produce tracks in the Muon Spectrometer, as well as in the Inner Detector. [33]

- **Hadronic Calorimeter (Hcal)**: outside the EMcal, the Hcal measures the energy of hadrons. Hadrons penetrate through the EMcal and are stopped in the Hcal where dense material is used to stop these particles, producing hadronic showers in the various layers of the calorimeter system. Thanks to the usage of dense material, high energy showers can be measured allowing at the same time access to measure the jets sub-structure with a fine granularity [34].

- **Muon System**: The muon spectrometer is the outermost layer of the ATLAS detector and it is immersed in a toroidal magnetic field of $\sim$0.5 T, providing an accurate muon identification and momentum measurement [35]. Different gas detector technologies are used in the muon system to cope with the different occupancies. In the central region, Monitored Drift Tubes (MDT) are used to provide an accurate measurement on the bending direction. At higher pseudo-rapidities ($2.0 < \eta < 2.7$), higher granularity Cathode Strip Chambers (CSC) are used to withstand the high background rate. Additionally to the muon spectrometer, Resistive Plate Chambers (RPC) and Thin Gap Chambers (TGC) are used in the barrel and End-Cap regions respectively for the trigger.

Due to the ~ 100 million of channels within ATLAS and the 40 MHz collision rate of the LHC, a dedicated complex trigger strategy for data reduction needed to be implemented. The ATLAS trigger system is organised in three levels: Lv1, Lv2 and Lv3. This multi-level trigger architecture is needed in order to cope with the very high rates of LHC and due to the bandwidth and computing process limitation. Each level refines the decisions made at the previous level by applying additional selection criteria and increasing the selection complexity. The Lv1 is a fast trigger based on custom made electronics that, by combining the Muon Trigger System and the Calorimeter signals, is able to discriminate among events. It generates *Lv1 accept* signals at a rate up to about 100 kHz and defines "Regions of Interest" for the subsequent levels. Lv2 and Lv3 (so called High Level Triggers, HLT), are entirely based on commercially available computers and networking hardware. Thanks to the parallelised computing power, the HLT exploits the full sub-detectors potential and granularity. Events passing the Lv2 trigger ($\sim$3.5 kHz), are then fully reconstructed by the Lv3. Carrying out a selection using offline analysis procedures, a processing time of the order of few seconds is required with a maximum output trigger rate of 200 Hz [24].

The detector hermiticity allows also the measurement of the missing transverse momentum which is produced by the escaping particles (such as neutrinos or new exotic particles).

In the following sub-section for the sake of this thesis, the Inner Detector will be covered in detail.
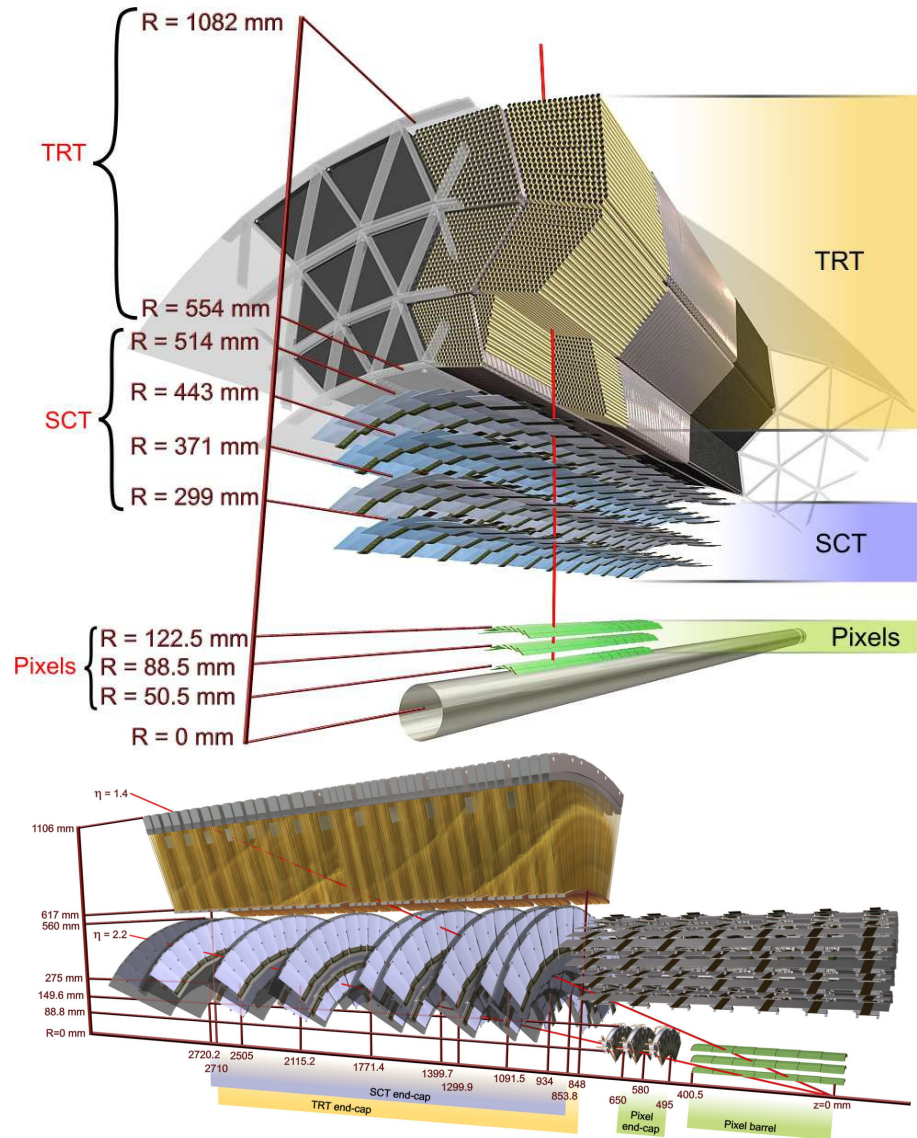
2.3.2   The ATLAS Inner Detector

As shown in Figure 2.7, the Inner Detector (ID) is composed of three subsystems: the Pixel Detector, the Semiconductor Tracker (SCT) and the Transition Radiation Tracker (TRT). The ID was designed to reconstruct the momentum of charged particles in the transverse plane up-to the TeV scale. Thanks to its high pointing resolution, it also provides primary and secondary vertices identification. Silicon based detectors are being used in the innermost layers for their excellent position resolution (of the order of microns), low material budget and high radiation hardness.

The ATLAS Pixel Detector   Composed (in Run-I) of three layers at a radius of 50.5 mm, 88.5 mm and 122.5 mm, the ATLAS Pixel Detector system is responsible for track reconstruction near the collision point, and its resolution determines primarily the ability of the ID to identify primary and secondary vertices. Therefore, the innermost pixel layer, the so called the B-layer, is located as close as possible to the interaction point to provide the highest impact parameter resolution. Additionally, the Pixel Detector required the most cutting edge sensor technology to meet not only the space-point resolution of ($\sim$12 µm, $\sim$90 µm) in the ($R\phi$, z) ATLAS coordinate system and the low occupancy requested[2], but also the very demanding specifications on radiation hardness, of up to 50 MRad and 10^{15} 1-MeV-neutron-equivalent fluence (neq/cm^2).

Each of the pixel modules is composed of an oxygenated n-in-n silicon sensor of 2×6 cm^2 and 250 µm-thick, readout by sixteen 200 µm thinned Front-End (FE) chips connected via bump-bonding with a 50 µm pitch. All 16 FEs communicate with the off-detector electronics via a module-control chip (MCC) loaded on a kapton-flex hybrid glued onto the back side of the sensor and wire bonded to the 16 FEs. A schematic view of a pixel module can be seen in Figure 2.8. The final sensor design has 41984 "standard" pixels of 50×400 µm^2 and 5284 "long" pixels of 50×600 µm^2 located in the boundaries between FE, to cover the gap and minimising the inactive regions.

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[2]The occupancy is defined as the ratio of firing channels over all active channels.

R = 1082 mm

TRT

R = 554 mm
R = 514 mm

SCT

R = 443 mm
R = 371 mm
R = 299 mm

Pixels

R = 122.5 mm
R = 88.5 mm
R = 50.5 mm

R = 0 mm

TRT

SCT

Pixels

Figure 2.7 – Inner detector sensors and structural elements in barrel (top) and End-Cap regions (bottom) [24].

The FE-I3 is the pixel read-out ASIC. It matches the sensor matrix with 2880 individual charge-sensitive analogue pixels, readout by 40 MHz clocked digital circuits. The analogue part consists of a double stage high-gain DC-coupled preamplifier and a differential discriminator. The threshold of the discriminator ranges up to 6000 e$^-$, its nominal value being 3000 e$^-$. Thanks to the Time over Threshold information and the offline clustering algorithm, a position resolution in the azimuthal axis of better than 10 μm after irradiation is expected.

Mechanically, the barrel and the End-Cap disks are supported by a carbon-fiber shell hosting the pixel modules as well as the services (grouped in service panels). The carbon fiber structure as well as the services were designed in oder to minimise the material budget of the Pixel Detector, limiting multiple scattering and secondary interactions. Figure 2.9 summarises the Pixel Detector radiation length breakdown as a function of the pseudorapidity.
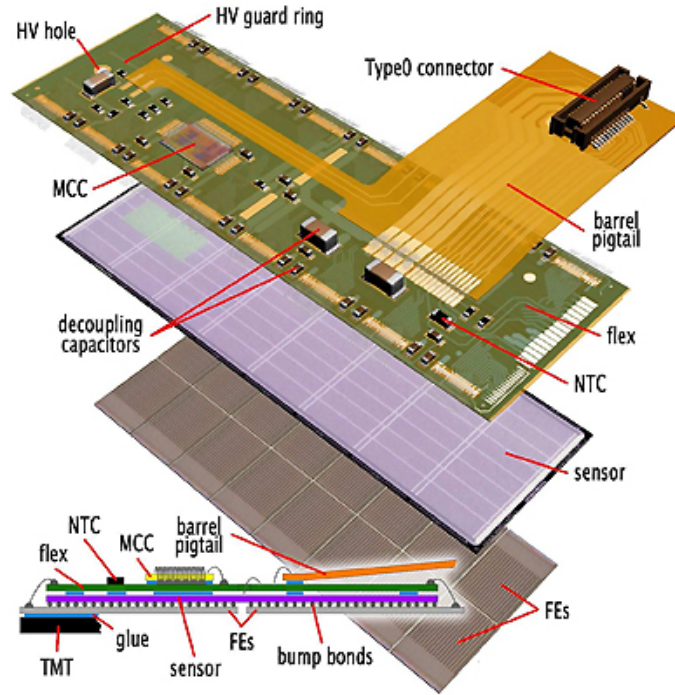
Figure 2.8 – Exploded view of an ATLAS Pixel Detector and transversal cut.
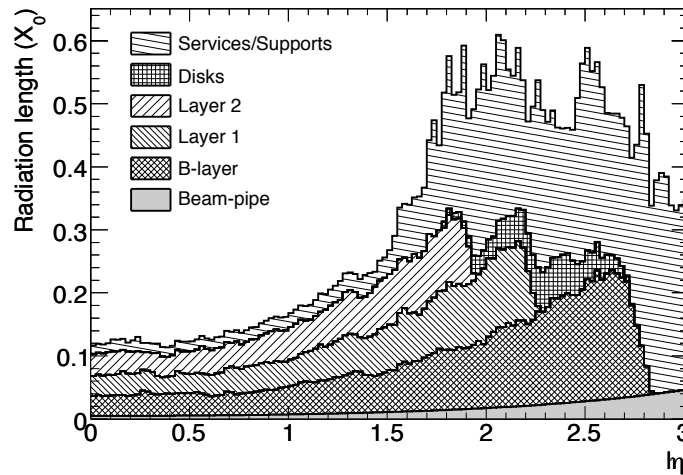
Figure 2.9 – Radiation length of the Pixel Detector versus pseudorapidity showing the contribution from each layer and from all disks. Layer and disk contributions include services and supports directly in front of and behind the layer/disk. All remaining services and supports, including services in the region between the barrel and End-Cap are included in the "Services/Supports" category [36].

The Semiconductor Tracker   The SCT is at its time composed of four double layers of microstrips sensors with a stereo angle between layers of 40 mrad. Two different sensor designs were used for the 4 layer planes and the 9 disks (per side): a strip pitch of $80\,\mu$m with two 6 cm-long sensors was chosen for the rectangular barrel sensors and radial strips of constant azimuth (161.5 μrad) with mean pitch of $\sim$80 μm were chosen for the trapezoidal disk sensors (End-Cap). In the barrel region each plane has an intrinsic accuracy of $17\,\mu$m ($R\phi$) and $580\,\mu$m (z). The SCT,

although with a lower resolution, thanks to its larger radius and increased number of measurement points, allows to reduce combinatorial effects during the pattern recognition particularly in dense environment [24, 37].

Located as the outermost component of the Inner Detector, the TRT is based on the detection of the transition radiation of charged particles. Composed of detecting layers made of 4 mm diameter straw tubes filled with $Xe\,CO_2\,O_2$ gas mixture, interleaved with transition radiation material, the TRT provides large signals from the low energy photons emitted from charged particles traversing the material boundaries. The transition emission depending on the velocity of the particle, the TRT is able to distinguish between light charged particles (i.e. electrons) and heavy charged particles (such as hadrons, typically pions and protons). The detector performance is shown in Figure 2.10. Typically operated at -1500 V, due to the high electric field around the central electrode inducing a cascade effect, gains of the order of 2.5×10^4 are obtained allowing a direct readout of the signal from both sides of the straw tubes. The TRT straws only provide measurements in the $R\phi$ bending plane, with an intrinsic accuracy of 130 μm, and no measurements can be made along the straw direction.
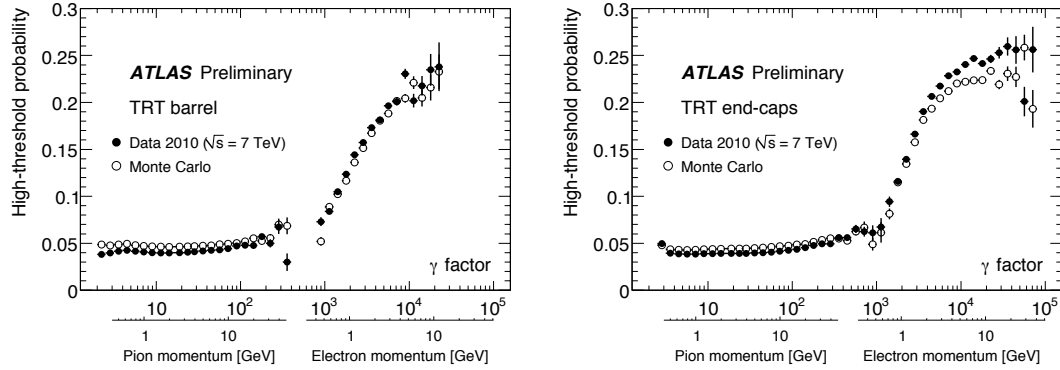

Figure 2.10 – TRT high-threshold (HT) probability distribution as a function of the Lorentz factor, $\gamma = E/m$, for the TRT barrel (left) and end-cap (right) regions, as measured in 7 TeV collision events and compared with Monte Carlo. At high values of ? (above ?=1000), a pure sample of electrons is obtained from photon conversions. For low values of gamma, all selected tracks in the event are used and are assumed to have the mass of the charged pion. As expected from the production of transition radiation (TR), the probability of a HT hit increases for particles with a gamma-factor above 1000, which enables the TRT to separate electrons from pions over a momentum range between 1 GeV and 150 GeV.

2.4   Run-I ATLAS Detector Performance

Since 2010 the ATLAS detector has been recording data with an efficiency of 93.4% with respect to the total luminosity delivered by the LHC as shown in Figure 2.11. The unrecorded luminosity during Run-I was mainly driven by the ID warm start (when the stable beam flag is raised, the ID undergo a ramp of the high-voltages and, for the pixel system, turning ON and configurating). Additionally to the large recorded luminosity, it is important to point out that 95% of the recorded luminosity passed all the strict criteria of the offline monitoring (quality check), proving the excellent detector stability and efficient operation for physics.
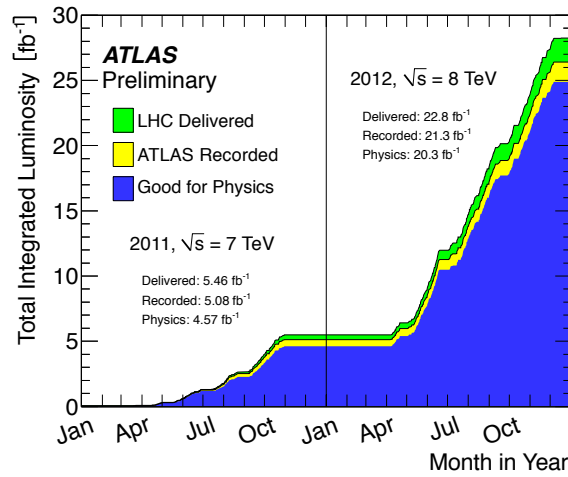
.11 – Integrated luminosity versus time delivered (green), recorded by ATLAS (yellow), and :o be good quality data (blue) during stable beams and for pp collisions at 7 and 8 TeV centre- :nergy in 2011 and 2012.
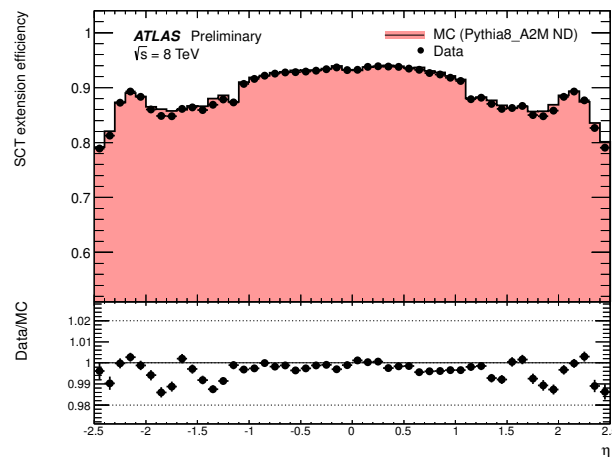

Figure 2.12 – SCT extension efficiency as a function of pseudorapidity (η) of the pixel tracklet. Track selection criteria are applied to the Pixel tracklets to ensure a high probe purity.

As an example of the detector understanding during Run-I, Figure 2.12 shows the SCT extension efficiency[3] agreement between data and Monte Carlo for all pseudorapidities, proving the detailed understanding of the detector material, simulation and sub-detectors efficiencies.

Due to the increase of peak luminosity and energy, an average of 21 interactions per BC were observed during the end of Run-I as shown in Figure 2.13. This challenging high density environment motivated the introduction of new and more sophisticated reconstruction software algorithms, improving the reconstruction performance with respect to previous methods. One of the critical issues in the B-layer in very high density environment was the association of a single cluster from pixels traversed by multiple close-by particles, losing information about the number of traversing particles and therefore an eventual track reconstruction inefficiency. In order to mitigate

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[3]The SCT extension efficiency is measured by standard tag-and-probe method. The principle of this technique is a measurement of the rate at which Pixel tracklets (track fragments reconstructed in the Pixel Detector) are extended into the SCT by finding a combined track (tag) that matches the Pixel tracklet (probe)

this the Connected Component Analysis (CCA, [38]) was therefore replaced by a Neural Network Clustering (NNC, [39]) algorithm, reducing the double hits by a factor three as shown in Figure 2.14 (left). The introduction of the NNC enhanced the impact parameter resolution with respect to the primary vertex by up to 7% (3%) in the longitudinal (transversal) impact parameters compared to the CCA algorithm. This was done to the improved cluster position estimate shown in Figure 2.14 (right) for 4-pixels wide clusters.
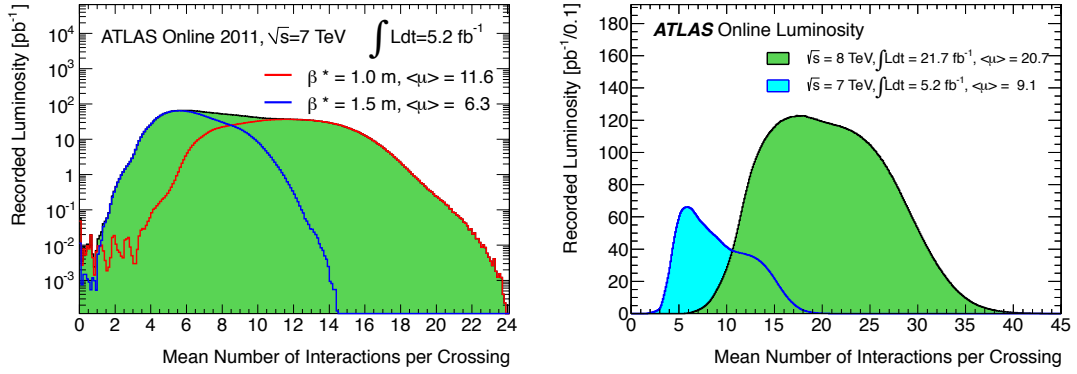

Figure 2.13 – Luminosity weighted mean number of interactions per crossing for 2011 (left). The plot is shown for data taken before and after the September Technical Stop where the beam beta was reduced from 1.5 m to 1.0 m showing the impact in the pileup. Luminosity weighted mean number of interactions per crossing for the 2011 and 2012 data (right). This shows the pile up increase due to the energy increase.
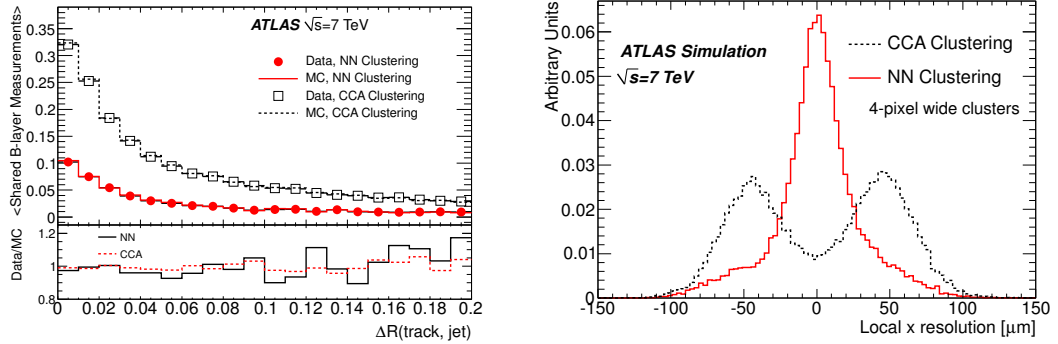
Figure 2.14 – Left: Average number of shared measurements in the B-layer on tracks associated to jets with 500 < pT < 600 GeV for data and simulation as a function of the distance of the track from the jet centre. Right: cluster residual in the local x direction for clusters with a width of four pixels reconstructed with the CCA and NNC algorithms [40].

The new analysis techniques, increasing the resolution of the detector reconstruction algorithms, allow a better identification of secondary vertices otherwise included in the primary vertex. This effect can be observed particularly in the low granularity z direction as shown in Figure 2.15 (top). As it can be observed, in the central region (±5 mm) vertex pairs are misstaged as a single vertex. Figure 2.15 (bottom) shows the MC simulation of the so called "shadow effect" at high pileup conditions. The significant increase of shadow vertices with pileup due to the higher density environment and higher proximity between primary vertices, will lead to non-negligible inefficiencies in the b-tagging performance.
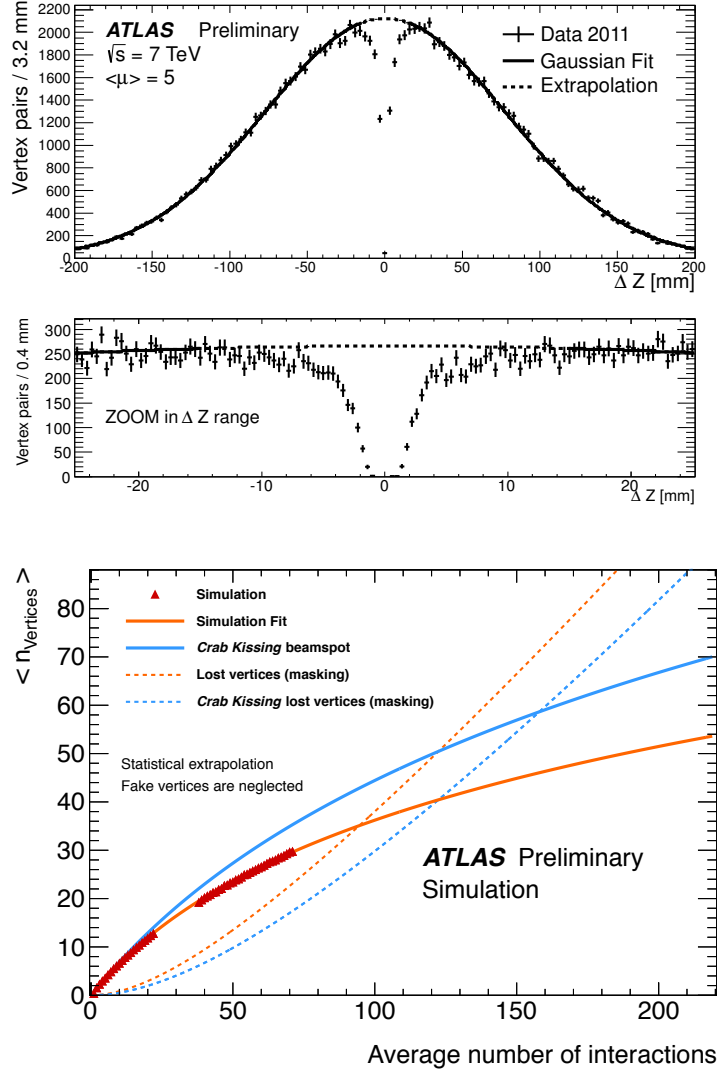
Figure 2.15 – Longitudinal separation between primary vertices for minimum-bias events with two reconstructed primary vertices (top). The extrapolated Gaussian fit underlines the fraction of primary vertices missing due to the merging of primary vertices at close distances. The average number of reconstructed vertices is shown as a function of the average number of interactions μ (bottom). The red triangles show the simulation prediction for minimum-bias events without any trigger bias using the 2012 setup for beam and detector conditions. The simulation covers the μ range up to 22 and a higher interval which was observed in some specific high-μ data taking runs. The simulation has been fitted (orange line) with a function taking into account the vertex reconstruction efficiency ϵ and the inability of resolving nearby interactions in distinct vertices (vertex masking): <nvertices> = $\epsilon\mu \cdot F(\epsilon, \mu)$. $F(\epsilon, \mu)$ is a function that estimates the correction to the number of reconstructed vertices for masking effects. The correction to the number of reconstructed vertices for masking effects $F(\epsilon, \mu)$ is show by the dotted lines for two beam configurations.

2.5   ATLAS Upgrades and Future Plans

In order to cope with the LHC upgrade schedule and to compensate for the detector degradation (Section 3.1.2) due to radiation damage, the ATLAS detector need to be upgraded.

- During the first Long Shut down (**LS1**) in 2013-2014, the ATLAS detector has seen its first maintenance of the Pixel Detector, Muon system and beam-pipe. During Run-I, the Pixel Detector showed an increasing fraction of dead modules due to dead or misbehaving optical links, as well as failing services. Figure 2.16 summarises the different sources of defects for the 88 malfunctioning pixel modules. Therefore, to guarantee a high efficiency tracking during Run-II, the Pixel Detector services were updated with the so called "New Service Quarter Panels" (nSQP), completely renewing the data cables, the electrical-to-optical converter boards, and data-transition fibres. In addition, the data bandwidth for the two outermost layers was increased by a factor of two (80 Mbps and 160 Mbps per module on Pixel layers three and two respectively). Increasing the layer bandwidth will allow to maintain high efficiency tracking up to a luminosity of 3×10^{34} cm^{-2}s^{-1} (larger than the maximum design luminosity of 2×10^{34} cm^{-2}s^{-1}). After nSQP installation, the defective modules were reduced from the 5.0% at end of Run-I to 1.9%, as shown in Figure 2.17.

  Additionally, the installation of the muon chambers in the Barrel-End Cap overlap region was completed during LS1, increasing the Muon-system hermiticity. The beam-pipe sections located at the End-Cap calorimeters and End-Cap toroids, has been replaced with aluminium pipes, reducing the radiation background in the cavern affecting the Muon Spectrometer and allowing future interventions in the End-Cap region by reducing its activation.

  Due to the expected significantly exceed of the design luminosity during Run-II and to the higher collision energies (13-14 TeV) large pileup events (>50 events per BC) and occupancies are expected. This, combined with the FE-I3 inefficiency at high occupancies shown in Figure 2.18, the shadow reconstruction vertices expected at higher pileup (Figure 2.15), and the expected detector degradation after 50 Mrad ionising dose and 1×10^{15} cm^{-2} neq dose expected by the end of Run-II, motivates an ID upgrade. Therefore, during the present LS1, the Pixel Detector was upgraded with a new 4th innermost layer with improved radiation hardness and resolution, the Insertable B-Layer (IBL). The IBL being the main subject of this thesis, is discussed in detail in Chapter 4.
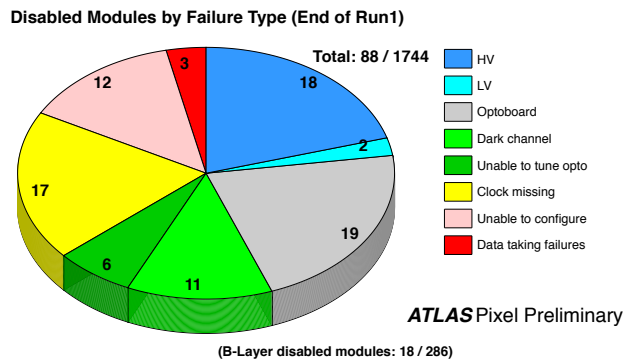

Figure 2.16 – Results of defect analysis on the 88 defective pixel modules at the end of Run-I, 88 modules constitute 5% of the Run-I Pixel Detector. 18 of those 88 modules were located in the B-Layer.

Modules to be disabled (After LS1 Re-installation)
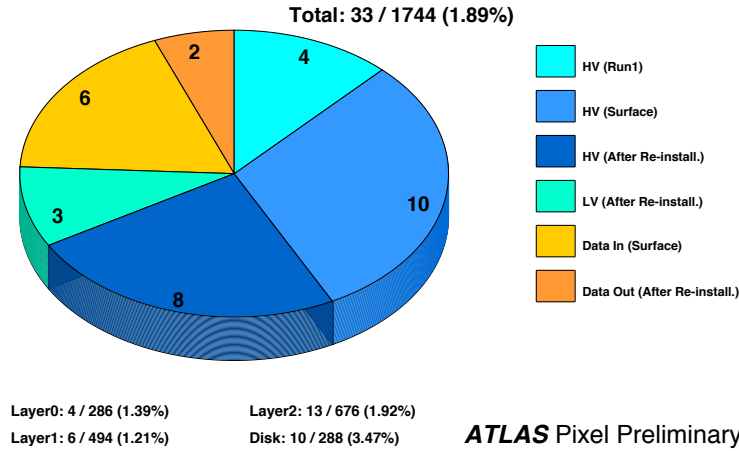
Figure 2.17 – Number of modules of the Pixel Detector to be disabled after refurbishment and re-installation in ATLAS during LS1 classified by failure mode and the phase of causing problems. Modules having issues but being operable are not included.
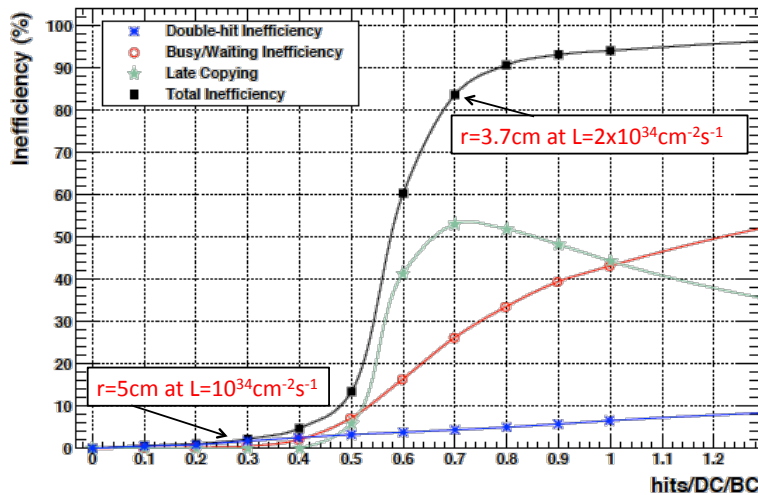
Figure 2.18 – FE-I3 inefficiency as a function of the occupancy (hits per double column per bunch crossing, hits/DC/BC)

- During **LS2** (2018-2019), ATLAS will face its first major upgrade. The Muon Small-Wheel will be replaced and included in the LV1 trigger, allowing to better discriminate between events and so to maintain the trigger rates under the maximum Level-1 frequency of 75 kHz and total recording rate of $\sim$300 Hz. Additionally, the forward calorimeters will be replaced, increasing their granularity to cope with higher particle-density environment. Although calorimeter technologies and layouts are not yet defined, feasibility simulation studies are ongoing [41]. Finally the Fast TracKer (FTK) [42], installed during Run-I, will be fully integrated in the High Level trigger system, allowing a fast track reconstruction at a speed of the nanosecond per track.

- During **LS3**, where the last upgrade phase for HL-LHC is currently foreseen in 2023-2025, the ATLAS detector will be upgraded to work at a luminosity of $5 - 7 \times 10^{34}$ cm^{-2}s^{-1}. During this Long Shut down, the ID will be replaced by a full silicon tracker, designed to survive up to 7.7 MGy and fluencies of 1.4×10^{16}cm^{-2}neq in the innermost layers and up to 0.9 MGy and 1.7×10^{15}cm^{-2}neq fluencies in the outermost layers.

The pixel technology presently operating in the LHC experiments can not cope with this challenging radiation environment and therefore new technologies need to be implemented.

The current design proposal is composed of a pixel and a strip detector. The Pixel detector will have a total surface of 8.2 m^2 (compared to the 2.3 m^2 of the current Pixel Detector) and about 700 million channels. It will be composed of four barrel and six additional disks in the forward region. Currently, two pixel designs are under study for the different radiation hardness and precision requirements within the different planes of the Pixel Detector [43]. The two innermost layers have a proposed pixel size of 25×150 µm^2 and a new readout electronics to cope with the high radiation environment. Due to the increased radii of the the two outermost pixel barrels and the seven End-Cap disk, a compromise pixel size of 50×250 µm^2 between resolution, cost effective and occupancy is planned to be used. Additionally the pixel size has been set to match the current FE-I4 readout electronics capable to stand up to 250 Mrad [44] and therefore reducing the R&D cost of the outermost pixel layers. Additionally, studies are undergoing in order to develop new detectors based on commercially available processes, reducing the production costs and simplifying the module production. As an example, the High-Voltage Complementary Metal Oxide Semiconductor (HV-CMOS) detector technology, is currently being investigated and will be covered extensively in chapter 7. The strip detector already under final prototyping would be composed of 3 inner layers of short strips (24 mm), 2 outer layers of long strips (96 mm) and 5 double sided disks on each End-Cap. In total of about 200 m^2 of silicon strips with a radiation tolerance requirement of 5.6×10^{14} neq cm^{-2} and 1.2×10^{15} neq cm^{-2}, in the short and long strips barrels respectively [43]. A detailed summary of the current strip prototyping status can be found in [45].

Furthermore, due to the increased luminosity a new trigger architecture will be deployed in ATLAS with a 500 kHz Level-0 using the ID tracks p_T during the Level-1 decision. This L1 track trigger will be implemented with a parallel track processing, being the ID readout bandwidth the main limitation due to the significant increase on data transfer and services material budget.

Hybrid Pixel Silicon Detectors

## 3.1 Charged Particle Detection with Silicon Sensors

3.1.1 Motivation for Pixel Detectors

The perpetual need for faster and more precise detectors in High Energy Physics (HEP) is driven by the constant improvement of the accelerators luminosities and energies. High resolution detectors are needed for high precision track reconstruction and vertex identification while keeping low occupancy rates. In collider experiments, where two particle beams collide head-to-head, particles of each beam can interact producing a primary vertex. A simplistic scenario of two primary vertices and the decay of a long-lived particle is shown in Figure 3.1. In order to distinguish between primary vertices (typically distant of about $100\,\mu m$ at the LHC) and the decay signatures of long-lived particles such as b-quarks, high pointing resolution is needed. Additionally, due to the high particle density environment, high granularity detectors are needed in order to mitigate combinatoric effects leading to fake track reconstruction. Figure 3.2, schematically shows how a low granularity detector can lead to a fake track reconstruction (left), or a mis-identification of collinear particles into a long-lived particle decay (right).

Although the definition of a pixel detector might vary depending on the sub-detector considered (and technology), pixel detectors are generally defined as devices able to reconstruct an image thanks to the measurement of small independent *picture element* (pixels) covering the integrity of the picture area. Most commonly used pixel detectors are imaging detectors, such as the one installed in digital photo-cameras, where the photons arriving to each pixel are captured, reconstructing a full picture. In HEP, the particles resulting from the interaction point need to be detected. Different approaches to particle pixel detectors exist such as Monolithic Active Pixel Sensors (MAPS), HV-CMOS and Hybrid pixel detectors. Due to the interest in fast and high efficiency detectors, and their relative simplicity with respect to other technologies, hybrid pixel detectors are most commonly used in HEP.
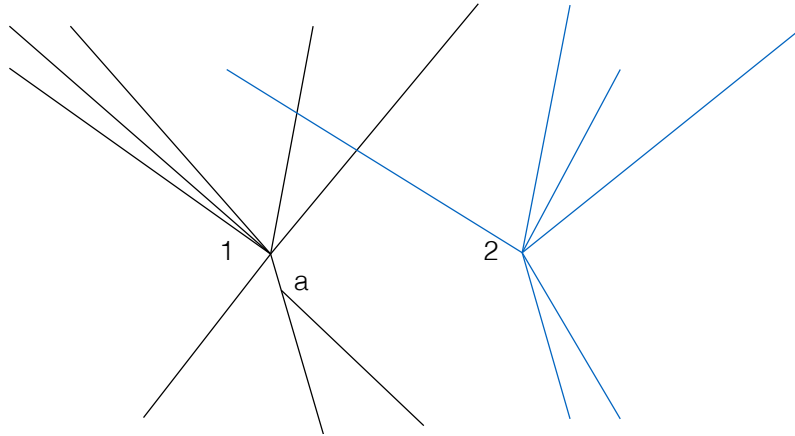
Figure 3.1 – Schematic representation of two iteraction vertices (1 and 2), and of a secondary vertex (a) created from a particle decay.
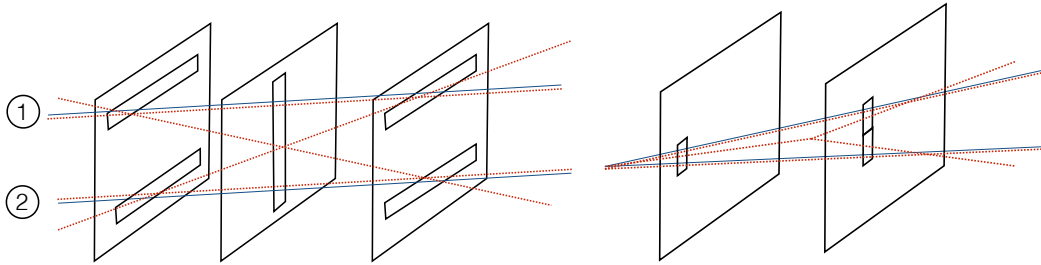
Figure 3.2 – Schematic representation of two particles crossing three low resolution detector planes (left). Due to combinatorics, two track pairs can be reconstructed leading to possible fake tracks. Two particles (right) crossing two pixel detectors showing and ambiguity in the track reconstruction due to an insufficient granularity in the first plane. Real tracks are shown by full line while possible reconstructed tracks are shown by dashed line.

3.1.2   Working Principle of Silicon Detectors

The pn-Junction

Semiconductors were used since the very early stage of electronics development in the field of frequency modulated radio applications for their electronics properties. Although in the early stages (late nineteen century) the underlying working principle of the diode-like properties of semiconductor devices was still unknown, all electronic applications rely on their electronic level population of charge carriers. Even though a vast variety of semiconductors exist, classified in elementary and compound materials, only silicon will be covered here for its vast use in the industry and particularly in HEP.

Semiconductors are characterised by their variable conductivity, due to their charge-carriers population and energy levels. As illustrated in Figure 3.3, semiconductors have their valence band fully populated, contrary to their conductive band. The electrical conductivity, defined as the capacity to flow electrons from the valence to the conduction band is therefore limited by the band gap energy (that electrons can only overcome if an external energy, e.g. thermal, is supplied).
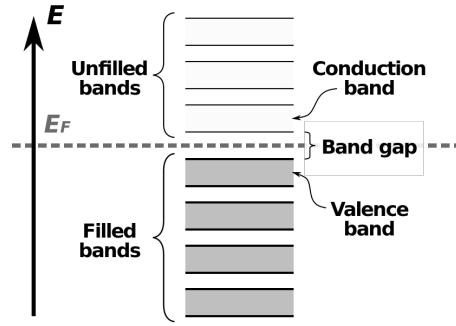
Figure 3.3 – Schematic semiconductor band structure diagram. E_F is the Fermi energy level. The valence (conduction) band is the filled (unfilled) band closest to the E_F.

In the case of *intrinsic* semiconductors, the number of free electrons n (i.e. the number of electrons in the conduction band) can be calculated as follows:

$$n = \int_{E_V}^{E_C} N(E)F(E)dE$$

where $N(E)$ is the density of states in the conduction band, $F(E)$ is the electron probability distribution given by the Fermi-Dirac function and E_V and E_C are the valence and conduction band energies respectively. The density states $N(E)$ can be computed from the periodic structure of the silicon crystal as explained in [46]:

$$N(E) = 4\pi \left(\frac{2m_n}{h^2}\right)^{2/3} E^{1/2}$$

where m_n is the effective electron mass[1]. The Fermi function being:

$$F(E) = \frac{1}{1 + e^{(E_C - E_F)/kT}} \approx e^{-(E_C - E_F)/kT}$$

the Fermi energy level E_F is defined as the hypothetical energy level of an electron such that, at thermodynamic equilibrium, this energy level would have a 50% probability of being occupied at any given time. Therefore, the number of free electrons n can be computed, as:

$$n = 2 \left(\frac{2\pi m_n kT}{h^2}\right)^{3/2} e^{-\frac{E_C - E_F}{kT}} \tag{3.1}$$

It is worth to mention, that the number of free electrons for an *intrinsic* semiconductor is only dependent on intrinsic parameters such as the effective electron mass and the band energies, and one external parameter: the temperature.

In order to build electronic devices with different charge-carrier densities and types (electrons and holes), silicon can be doped with donors (leading to a n-type silicon with a populated conductive band) and acceptors (leading to a p-type silicon where the valence band is not fully populated). This doping corresponds to the introduction of allowed energy states close to the conduction (i.e. donor) level, leading to a concentration of free electrons n being equal to the number of doping

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[1]The effective mass of an electron is defined by analogy to a free particle that responds to an external force given its mass. An assumption that all the moving charge carriers are close to the band edge is needed so that a second order approximation describes properly the band potential similarly to a mass field.

atoms (N_D). Using equation 3.1, it can be observed that a shift of the Fermi level due to the doping is given by[2]:

$$E_F = E_{F,i} + kT \ln \left(\frac{N_D}{n_i} \right)$$

where $E_{F,i}$ is the non-doped intrinsic Fermi energy level and n_i is the total number of silicon atoms.

One of the main applications of doped semiconductors is the *pn-junction*, defined as the intersection between two types of semiconductor materials (p-type and n-type), inside a single crystal. Due to the different band populations and Fermi levels, a potential barrier between the two doped materials is created, producing an asymmetric conducting device, better known as the *pn-junction* diode.

The pn-junction possesses some interesting properties. Although the p-doped and n-doped semiconductors can be relatively conductive, the junction between both is depleted of charge carriers and therefore becomes non conductive. The pn-junction has therefore two bias operation modes: *forward bias* and *reverse bias* as shown in Figure 3.4.
In *forward bias*, the p-type side of the junction is connected to the positive potential (of the bias supply) and the n-type to the negative terminal. In this configuration, the holes (electrons) of the p-type (n-type) region are pushed toward the junction, reducing the depletion zone. Once the built-in potential (between both dopings) of the diode is overcome (known as the "knee" voltage), the current will flow through the diode. In the contrary, in *reverse bias*, where the p-type (n-type) is connected to the negative (positive) terminal, the holes (electrons) in the p-type (n-type) material are pulled away from the junction, therefore increasing the depletion zone. The resistivity increases with the applied voltage (depletion voltage), reducing the electric current flowing through the diode. At very high voltages, the depletion zone breaks down and current begins to flow.

Silicon detectors in particle physics are simplistically a pn-junction operated in reverse bias, where, as explained in the following sections, charged particles traversing the sensor are detected by collecting the signal induced by the charges produced by ionisation moving in the depletion zone.

Charge Generation and Transport

When a charged particle traverses a layer of material, part of its energy is deposited through scattering with the electrons and nuclei along the particle track. For a good tracking detector, the particles ideally deposit only a small amount of their energy in the sensitive material, reducing the impact on the particle trajectory.

Charged particles interact with the sensitive material (mainly with the electrons) via the electromagnetic force, producing ionisation and Compton scattering. Although the interaction process is a succession of small interactions over the track length, the mean energy loss dE per unit length dx is well described by the Bethe-Bloch formula [47]:

$$-\frac{dE}{dx} = \frac{4\pi r_e^2 m_e c^2 N_A Z z^2}{A\beta^2} \cdot \left[\frac{1}{2} \ln \left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} \right) - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right]$$

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[2]Although quantum considerations and Pauli's exclusion principle need to be considered for high doping profiles, at the doping concentrations typically used for silicon detectors below $10^{17} cm^{-3}$ its effect on band structures can be neglected.
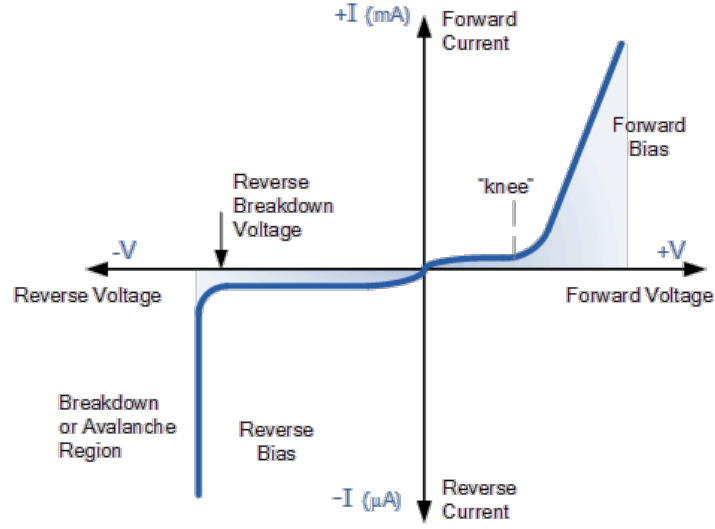
Figure 3.4 – IV curve of a pn-junction in reverse and forward bias.
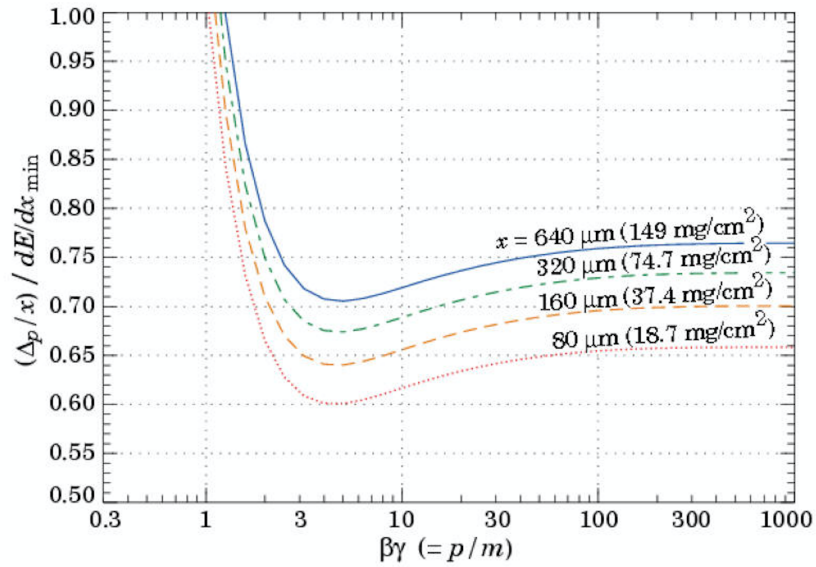
Figure 3.5 – Most probable energy deposition as a function of $\beta\gamma$ for different silicon thickness, scaled to the mean loss of a minimum ionising particle, 388 eV/μm [3].

where, Z, A and I are the atomic numbers, mass number and mean excitation energy of the material respectively, N_A is the Avogadro number, m_e and r_e are the electron mass and classical radius, c the speed of light and $\beta = \frac{v}{c}$ and $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ the relativist kinematic variables. Finally, $\delta(\beta\gamma)$ is defined as the density correction for relativistic particles and T_{max} the maximum kinetic energy that can be transferred to a free electron within a single interaction.

As it can be observed, the energy loss of a particle only depends on its charge Z and its velocity. Therefore, the energy deposition $-\frac{dE}{dx}$ can be conveniently represented versus $\beta\gamma$, as shown in Figure 3.5.

The ionisation energy deposited in the material directly produces pair of electron-holes (e-h), by exciting free electrons to the conduction band. For silicon, where 3.6 eV are needed to create an e-h pair, minimum ionising particles (MIP) create in average of about 80 e-h pairs per transversed micron. In a reversed biased pn-junction, due to the presence of the external electric field, charges are accelerated between collisions with a drift velocity:

$$\vec{v}_{n(p)} = \frac{-e\tau_c}{m_{n(p)}}\vec{E} = -\mu_{n(p)}\vec{E}$$

where $\vec{v_n}$ and $\vec{v_p}$ are the average drift velocities of electrons and holes respectively, m_n and m_p are the effective electron and hole masses respectively and $\vec{E}$ is the electric field. The mobility μ is a function of the effective mass and the mean free time τ_c, defined as the average time between collisions of the moving charges and the crystal structure. At higher temperatures, lower mobilities are observed as expected from the increased rate of thermal collisions. Standard drift velocities for silicon at low field (below 10^4 V/cm) are of the order of [48]:

$$\mu_n \simeq 1500\frac{cm^2}{Vs} \qquad \mu_p \simeq 480\frac{cm^2}{Vs}$$

Electron-hole pairs produced in the depleted zone of the pn-junction get accelerated towards the electrodes. This charge movement instantly produces a current at the electrodes much larger than the thermal background. On the contrary, in the undepleted zone, e-h pairs thermally diffuse (due to the absence of an external electric drift field). Slow diffusing particles have multiple collisions with the majority carriers present in the undepleted zone, so charge recombination is more likely.

It is important to notice that in a standard $300\,\mu$m-thick silicon detector with a bias-voltage of 150 V (equivalent to an electric field of the order of 5000 V/cm), charge collection time is of the order of 10 ns producing a current of $\sim$5 μA. Although charges are created along the trajectory of a charged particle and drift following the field lines, due to the mentioned thermal collisions, the spatial distribution of the collected charge arriving at the electrodes follows a gaussian probability distribution with standard deviation:

$$\sigma = \sqrt{2Dt}$$

where t is the transit time and D the diffusion constant ($D = \frac{\mu k_B T}{q}$) with μ being the charge ability of the collected charge carriers. Silicon detectors are often operated within magnetic fields to measure particle momentum from the track deflection. This magnetic field also acts on the drifting charges created inside the silicon, deviating them by an angle Θ_L, called Lorentz angle, as shown in Figure 3.6 and given by:

$$\tan\Theta_L = \mu B$$

where B the magnetic field.

Properties of Silicon Detectors

Although separately processed n- and p-doped pieces of semiconductor that are mechanically joined together would form a pn-junction, this process remains until today practically impossible at the industrial scale due to technical limitations such as the silicon surface oxidation, and the alignment of both crystalline structures to the atomic level. Instead, commercial pn-junctions are
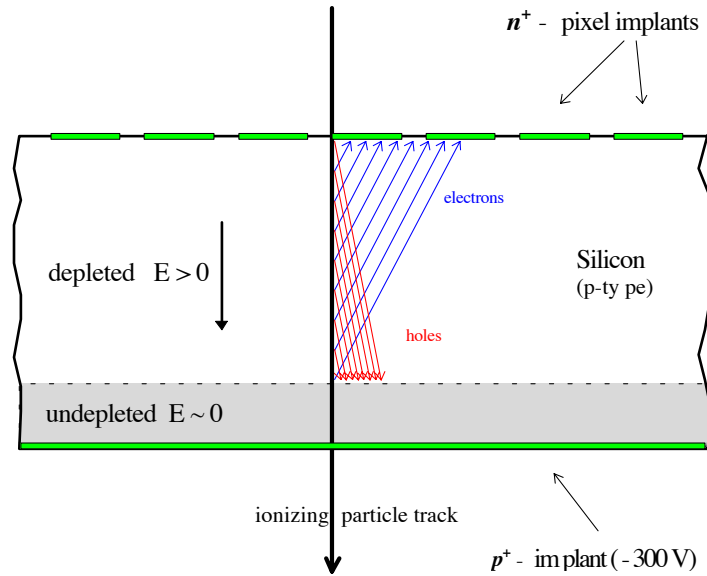
Figure 3.6 – Electrons and holes drifting in the electric field are deflected under the influence of a magnetic field, which might produce a large-enough shift to fire neighbouring pixels. This shift causes an offset between the particle track and the measured position.

produced from a wafer (bulk) of doped semiconductor (e.g. n-type), with diffused impurities (e.g. p-type) at its surface, creating the pn-junction[3]. Silicon detectors typically consist of a n- or p-type doped bulk material and n^+- or p^+-type collection electrodes. Table 3.1 summarises the four possible combinations of the pn-junction implementations, their advantages and disadvantages. Although all four combinations could be used for pixel silicon detectors, due to the high radiation tolerance required at the LHC experiments, n^+-in-p and n^+-in-n types are the most suitable technologies and these are covered in the following paragraphs.

electrode	Substrate	
	p-type	n-type
p^+	• double-side process • slow charge carriers collection (holes)	• single-side process • not suitable for high radiation environments
n^+	• single-side process • no type inversion • not fully develop until recent years	• double-side process • need to be operated fully depleted before type inversion

Table 3.1 – Summary of the different substrates and electrode doping combination for pixel detectors

In the case of n^+-in-n detectors, the electrodes (n^+ implants) are located in the front-side of the n-type bulk. A p^+ implant in the back-side allows to create the pn-junction. Non-irradiated sensors start to be depleted from the p^+ implant. The collecting electrodes being placed on the front side, a full depletion needs to be achieved for operation. After type inversion (see following subsection), where the n-type bulk gets inverted to p-type, the depletion grows from the n^+-type electrodes and the sensor can be operated under-depleted. Due to the crystal cutting during production,

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[3]In this case, the p-type implant it is actually counterdoped, meaning that although it contains n-type impurities, there is a higher p-type impurity density, giving a p-type characteristics

sensor edges can become conductive and therefore the edge voltage has to be controlled. For this purpose *guard-rings* are actually implemented in the p$^+$ backside implantation[4], reducing the voltage via punch-through resistors. This backside structure therefore requires a lithography process on both sides (double-side process), increasing the production cost. n$^+$-in-p sensor operate similarly to the n$^+$-in-n after irradiation. With the depletion growing from the electrodes (front side), a single-side processing is just required, therefore reducing significantly the manufacturing cost. Still an n-side isolation is necessary and therefore alternatives to the guard-ring approach need to be implemented. The n$^+$-in-n and n$^+$-in-p sensor structures and depletion growth are shown in Figure 3.7.
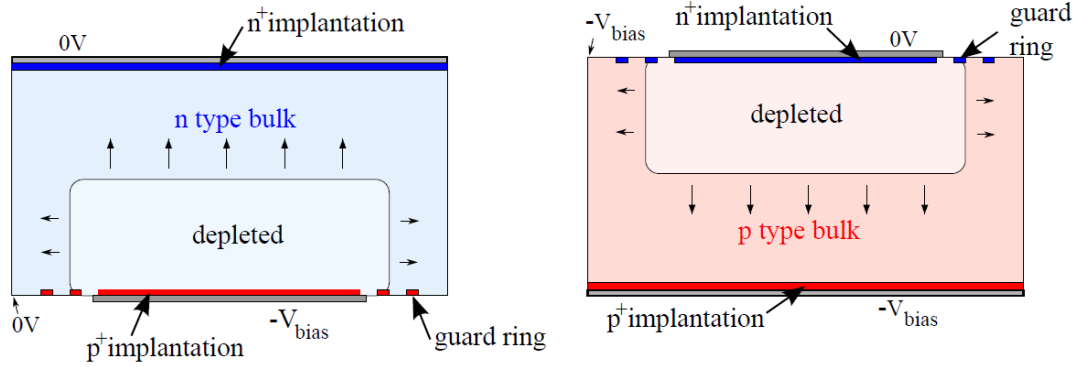
Figure 3.7 – Cross section of a n- (left) and a p-type (right) substrate planar silicon sensor. The direction of the depletion zone growth is indicated with arrows. Adapted from [49].

All sensor types need to be depleted or fully depleted for operation in the reverse bias mode. The applied voltage will therefore increase the depletion zone width (W), that can be calculated by solving the Poisson equation, giving:

$$W = \sqrt{\frac{2\epsilon_0\epsilon_{Si}}{e}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V + V_{pn})} \tag{3.2}$$

where V is the external applied voltage and V_{pn} is the built-in pn-junction voltage. The $1/N_{A(D)}$ factor accounts for the doping concentration of acceptors and donors, where the depletion zone reaches a higher depth in low-doped material (high resistivity). In the case of silicon detectors, where a high-doped implant ($N_A > 10^{18}\text{cm}^{-3}$) is built on a low-doped bulk ($N_D > 10^{12}\text{cm}^{-3}$), the depletion grows deeper in the bulk active area as desired. Additionally, the built-in voltage (of the order of 0.5 V) can be neglected with respect to the external applied voltage and therefore equation 3.2 can be simplify to:

$$W \approx \sqrt{\frac{2\epsilon_0\epsilon_{Si}}{eN_D}V}$$

In the depletion zone, where thermally created e-h pairs are pulled towards the electrodes, a small *leakage current* or *dark-current* (J_{leak}) arises. Although thermal charges might be also

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[4]The double-side process and the guard-ring structure allows to keep the sensor edge at ground potential facilitating the sensor integration in a larger-scale full detector system and limiting the risk of discharge with neighbouring structures.

created in the undepleted region, due to recombination their contribution to the *leakage current* can be neglected. Therefore the *leakage current* can be expressed as [48]:

$$J_{leak} \approx -e\frac{n_i}{\tau_g}W \approx -e\frac{n_i}{\tau_g}\sqrt{\frac{2\epsilon_0\epsilon_{Si}}{eN_D}V} = \frac{-e2}{\tau_g}\left(\frac{2\pi m_n kT}{h^2}\right)^{3/2}\sqrt{\frac{2\epsilon_0\epsilon_{Si}}{eN_D}V}\,e^{-\frac{E_C-E_F}{kT}}$$

where τ_g is the carrier generation life-time. As expected, the leakage current is proportional to the depleted volume W and to the temperature. When the reverse bias voltage increases and the full volume is depleted (full depletion voltage), the leakage current saturates and remains stable until break-down as shown in Figure 3.4. When the reverse bias increases to higher values, the electric field in the pn-junction breaks-down, increasing significantly the leakage current.

During operation, sensors are normally operated fully depleted and below breakdown while maximising the collected signal. After irradiation, due to the displacement of the cristal atoms (bulk damage), an increase of the leakage current is expected and therefore a lower depletion voltage can be applied preventing thermal runaway[5]. Local defects in the bulk or in the sensor manufacturing can lead to a localised breakdown, increasing the leakage current and thus creating noisy pixels clusters.

Radiation Effect on Silicon Detectors

Pixel detectors installed in the innermost layers of collider experiments face very high fluencies, of the order of 2×10^{11} per cm^2 per hour at the LHC. High energy ionising particle fluencies are responsible for damages in the silicon cristal (bulk damage) as well as surface damage, particularly in the dielectrics and interface regions.

High energy particles going through a silicon detector interact with the electrons of the silicon atoms (ionisation) but also with the silicon nuclei. Incident energetic particles can transfer the required recoil energy $E_d \simeq 25$ eV to displace a silicon nuclei out of its lattice position. The maximum recoil energy a particle can transfer in a single interaction depends on it mass and energy. For example, electrons require a minimum energy of 260 keV in order to provide 25 eV, contrary to protons and neutrons where only 190 eV are needed. Heavy particles (p, n, etc.) with higher energies can produce a cascade effect, where the initial displaced silicon nuclei produces cristal defects via secondary collisions, creating a cluster of defects [48]. The introduced defects have a reduced mobility and therefore recombination is very limited. It has been observed that irradiated silicon sensors show a damage recovery at high temperature, so called annealing, where higher mobility defects (due to temperature excitement) meet during their drift allowing recombination [48]. Induced defects in the cristal electrically behave as acceptors, adding levels in the band-gap and thus allowing e-h generation. These cristal defects can be seen as a p-type doping, increasing the leakage current proportionally to the fluence:

$$I_{vol} = I_{vol,\phi=0} + \alpha \cdot \phi$$

where I_{vol} is the leakage per volume unit, ϕ is the fluence and α is a universal constant parametrising the current related damage.

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[5]The thermal runaway is defined as the breaking point where the power dissipated by the high-voltage overcomes the maximum power dissipation capability of the cooling system. At this point, the sensor temperature increase multiplies the available thermal charge carriers, increasing at their turn the leakage current and therefore the power dissipation.

The leakage current flowing through the electrodes is a source of noise for the input amplifier (see following section), and although its contribution before irradiation can be neglected, due to the increase of defects after irradiation it can become a non negligible source of noise. This is particularly true in the case of clustered defects where a significant fraction of the leakage current can flow to a single pixel firing their discriminator systematically and saturating its readout.

Additionally, at very high doses atom displacements accumulate with irradiation creating p-type doping defects and therefore modifying the cristal effective doping. High resistivity n-type sensors can therefore become intrinsic and follow a type-inversion after fluencies of the order of $\phi \sim 5 \cdot 10^{12}$ cm^{-2}. This effect called *type inversion* affects the effective doping and therefore also the resistivity and the full depletion voltage as shown in Figure 3.8.
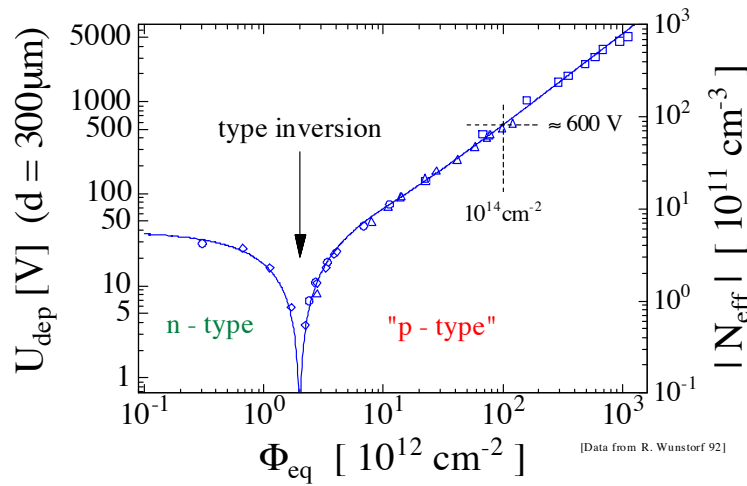
Figure 3.8 – Evolution of the full depletion voltage (left-vertical axis) and effective doping concentration (right-vertical axis) of an n-type 300 μm-thick sensor as a function of the fluence [50].

Additionally to the bulk defects, ionising particles can also influence the front-end and the sensor performances due to *surface damage*. Charged particles can create e-h pairs by ionisation in the overlaid dielectrics (*i.e.* silicon oxides), where e-h have very low mobility. Although most e-h will recombine due to the absence of high electric field, higher mobility electrons can drift in the presence of weak electric fields to the positive electrode. Similarly, low mobility holes can accumulate in the boundary region between dielectric and silicon. This effect is well known to affect the MOS structures, where the electric field of the gate is significantly reduced due to the charge screening on the silicon oxides. In pixel detectors, silicon oxide is used in the fabrication process of the electrodes, and therefore dielectric charge trapping has to be taken into account in the design. As represented in Figure 3.9, surface electric field between pixels created by irradiated silicon oxide can create MOS channels shortening pixels together. This can be prevented thanks to the introduction of *p-stoppers* surrounding the n-type electrode, providing an electrical isolation.
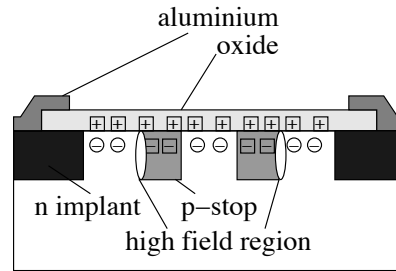
Figure 3.9 – Isolation techniques for adjacent n-type implants. Fixed (□) and free (○) charge carriers are indicated. The field maxima are located at the lateral p-n junctions [51].

3.2 Hybrid Pixels Modules, the FE Electronics

3.2.1 Hybrid Pixels Modules

Finely segmented silicon sensors can be readout by developed integrated circuits with readout elements matching the sensor pixel matrix, so called Front-End (FE), and directly connected via bump-bonding to the sensor. A schematic representation of the so-called hybrid pixel detector unit cell is represented in Figure 3.10. The diode-like sensor has a metallisation covering the full implant (collecting electrode) directly coupled to the FE electronics. From the early 90's, the resolution of pixel detectors has been improved by reducing the pixel size and by increasing the signal-to-noise ratio. Limited by the complex electronics required on each readout element, the pixel size was limited in its early stages by the FE integrated circuit dimensions. The fast evolution of semiconductor manufacturing process allowed a significant reduction of the node-size from the µm scale in the early 90's to the most cutting edge $14\,\mathrm{nm}$ technology nowadays. Pixel sizes of the order of $50{\times}50\,\mathrm{\mu m}^2$ can therefore be achieved nowadays using affordable technology (e.g. $180\,\mathrm{nm}$) with increased logic performances.
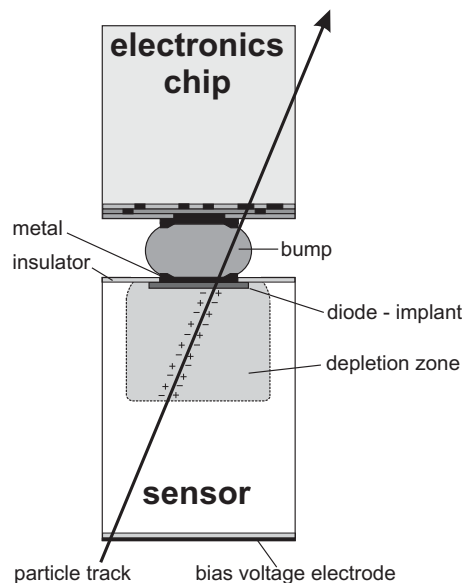
Figure 3.10 – Schematic view of the building block of a hybrid pixel detector. The ionising particle crosses the sensor and generates charges, producing the electric signal, which is then amplified and processed by the electronics.
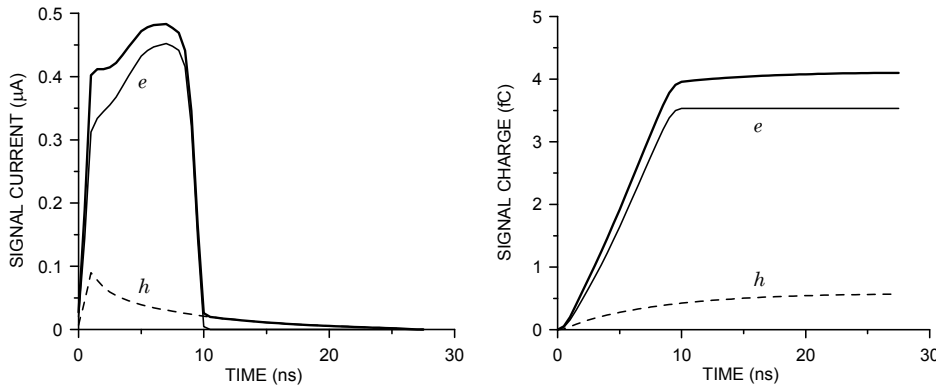
Figure 3.11 – Signal (left) and integrated current (right) on a n-type electrode. The electrons (e) and the holes (h) components are shown together with the total signal (bold) [53].
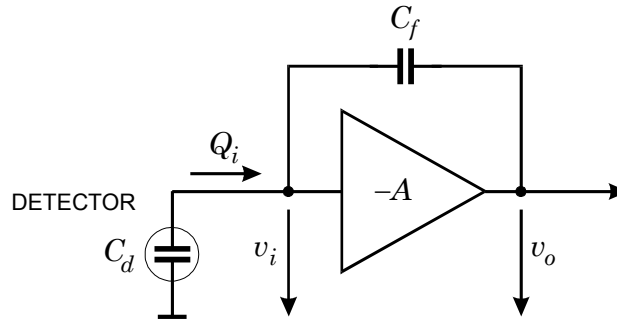

Figure 3.12 – Simplified schematic of a charge amplifier.

3.2.2   Overview of the FE Electronics for Hybrid Pixel Sensors

The FE electronics for hybrid pixels is typically composed by an analog signal processing stage and a digital logic. In a very simplistic way, the analog part is composed of three main blocks: a charge preamplifier, a current feedback and a discriminator.

The current produced by the drifting e-h pairs in the electrode (Figure 3.11) is, on a first stage, integrated by the charge amplifier or pre-amplifier. Figure 3.12 shows the basic schematics of a charge amplifier, where its output voltage (v_o) is inversely proportional to the reference capacitor (C_f) and proportional to the integrated input charge (Q_i). Additionally to the amplification factor, typically of the order of 100, real amplifiers need to cope with the response time driven by its internal capacitance as well as by the input residual voltage directly affecting the charge sharing between pixels. The effective impedance of the amplifier needs therefore to be significantly larger than the detector capacitance, reducing the charge sharing. As the noise of the amplifier dominates the overall FE noise, the response time and the capacitance have to be tuned carefully for a better rejection of these noise sources depending on the detector capacitance [52]. Values of the order of $\mathcal{O}(10)$ fF are used commonly in pixel detectors. Low noise performances can be achieved therefore thanks to low capacitance electrodes and so, the electronics must ideally be located in close proximity of the detector. Due to this design constrains, the FE power dissipation needs therefore to be minimised (limiting the pixel density), so that the sensor performance, due to thermal-induced noise, remains unaffected.

The charge amplifier is coupled to a feedback circuit responsible to reset the amplifier internal capacitor and cope with the leakage current (particularly after irradiation). Different discharge mechanisms can be adopted for the feedback circuit such as, ohmic feedback, current feedback or switched discharge. In the case of an ohmic feedback implementation, a resistor in parallel to the amplifier capacitor is used to discharge the feedback capacity. This technique although conceptually simple and robust, presents several implementation challenges when used in pixels detectors due to the small capacitance and therefore large resistance needed. Alternatively, the current feedback technique discharges the capacitance via a constant current allowing at the same time a compensation (sink) of the leakage current. the shape of the amplifier output signal depends on the feedback circuitry as shown in Figure 3.13. The signal amplitude is proportional to the input charge and the function slope can be tuned via the feedback resistor or current thanks to global and local (at pixel level) Digital to Analog Converters (DACs) , increasing the dynamic range of the input charges.
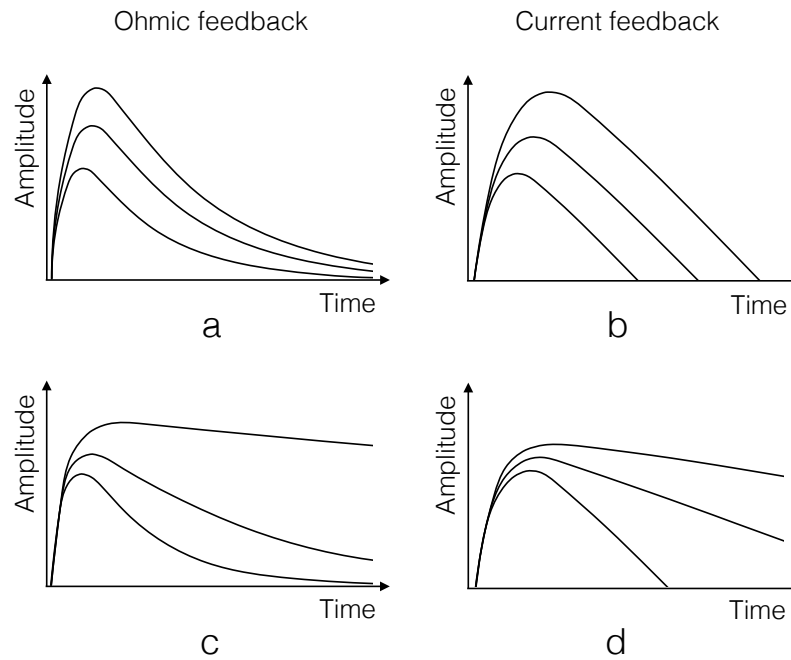
Figure 3.13 – Amplifier output signal shapes for an ohmic (left) and current (right) feedback circuit. For the ohmic case, as we effectively have a RC circuit, the amplitude shape decreases exponentially with time. In the current feedback, the relation is linear as a constant current is discharging the amplifier capacitor. Top plots (a,b) show output signal for different input charges, showing the dependance of the Time over Threshold and the charge. Bottom plots (c,d) show the output signals for different feedback current or resistance, illustrating how the tuning of the feedback circuit could increase the dynamic range of amplifier. Inspired from [48]

Finally, the output signal of the amplifier is sent to a discriminator to compare the signal amplitude to a threshold setting. In order to achieve very high efficiencies even for low amplitude signals (in the case of charge sharing between adjacent pixels), the threshold has to be set as low as possible while maintaining a good discrimination power between signal and noise. To achieve a dynamic and uniform threshold over all the FE matrix, the discriminator threshold voltage can be set via global and local DACs and tuned thanks to a charge injection circuitry. Being responsible for the signal identification, the discriminator timing response to all charges range is crucial so that the hits get associated to the proper event without ambiguity. Additionally to the event timing,

due to the local memory storage in the FE, charge information can be stored thanks to the Time Over Threshold (ToT), defined as the time interval in which the signal from the charge amplifier remains over threshold. Therefore, the ToT of each event depends directly on the collected charge as well as on the FE configuration such as feedback current and the amplifier bias voltage.

The ATLAS Insertable B-Layer

The Pixel Detector was designed to operate satisfactorily up-to an ionising radiation dose of $50\,\mathrm{Mrad}$, and a peak luminosity of $1 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ to collect up to $\sim\!300\,\mathrm{fb^{-1}}$ of proton-proton collision. Recent progress with the operation of the LHC showed that peak luminosities beyond $2 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ might be exceeded, generating some inefficiency in the innermost layer where the occupancy is higher.

In order to maintain and improve the performance of the ID at higher occupancies and in order to cope with possible failures in the current ID, a new pixel barrel layer, the Insertable B-Layer (IBL) [54] was added during the first long shutdown (LS1) of the LHC in 2013-2014 as a fourth innermost pixel layer.

## 4.1 A Fourth ATLAS Pixel Layer: Expected Performance and Overview

4.1.1 Expected IBL Performance

The key parameters of track reconstruction in dense environments to reduce the combinatorics and increase the tracking efficiency and resolution, are the number of space points, their spacial position and their resolution. The ATLAS Inner Detector (Pixel, SCT and TRT) is responsible for the charged-particle tracking. Given its radial proximity to the interaction point and high resolution, the Pixel Detector plays a key role in track reconstruction and vertex identification. As shown in Figure 4.1, the number of reconstructed tracks deviates significantly from truth for more than 50 pileup interactions if tracks are allowed to have less than 3 pixel hits. This, combined with the expected pileup during Run-II and the B-layer performances deterioration from radiation damage (Section 2.5), calls for the installation of a new pixel layer which would preserve the tracking performance and robustness at high luminosity and pileup.

In particular, the intrinsic resolution of the inner most layers determines the identification efficiency of primary and secondary vertices, essential for the identification of jets coming from the decay of B-hadrons (so called b-tagging). The B-layer and later the IBL, being the innermost layer of the ID, play therefore a key role in the mentioned performances. Figure 4.2 shows the effect of including the IBL in the expected resolution in the transverse (d_0) and longitudinal (z_0) impact parameters.
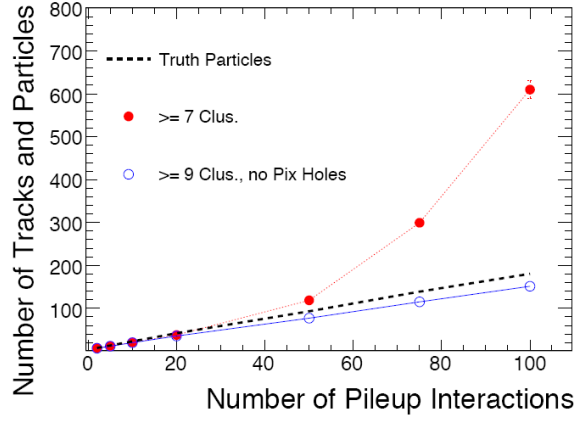
Figure 4.1 – Number of reconstructed tracks per event in 500 GeV di-jet events for the ATLAS Inner Detector as a function of the average number of pileup interactions. The results are shown for different track selections for track candidates with $p_T > 1$ GeV and $|\eta| < 1.0$.
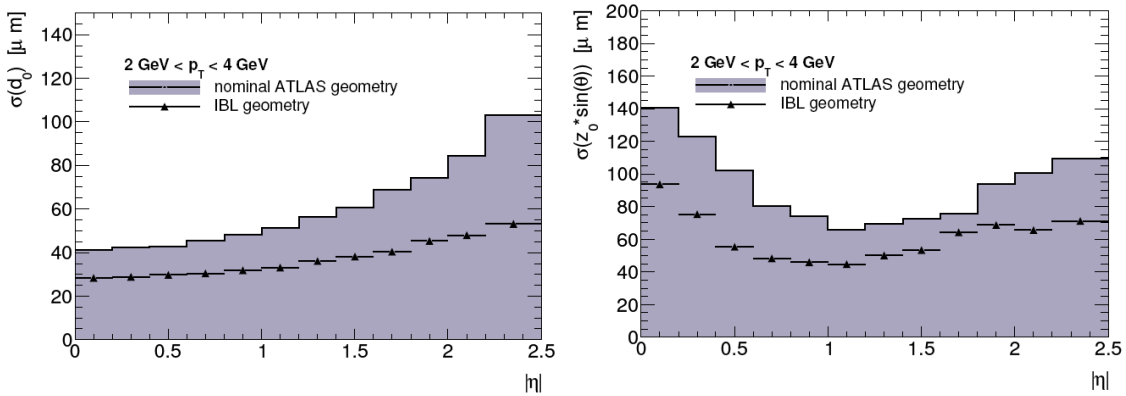

Figure 4.2 – Impact parameter resolution as a function of p_T for simulated tracks in $t\bar{t}$ events without pile-up. The transverse impact parameter resolution d_0 (left) and the longitudinal one (right) ($z_0 \cdot \sin(\theta)$) are compared for an ID layout without and with inclusion of the IBL layer.

As expected from IBL smaller longitudinal pixel size and smaller radius (Table 4.4), both impact parameter resolutions will be improved. A complete evaluation of the expected tracking and vertex reconstruction performance can be found in ref. [54].

One of the major impacts from the improved track parameter resolution is the performance increase of the b-tagging. The increased d_0 resolution with the IBL allows to identify secondary vertices with higher resolution, improving the discrimination of secondary vertices and the reconstruction of tracks in dense environments. The following results were obtained on Monte Carlo simulated top pair production events (using AntiKt reconstructed jets [55] with radius R = 0.4). A final IBL geometry was implemented within the ATLAS simulated geometry as well as a detailed digitalisation model and a refined neural network clustering algorithm [39]. For simplicity, the b-tagging efficiency comparison presented was performed with the end of Run-1 conditions (pileup ~ 20).

The b-tagging algorithm MV2c20 [56] was used for the presented studies. Based on the impact parameter, secondary vertex reconstruction and the reconstruction of the complete decay chain, MV2c20 allows a high efficiency light-jet identification (u,d,s-quark or gluon jets) and c-jet tagging. Primarily, the impact parameter algorithm relies on the lifetime of the quark associated to the single track matched to the jet. The decay jet is then analysed by the vertex algorithm, based on the jet properties such as track multiplicity, mass, energy fraction and charge decay fraction. Finally, the multi-vertex algorithm reconstructs the decay chain from the primary vertex to the final jet. The b-tagging performances obtained are shown in Figure 4.3.
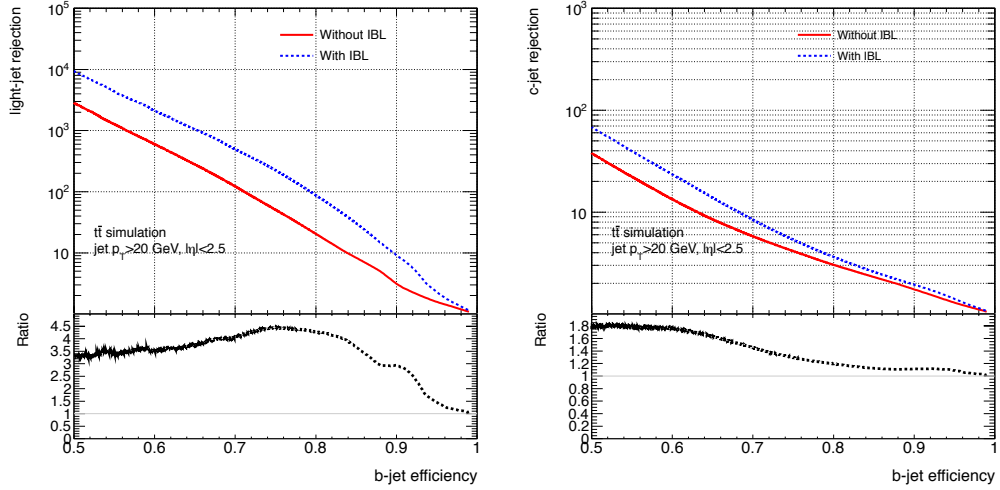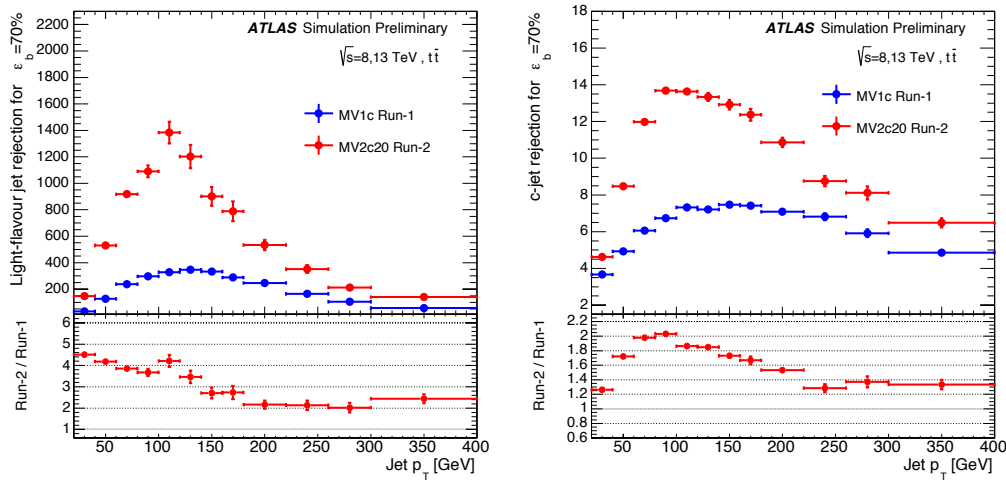

Figure 4.3 – MV2c20 b-tagging performance expressed in terms of light-jet (left) or c-jet (right) rejection as a function of b-tagging efficiency. The algorithm is applied to jets from top pair events with a basic jet selection ($p_T > 20$ GeV and $|\eta|$<2.5%). The performance of the Run-I and Run-II detector layouts are compared, where the latter includes IBL. The rejection is defined as $R = 1/\epsilon$, with ϵ being the tagging efficiency. The ratio plot shows "with/without" rejection factor.

The inclusion of IBL improves the light-jet rejection by a factor 3 to 4 for b-jet tagging efficiencies up to 85%. Due to the c-quark mass the improvement in c-jet rejection is only 80 to 20 % for b-jet tagging efficiencies up to 80%. Simulation results for a given light jet rejection comparing the b-tagging performances with and without IBL are summarised in Table 4.1.

Light-jet rejection	b-jet efficiency w/o IBL	b-jet efficiency with IBL
1000	57%	65%
100	71%	79%
10	84%	90%
Constant c-jet rejection	b-jet efficiency w/o IBL	b-jet efficiency with IBL
20	56%	62%
10	63%	68%
5	72%	76%

Table 4.1 – b-jet tagging performance expressed in terms of b-jet efficiency for a fixed light- or c-jet rejection, comparing the Run-I and Run-II detector layouts, where the latter includes IBL. The results are derived from jets from top pair production, which pass the $p_T > 20$ GeV and $|\eta| < 2.5$ selection requirements.

Due to the dependence of the impact parameter on the jet transverse momentum, the b-tagging performance is strongly p_T dependent. B-tagging performances as a function of the jet p_T are shown in Figure 4.4. Particularly at low p_T, the impact of multiple scattering from the beam pipe was significantly reduced due to the small IBL radius, improving the light-jet and c-jet rejection over all mass ranges. At high p_T, the jet identification is limited by the track identification due to the collimated tracks producing shared clusters. The IBL being significantly closer to the beam pipe (from ~ 5 to ~ 3.2 cm) is more affected. The reduced pixel size combined with the development of pixel clustering algorithms to deal with such an environment [39, 57] allowed to improve the performance at high p_T otherwise compromised.


Figure 4.4 – Performance of the b-tagging algorithm MV1c (run-I) and MV2c20 (run-II) expressed in terms of light (left) or c-jet (right) rejection as a function of jet transverse momentum (p_T), while keeping the b-tagging efficiency fixed at 70% in each p_T bin. The rejection is defined as $R = 1/\epsilon$, with ϵ being the tagging efficiency.

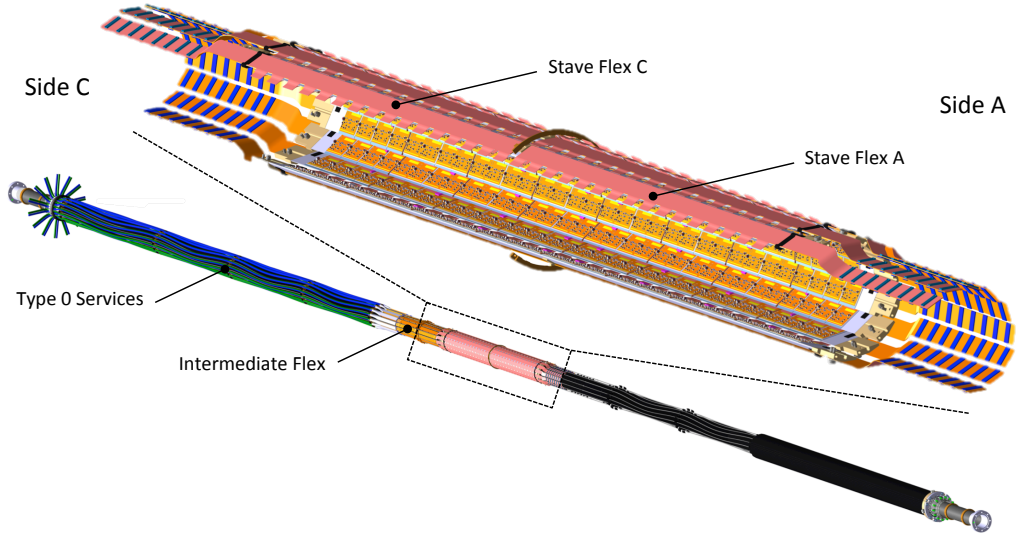### 4.1.2   Overview of the IBL Detector within the Pixel Detector

The IBL detector was inserted between the Pixel B-layer and the beam pipe, providing a fourth innermost pixel space-point. Due to the small B-Layer inner envelope of only 42.5 mm radius, the existing beam pipe was replaced by a new beryllium pipe with a reduced radius of 23.5 mm and therefore allowing the insertion of the new layer.

The IBL Detector and its services were installed inbetween an external Inner Support Tube (IST) fixed on the Pixel structure and a precision mechanical support located around the beam pipe, the Inner Positioning Tube (IPT). During the LHC LS1, the Pixel Detector was brought to the surface for various service repairs and standard maintenance. During this surface intervention the IST was installed inside the Pixel Detector, preparing for the future IBL insertion in the experiment. The 4-layer Pixel Detector is shown in Figure 4.5, including the IBL and its services.

The IBL Detector is composed of 14 carbon-fibre mechanical structures (staves) arranged in ϕ with a mean radius of 33.5 mm (compared to 50.5 mm for the Pixel B-Layer). They are read out at both stave's extremities (End-of-Staves, EoS) via independent services as shown in Figure 4.6. The IBL staves are therefore electrically divided at their centre (leading to the A- and C- side of the staves). The most important layout parameters of the IBL detector are listed in Table 4.2.
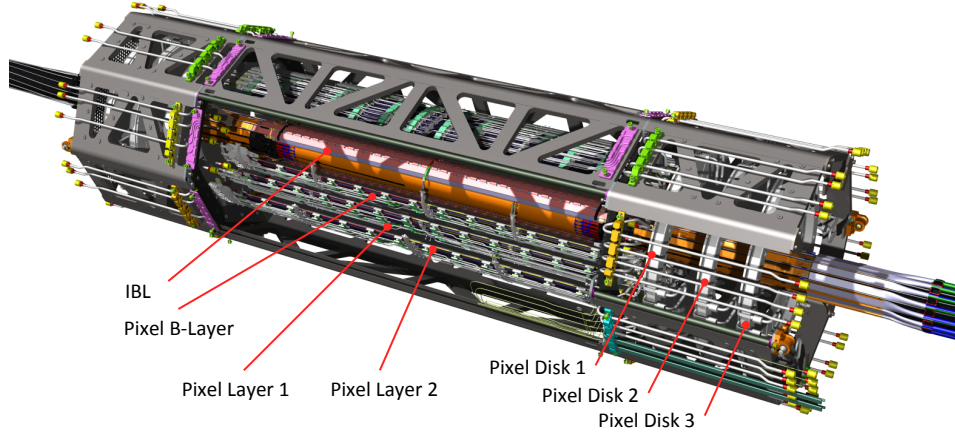
Figure 4.5 – View of the IBL detector positioned in the Pixel Detector.

Figure 4.6 – Longitudinal view of the IBL detector and its services. The insert shows the IBL detector with its staves arranged around the beam pipe.

Parameter	Value
Number of staves	14
Number of physical modules per stave	20 (12 planar + 8 3D)
Number of FEs per stave	32
Coverage in η, no vertex spread	$|\eta| < 3.0$
Coverage in η, 2σ (122 mm) vertex spread in z	$|\eta| < 2.58$
Active $|z|$ stave length (mm)	330.15
Overlap in ϕ (degree)	1.82
Center of the sensor radius (mm)	33.5
Radiation length at $z = 0$ (% X_0)	1.9

Table 4.2 – Main parameters of the IBL detector. The quoted radiation length is averaged over the stave width and includes the IBL support and positioning tubes. The vertex spread at the collision point is expected due to the gaussian profile of the beam as well as their crossing angle at the interaction point.

In order to provide a full azimuthal (ϕ) hermeticity, the staves were mounted with an overlap of the sensor active area of $1.8°$ on ϕ, allowed by a stave tilt of $14°$ with respect to the radial direction[1]. Longitudinally, modules are not shingled due to space limitations. However, in order to minimise the dead region between modules, modules were glued with only $200\,\mu m$ gaps (Section 5.2). The IBL staves active area have a pseudo-rapidity coverage of up to 3 from the nominal interaction point.

Due to the innermost position of the IBL (small radii and large pseudo-rapidity coverage), its material budget has a direct impact on the overall ATLAS performance (such as tracking due to multiple scattering). The final IBL has a total radiation length of $X_0 = 1.88\,\%$ for normal incident tracks at $z = 0$, mostly driven by the modules contribution as shown in Table 4.3. In comparison, the IBL material budget is $\sim 70\,\%$ of the Pixel B-Layer. The radiation length reduction has been achieved by using more aggressive sensor technologies, cooling and services as discussed in the following sections.

Item	Value (% X_0)
IPT	0.12
Module	0.76
Stave	0.60
Services	0.19
IST	0.21
IBL total	1.88

Table 4.3 – Averaged IBL material budget over the azimuthal direction for normal incident tracks at $z = 0$. The beam pipe material is excluded from the IBL total.

Each of the fourteen staves are equipped with 20 silicon pixel modules. Two different types of modules were installed on each stave [58]. The central region was loaded with 12 "double-chip" (DC) modules with planar pixel detectors (Section 4.2.2), each read out by two Front-Ends. At each of the two EoS, four "single-chip" modules with 3D sensor technology were loaded. Figure 4.7, shows the stave loading scheme as well as a transverse view of the IBL package.

At the EoS, the detector services, providing data transmission and power to the modules, are connected to the stave-flex (Section 4.2.5). With a total length of $\sim 9\,m$, they reach the Inner Detector End-Plate (PP1), where the connections to the external services are made after installation inside ATLAS.

The IBL and Pixel Detector technical characteristics are compared in Table 4.4.

4.2 IBL Components Design

4.2.1 New Hybrid Pixels Modules for the LHC Run II

Design of the new FE-I4 Chip for LHC Run II

Due to the expected radiation doses [59] and hit occupancies for instantaneous luminosities of up to 3×10^{34} cm^{-2}s^{-1} [60] during the next LHC run II, the current pixel detector FE chip (FE-I3) will not be adequate any more for an efficient data tacking [60]. Therefore, a new FE (the FE-I4, see Figure 4.8), was developed. Built with a 130 nm Complementary Metal

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[1]This tilt also compensates for the Lorentz angle of drifting charges in the case of planar sensors.
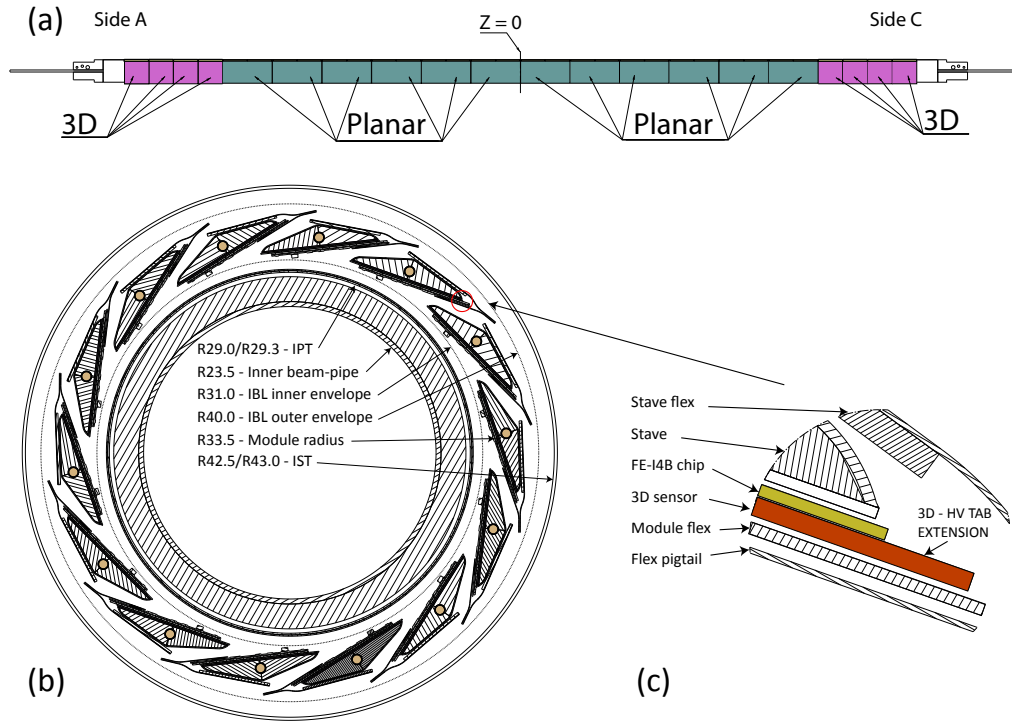
Figure 4.7 – IBL layout: (a) Longitudinal layout of planar and 3D modules on a stave. (b) A $r - \phi$ section showing the beam pipe, the IPT, the IBL staves and the IST. (c) An enlarged $r - \phi$ view of the corner of a 3D module fixed to the stave.

	Pixel	**IBL**
Active Surface (m^2)	1.73	0.15
Number of channels (x 10^6)	80.36	12.04
Pixel size (μm^2)	50×400	50×250
Pixel array size	18×160	80×336
Chip size (mm^2)	7.6×10.8	20.2×19.0
Fraction of active area (%)	74	89
Analog current (μA/pixel)	26	10
Digital current (μA/pixel)	17	10
Analog voltage (V)	1.6	1.4
Digital voltage (V)	2.0	1.2
Data out transmission (MBit/s)	40	160
Sensor type	planar	planar / 3D
Sensor thickness (μm)	250	200 / 230
Layer thickness (% X_0)	2.8	1.9
Cooling fluid	C_3F_8	CO_2

Table 4.4 – Comparison of the main characteristics of the Pixel Detector (B-layer and Layer 2 and 3) and the IBL detector. The currents reported are those expected before irradiation.
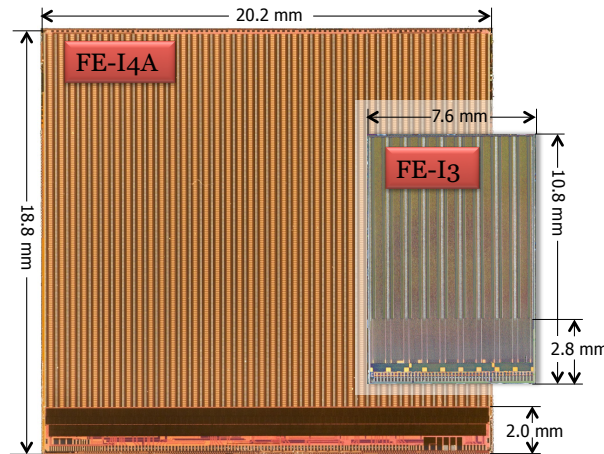
Figure 4.8 – Picture of the FE-I4A IC (the to-scale FE-I3 IC is shown for comparison) [44].

Oxide Semiconductor (CMOS) technology, its new design with thin gate oxides layers (of about 2 nm) reduces the charge trapping in the dielectric materials [61] and therefore improves its radiation hardness with respect to the FE-I3. With an active area of 20.2×18.8 mm^2 (organised in 80 columns and 336 rows), a pixel granularity of 250×50 µm^2 was chosen to fit the minimum bump-bonding distance in the ϕ coordinate increasing the detector resolution for high p_T measurements while keeping a larger pixel size along the beam axis to host the complex embedded electronics (particularly its digital circuitry design to cope with much higher hit rates and local tunings).

The design of the FE-I4 is based on a hybrid IC combining an analog and digital section. As shown in the schematics of Figure 4.9, in order to provide a linear amplification versus input charge and to maintain the amplifier performances up to doses of 250 Mrad, a double stage amplifier was implemented, with a tuneable first stage current feedback reset preamplifier. A second stage amplifier is AC coupled to the preamplifier decoupling the second stage from sensor leakage current. The AC coupled second-stage allows a capacitance optimisation of the amplifiers so that a larger amplification factor can be achieved in the second stage while allowing a preamplifier optimisation for charge collection efficiency, signal rise time and power consumption [62]. In the FE-I4, where no shaper was implemented, a classic two-stage architecture discriminator is used. The return to baseline behaviour (feedback current) and the discriminator level (threshold) of each pixel can be set independently thanks to global and local DACs.

The digital circuitry is based on standard synthesised cells, allowing the use of well developed and verified industry standards. The digital logic of the FE-I4 is designed so that four analog pixels share a digital unit (so called "4-pixel digital region", 4-PDR), allowing a local storage of the hit information until triggering or erasing and efficiently reducing the data transfer and power consumption [63]. This new approach was achieved thanks to the smaller feature size and the introduction of a deep n-well providing the needed isolation, avoiding noise coupling of the digital cell local substrate from the global one hosting the analog part. Figure 4.10 shows schematically the digital organisation of a 4-PDR. Each analog pixel has an associated hit processing unit and a buffer memory, where up to 5 ToT hits information can be stored. When a hit is recorded by one of the analog units of the 4-PDR, a record is kept in the latency counter allowing the timing association (time-stamp) of the hit and the trigger processing. Additionally to the hit processing, a local pixel configuration is stored in the digital part for tuning and operation.
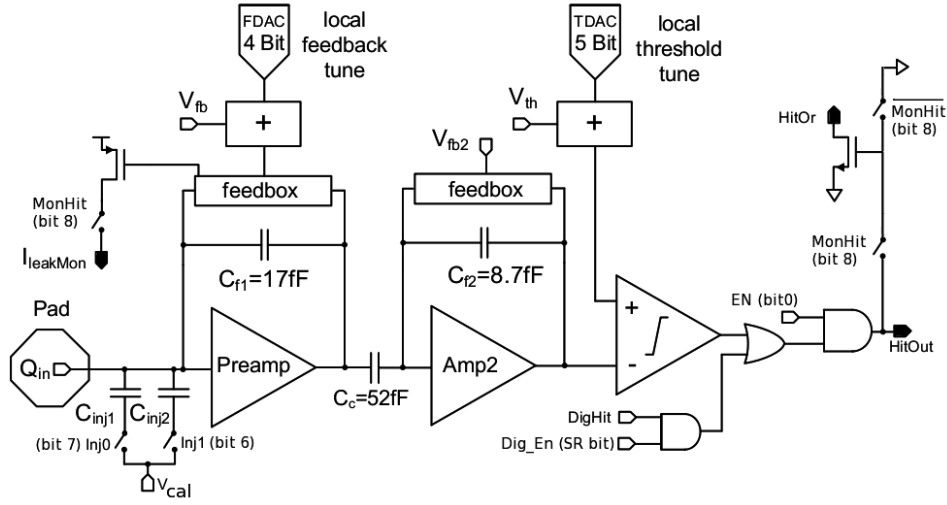
Figure 4.9 – Schematics of the analog pixel section of the FE-I4 chip [58].
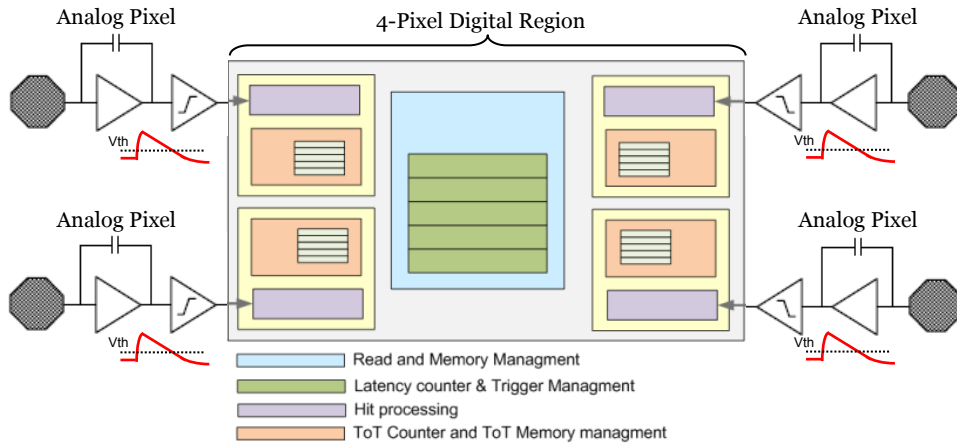
Figure 4.10 – Organization of the 4-pixel region, focusing on a schematic of the digital region [58].

Thanks to the high-level logic implemented in the pixel matrix, only the FE-I4 global functionalities such as communication, powering and LV-level generation had to be implemented at the chip periphery, achieving an active area of ∼90%. The FE-I4 can therefore be operated via a single LV input line (where analog and digital voltages are generated internally), and three 40 MHz LVDS signals for clock, command and data out (streaming 160 Mb/s). The sketch overview of the FE-I4 is shown in Figure 4.11, showing the analog pixels arranged in double columns and their associated digital blocks, as well as the periphery.
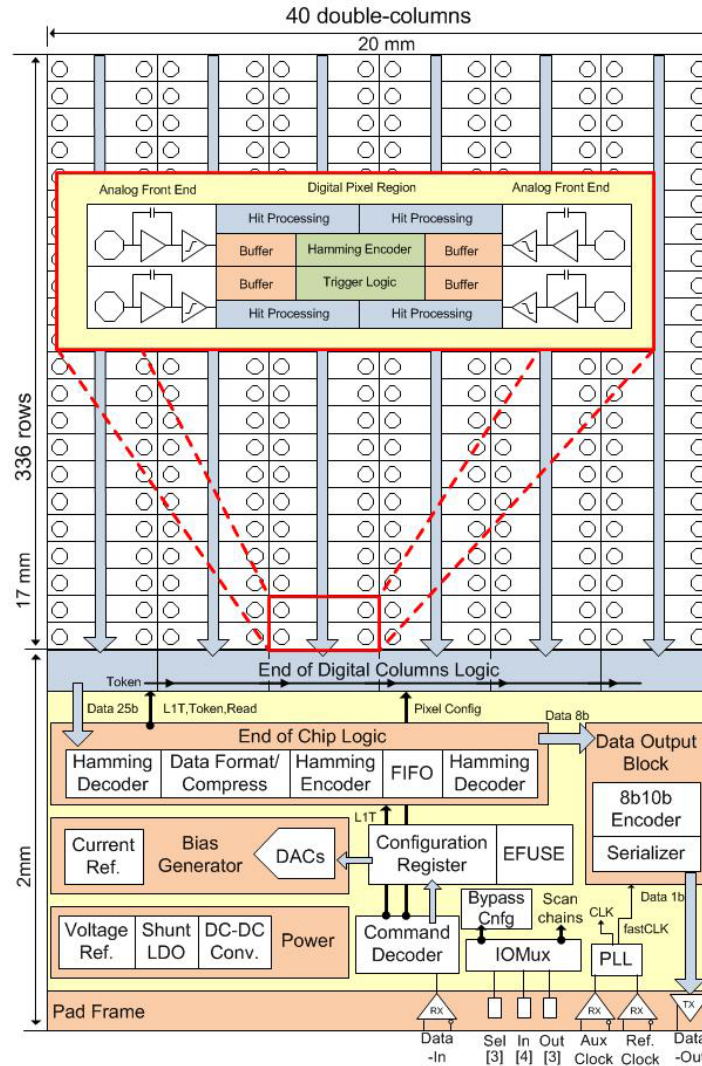
Figure 4.11 – Sketch of the organisation of FE-I4 IC [58].

Performances of the FE-I4

One of the key parameters of the FE-I4 is the on-chip generation of reference voltages and currents. In order to achieve a good voltage stability over a large range of radiation doses and digital activities, a *reference current* (Iref) of 2 μA is used. This current being the reference for all subsequent generated voltages, the range response of each FE was checked during wafer probing as shown in Figure 4.12, discarding the FE's that could not match the 2 μA current. The corresponding Iref setting of successful FEs was then retained and implemented during module loading.

Additionally to the reference current, the tuneable digital and analog supply voltages of the FE-I4 were tested during wafer probing. Figure 4.13 shows the maximum and minimum output values of the on-chip tuneable reference LV circuit. As expected, no significant difference is observed between the analog and digital output voltages being both feed by the same input LV line and having identical circuit designs. The analog and digital reference voltages are used for the Analog (VDDA) and Digital (VDDD) output voltages generation with a multiplication factor of two.
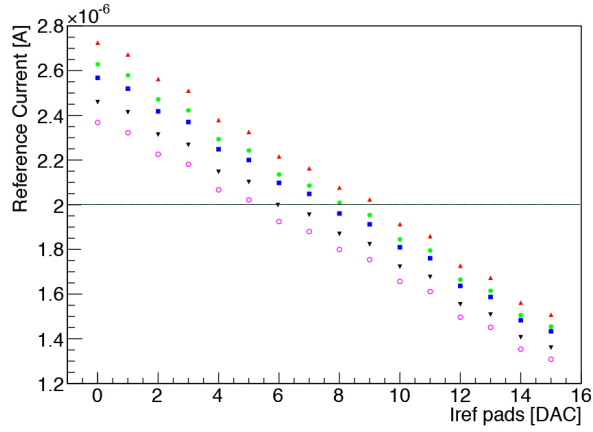
Figure 4.12 – Measured reference current as a function of the corresponding DAC setting for five FE-I4 chips. The x-axis "Iref pads" refers to the wire bonding setting of the 4 bit DAC. In this case, all five chips were accepted because the reference current of 2μA could be achieved within resolution. Adapted from [64].
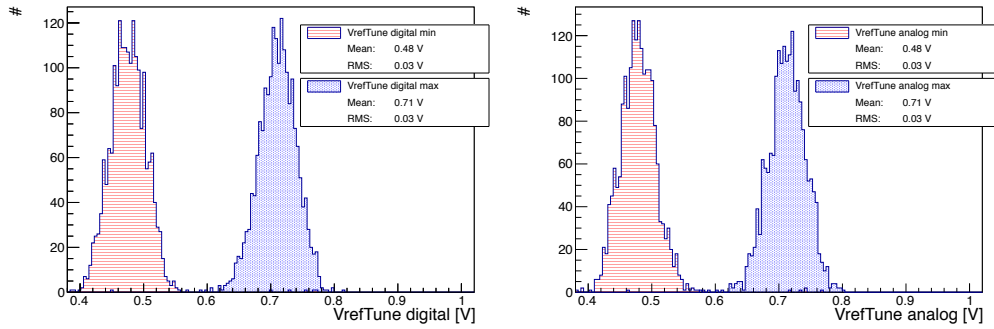

Figure 4.13 – Minimum and maximum output voltage of the digital (left) and analog (right) tuneable reference voltage circuit. Both circuits are identical and no significant difference is expected. Adapted from [64]

The VDDA and VDDD of the FE-I4 being of 1.5 V and 1.2 V respectively, analog and digital supply voltages were required to match the 0.75 V and 0.6 V respectively with a 10% safety margin. Digital and analog supply output voltage depend linearly on DAC setting. The slope of the linear fit obtained for all produced FEs is shown in Figure 4.14, as well as the LV output voltages after DAC tuning to match the design values.

During part of Run-II the LHC operated at a 25 ns Bunch Crossing (BC) frequency, making the FE-I4 timing performance critical for track reconstruction. These can be measured thanks to the charge injection and the phase delay between the clock and trigger (i.e. delayed injection). In Figure 4.15 (left) the hit detection probability is shown for a large injected charge of 45 ke$^-$ as a function of the injection delay. For an ideal detector it is expected a perfect box-like detection probability with a 25 ns plateau (i.e. if the charge is injected at any time during the reading time) with a constant delay from the circuitry. Despite of the large injected charge, it can be observed that the pixel response is close to the ideal behaviour but with a small detection turn-on time, defined as the 50 % hit detection probability. In order to safely operate the chip, a global delay t_0 was set to the FE mean turn-on time plus a safety margin of 5 ns. With this procedure, 20 ns
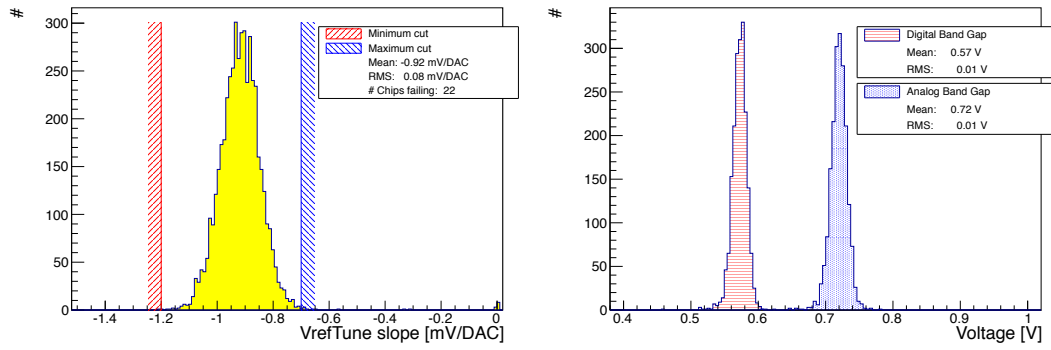
Figure 4.14 – Distribution of the slope of the linear fit to the output characteristic of the tuneable reference voltage (left). Due to the identical circuit design of the analog and digital regulators, the histograms of the reference voltages for the digital and analog are added together. The output voltage distribution of the "tuned" reference voltage for the analog and digital regulators (right). It becomes clear the tuning effect by comparing the RMS of these distributions with those shown in Figure 4.13. Adapted from [64].
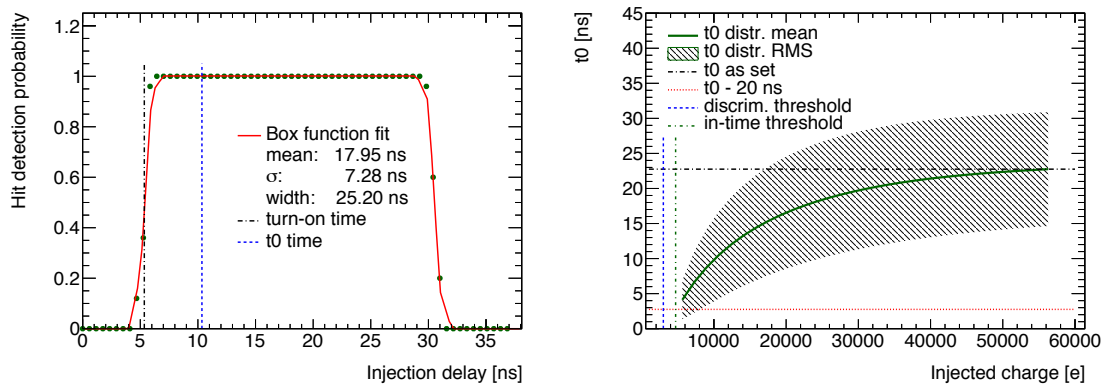

Figure 4.15 – (left) Single pixel hit detection probability during a t_0 scan where analog injections with high charge are performed while scanning the on-chip injection delay and a single consecutive bunch crossing is read. The pixel t_0 is set to the turn-on delay plus 5 ns. (right) FE mean t_0 as a function of the injected charge. The effect of the time-walk is visible for the small charge.

are left for time-walk and late events, and a 5 ns window is left for early pixel/events. As seen in Figure 4.15 (right), a time-walk effect of 20 ns is visible in the t_0 dependence versus charge. According to simulations, the total amount of missed FE-I4 hits at LHC Run-II conditions due to timing performances (mostly driven by double hits and overflow) was estimated to be 0.56%.

Additionally to the timing scan, the charge injection circuitry allows the calibration and test of each channel response by feeding the preamplifier of each pixel. For calibration purposes, the voltage V_{cal} which defines the voltage step over the injection capacitance (equivalent to charge: $Q\,[e] = C_{inj} \cdot V_{cal}/e$), is measured using an external voltmeter. The charge injection of the FE-I4 pulser is controlled via a 10 bit DAC, allowing to inject up to 1.4 V. Figure 4.16 shows the resulting voltage as a function of the PulserDAC (left), as well as its deviation from the expected linear response (right). It can be observed the pulser saturates when all the pixels of the matrix are injected simultaneously, reaching the maximum amplitude voltage injection at low DAC values. During scans, where large injected charges are needed, the FE-I4 Double-Columns are divided in

subgroups and injected sequentially, increasing the charge range up to 54 000 e$^-$ per pixel when both capacitances are active ($C = 5.7$ fF). During tuning and operation, a linear relation between charge and voltage is assumed, due to the negligible (‰) discrepancies observed (Figure 4.16 right).

Figure 4.17 summarises the failure modes of the FE-I4 during wafer probing. A total of 1,821 chips passed all tests giving a production yield of approximately 60 %. As it can be seen, most FE were rejected due to a large fraction (>0.2 % failing pixels or >20 pixels per column) of bad pixels (defined as pixels not passing the test summarised in Table A.1 of Appendix A). FEs failing the injection circuitry, high digital and analog current requirements, as presented previously, represent about 10 % of the total.
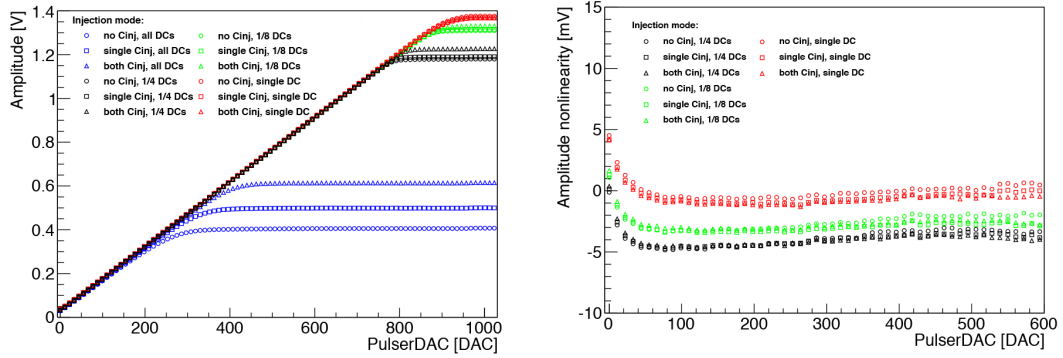
Figure 4.16 – Amplitude of the output pulse voltage as a function of the corresponding 10 bit DAC setting (left) for different injection modes. Four different injection masks are shown: all the pixels simultaneously ("all DCs"), one every four pixels ("1/4 DCs"), one every eight pixels ("1/8 DCs") and one every forty pixels ("single DC"). Difference between the measured amplitude and the ideal amplitude (obtained from a linear fit to the single double-column injection mode) (right). Data from [64].
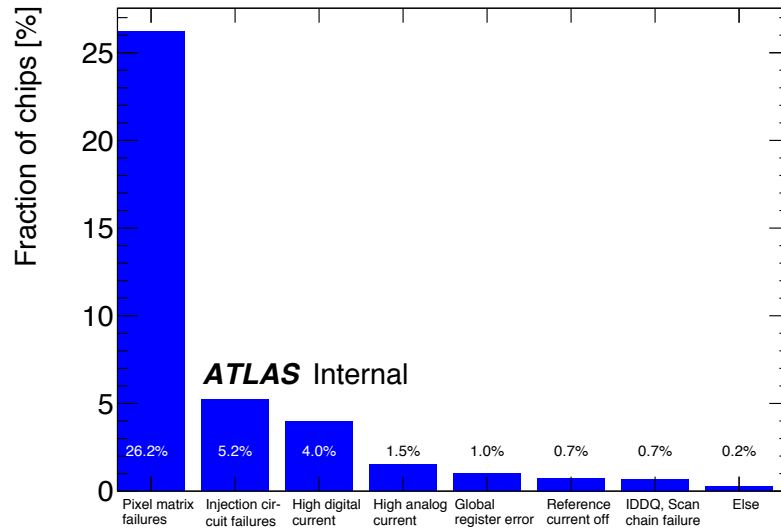
Figure 4.17 – Failure modes leading to a disqualification of the FE-I4 for IBL operation. All 2814 fully probed chips were taken into account. Each bin shows the failure mode in percent.
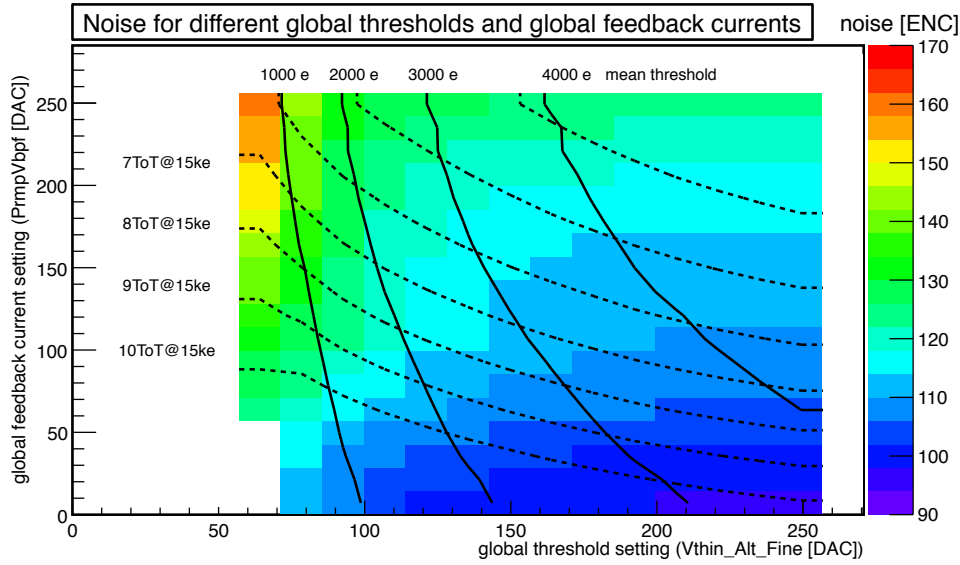
Figure 4.18 – Dependence of the ENC on the global threshold setting (x-axis) and the global feedback current (y-axis) for a typical FE-I4. The solid lines show the mean threshold determined using a gaussian fit. The dashed lines show the mean of the ToT distribution for an input charge of 15 ke$^-$.

Finally, the noise performances of the FE-I4 as a function of its working point was studied. Figure 4.18 shows the dependence of the Equivalent Noise Charge (ENC) as a function of the Global threshold setting and feedback current. As it can be seen, the FE-I4 has a significant noise variation as a function of the setting parameters. High threshold configurations with low feedback currents, have a lower ENC of ~110 e$^-$ compared to ~150 e$^-$ ENC for low threshold and high feedback current. During LHC operation, the FE-I4 will operate in the noise range of 110-120 ENC, with a threshold setting of 2000-3000 e$^-$ and 9 ToT at 15 000 e$^-$.

The FE-I4 Scans

In order to test the FE functionalities and to tune and characterise the pixel performance, a set of scans has been developed and implemented. Presented in the following list, they will be used along this thesis for all pixel modules characterisation and performance measurements.

Register test: During this test, all 32 global and 13 local registers are written and read back for error checking.

Digital test: The aim of this test is to verify the functionality of the digital part of the pixel. Pulses are injected repeatedly at the output of the discriminator (simulating the discriminator signal) allowing to test the digital functionality without involving the analog circuit. During the test a given number of pulses are injected and the digital response count is measured.

Analog test: This test is similar to the *digital test* but with an injection before the preamplifier and therefore used to verify the amplification and discriminator stages. A given number of large charges are injected and counted in the digital part. The need of the digital processing requires therefore the standalone digital verification to be done before via the *digital test*.

Threshold scan: The main goal of the *threshold scan* is to measure the threshold and the noise (in ENC) for each pixel. In order to measure the pixel threshold, a set of charges are injected at the preamplifier level for each step, scanning from low to large charges. When the set threshold is achieved, the discriminator provides the input to the digital part and events are counted. In an ideal pixel, a step function is therefore obtained with zero occupancy before the set threshold and 100% afterwards. Thanks to the known injection circuitry capacitance, a threshold measured in electrons can be obtained.

In real pixels, due to noise and voltages fluctuations a s-curve occupancy is obtained. Charge values close below the threshold will trigger the discriminator with low probability and charges over the threshold might not reach 100% occupancies just after the threshold is matched. For realistic pixels, the threshold is defined as the 50% efficiency while the noise is inversely proportional to the steepness of the curve in the transition region.

The discriminator threshold for each pixel is controlled via a global 8 bit DAC at the chip level (for global threshold adjustments) and a 5 bit DAC for a pixel level fine-tuning. Therefore, during threshold tuning, global pixel parameters are tuned on a first step to match the set threshold and secondly a fine tuning is performed thanks to the local DACs at the pixel level. The tuning is performed as follows: multiple charge injections are performed at the target threshold (charge) and the number of processed hits at each global and pixel DAC settings is recorded. The DAC setting matching a 50% occupancy is retained as working point.

ToT: The *Time-Over-Threshold (ToT) scan* aims to measure each pixel ToT for a given charge. This is performed by injecting the target charge (charge at which we want to determine the ToT) and read out the ToT of the event in bunch crossing units of 25 ns. During a normal ToT scan, several injections are performed and therefore an error can be associated to the measurement.

During tuning, the ToT is set similarly to the threshold: multiple charge injections are performed at the tuning charge and the ToT DACs are scanned. The events DAC matching the desired ToT are retained as working point. The ToT tuning is done after the threshold tuning as the discriminator threshold is one of the pixel properties that affects the measured ToT along with the feedback current of the amplifier. During tuning, Threshold and ToT are adjusted iteratively.

Crosstalk scan: The *crosstalk scan* verifies the pixel-to-pixel isolation by injecting large charges (55 ke$^-$) in the neighbouring pixels, while reading the tested pixel. Due to the need of very high charges and the neighbouring pixels injection, this test needs to be performed in several mask stages. Although the crosstalk scan is not often used during the FE characterisation, after module assembly it allows to test the bump-bonding quality.

4.2.2   The IBL Sensors

The two different module types of the IBL (SC and DC) were equipped with two different sensor technologies: planar and 3D. The sensor designs were optimised to achieve a geometrical inefficiency[2] of less than 2.2% owing to new pixel design and guard rings. Both silicon sensor technologies were designed to resist up to $5 \times 10^{15}\, n_{eq}\,/cm^2$ while maintaining 97 % efficiency after irradiation [65].

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[2]The geometrical inefficiency is defined as the fraction of non-active area with respect to the total module area.

The Planar and 3D Sensor Technologies

The planar silicon technology used in the IBL was inherits from the current Pixel Detector [24, 36] a (n^+-in-n) sensor. The maturity of the well-known planar technology, together with the high production yield allowed the use of $200\,\mu$m-thick double-chip sensors produced by CiS [66]. This sensor with a pixel matrix of 160×336 and a pixel size of $250 \times 50\,\mu$m^2 is read out by two FE-I4 bump-bonded to the pixelised n-side of the detector.

In order to decrease the geometrical inefficiency, the module's central pixels (between adjacent DC module's FE) were elongated to $450\,\mu$m eliminating any dead region. Similarly, sensor-edge pixels of $500\,\mu$m were adopted combined with a new guard ring approach (slim edge) to obtain a geometrical efficiency > 77.8%. Additionally to the new guard ring positioning below, the active pixel (thanks to the n^+-in-n sensors design and the double side process), the number of guard rings was optimised and reduced from 16 to 13. Figure 4.19 illustrates the new guard ring in comparison with the old Pixel design. The new slim edge design combined with the reduced silicon edge cutting allowed to bring down the inactive edge to only $200\,\mu$m for the slim-edge IBL sensors [49]. The final IBL planar sensor dimensions are of $41\,315\,\mu$m $\times$ $18\,585\,\mu$m.
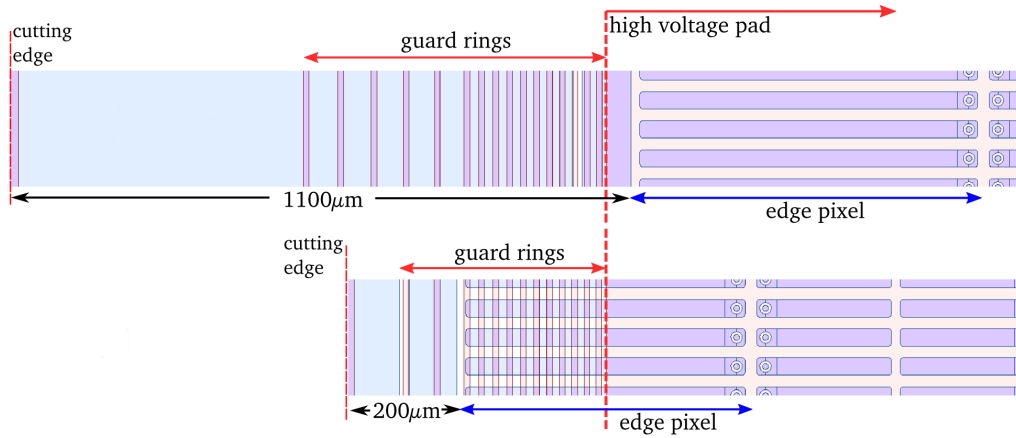

Figure 4.19 – Comparison of the edge designs of the current ATLAS pixel sensor (top) and of the planar IBL pixel sensor (bottom). The inactive edge has been reduced from $1100\,\mu$m to $200\,\mu$m. In the guard-ring area cooler colours (such as blues) represent the n-implantation on the front-side of the sensor, warmer colours (such as reds) the p-implantation on the back-side [49].

To ease the module assembly and loading processes, four fiducial marks were placed on the sensor allowing to precisely measure their position after loading. These marks are placed outside the guard-ring area of the sensor at each of the sensor corners.

A new n-in-p double-side 3D sensor technology was developed by FBK [67] and CNM [68]. With column-like electrodes penetrating the subtrate, a spacing between the electrodes of the order of the pixel size could be achieved. This fact, combined with the depletion growing parallel to the wafer surface, dramatically reduced the charge-collection distance and the operational voltage. A shorter charge-collection distance makes 3D sensors less sensitive to charge trapping after irradiation. This technology is particularly beneficial at high pseudo-rapidity, where traversing particles can cross the silicon sensor at shallow angles and so releasing a significant fraction of their energy in the sensor back side far from the electrodes. In addition, the low voltage depletion is less demanding in terms of power consumption and therefore in terms of cooling requirements.

IBL 3D sensors were produced on a 230 μm-thick sensor wafer. Due to a Deep Reactive Ion Etching (DRIE) technique and a dopant diffusion from both wafer sides, 12 μm-wide n+ columns from the frontside and p+ columns from the backside were edged without a support wafer. Figure 4.20 shows the 3D column layout for both FBK and CNM. Although both foundry detectors share the same basic sensor design, small process differences can be found, e.g. FBK sensors have full traversing electrodes (full 3D) contrary to CNM where the electrodes stop ∼20 μm before reaching the wafer edge.
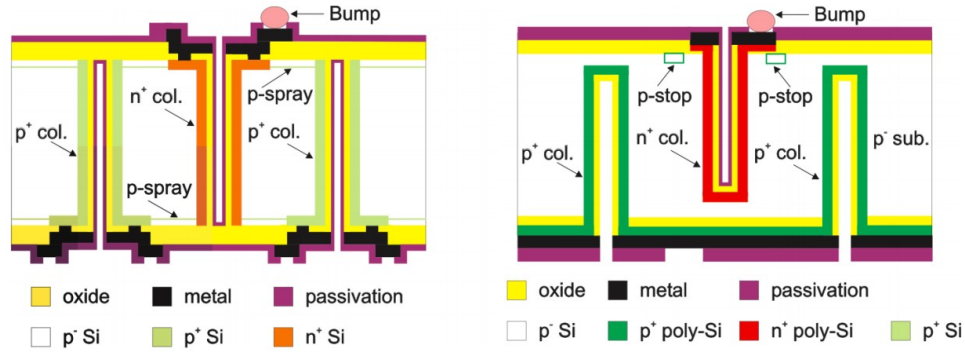
Figure 4.20 – Design of the columns of the FBK (left) and CNM (right) 3D sensors. This sketch is for illustration only and is not to scale.

The 3D sensors pixel matrix is made up of of 80×336 pixels with a pixel size of $250\,\mu m \times 50\,\mu m$. The inactive edge (defined as the distance between the active pixel to the physical sensor edge) is of 200 μm. This is achieved in the FBK sensors by a multiple ohmic column fence lowering the voltage of the depletion region at the sensor edges. In the CNM design, a 3D guard ring approach was used, where the active area is surrounded by a double row of ohmic columns. The 3D sensor have a nominal size of $20\,400 \times 18\,700\,\mu m^2$. Due to the new and complex sensor technology (and its expected lower yield), a single chip module (SC) was produced in order to maintain a reasonably high production yield.

For comparison, specifications of all three sensor provider CiS, FBK and CNM are summarised in Table 4.5.

4.2.3   IBL Modules Assembly and QA

Modules Assembly

IBL modules are hybrid silicon detectors composed of the presented planar and 3D sensors, read out by the new FE-I4. A modules-flex added on top of the sensor finalise the so-called "IBL modules", presented in the following paragraphs.

The connection between the FE and the sensor was performed using an electroplated (SnAg) bump-bonding process provided by IZM [69], with a pitch of 50 μm. During this process, the 150 μm-thick FE showed a deformation due to the thermo-mechanical stress and a glass carrier was therefore added during the bump-bonding process and removed afterwards.

The End-of-Column electronics, representing 2 mm of the chip length, overflows the sensor length and allows the placement of the wire-bond pads. A double-sided flexible printed circuit board (module-flex) was glued to the back-side of the modules, bridging the stave flex and the FE wire-bond pads. Two types of module-flexes were produced for SC and DC modules.

Parameter	Planar	3D CNM	3D FBK
Tile dimension [μm^2]	41315×18585	20450×18745	20450×18745
Sensor thickness [μm]	200	230	230
Pixel size (normal) [μm^2]	250×50	250×50	250×50
Pixel size (tile edge) [μm^2]	500×50	250×50	250×50
Pixel size (tile middle) [μm^2]	450×50	-	-
Edge isolation	Guard-rings	3D guard-ring, fences	Fences
Pixel isolation	p-spray	p-stop on n-side	p-spray
Operating bias voltage [V]:			
non-irradiated	80	20	20
after 5×10^{15} n_{eq} /cm^2	1000	160	160
Power at $-15\,^\circ$C [mW cm^{-2}]			
after 5×10^{15} n_{eq} /cm^2	90	15	15

Table 4.5 – Summary of the main design specifications of planar and 3D sensors.

Passive components were mounted on the module-flex for decoupling, filtering and terminating the signal traces. Due to the requirement that the modules need to withstand up to 1000 V bias voltage, the high-voltage lines and filtering were carefully designed and qualified. The module-flexes were wire-bonded to the FE using 25 μm-thick aluminium wires. Additional bonds were made to the powering pads for the low and high voltages for redundancy and safety. Figure 4.21 shows photographs of a single-chip and a double-chip module.
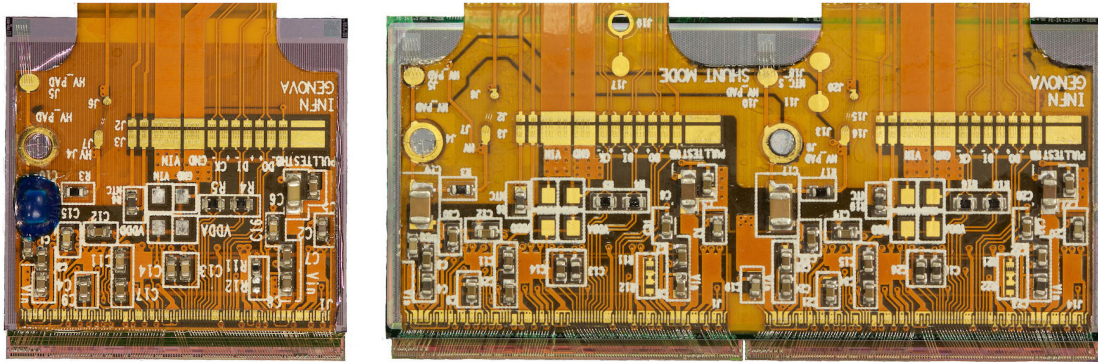
Figure 4.21 – Photographs of fully populated IBL single-chip (left) and double-chip module (right). The flex extension visible on the top allows testing of the module before loading on the stave. It is cut during the stave loading procedure at a cutting line slightly above the bare module. The size of the SC and DC is 2.0×1.9 cm^2 and 4.1×1.9 cm^2 respectively.

**Module Quality Assurance (QA)**

Assembled modules were tested and qualified before being sent for stave loading at the University of Geneva. The module testing was performed in parallel at INFN Genova (Italy) and Bonn University (Germany) in two steps. A first electrical check verification was performed after module assembly at room temperature, checking all FE and sensor functionalities. Modules failing this short test with a defective powering, biasing voltage or digital register were rejected. In the second step the modules were thermally cycled ten times from -40 °C to 40 °C, to avoid infant mortality

after loading on the final detector. A more extensive test was then performed on thermal-cycled modules, including on-chip regulators calibration, module basic functionality tests and tuning. The full performance validation, presented in the following paragraphs, was performed at $-15\,°C$ covering pixel-level failure measurements, timing, and operational range validations (for example: powering voltages, pixel noise and low threshold operability).

Only modules passing all required tests (detailed in Table A.1 appendix A) were considered for stave loading. Modules with a total number of "bad"-pixels larger than $1\,\%$ (i.e. 270/FE) were discarded. In order to take into account possible module reworks, a pixel equivalent penalty was associated in terms of bad pixels (Table A.2 appendix A).

One of the critical parameters of the IBL modules is the pixel noise, impacting the module performances and efficiency. The pixel noise is driven by the FE and the sensor capacitance, directly related to the FE preamplifier. In order to minimise the impact on the pixel noise from external parameters (such as Low Voltage (LV) powering, High Voltage (HV) and grounding), LV regulators and decoupling capacitors were installed in the FE and module-flex [70, 71]. The pixel noise is quantified in ENC, defined as the equivalent charge needed before the amplifier to create the equivalent signal to the measured noise. Pixel noise and module average distributions are shown in Figure 4.22 for each pixel type. Planar "long" pixels are shown independently of planar "standard" pixels due to their increased area and therefore capacity, showing a higher noise of $132\,e$ with respect to the $113\,e$ standard planar pixels average. Similarly, the 3D sensors have a slightly higher noise ($140\,e$ and $131\,e$ for FBK and CNM respectively) when compared to planars.
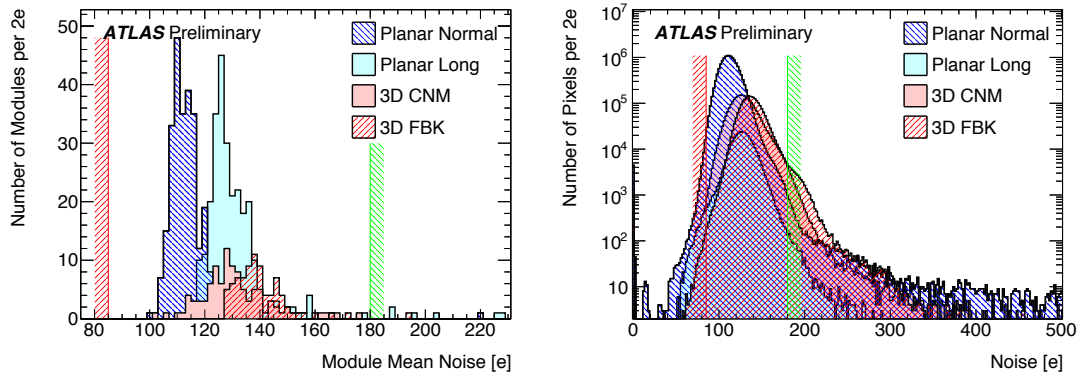

Figure 4.22 – The module mean noise distribution (left) and the pixel to pixel noise distribution (right) of all modules matching the IBL quality criteria. The noise is measured after tuning the modules to $3.000\,e$ threshold and 10 ToT counts for a charge injection of $16\,\text{k}e$ at approximately -15\,°C. The mean value of the Planar Normal (Long) distribution is $113\,e$ ($132\,e$) with a RMS of $12\,e$ ($144\,e$). The 3D CNM distribution has a mean value of $131\,e$ and a RMS of $70\,e$. The 3D FBK distribution's mean value is $140\,e$, the RMS is $66\,e$. 0.6% of the pixels fails the minimum (red line at $90\,e$) and maximum (green line at $180\,e$) cut (module mean noise value used for module selection only).

IV measurements were performed on each of the assembled modules and the break-down voltages were compared before and after module assembly. The module break-down voltage was carefully measured to guarantee a full depletion during the entire life-time of the detector. Due to the different electrode implementation in the planar and 3D technologies, the two sensor types had different operational voltages and break-down minimal voltage quality criteria.

Planar and 3D sensors operate at full depletion at $-80\,$V and $-20\,$V respectively, with a quality cut criteria during production of $-150\,$V for planar and $-20\,$V for 3D. All dressed IBL modules break-down voltages are summarised in Figure 4.23.
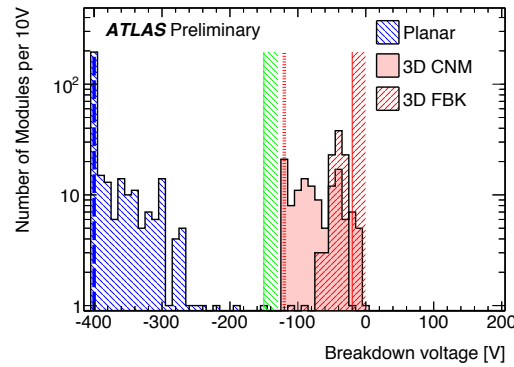
Figure 4.23 – The breakdown voltage distributions of all tested IBL modules at room temperature. The dashed vertical line indicates the maximum measurement point of -400 V for the planar modules and the dotted vertical line the maximum measurement point of -120 V for the 3D CNM and FBK modules. Additionally, the acceptance criteria for the Planar and 3D modules above -150 V (green) and -20 V (red) are indicated by the shaded areas. The mean value of the distribution of 313 planar sensors is -375 V. The 3D CNM distribution of 128 CNM sensors has a mean value of -73 V. The distribution of 93 FBK sensors has a mean value of -43 V.
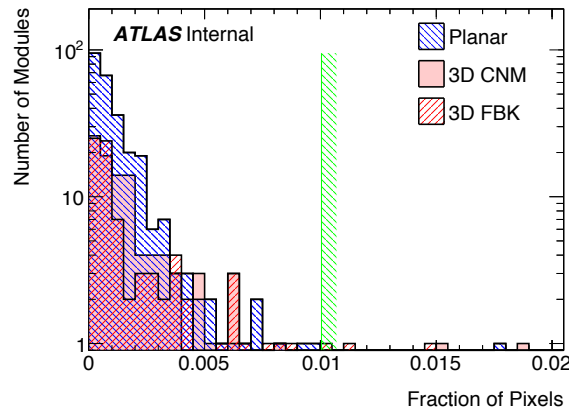
Figure 4.24 – The distribution of the fraction of pixels failing the occupancy criteria in the ^{241}Am source scan. A pixel is considered as failing if it has less than 5% or more than 450% of the mean module occupancy.

In order to detect open bumps, threshold measurements where taken without sensor bias and source measurements were performed. The threshold scan without high-voltage provided a good estimate for open bumps, as these could be identified from an observed significant decrease of the noise due to the absence of the sensor contribution. Occupancy scans were performed with an ^{241}Am 59,54 KeV γ source, irradiating uniformly the full sensor. Out of the two methods, the occupancy test was used for final bad pixel identification. In Figure 4.24 the distribution of the fraction of pixels failing the source test per module is shown.

The final fraction of bad pixels (i.e. the relative number of pixels having failed any of the quality tests) is shown in Figure 4.25. Due to IBL specifications, as mentioned, modules above 1% were discarded for IBL loading. The mean number of failing pixels of the accepted planar modules is about 0.56%. CNM and FBK modules have a similar bad pixels mean fraction of about 0.52% and 0.68% respectively.
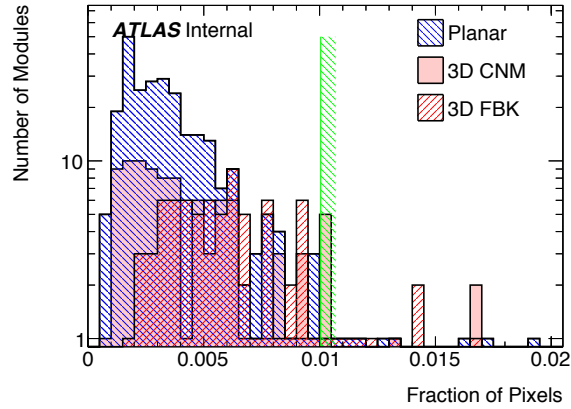
Figure 4.25 – The distribution of the fraction of pixels failing in any test. A pixel is considered as failing if it fails any one of the tests as described in the text.

4.2.4   The Support Staves

The fourteen IBL staves provide the mechanical support and cooling of the IBL modules. The material choice for the staves was dictated by the stringent requirements in terms of cooling, mechanical stability and radiation hardness [54]. As shown in Figure 4.26, each stave is composed of a 1.5 mm inner diameter and 100 μm-thick wall titanium pipe for the CO_2 cooling, a carbon foam, the carbon laminates (to reinforce the stave stiffness) and the EoS and central fixation to fix the stave around the IPT. The final material budget achieved is only $0.62\,\% \; X_0$ with a total weight of 26 g per stave.
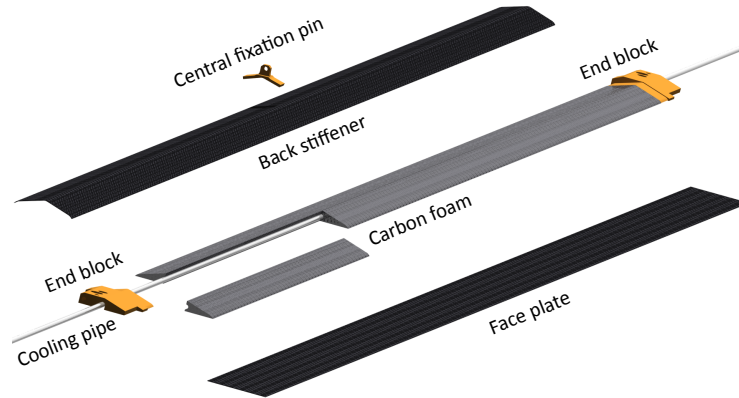

Figure 4.26 – Sketch of the bare stave.

In order to minimise the effect of the reverse annealing [72] and the thermal runaway, the IBL modules will operate below $-15\,°C$. Therefore, to guarantee a uniform cooling over all the stave length, a double-phase CO_2 cooling was adopted [73]. The stave cooling performances can be estimated by their Thermal Figure of Merit (*TFoM*), which is defined as the temperature difference (in a unit area per unit power) between the modules and the CO_2 cooling. As shown in Figure 4.27 (left), the *TFoM* remains constant over a wide range of power consumption and over all the stave length as expected from a double-phase cooling system. The temperature stability within the stave is shown in Figure 4.27 (right), which reports the modules temperatures for a cooling set point of $19\,°C$.
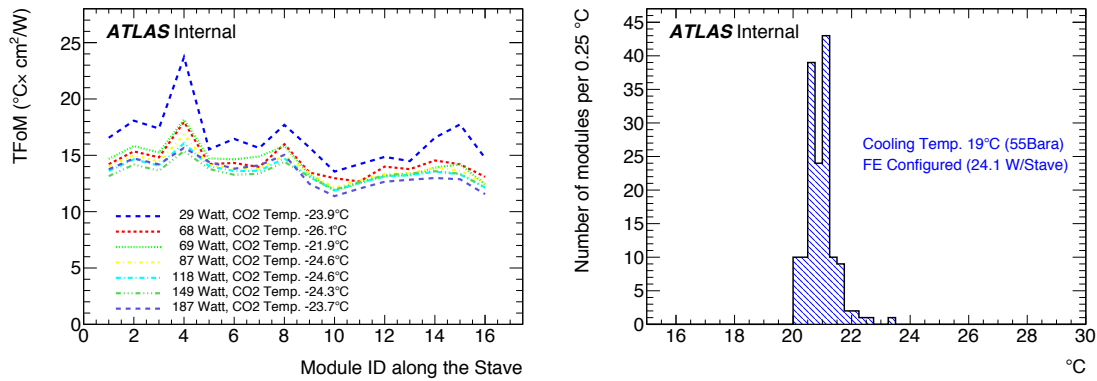
Figure 4.27 – $TFoM$ of $1.5\,mm$ diameter cooling tube along the cooling line (left). Distribution of modules temperature for all produced staves, at a cooling temperature of $19°C$ and with the read out electronics clocked and configured (right). The histogram has 152 entries, a mean value of $20.9\,°C$ and a RMS of $0.5\,°C$.
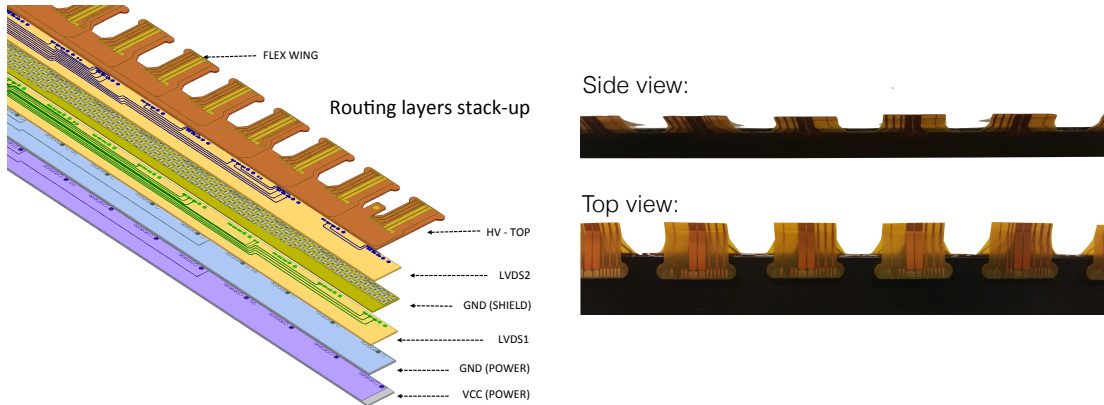

Figure 4.28 – Expanded view of the overlapping six layers in the stave flex (left). Glued stave-flex (left) side and top view.

## 4.2.5   IBL Readout and Services

As already introduced, the module-flex are connected via wire-bonding to the stave-flex routing the signals to the EoS. The stave-flex, is a multi layer flexible PCB that provides all the I/O signals and power lines to the IBL modules with a voltage drop below $400\,mV$ (within the 50 cm cable length) as required to safely operate the FE-I4 over the full range of drawn currents. Figure 4.28 shows the break down of the stave-flex layers (left) as well as a final stave-flex glued on a stave. The stave-flex has six metal layers of which two are $50\,\mu m$-thick aluminium for the LV and four are made of copper. This aggressive service design was chosen in order to cope with the limited available space, the required assembly accuracy, the radiation hardness (250 Mrad) and to maintain the service material budget below $0.2\,\%\,X_0$ at the stave level.

Two symmetric stave flexes were glued on the back of the stave facing away from the inter-action point. Each half of the stave modules (consisting of 16 FEs) placed in the face-plate of the IBL staves are connected via "wings" to each of the stave-flexes, routing the clock, command, data, LV, HV and ground lines to the modules from the EoS.
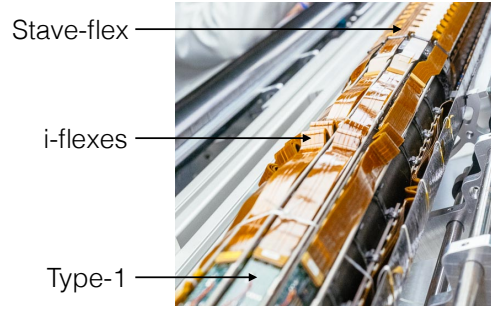
Figure 4.29 – IBL services: stave-flex, i-flex and type-1 installed around the IPT.

The stave-flex is connected at the EoS to the cable board via 6 intermediate flexes (i-flexes) as shown in Figure 4.29. The S-shape design of the i-flexes, was introduced to absorb the longitudinal movement of the services due to thermal deformation. At PP0, the *type-1* services is connected at the cable board to the i-flex on account of the high density Panasonic AXT540124 connectors. Type-1 cables have a total length of ~ 3.5 m for the powering and the Detector Control System (DCS) signals and ~ 8 m for data, clock and command lines. A schematic view of the IBL services is shown in Figure 4.30.
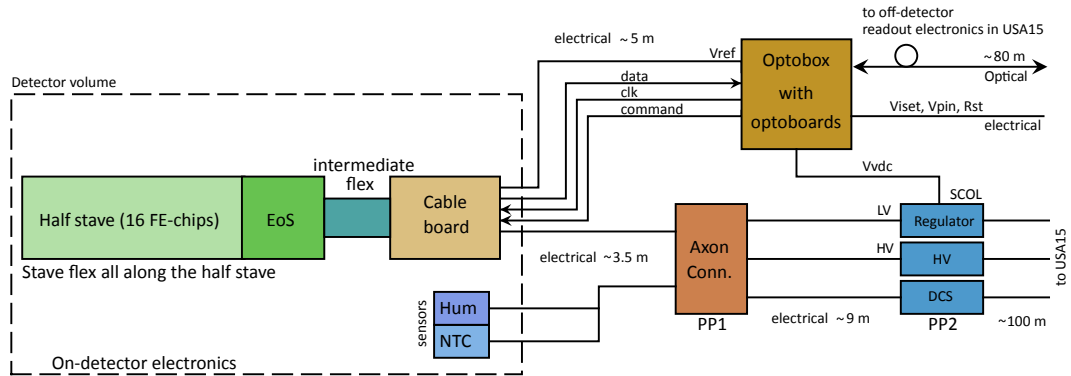
Figure 4.30 – Block diagram of on-detector electrical services for half a stave [74].

Stave loading and Quality Assurance

5.1 Components Reception and QA

5.1.1 Bare Stave and Stave-flex Quality Check

Optical Inspection

IBL staves and flexes glued at CERN were optically inspected and all LVDS and power lines electrically checked. Additionally, a high-voltage test checking for short and isolation defects was performed up to 1000 V for each HV line.

Before shipping the qualified staves to the University of Geneva for loading, the stave PCB-saver and intermediate flexes were installed. As shown in Figure 5.1, the intermediate flexes were connected to the stave-flex, routing all signals to the PCB-saver. This allowed the use of standard connectors for testing and thus limiting the connections on the delicate stave-flex connectors. For transportation and handling purposes over the production process, a stave handling frame hosting the stave and temporary services was developed. As shown in Figure 5.1, the handling frame was composed of a carbon fibre base and the support mechanics for the temporary readout electronics (PCB-saver and flexes) and cooling pipe. A transparent cover allowed access to the PCB-saver, while keeping the stave modules protected.

After having received the staves at the loading site, several components were inspected to guarantee no damage had occurred during transportation. The stave wings were carefully checked for bent or scratched pads which could have potentially affected the data signals transmission. At the same time, the face-plate and coating (guaranteeing the electrical insulation between the modules and the conductive carbon fibre stave) were checked for scratches and glue excesses that could affect the modules operation or positioning accuracy. Additionally, the stave end-blocks were carefully checked for any surface deformation (since the stave fixation and positioning depends strongly on the end-blocks tolerance).
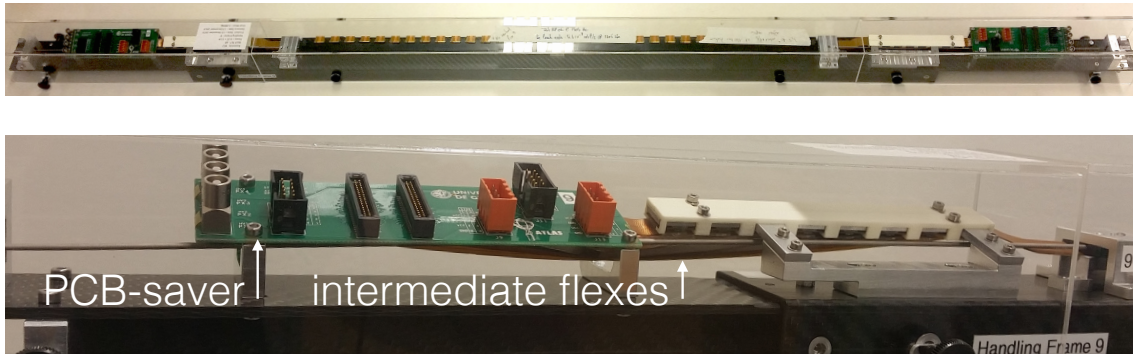
Figure 5.1 – Stave handling frame (top) carrying a bare stave+flex. PCB-saver and intermediate flexes (bottom) loaded on the handling frame and connected to the stave-flex. The plexiglas protection cover is visible in the pictures.

Metrology Survey

Due to the stave-to-stave overlap in ϕ and the limited available space between the beam pipe and the b-Layer, the IBL staves envelope need to be carefully monitored. During the IBL production, metrology measurements were performed after each major intervention on the staves. One of the main monitored parameters of the staves geometry was the face-plate planarity, defined as the minimum distance between two parallel planes containing the stave surface. The face-plate being the anchor point for the IBL modules and at the same time the closest stave-to-stave point, any stave showing a planarity larger than $350\,\mu m$ was not considered for integration.

During face-plate metrology a total of 99 different points were measured to sample the stave surface. This method, although not sensitive to local deformations (such as glue excess), measured the stave excursion precisely. The arrangement of the 99 points and the orientation of the axes are shown in Figure 5.2. For simplicity, the origin of the coordinate system was set on the stave end-blocks at the IPT fixation point.

Planarity measurements at the University of Geneva were performed with a Mitutoyo EURO C 9106 metrology machine, using a mechanical probe. In order to reduce the applied force, the stave was probed with an angle of $75°$ with respect to the face-plate normal, reducing the force to $2.5\ g_F$[1] (compared to the $8\ g_F$ applied at $0°$).
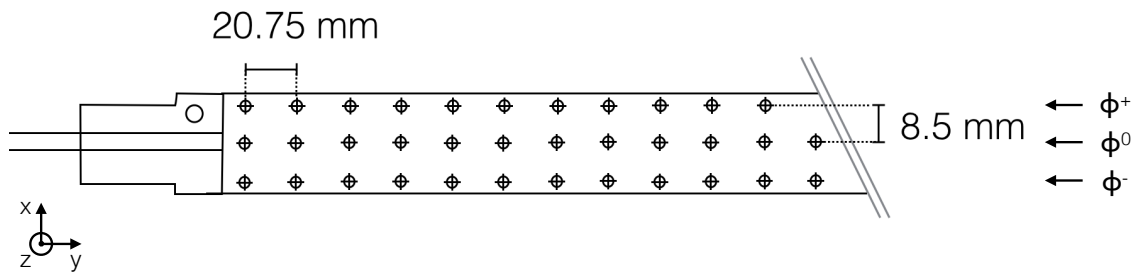
Figure 5.2 – Schematic view of the stave showing the location of the metrology points and reference axes. 99 probing points are organized in 3 lines spaced by 8.5 mm. The step of the points along the same line (ϕ) is 20.75 mm.

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[1]A g_F (gram-force) is the magnitude of the force exerted by one gram of mass in the gravitational field

Metrology measurements were performed on IBL staves on reception, after thermal cycling and after module loading. For comparison purposes, all measurements were performed with only the origin EoS fixed to the handling frame while keeping free the central support pin and the opposite EoS.

Thermal-cycling

After visual inspection and metrology measurements, the staves+flex assemblies were thermally-cycled. This process aimed to simulate the mechanical stress of the assemblies that they will face during the ATLAS cool downs (IBL nominal operation temperature being of $-15\,°C$) and warm ups (temporary shut downs). The thermal cycling was performed inside a climate chamber with temperature and humidity control. A vertical air flow maintained a uniform temperature within the chamber. The programmed cycle started with an initial temperature of $35\,°C$ for one hour, stabilising the temperature and drying the environment inside the climate chamber to reach a relative humidity of 1%. Then the temperature was cycled from $40\,°C$ to $-40\,°C$ ten times and kept stable for thirty minutes at each stage. At the end of the procedure the chamber temperature was set to $20\,°C$ for three hours.

After the thermal cycling, the face-plate metrology and the visual inspection were repeated. Figure 5.3 shows the result of the metrology measurements of a stave along each of the ϕ-lines, before and after flex gluing, and after thermal cycling. Despite the larger values of the stave extrusion after the thermal cycling, due to the Coefficients of Thermal Expansion (CTE) mismatch of the stave-flexes and the bare staves, all the staves fulfilled the planarity specifications (|planarity| $< 350\,\mu m$) before module loading. Measurements of the staves planarity before and after thermal cycles are summarised in Table 5.1.
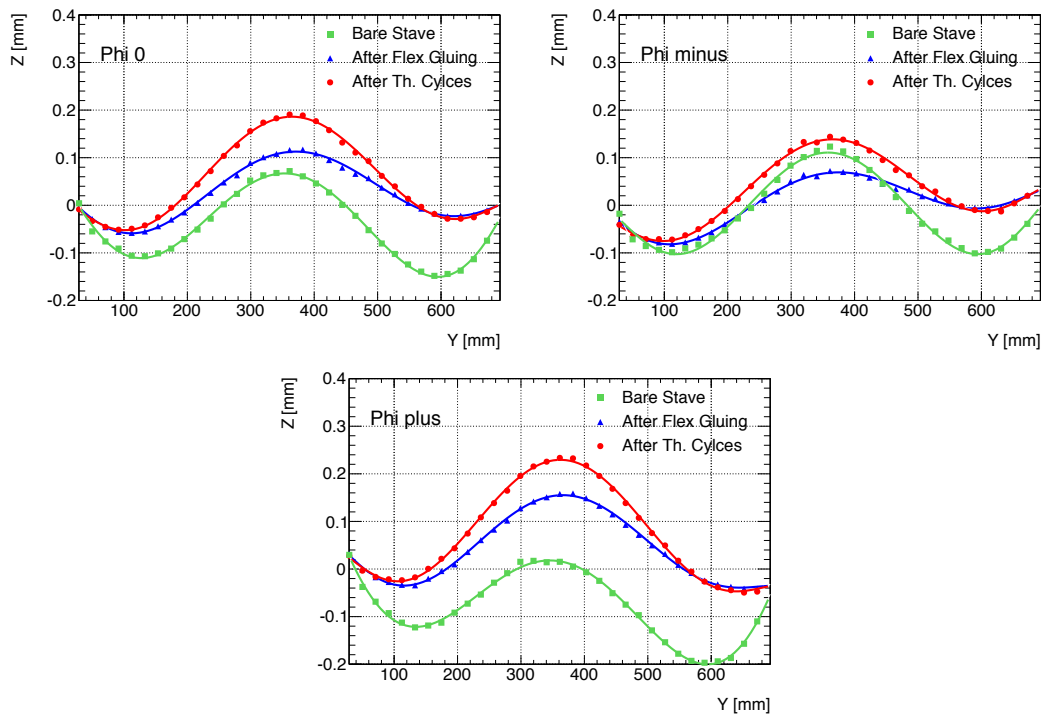
Figure 5.3 – Stave metrology measurements before stave flex gluing (Bare Stave), after flex gluing and after thermal cycling at different ϕ as shown in Figure 5.2.

	stave 1	stave 2	stave 3	stave 4	stave 5	stave 6	stave 7	stave 8
Planarity before [μm]	218	178	176	217	108	219	177	157
Planarity after [μm]	244	205	223	235	189	290	222	193
Dif. [μm]	26	27	47	18	81	71	45	36
	stave 9	stave 10	stave 11	stave 12	stave 13	stave 14	stave 15	stave 16
Planarity before [μm]	195	194	230	280	186	181	135	283
Planarity after [μm]	229	243	298	314	224	218	325	329
Dif. [μm]	34	49	68	34	38	37	190	46
	stave 17	stave 18	stave 19	stave 20				
Planarity before [μm]	-	282	220	257				
Planarity after [μm]	114	336	266	237				
Dif. [μm]	-	54	46	-20				

Table 5.1 – Measured planarity of the twenty loaded staves, before and after thermal cycling. Stave 17 data before thermal cycling was lost during production.

The overall stave production is summarised in Table 5.2. One stave failed the HV electrical test after flex gluing, showing a short after 600 V and was rejected. During the optical inspection of the IBL prototype staves, a flex delamination was observed at the EoS after thermal cycling. Therefore, a carbon fibre clamp was glued on production staves at the EoS, releasing the mechanical stress.

5.1.2   Hybrid Modules QA

The qualified modules (Section 4.2.3) produced at Bonn and Genova were tested on their arrival at the University of Geneva for final qualification before loading. After an optical inspection, further electrical tests were performed in a climate chamber where up to 4 single chips (SC) and 4 double chips (DC) were tested in parallel.

Optical Inspection

Due to the limited production time (∼one year), modules were shipped from the loading site on a weekly-basis. Although a special frame was developed to protect the modules during transportation [75], an optical inspection was performed again at their reception to check for their integrity. Particular attention was given to the wire bonds, since they are fragile and positioned at the FE edge. After transportation, wire bonds occasionally showed deformed or weakened wire-feet, which could potentially caused read out and powering issues.

Type	#
Staves accepted for flex assembly	24
Staves used for system test prototypes	2
Staves assembled with flex	22
Staves rejected after flex assembly	1
Staves qualified for module loading	21
Staves loaded with modules	20

Table 5.2 – Produced and qualified bare staves.

Pictures were taken systematically during the optical inspection (an example is shown in Figure 5.4, with a particular care for:

- *The fiducial marks*: located on each corner of the sensor and were the reference points used during the metrology survey.

- *The HV pads and wire bonds*: positioned at the edge of the module flex. Because of the reduced amount of glue used to minimise the material budget, the correct gluing of the module flex was checked. Additionally, the High-Voltage wire-bond redundancy and quality was checked.

The optical inspection has proven to be a fundamental step in the modules Quality Assurance, allowing to track most of the module failures that raised during the IBL production. A high definition global picture was added to the optical inspection in order to track other visible defect of the modules.


(a) (b) (c)

(d) (e) (f)
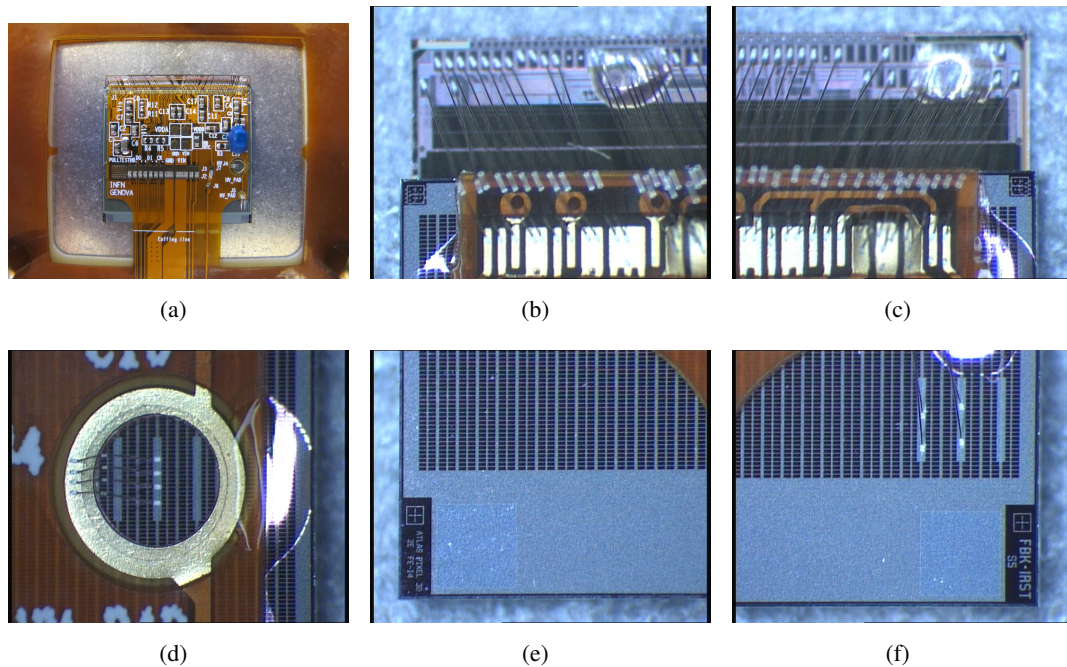
Figure 5.4 – Example of pictures taken during module optical inspection. These pictures show a global picture of the module (a), the fiducial marks of a FBK 3D module (b,c,e,f) and the HV-ring (d).

The USBpix Readout Setup

The USBpix [76] and STcontrol [77] is a hardware and software readout-system developed for silicon detector development. Adapted to the FE-I4, it was used for module characterisation before stave loading.

- The USBpix,is a Multi Input Output USB board equipped with a Field-Programmable Gate Arrays (FPGA) for scan processing. When connected to a *burn-in adapter-card*, it can control up to 4 FE providing LV regulation and serial testing. A schematic view of the testing setup used for module QA is shown in Figure 5.5.

• The STcontrol software manages the configuration and the test of the modules. The configuration parameter of the modules can be set by the user via a GUI, and the selected scan or list of tests to be run in sequence. All digital functionalities are implemented directly on the USBpix FPGA (see next paragraph) in order to reduce communications with the PC and so, the processing time. Parallel testing of multiple modules was not implemented on the production software release and therefore modules were tested sequentially. A double USBpix setup (two clock synchronous USB-pix boards) was used to test DC modules.
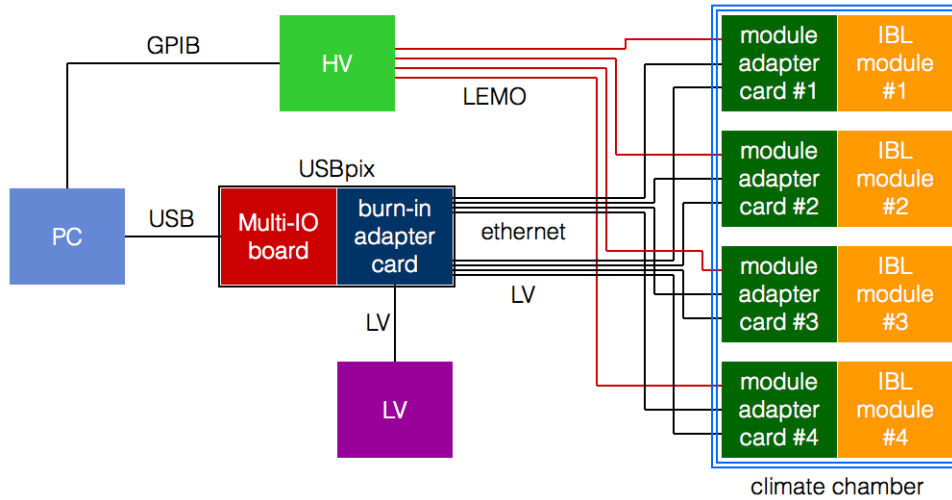
**Figure 5.5 –** Schematic representation of the USBpix setup.

Modules were powered with a single LV power supply and the burn-in card LV-regulators. Controlled via the the USBpix and its control software, they could be powered automatically during the testing and automatically switched off. Data between the FE-I4s and the USBpix was transmitted via an LVDS connection over an Ethernet cable[2]. Due to the large number of modules tested, adapter-cards were installed on a aluminium frame inside the climate chamber, providing HV, LV and data. Via a flexible pig-tail on the adapter-card, the connection and disconnection of the modules was simplified while guaranteeing a good thermal contact and cooling (Figure 5.6).

Reception Test Results

Although received modules were all qualified at the production site, their functionality was thoroughly checked on their reception using a standard list of scans before loading. Digital, Analog, Threshold (with and without HV), Noise, ToT and IV scans were performed. A total of 456 modules were tested for stave production. The distribution of modules used for loading, stave rework or spares, is shown in Figure 5.7. Modules showing any defect or discrepancy with the results obtained at production site were discarded or sent back for repair (and therefore not included in the plot).

In order to provide a reliable and consistent check on the module performance and the stave functionality (explained in the following section), an analysis framework was developed. Thanks to a centralised database, the results were automatically loaded and analysed, summarising the bad

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[2]It is important to note that the ethernet cable choice was made for hardware convenience. Modules communication with the USB-pix and later the ATLAS readout system, is performed via LVDS signals.
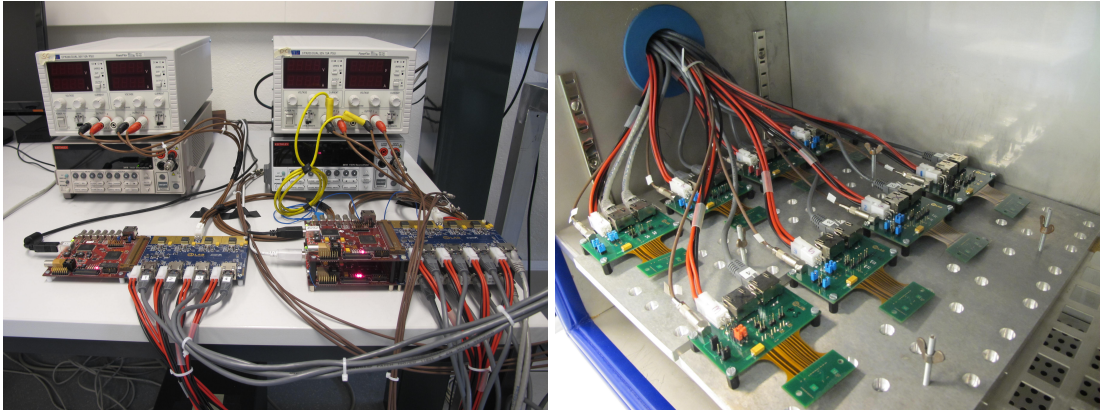
Figure 5.6 – Left: USBpix SC (left) and DC (right) readout systems and power supplies. Right: Module adapter-cards for DC (rear) and SC (front) installed inside the climate chamber. The flexible PCB part (orange) allows an easy connection and disconnection of the modules.
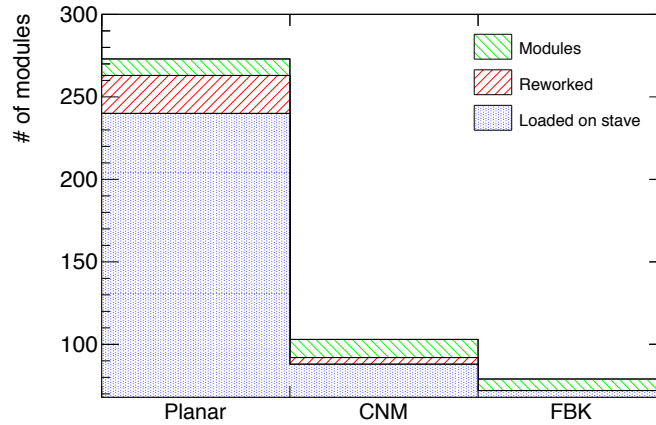

Figure 5.7 – Total number of modules tested (planar, 3D CNM and 3D FBK).

pixels per module or stave. Additionally, the software was largely used to compare the results at different stages of the stave production to find new failing pixels (before/after loading, before/after thermal cycle, etc). The results presented in the following were obtained with the mentioned software.

Figure 5.8 shows an example of the standard IV curves for each of the sensor technologies (left), as well as the distribution of the measured breakdown-voltage values during module production (right). All planar sensors showed a voltage breakdown larger than 120 V. For 3D, the sensors from the two producers presented different characteristics: the breakdown distribution of the FBK production had a mean value of 42.5 V, while the CNM sensors had a uniform distribution between 20 V and 105 V.

In particular, 14 CNM sensors presented a linear increase of current as a function of the increasing bias voltage (ohmic behaviour). Modules showing an ohmic depletion had similar performances and efficiencies, and so were considered for loading. Measured HV break downs were compatible with the production sites. Few modules showed a lower voltage break down with respect to production site and were discarded.
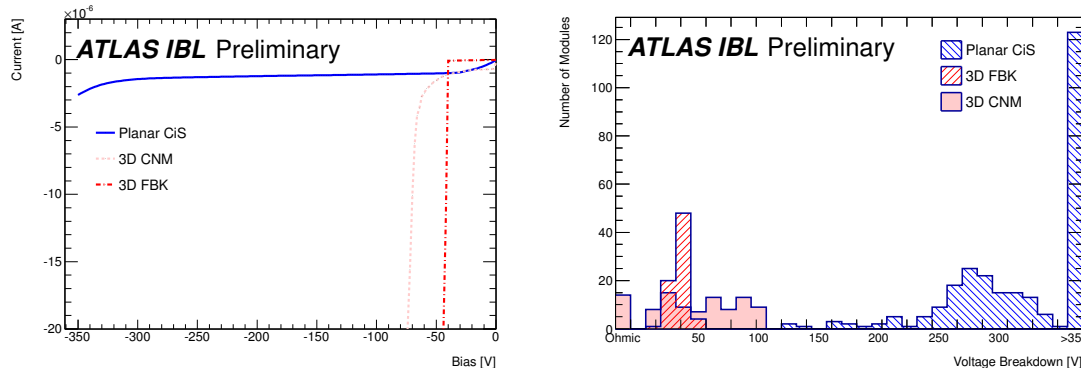
Figure 5.8 – Standard IV curves of the modules (left). Distribution of measured breakdown values for the three types of silicon sensors (right).

During production it was found that, due to a low reset capacitance loaded on the module flex, some modules could not be configured properly thus showing communication problems. The nominal reset capacitance was increased and defective modules reworked. Whenever a problem in communication between the USBPix readout system and the module persisted, further checks were performed with an alternative readout system, the Reconfigurable Cluster Element (RCE). If the communication problem was confirmed, the module was disqualified and sent back to production sites. During production, less than 10 modules were rejected due to communication issues with the front-end electronics.

As mentioned, due to the limited production time and late the availability of modules, the stave loading was performed in parallel to the module production, and thus before a ranking of all modules could be available. The selection and positioning of the 12 planar and the 8 3D sensor modules loaded on each stave was based on the following criteria:

- *Module Bad pixels:* based on the average module bad pixels during early production, the expected module yield and quality was estimated. Therefore, modules with a satisfactory ranking based on the number of bad pixels were loaded on the staves. The best available modules were loaded in the stave centre, while modules with a lower ranking were loaded at higher η. This choice was motivated to keep the highest tracking performances in the central region for the search of new physics at high p_T. In order to avoid the loading of too many bad modules in a single stave, the modules ranking was compared with the average production rates. The staves were therefore loaded, once a significant module-production quality was reached.

- *High voltage break-down:* due to the HV sector granularity (were up to 4 modules are depleted in parallel), modules with similar breakdown performance were grouped. Moreover, FBK and CNM 3D modules were not mixed in the same HV group.
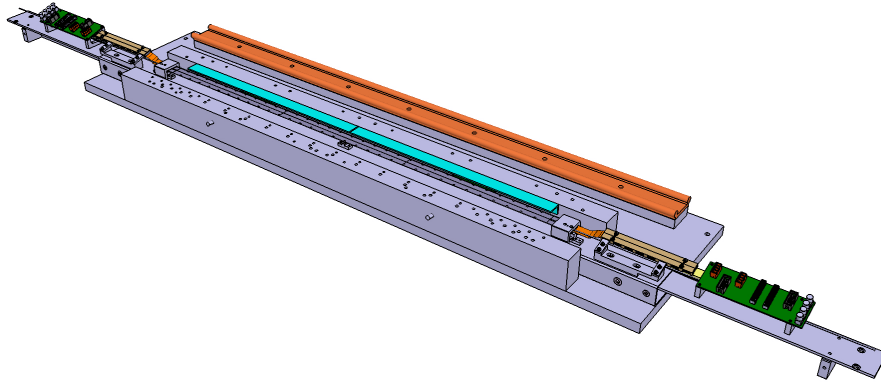
5.2 Stave Loading

5.2.1 Module Loading Procedure

Once the stave layout was defined, an approval request was sent within the IBL production institutes. Upon validation, modules were prepared for loading. The pigtail and temporary connector

of both DC and SC modules were removed. A guillotine was developed in order to hold the modules while precisely cut at the cutting line, placed only ~1 mm away from the sensor edge. Additionally SC modules, all produced with a default geographical address of 7, were set to 6 or 7 accordingly, thus allowing to independently configure neighbouring FEs sharing the same command line.

In order to proceed with the module loading, the stave and its handing frame were aligned with respect to the loading tool (Figure 5.9). This step was particularly important since the module positioning (defined by the loading tool) had no reference with respect to the face-plate other than the mentioned alignment. A shift or deviation of the stave with respect to the nominal position would lead to a global shift of the "module matrix" on the stave face-plate. A fine adjustment in the positioning of the stave handling frame with respect to the loading tool was performed by to a metrology measurement with sub-micron resolution, precisely aligning the stave face-plate edge to the loading tool reference points. At the same time, a loading tool was designed to protect both the stave supporting structure and the stave-flex during loading.


Figure 5.9 – 3D model of a stave and its handling frame positioned on the loading tool. The stave-flex wings protector is represented in blue.

The loading was done sequentially on each stave side. This side-to-side loading was motivated to keep the centre of the stave as a reference point for the stave loading. Due to the stack process used for the module positioning (see below), no other feasible alternative was found to keep the reference point at the stave centre.

After the stave alignment, a 70 µm-thick stainless steel mask was positioned on the stave face-plate for the deposition of the thermal grease [78] (Figure 5.10(a)). In order to avoid any movement of the mask during the grease application and to guarantee sharp edges on the mask openings (for the glue points supporting the modules), the stainless steel shim was previously sprayed with a universal adhesive for large surface bonding and temporarily glued to the face-plate. A 70 µm-thick layer of thermal grease was applied in order to guarantee a good thermal contact between the face-plate and the modules. When the mask was removed a clean pattern of thermal grease was revealed (Figure 5.10(b)).

A positioning jig with plastic stoppers was installed to constrain the modules to be loaded on the x-axis all along the stave and on the y-axis for the central module (Figure 5.10(c)). Two glue drops (Araldite 2011[79]) were applied per front-end chip with a needle on the thermal grease template openings for module fixation.
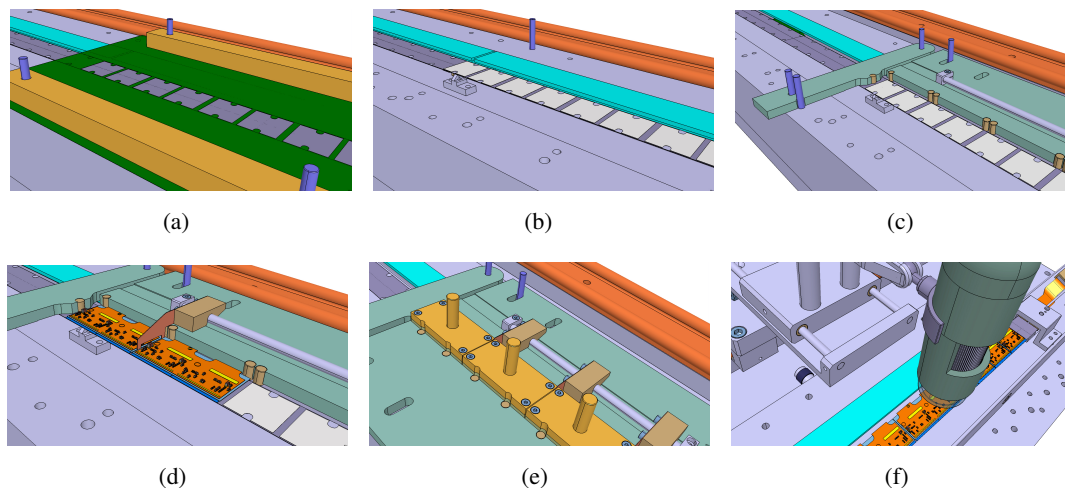
Figure 5.10 – Representation of each of the main stave module loading steps (see text for details) from the 3D CAD.

The module loading was then performed in a stack, as described in the following paragraph. The first module was pushed against the central stoppers, and a 205 μm thick spacer was placed between neighbouring modules (Figure 5.10(d)). This spacer sets the module-to-module distance and avoids any tilt angle due to any modules cutting edge defects. Once all modules placed along half a stave, a final positioning tool allowed to compress the modules in both directions, guaranteeing the stave envelope.

Weights of 20 g per FE were placed on top of the modules[3], during the glue curing process (24 hours at room temperature), guaranteeing a proper contact between the module, the grease layer and the glue dots (Figure 5.10(e)). After curing, the loading tools of the loaded side were removed and an optical inspection was performed for each FE by means of a built-in sliding camera (Figure 5.10(f)).

The same process was repeated for the other stave half.

5.2.2   Stave-flex Wing Gluing and Wire Bonding

The stave-flex wings (see section 4.2.5) were glued to the modules after stave loading. The following section describes the steps of the process.

In order to glue the stave-wings on top of the module flex (kapton-to-kapton gluing) a thin layer of Araldite 2011 was used. This was applied very closely to the module final wire bonding pads as any glue excess or contamination could affect the wire-bonding quality. In order to control at best the glue deposition, the stave was placed under a mask with an opening at each stave-wing position. Glue was applied with a stamp, depositing a consistent glue layer at the correct location to avoid any glue excess on the bond-pads. The stave wings were kept on the stave back with the use of individual holders allowing easy access to the modules flex.

The final curing was then performed with a wing positioning tool, defining the wing gluing position as well as the wing angle and height. This tool locks the stave in its final position by means of a wedge which pushes against the carbon laminate, forcing the wings to their nominal position by using two clamps. The glue was left to cure during 24 hours while a weight of 16 g

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[3]In order to prevent any damage to the module the weight were equipped with three Teflon feets, leaving space for the wire-bonds and the loaded SMD components

was positioned on top of the wings. In order to avoid any gluing or damage to the module nor to the wing pads, the weight contact surface was covered with Teflon. An overview of the process is shown in Figure 5.11.
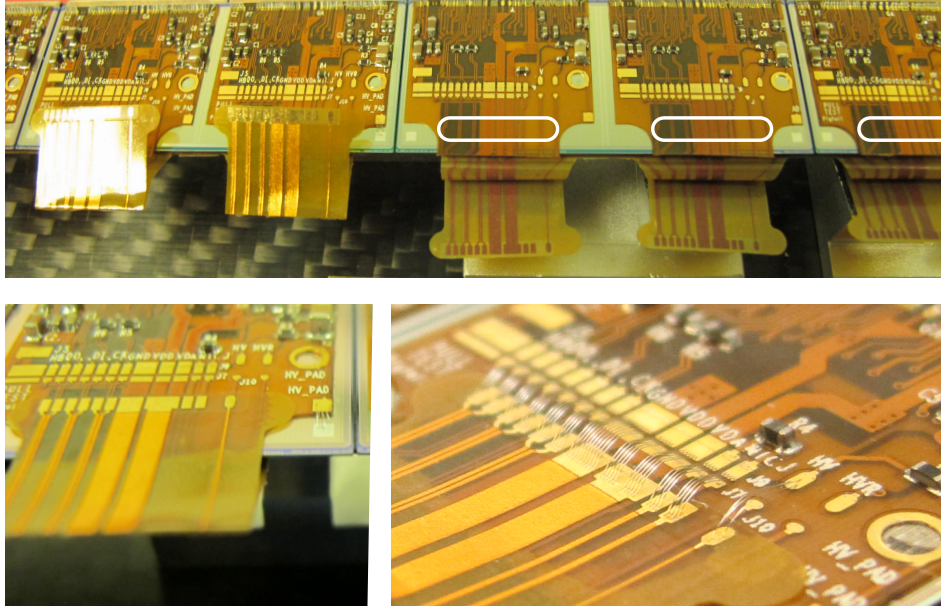

Figure 5.11 – Stave-flex wings before gluing (top). For comparison, few stave wings were kept with the individual wing holders. The glue mask position is shown in white. Bottom left: wing glued to the module. Bottom right: final wire-bonded module showing the distance between the stave flex and the end of wing.

In order to prevent possible breakdowns between sectors, a thin Kapton insulator of $\sim100\,\mu$m-thickness was inserted in between each powering sector. This was motivated particularly by the possible HV difference between the planar and 3D after irradiation, where up to 1000 V difference could be applied with only $\sim200\,\mu$m gap. Additionally, in order to avoid getting any glue between powering sectors and to protect the wire-bonding envelope, a "bridge-holder" was glued to the module-flexes. As a last step, the stave envelope was checked to verify the fulfilment of the mechanical constraints of the IBL.

Finally, the electrical connection between the stave-flex and the modules was performed via wire-bonding, connecting the HV, clock, command and data lines via $25\,\mu$m AlSi(1%) wire-bonds. For redundancy reasons and because of the wire-bonding angles with respect to the ATLAS magnetic field, four wire-bonds were performed for each Low Voltage Differential Signal (LVDS) and HV pad. Due to the larger current of the LV and ground lines, ten wire-bonds were performed to cope with the expected 0.5 A current per FE.

For a proper wire-bonding and to ensure a correct wire-foot deformation, a reinforcement needed to be applied to avoid any deflection of the stave from the wire-bonding pressure. A shim block was placed under the wire-bonded FE increasing the stave stiffness (Figure 5.12). The bond-loop height was limited to a maximum value of $250\,\mu$m. Wire-bond quality was tested by pull tests, performed every 2 FE on empty pads. The results of the pull tests are reported in Table 5.3.
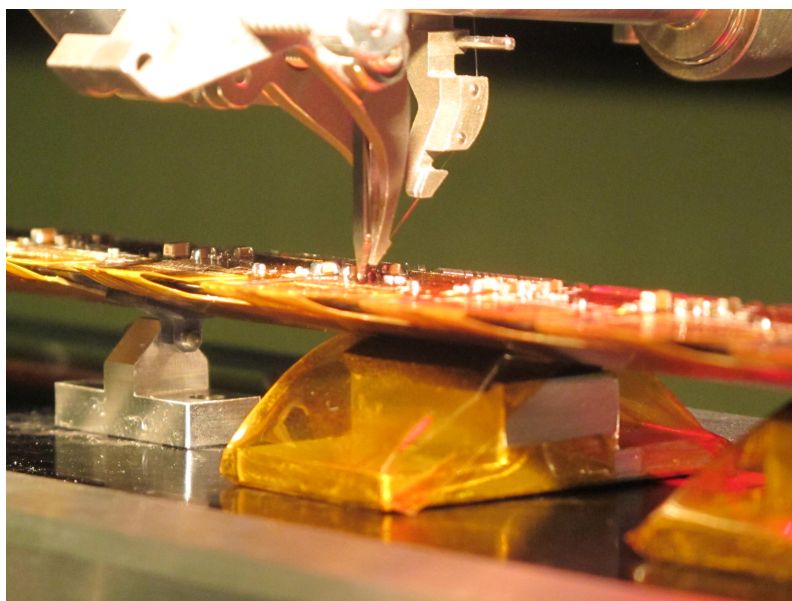
Figure 5.12 – Stave-flex wings under wire-bonding showing the wire-bonding head and the shims placed under the stave to increase its mechanical stability.

Dedicated studies were performed on the behaviour of the IBL wire bonds under the magnetic field. IBL wire bonds connecting the flex to the FE-I4 are tilted with respect to the B-field at orientation angles between $50°$ and $90°$. Due to the different nature of the powering and LVDS signals, two case scenarios were studied:

- *Bending of the powering wire-bonds during the FE turning ON/OFF.* Particular attention was given to these wire-bonds since they are the longest wires on the module. Although the multiple wire bonds were connected in parallel to split the current, because of their low resistance the current distribution among them is not well defined. The worst case scenario would be if all current passes through only one of the three wires and therefore was studied. As presented in [80], it was proven that although the powering of the FE under the magnetic field will cause wire-bonds fatigue, this effect does not represent a risk for the expected life-spam of the FEs.

- *Resonance of the LVDS and powering lines due to the digital activity driven by the trigger ratio.* The maximum AC current of digital wire bonds was found to be about 100 mA with a non-ideal square wave shape. A perfect square wave shape with 100 mA amplitude was studied and considered as the worst case scenario. During this study, it was proven that operating the IBL with a trigger frequency of 9800 Hz, the resonance frequency of the FE wire-bonds, will irreparably damage the wire-bonds after a small number of oscillations and could quite easily break them at the foot level. In order to prevent this, a safety in the ATLAS trigger was added to avoiding the IBL resonance frequency during calibration and data taking.

	stave 1	stave 2	stave 3	stave 4	stave 5
Mean pull force [g_F]	6.23 ± 0.78	5.70 ± 0.59	6.13 ± 0.63	5.75 ± 0.62	5.94 ± 0.43

	stave 6	stave 7	stave 8	stave 9	stave 10
Mean pull force [g_F]	6.22 ± 0.74	6.30 ± 0.64	6.23 ± 0.51	5.85 ± 0.53	6.09 ± 0.58

	stave 11	stave 12	stave 13	stave 14	stave 15
Mean pull force [g_F]	6.19 ± 0.56	6.00 ± 0.69	7.20 ± 0.29	7.26 ± 0.33	6.80 ± 0.50

	stave16	stave 17	stave 18	stave 19	stave 20
Mean pull force [g_F]	-	7.11 ± 0.41	7.03 ± 0.42	6.32 ± 0.66	5.85 ± 0.76

Table 5.3 – Mean and RMS values of the wire-bond pull-tests performed on the 20 staves produced. Values for stave 16 were accidentally lost.

5.2.3 Module Replacement

Due to the manipulation of the IBL modules and the applied mechanical stress during the loading, a few sensors and FEs presented non-repairable defects after loading, such as broken corners or defective FE functionalities. Therefore, in order to guarantee a fully functional detector and because of the limited available staves, a module rework procedure was developed.

In order to replace a defective module without damaging the neighbouring ones, two 100 μm-thick Kapton spacers were positioned to protect the edge of the adjacent modules as well as the wire-bonds (Figure 5.13(a)). The defective module was then removed by inserting a plastic spatula in between the module and the face-plate, breaking the glue drop bonds (Figure 5.13(b)). The face-plate was then cleaned to remove any excess of thermal grease or glue. A new thermal grease layer and glue dots were applied and the new module was then placed with the aid of a dedicated positioning tool (Figure 5.13(c)).

After the module placement, the wing gluing, the optical inspection, the envelope check and the HV insulator insertion were performed following the same procedure as for the standard loading.

(a)   (b)   (c)
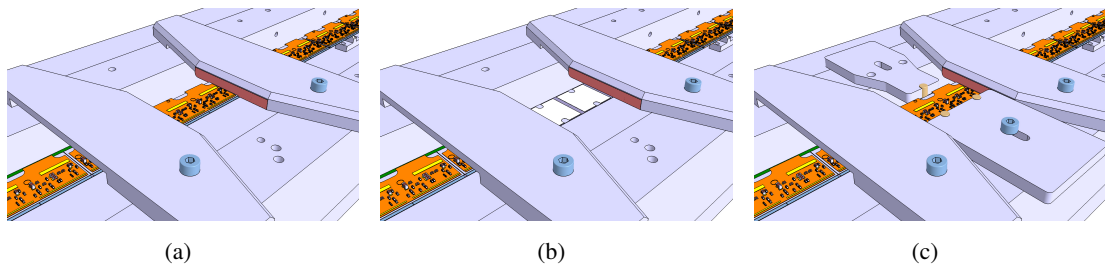
Figure 5.13 – Representation of each of the main module replacement steps from the 3D CAD.

During the IBL production, 28 modules needed to be reworked. A breakdown of the reasons for the IBL repairs is shown in Figure 5.14. Most of reworks were due to modules accidentally damaged during the module loading. It is important to mention that up to 6 modules needed to be replaced after a re-work of a module in the stave. This high yield of double repairs, may be explained by the non-standard reworking procedure and the exposure of modules. During the IBL production, a corrosion at the wire-bond level was observed, induced by the eventual condensation
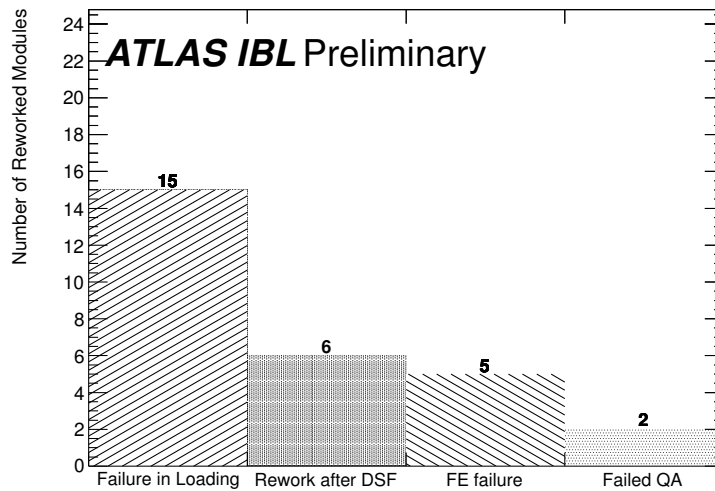
Figure 5.14 – Number of modules reworked for each of the category. Reworks were mainly motivated by accidents during the loading or modules re-bonds and FE failures during the early testing. A minority were replaced after the stave QA due to some failing registers.

during the staves thermal cycling. In order to correct for it, all produced staves were cleaned and re-bonded at the CERN Detector-Silicon-Facility, where six modules needed to be replaced out of the twelve re-bonded staves. After the corrosion observation the staves thermal-cycling after loading was not any longer performed in the climate chamber, but directly performed via the stave CO_2 cooling during testing.

5.3 Stave Quality Check

5.3.1 Metrology Survey

After each stave was fully dressed, the positioning of the modules in the x, y and z-axis were checked in the stave coordinates system. The x and y module positions were measured via an image reconstruction of the sensor fiducial marks. The z coordinates of the modules were obtained by probing the sensor surfaces at their four corners (Figure 5.15), to provide the position and plane orientation.

The loaded staves were thermally cycled following the same procedure as for the bare-staves (Section 5.1.1), i.e. ten times from $-40\,°C$ to $40\,°C$[4]. Additionally, metrology measurements were performed on the first stave before and after thermal-cycling to check the module positions. Results of the fiducial mark position obtained before and after the thermal cycle for stave 1 are summarised in Figure 5.16, showing no module displacement. Due to mechanical damage, a module was replaced between the two metrology measurements, represented independently in Figure 5.16. As can be observed, the positioning resolution of the re-worked module was significantly lower due to the manual interventions needed. The position of the modules on following staves were measured only before thermal-cycling to simplify the loading.

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[4]As already mentioned, the stave thermal-cycling after loading in the climate chamber was stopped after the corrosion issue (i.e. stave 12).
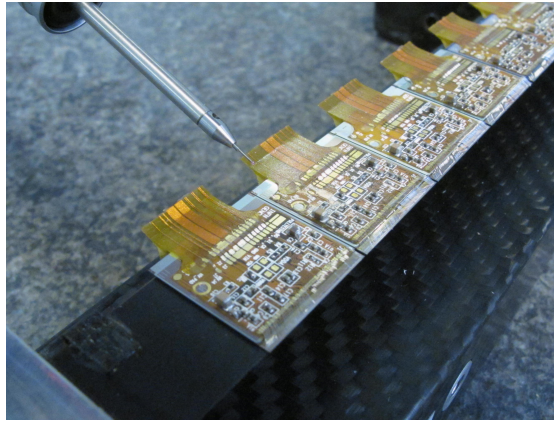
**Figure 5.15** – Stave metrology after loading. The picture shows the probing of a 3D module.
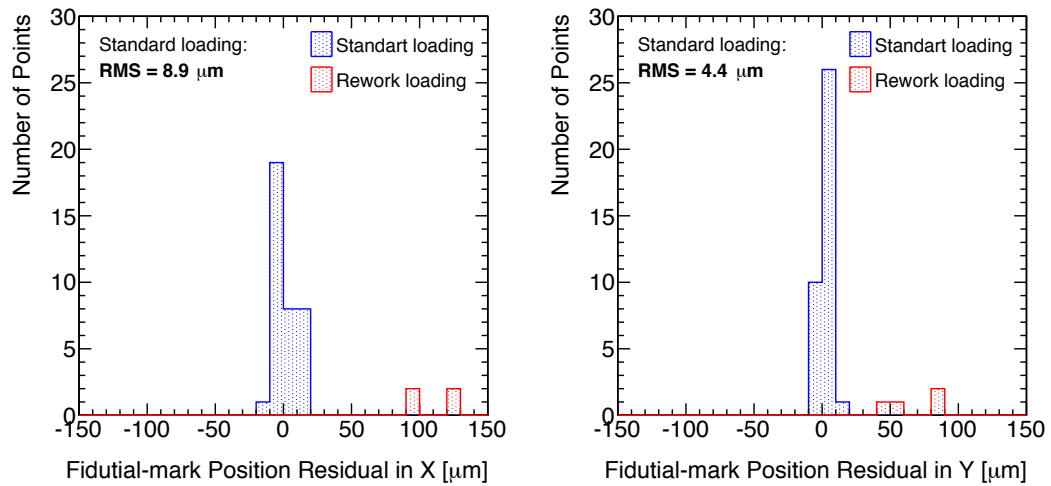
Figure 5.16 – Fiducial-marks position difference before and after thermal-cycling in the x (left) and y-axis (right).

The measured z-axis profiles at both staves edges (ϕ^- and ϕ^+), are shown in Figure 5.17. As compared to the metrology before loading (Figure 5.3), the stave mean face-plate remained within the same range [-0.2 0.2 mm], while tilted modules extended the stave envelope to the maximal deviation represented by the filled area.

The module loading precision was estimated by comparing the measured position with respect to the nominal. Figure 5.18 shows the distributions of the module residuals on both the x and y-axis. As observed along the y-axis (along the stave), DC modules RMS is $\sim$50 µm compared to $\sim$57 µm for SC. This larger deviation for SC with respect to DC is to be expected because of the sequential loading procedure of the modules, where outer modules on the staves accumulate the misplacement of previously loaded modules. On the contrary, along the x-axis, the DC modules RMS ($\sim$50 µm) is larger than that of the SC ($\sim$34 µm), as expected from the larger size of DC for which any small angle within the stave plane will impact twice as much on the DC position with respect to the SC.
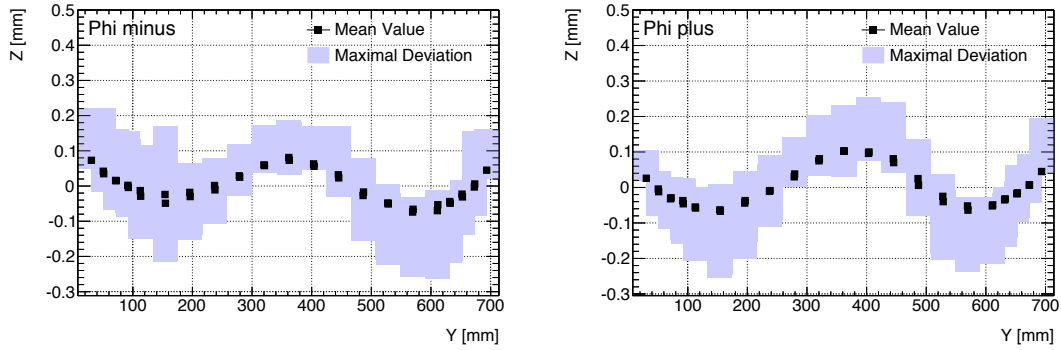
Figure 5.17 – Average module fiducial marks position on the z-axis for the 20 staves produced (black dots) along the two staves profiles: ϕ^- (left) and ϕ^+ (right). The profile having been measured on the modules, consecutive points can be discrepant due to the uncertainties of the module positioning. Maximum and minimum measured z values at each measurement point are represented by the filled area.
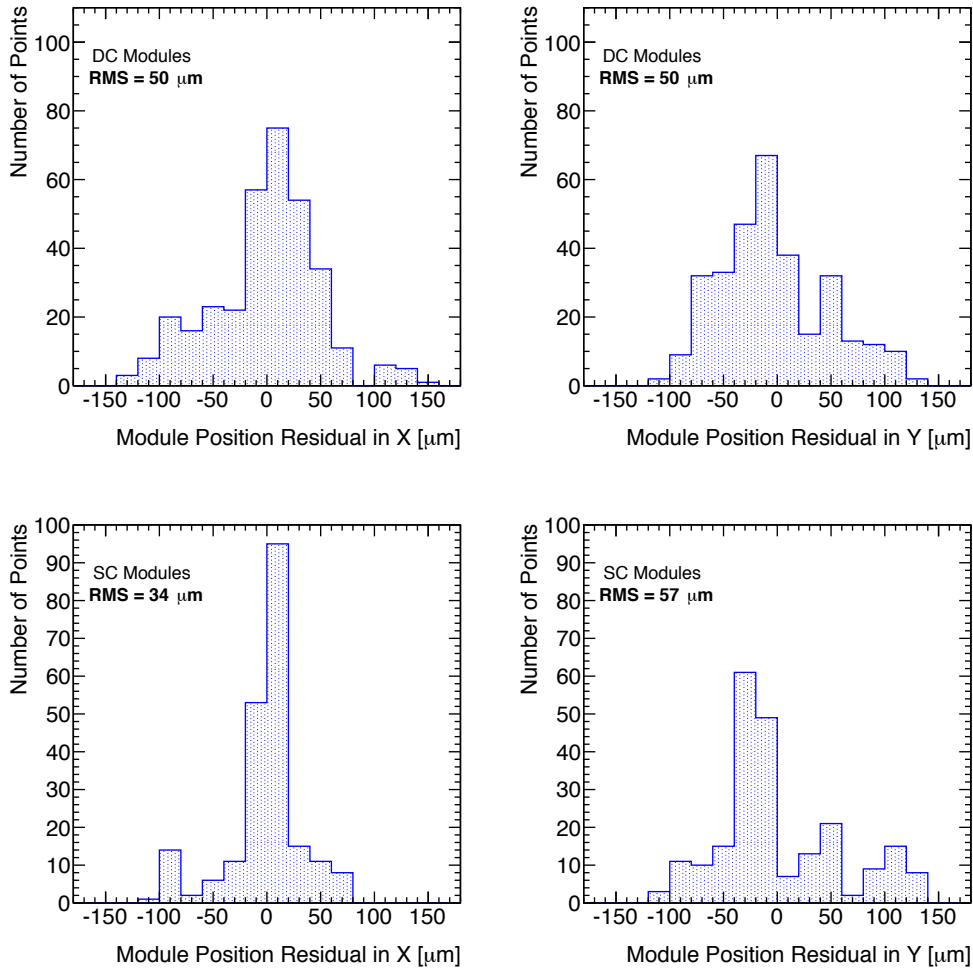

Figure 5.18 – Residual values of the DC (top) and SC (bottom) modules fiducial marks with respect to their nominal position in x and y-axis (along the stave axis).

5.3.2   Electrical and Functional Quality Checks

After loading and before shipment to CERN for a final calibration and qualification, the IBL staves were tested at the University of Geneva to verify their functionality before transportation. A full electrical test consisting of a Digital, Analog, Threshold, Noise and ToT scan (See section 4.2.1) was performed systematically with a dedicated stave QA stand, which will be discussed in the following section.

Stave QA Setup

The stave QA Setup aimed to test the loaded staves simulating the readout and environmental conditions as of ATLAS. Due to the average production rate of one stave per week and the average four testing days required for the QA, a single stave testing setup was developed. The stave testing setup is shown in Figure 5.19.
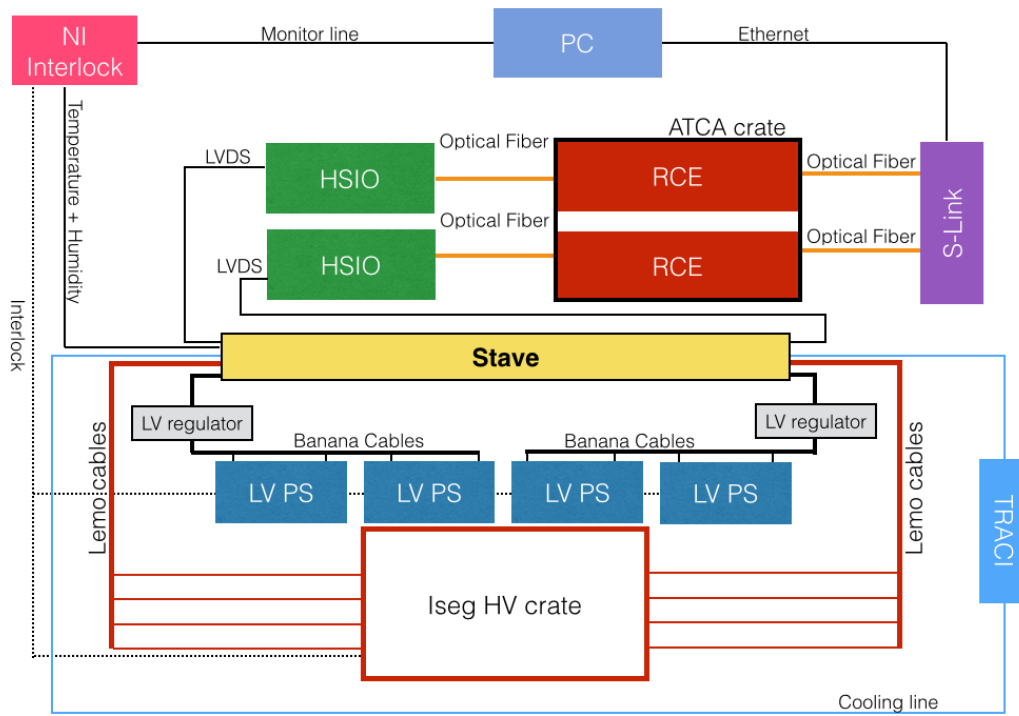
Figure 5.19 – Sketch of the stave testing setup.

Although staves were tested at $15\,^{\circ}\mathrm{C}$, a CO_2 system was used for the stave cooling, avoiding any possible contamination on the cooling pipes that could affect the subsequent stave brazing or the contamination of the final CO_2 cooling system. A CO_2 double phase TRACI (Transportable Refrigeration Apparatus for CO_2 Investigation), developed by NIKHEF [81], with an operation range between $-35\,^{\circ}\mathrm{C}$ and $20\,^{\circ}\mathrm{C}$ and a maximum cooling power of about $250\,\mathrm{W}$ was used. Thanks to temporary fittings, the IBL staves were connected to the cooling system where, before CO_2 circulation, a vacuum in the cooling pipe was created to avoid its contamination.

To control the environmental conditions, a box was designed in order to test a single stave, guaranteeing good hermiticity and dark environment. A custom DCS was developed for the monitoring of temperature and humidity. The DCS was based on two National Instrument (NI) NI6009 ADCs with a total of sixteen analog input channels (14 bits each), instrumented with humidity and temperature sensors and readout with custom NI LabView software. Four humidity and temperature sensors were installed inside the testing box for environmental monitoring. Additionally, eight of the stave modules NTCs were read out on the second NI ADC, including a custom hardware interlock, designed to prevent the modules reaching temperatures above $40\,°C$ by interrupting the Low Voltage and High Voltage power.

The LV for the FE operation was provided by four independent power supplies with 2 channels each. A single channel was therefore used for each of the eight LV sectors, reducing the noise and avoiding ground-loops that could be introduced by a parallel powering. Additionally, in order to prevent an over-voltage of the FE regulators, an intermediate LV regulation was implemented with a voltage output range within the FE operation voltages (1.7-2.4 V). For the sensor depletion, an eight channel HV ISEG card with a maximum output voltage of -1000 V was used. Controlled via a LabView program and a CAN bus, voltage values and maximum currents could be set and monitored independently for each channel. Additionally, as described in [82], the voltage ramp speed, IV curves and several other HV power supply functionalities were available.

The Reconfigurable Cluster Element (RCE) developed by SLAC was adopted as a readout system during the quality assurance. The RCE boards, thanks to their computational power, allowed an on-board test analysis and scan operation. The intermediate High Speed Input/Output (HSIO) boards, multiplexing the 40 MHz LVDS FE signals to the RCE via optical fibre at 3.125 Gb/s, allowed the reading of up to 8 FE chips in parallel. In order to adapt the RCE readout system to the IBL specifications, two RCEs were integrated per Cluster Interconnect Module (CIM) board, allowing a full stave (32 FEs) readout via two RCE-boards. The final stave readout was therefore composed of two RCE-boards loaded on an Advanced Telecommunications Computing Architecture (ATCA) crate (for powering and communication with the control PC), and two HSIO.

The QA tests and results

All produced staves were tested and tuned before shipment for final qualification. Even though a final ranking was performed after stave qualification at CERN, a preliminary stave ranking was performed to assed the impact of the loading on the modules. Once a stave was fully tested, an automatic analysis was performed, providing quick information of the stave pixels that failed the selection criteria (Table 5.4). As an example, the failing pixels of an IBL stave are shown in Figure 5.20.
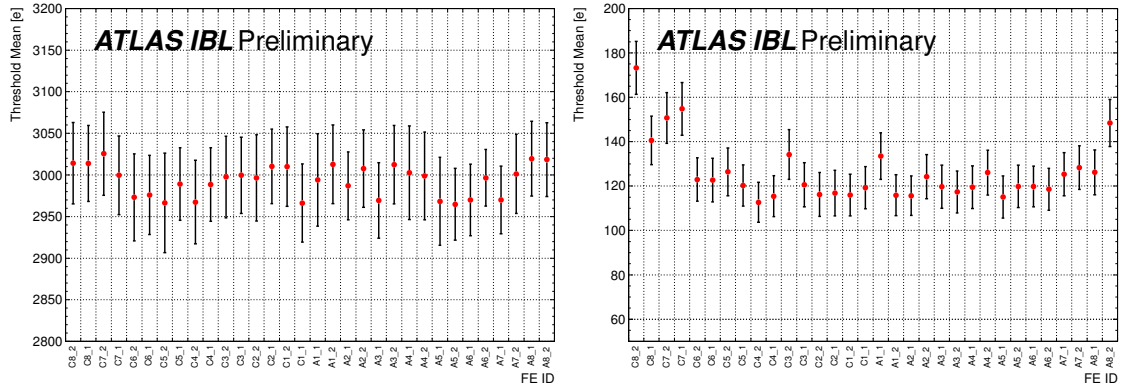
Scan Type	Criteria
Digital Scan	Occupancy < 98% or > 102% of injections
Analog Scan	Occupancy < 98% or > 102% of injections
Threshold Scan	s-curve fit failed
Noise Scan	Occupancy > 10^6 hits per BC

Table 5.4 – Bad pixels criteria per category and test.
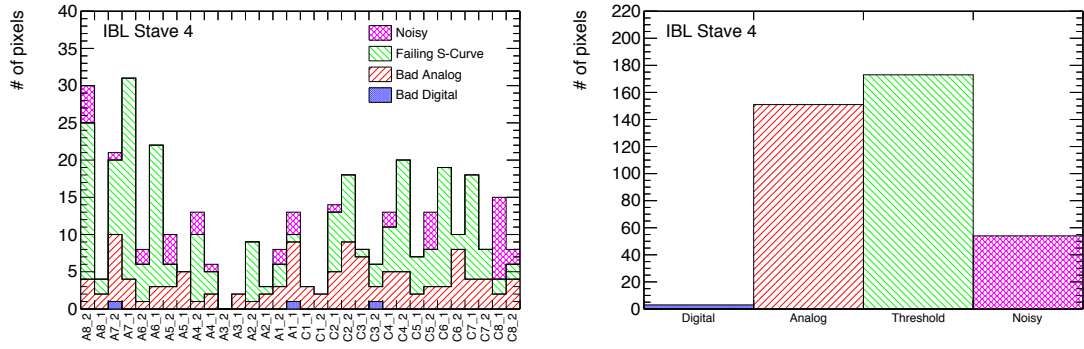
Figure 5.20 – Failing pixels of an IBL stave after the QA test and analysis beak-down per module (left) and total (right) for stave 2.


Figure 5.21 – Tuning performance of stave 2. Threshold distribution for 3000 e$^-$ target tuning (left), and noise distribution for 3000 e$^-$ target tuning (right). The vertical bars represent the RMS of the distributions.

In order to distinguish between the signal from charged particles and the electronic noise, the discriminator threshold and the ToT parameters of the FE-I4 needed to be calibrated and tuned during operation. The threshold uniformity within the FEs and the staves is of critical importance to determine the amount of charge deposited in all IBL pixels. Staves were tuned to a threshold value of 3000 e^- and 8 ToT at 20 ke^- injection. Figure 5.21 shows the FE threshold and noise mean values measured for stave 2 after tuning. For this stave, a threshold mean value of 2980 e^- and 50 e^- RMS was obtained. Modules showing a threshold RMS higher than 80 e^- were retuned. No further procedure was considered since after a second tuning all modules were within QA specifications.

The pixel response to the injected charge and its ToT value were checked throughout a ToT scan with an injected charge of 16 ke^- expecting a ToT of 6.4 bunch crossing. As an example, the results for stave 2 are shown in Figure 5.22, being compatible with the expected ToT of 6.4.

After a final optical inspection, staves were shipped to CERN for qualification and calibration.
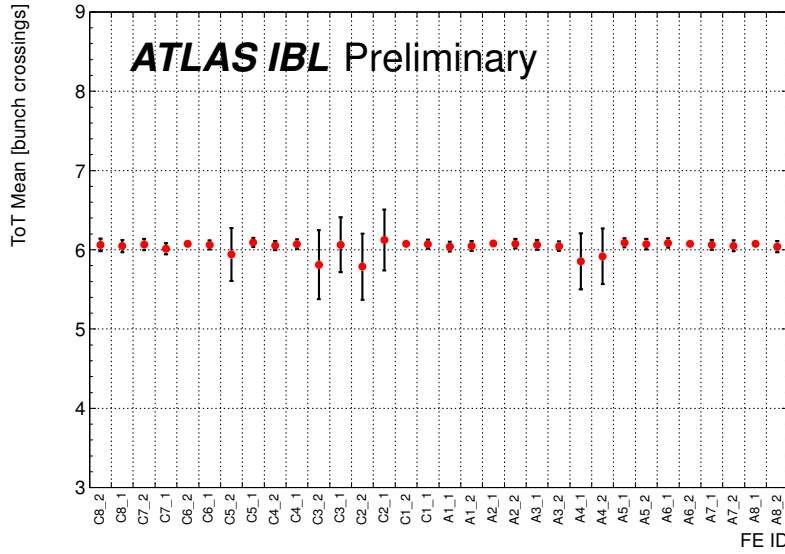
Figure 5.22 – ToT distribution obtained for a 16 ke^- injected signal and a 8 ToT target tuning for 20000 e$^-$ injected on stave 2 S.

### 5.3.3   Stave Calibration, Qualification and Ranking

Due to the extended tests performed at CERN to fully calibrate and characterise the staves, it was necessary to test two staves simultaneously. A similar setup as described above was used. While the readout system was kept unchanged, the adopted powering and DCS systems were chosen to mimic the real operation as close as possible. Additionally, for final characterisation with real particles, a ^{90}Sr source was installed on a linear stage allowing to irradiate the full stave length. Although twenty staves were delivered, the results presented here cover only eighteen of them. Indeed two staves had to be excluded from the analysis due to an accident during the tests.

After reception, an optical inspection was performed checking for defects and eventual impurities in the wire-bonds that could cause shorts (i.e. loose or deformed wire-bonds, debris, etc). IV measurements were performed on each of the HV sectors afterwards and before testing. The results were compared to those obtained during the production QA, where consistent results for all tested sectors were found. All measured IV are shown in Figure 5.23.

In order to guarantee proper operation over the lifetime of the IBL, a regular FE calibration to compensate for radiation effects in the silicon sensor (affecting the signal strength and noise) will be performed. Therefore, the IBL staves were tuned with a threshold discriminator values of 3000 e^- and 1500 e^- and 10 BC ToT for an injected charge of 16000 e^-, checking the detector operation at low thresholds required after irradiation. Due to the thermal noise[5] contribution from the sensor, the 1500 e^- threshold tuning was performed at $-12\,^\circ$C, while the temperature was kept at 20 $^\circ$C during testing with a 3000 e^- threshold.

The threshold and noise distribution obtained for 3000 e^- and 1500 e^- are shown in Figure 5.24. As explained in Section 4.2.2, the long planar pixels are shown separately due to their increased capacitance. Due to the large threshold operating range of the FE-I4, and the low noise electronics, no significant difference was observed between the two tunings (standard planar pixels

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[5]The thermal noise is the electronic noise generated by the thermal agitation of the charge carriers (electrons) inside the valence band.
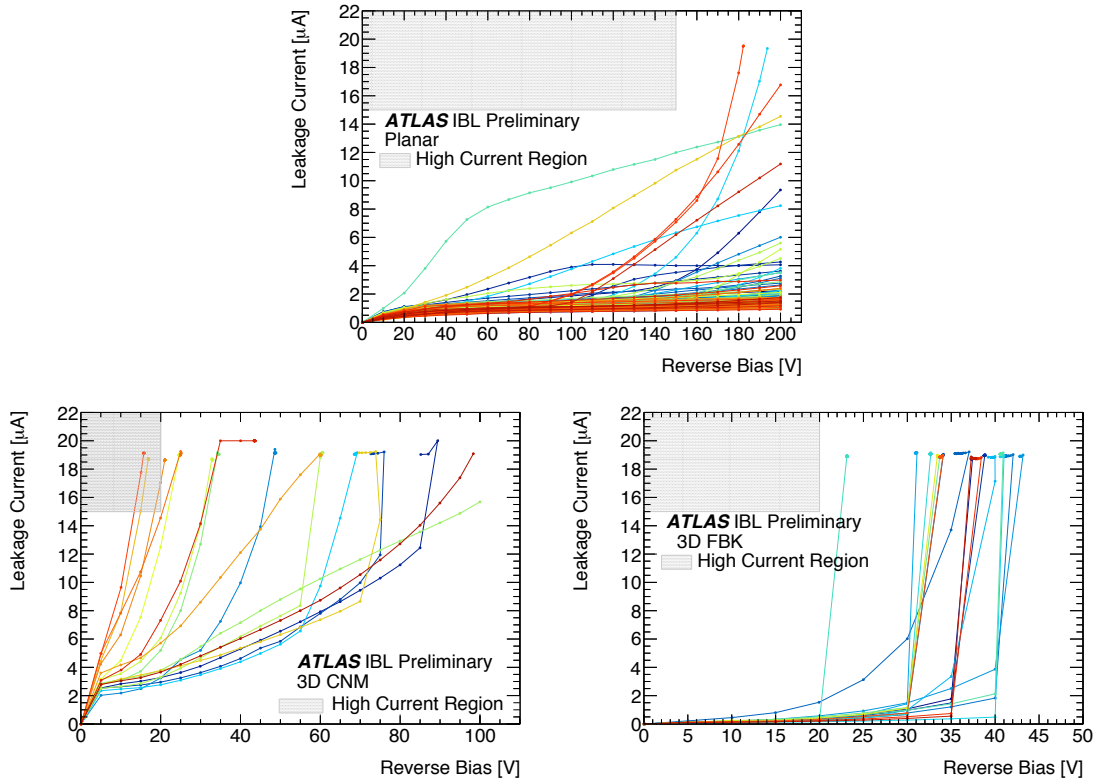
Figure 5.23 – IV curves of all tested sectors and sensor technologies: planar (top), FBK (bottom-left) and CNM (bottom-right). Sectors with a leakage current higher than 15 μA at low depletion voltages (< 20 V for 3D and < 150 V for planar) were considered as high current sectors (as indicated by a shaded area in the plots).

show an increase of 6 e^- noise increase between the 3000 e^- and 15000 e^-). As it can be observed in Figure 5.25, the threshold over noise at 1500 e^- and $-12\,°C$ was still of 10, allowing an automatic tuning of all FE-I4 pixels. Although lower thresholds such as 1000 e^- were achieved, due to the degradation of the Threshold over Noise performance, not all pixels could be tuned and noisy pixels did exceed the IBL low occupancy requirements. Threshold and noise mean values obtained for the 20 produced are summarised in Table 5.5.

The ToT mean values of the 20 produced staves for an injected signal of $16000e^-$ after tuning are shown in Figure 5.26. As expected from the tuning, all modules showed a mean ToT of 10 BC with a maximum deviation of 0.1 ToT. The pixel distribution ToT can be seen in Figure 5.27. Further more, the structure with peaks at integer values is on account of the integer ToT readout values. Obtained results during stave qualification were compatible with the results of the QA measurement performed before shipment.
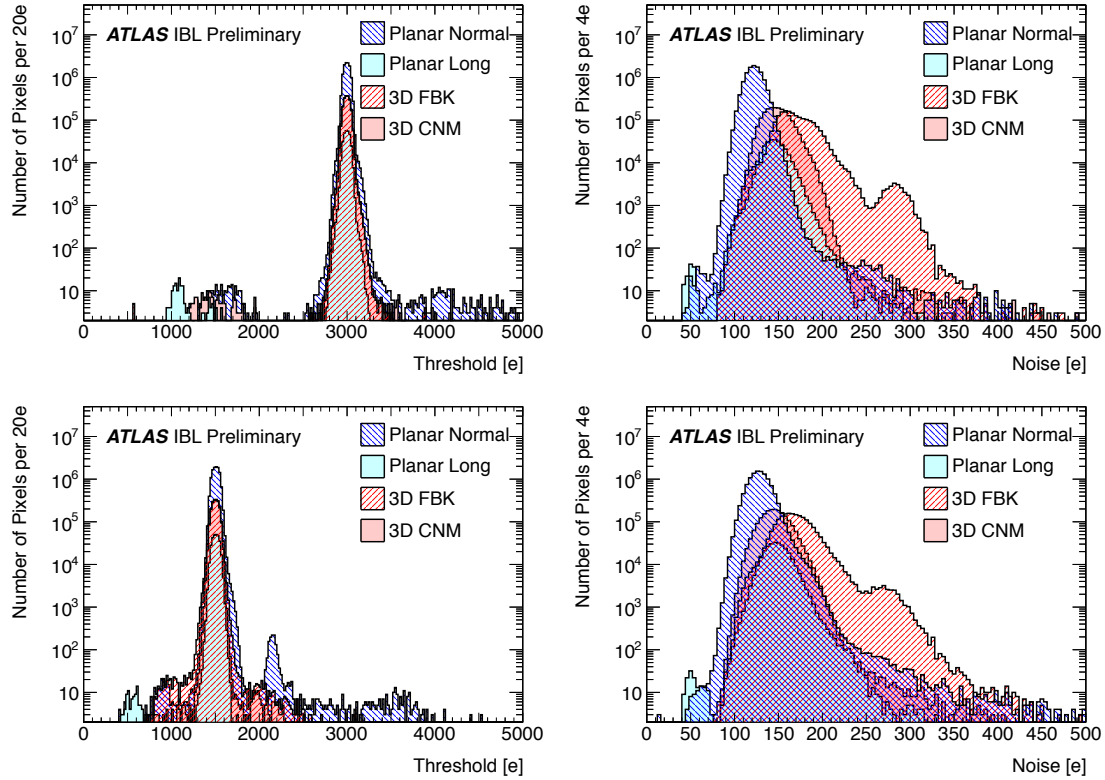
Figure 5.24 – Threshold and noise distributions after tuning to a threshold target of 3000 e^- at 20 °C (top) and 1500 e^- at −12 °C (bottom). The small peak around 2150 e^- on the planar normal pixels is an artefact of one mask step in the threshold scan, where noisy pixels bias the s-curve. By re-doing the threshold scan and injecting in less pixels per mask step, the incorrect measurement can be avoided, but for this particular chip it was not done due to time constraints. The bump around 300 e^- on the 3D FBK noise is caused by a small noise on the HV line of the setup and the sensitivity of FBK modules to such noise.
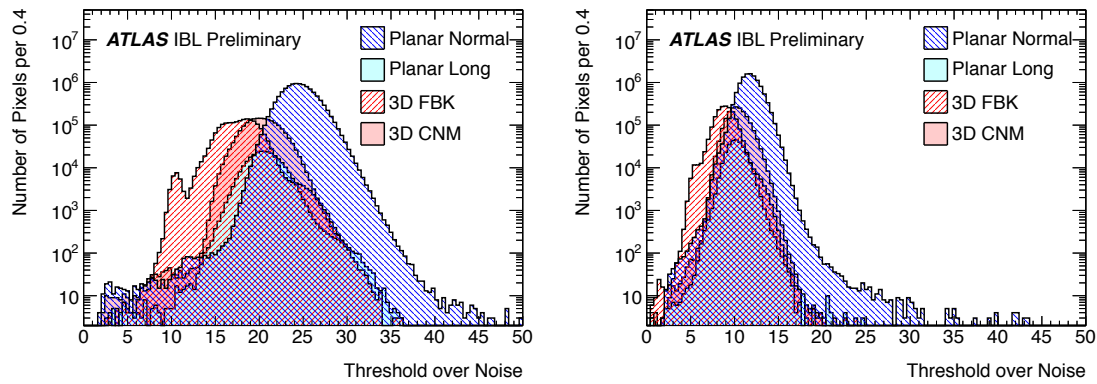

Figure 5.25 – Threshold over noise distribution of pixels for 3000 e^- (left) and 1500 e^- (right) threshold tunings at 22 °C and −12 °C module temperatures, respectively.

Tuned Threshold	Pixel Type	Std. Dev. [e^-]	Noise [e^-]	Threshold over Noise
3000e^- at 22 °C	Planar Normal	37	123±10	25±2
	Planar Long	58	146±15	21±2
	3D FBK	39	171±25	18±2
	3D CNM	40	149±9	20±2
1500e^- at −12 °C	Planar Normal	42	129±13	12±1
	Planar Long	47	149±16	10±1
	3D FBK	46	171±25	9±1
	3D CNM	41	146±16	10±1

Table 5.5 – Threshold calibration summary for different pixel types. Listed values are the standard deviation of the threshold, the mean noise and its standard deviation, and mean threshold over noise and its standard deviation.
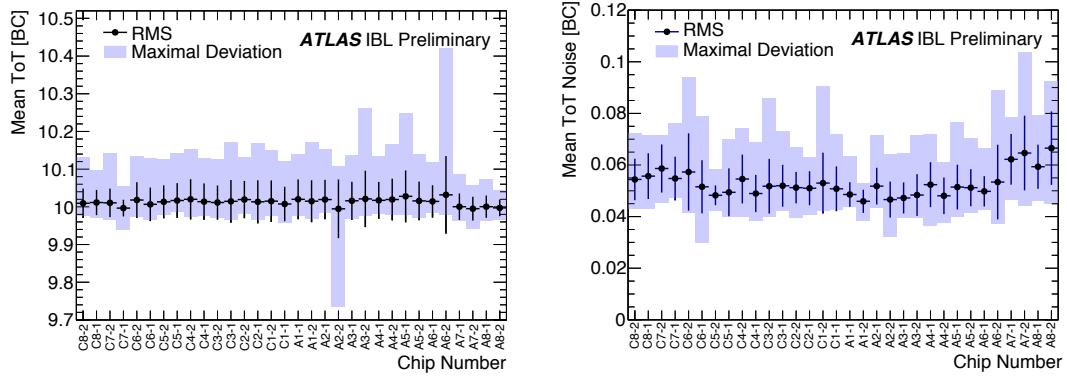

Figure 5.26 – Modules average (left) and noise ToT (right) distribution as a function of chip number. Noise ToT is defined as the RMS of the obtained ToT distribution after 50 injections.
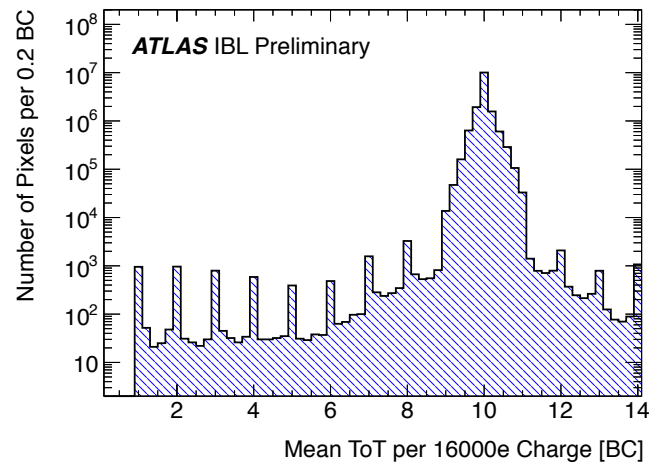
Figure 5.27 – Pixel mean ToT distribution.

Additionally, a source scan was performed with a 28.8 MBq ^{90}Sr, emitting 2.28 MeV electrons inducing a minimum ionising particle signal. By means of a linear motor, the source was swept along the stave to provide a uniform pixel occupancy. In order to easily spot any disconnected bumps, the source sweep speed was set so that ∼200 hits per pixels were obtained. An occupancy map and pixel occupancies for each sensor technology are shown in Figure 5.28. Dead and disconnected bumps could therefore be easily spotted by requiring a pixel occupancy lower than 1% of the FE mean. Further studies such as charge calibration using minimum ionising particles were also performed.
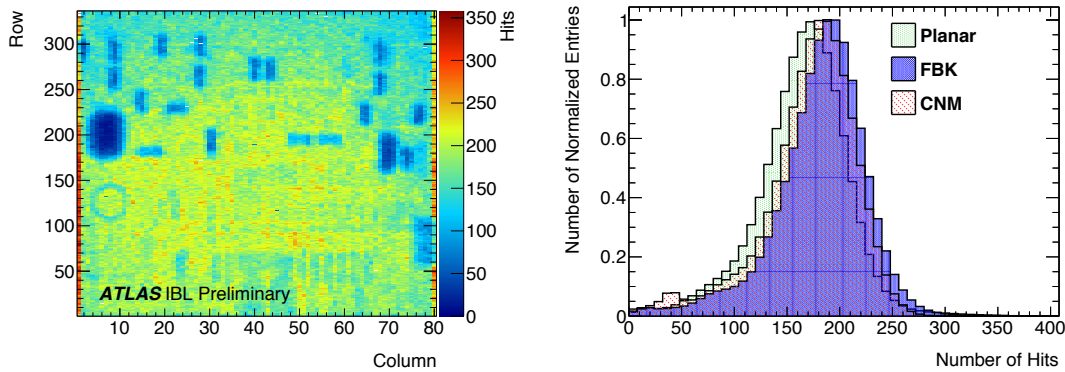
Figure 5.28 – Occupancy map (left) on a SC module and the occupancy for each pixel technology (right) after exposure to a ^{90}Sr source. The pattern on the hit occupancy map can be directly correlated to the SMD components and wire bonding pads on the module flex.

Pixel Defects

After the staves were fully tested and qualified, the results were analysed in order to determine the fraction of pixels that did not satisfy the IBL requirements. Pixel failures were categorised as detailed in Table 5.6.

Failure Name	Scan Type	Criteria
Digital Dead	Digital	Occupancy < 1% of injections
Digital Bad	Digital	Occupancy < 98% or > 102% of injections
Merged Bump	Analog	Occupancy < 98% or > 102% of injections
	Crosstalk	Occupancy > 80% of 25 ke^- injections
High Crosstalk	Crosstalk	Occupancy > 0 with 25 ke injection
Analog Dead	Analog	Occupancy < 1% of injections
Analog Bad	Analog	Occupancy < 98% or > 102% of injections
Tuning Failed	Threshold	s-curve fit failed
	ToT	ToT response is 0 or 14 BCs
Noisy	Noise	Occupancy > 10?6 hits per BC
Disconnected Bump	Source Scan (90Sr)	Occupancy < 1% of mean Occupancy

Table 5.6 – Bad pixels criteria during stave qualification per category and test.

As compared to the bad pixel categorisation during QA, the Analog and Digital sub-categories (i.e. "Digital Dead" and "Digital Bad") were considered separately with respect to QA. Additionally, occupancy results from the crosstalk scan were used to evaluate merged bumps; where a high charge (25 ke^-) was injected in the neighbouring pixels to the one under study while reading its response. Two different crosstalk categories were considered: very high crosstalk pixels (with occupancies higher than 80 % indicating merged pixels) and high crosstalk pixels for any other pixel presenting a crosstalk occupancy <80 %. Finally, disconnected bumps were spotted thanks to the source scan, where a minimum occupancy of 1% was required. Bad pixels for the twenty tested staves and categories are shown in Figure 5.29.
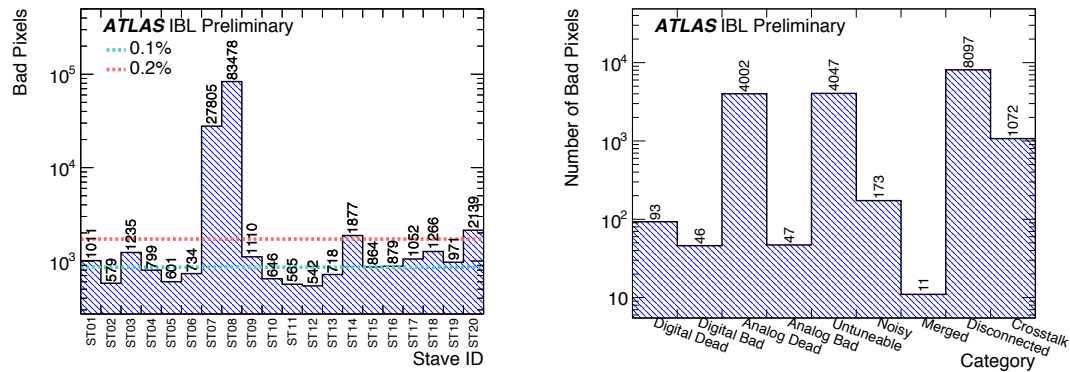
Figure 5.29 – Number of bad pixel per stave (left) for all tested staves. Bad pixels per category (right) for all tested staves excluding stave 7 and 8. Bad pixels fraction of 0.1% and 0.2% are shown as dashed lines in the left panel.

As it can be observed, stave 7 and 8 show a significantly larger amount of bad pixels with respect to all produced staves. This increase of bad pixels was due to an uncontrolled humidity in the testing box during a cold-run leading to some condensation on the stave modules. Both staves have therefore been removed from all previously shown results as mentioned.

A breakdown per category of bad pixels for each stave is shown in Table 5.7. During production, an increase in the quality of the loaded-modules can be observed on the total number of bad pixels up to stave thirteen. Due to the limited availability of modules (in particular 3D sensors), the requested cuts at the production site of less than 100 bad pixels per chip was relaxed towards the end of the production.

Finally, in order to assess the quality of the loading, a correlation analysis between the bad pixels identified at the production sites and after loading was performed. Figure 5.30 presents the correlation of the number of bad pixels per FE detected in the module production and stave QA. A good correlation between both rankings was obtained, with a decrease of bad pixels after loading. The increase in performance could be explained by the improved tuning procedure during stave qualification as well as by a more intense testing at module production.

All IBL stave loading and Quality Assurance, were performed in less than one year from April-2013 to March 2014. A detailed schedule of the stave production is shown in Figure 5.31.

Stave	Digital	Analog	Disconnected	Merged	Untuneable	Noisy	Crosstalk	Total
ST01	6	389	272	3	232	11	98	1011
ST02	10	255	54	3	117	15	125	579
ST03	6	375	473	0	182	21	178	1235
ST04	2	201	254	0	275	8	59	799
ST05	2	207	172	0	183	4	33	601
ST06	6	206	337	0	147	9	29	734
ST09	8	360	476	3	167	8	88	1110
ST10	16	179	304	0	141	3	3	646
ST11	10	196	159	0	155	8	37	565
ST12	15	172	169	0	166	7	13	542
ST13	9	127	205	0	336	6	35	718
ST14	4	161	1364	0	330	7	11	1877
ST15	5	222	350	0	259	20	8	864
ST16	1	237	414	1	187	15	24	879
ST17	2	214	598	0	229	5	4	1052
ST18	13	161	902	1	178	2	9	1266
ST19	10	163	543	0	228	11	16	971
ST20	14	224	1051	0	535	13	302	2139

Table 5.7 – Overview of the number of different bad pixel categories for the 18 qualified staves.
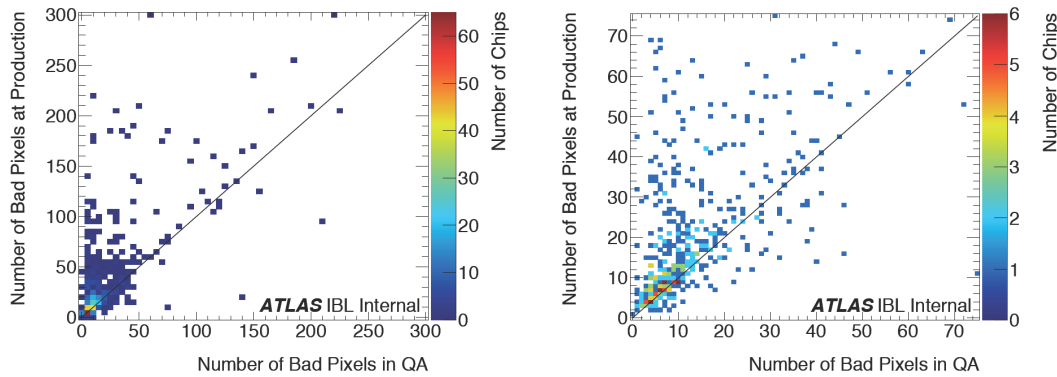
Figure 5.30 – Correlation of the number of bad pixels between the module production site and after stave loading in the stave QA (left). A zoom of the lower-left region is shown (right).

5.4 Stave Ranking and Integration Layout

In order to select the fourteen staves that would be integrated in the IBL and decide their loading position on the IPT, a stave ranking was established. The number of bad pixels, which drives the stave performance, was therefore considered as the main indicator. In the first stage, in order to penalise bad pixels in the central region, an η-weighted bad-pixel was introduced to account for the geometrical acceptance loss. The quality of loaded staves was therefore scored following the formula:

$$V = \frac{\sum_{i \,\in\, \text{bad pixels}} \cosh^{-1}(\eta_i)}{\sum_{i \,\in\, \text{all pixels}} \cosh^{-1}(\eta_i)} \tag{5.1}$$

where the factor $\cosh(\eta_i)^{-1}$ is the weight of the geometrical acceptance of the pixel i at a given η.

In a second stage, the stave position in ϕ around the IPT was evaluated. Due to the particularly tight mechanical contingency on the integration of the last stave, the most planar two staves were selected to be integrated at the first and last position. This was done to take into account the presence of both neighbouring staves during integration of the last stave, in comparison with previous staves where only one of the neighbouring stave was present. The remaining staves were arranged in order to minimise clustered bad pixels in both η and ϕ, by means of a developed algorithm that evaluates the non-uniformity of bad pixels. The final stave positioning and score are summarised in Table 5.8 for integrated staves and spares (without a loading position).

All qualification and performance results presented so far for only the loaded staves are shown in Appendix B. In comparison, Figure 5.32 shows the distribution of bad pixels as a function of η for all integrated staves. As can be observed, a more uniform bad pixel distribution along η was achieved with a total of $0.09\,\%$ and $0.07\,\%$ bad pixels for $|\eta| < 2.5$ (compared to the $0.18\,\%$ and $0.16\,\%$ for non loaded staves).
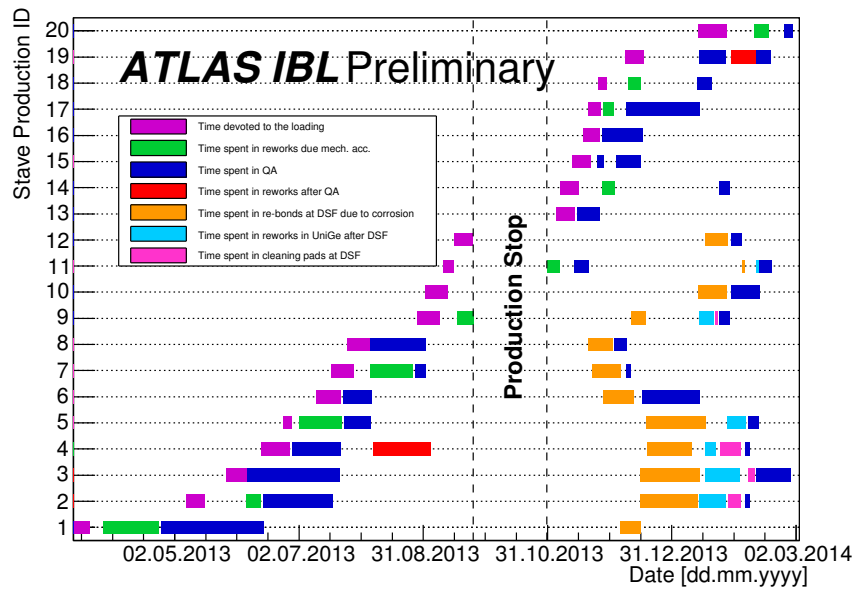
Figure 5.31 – Workflow of the stave loading activities. The dashed lines delimit the stop of the activities due to the observation of the stave corrosion.
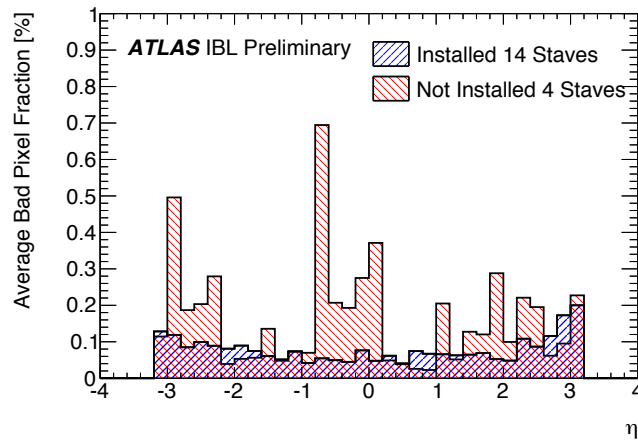
Figure 5.32 – Average bad pixel ratio distribution as a function of η for installed and not installed production staves.

Position	Stave	Number of bad pixels	Score	Planarity [µm]	Reworked
01	ST17	1052	1.01	114	no
02	ST02	579	0.44	205	yes
03	ST19	971	1.13	266	no
04	ST09	1110	1.00	229	yes
05	ST18	1266	0.94	336	no
06	ST04	799	0.69	235	yes
07	ST13	718	0.56	224	no
08	ST10	646	0.62	243	yes
09	ST11	565	0.58	298	no
10	ST12	542	0.62	314	yes
11	ST16	879	0.82	329	no
12	ST06	734	0.79	290	yes
13	ST15	864	0.84	325	no
14	ST05	601	0.68	189	yes
n/a	ST01	1011	1.04	224	yes
n/a	ST03	1235	2.48	223	yes
n/a	ST14	1877	1.11	218	no
n/a	ST20	2139	2.01	237	no

Table 5.8 – Ranking and loading order of the IBL staves. The cooling pipe of the stave in position 01 is at $\phi = -6.1°$, subsequent staves are displaced by $25.7°$ in ϕ. The score is determined by the number of bad pixels, each of which is weighted according to the position on a stave. The last column indicates whether a stave has been reworked at the CERN DSF bonding lab. For completeness, the bottom four lines show the information for the staves that were not chosen for installation. For the stave loading around the beam-pipe, not only this score but a uniform $\eta - \phi$ bad pixel distribution was also taken into account, as well as the engineering constraints.

Detector integration and commissioning

6.1 Stave and Service Integration on the IBL Mechanics

The fourteen selected staves (Section 5.4) were subject to the same integration steps from qualification up to the detector insertion. As a first step, staves were brazed extending their cooling pipe outside the pixel fiducial volume [83] thus avoiding fittings that otherwise may have compromised the material budget. The brazing procedure, connecting the embedded stave cooling pipe and the cooling pipe extension, was performed in a vacuum chamber (Figure 6.1). Both cooling pipes were connected by a titanium sleeve, placing a joint at the induction loop level. An alternating current in the induction loop produced a localised heat, melting the brazing compound rings installed between the cooling pipes and the sleeve. To qualify this procedure, two real staves (not used for final integration) were tested before and after the pipe extensions and showed no difference in terms of calibration and electrical performance.
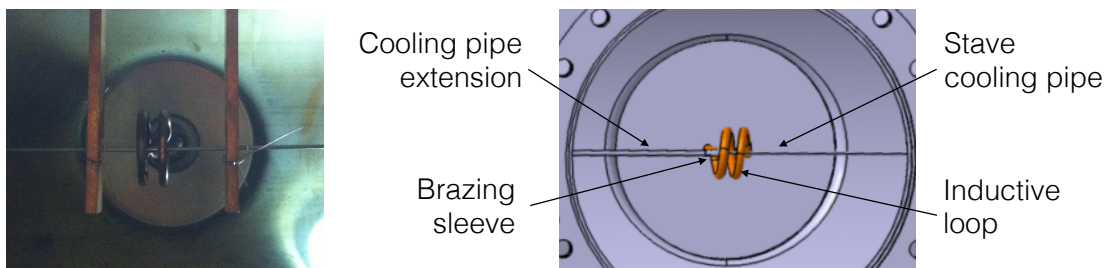
Figure 6.1 – Picture (left) and model (right) of the vacuum chamber and the inductive coil in its center. A stave cooling pipe and its extension are positioned horizontally and connected at the coil level.

Brazed staves were then integrated around the IPT. With the help of the loading stand mechanics, the staves were aligned to the IPT using micrometer screws, avoiding any clash with neighbouring staves (with only 0.8 mm clearance). Once the staves were properly positioned, a transfer from the handling-frame to the IPT was performed and the staves were fixed to the IPT stave-rings. A central ring bonding the staves at their central pin was installed maintaining the clearance in azimuthal coordinate between staves. Figure 6.2 shows the integration of the last
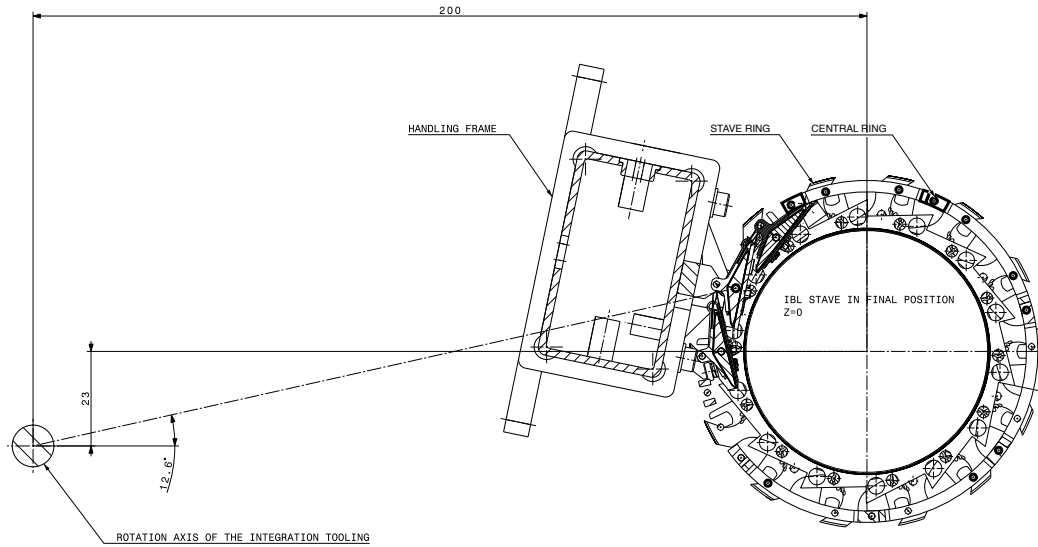
Figure 6.2 – Transversal view of the last stave integration around the IPT, showing only the neighbouring staves. The stave handling-frame is shown at its final position before stave fixation to the IPT stave-rings.

stave and handling-frame before transfer to the IPT. Neighbouring staves have been masked to show the stave-rings as well as the stave central ring.

After each stave integration, type-1 services [84] and i-flexes were installed allowing the stave powering and readout. A 3D model of the services installed around the IPT is shown in Figure 6.3. After the insertion of the IBL inside the ATLAS detector, only the type-1 extremities loaded with the AXON connectors will be accessible (Section 6.2.2).Therefore, all final components were tested after each integration step to guarantee a full functionality after installation in ATLAS, as explained in the following section.
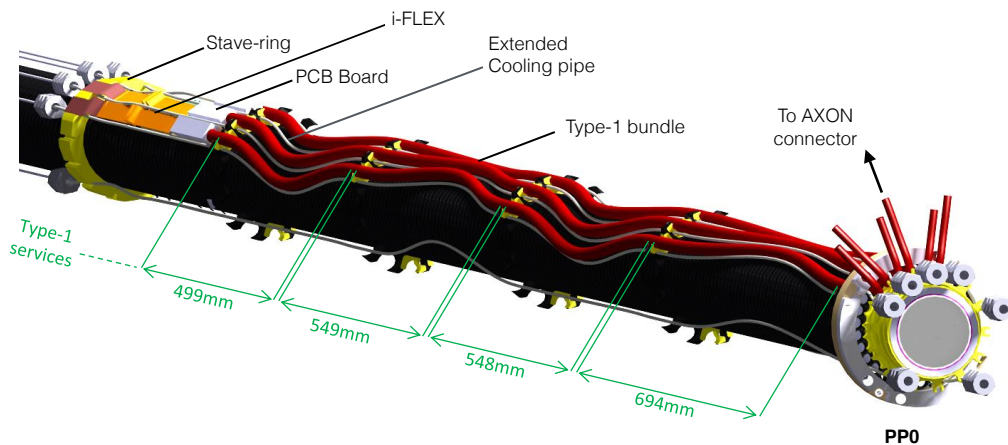
Figure 6.3 – Model of the IBL services showing the type-1 bundles installation around the IPT and the i-flexes connecting the staves and the type-1 PCB boards. On the other side the type-1 bundle is terminated with the AXON connector (see section 6.2.2).

6.2 IBL Commissioning During the Integration Around the IPT

6.2.1 The Connectivity-Setup

In order to verify the electrical integrity of the IBL staves over the different integration steps, a mobile system (connectivity-setup) embedding all the necessary hardware was developed. The mobile setup allowed the electrical checks to be conducted at all locations from the surface to its final installation in the pit, following the detector over the whole process. All front-end and services were systematically tested after each critical integration step. In order to prevent any damage to the final detector, all the test parameters and environmental conditions needed to be carefully monitored.

A customised mobile rack was designed and assembled to allow storing conveniently all the hardware components (Fig. 6.4). The choice was motivated by its compact size, availability and the possibility to transport it easily down to the experiment.

An RCE system was used to configure and run basic tests on half of a stave. Sixteen FE (corresponding to four powering sectors) were tested simultaneously in very short time ($\sim$7 s), avoiding over-heating the modules in the absence of an active cooling during the electrical tests. The RCE readout system GUI allowed the user to run a scan (or a list of scans). The LV power supply was directly controlled by the RCE, allowing the powering of the staves only during the configuration and scan time. In addition, a graphical monitoring of the current and voltage for all the output channels was developed.

Furthermore, the four channels could be activated and deactivated independently and with a pre-defined maximum on-time (added as an extra safety measure on top of the hardware interlock to avoid any potential overheating). Several levels of checks were implemented to guarantee that the PS is switched off at the end of the scan or after a time-out.

In order to check the silicon sensor behaviour and to track its leakage current, a HV power supply and a four channel switching matrix were used. The switching system allowed to select which channel was active.

A GUI allowed full control and configuration of the HV Keithley 2410 power supply such as setting the voltage, the current limit, the ramping speed, the output channel and monitoring. IV measurements were automatically performed for up to four channels sequentially. For each channel, the starting and ending voltages, the voltage step, the ramp speed, the waiting time before acquiring a measurement as well as the current limit were defined by the user.

Figure 6.4 – Front view of the IBL connectivity-setup.
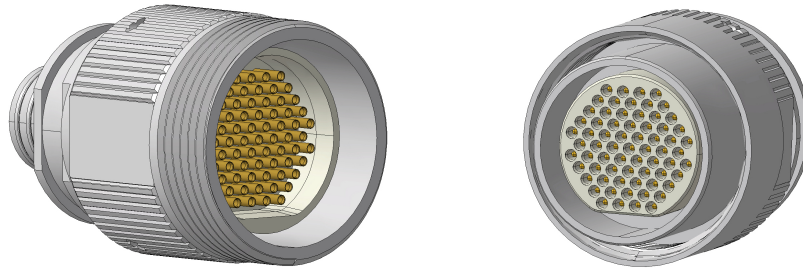
Figure 6.5 – CAD model of the AXON female (left) and male connector (right).

The stave temperature sensors as well as the other environmental sensors located on the pipe, the services and the cable-boards were read-out using a National Instrument [85] NI6009 ADC with eight analog input channels (14 bits each). The monitoring and recording of the detector condition was guaranteed by a custom-made LabView [85] program.

Additionally, a hardware interlock system cutting the power of the LV, HV and HSIO card designed to trigger when any of the module temperatures exceeded $40\,°\text{C}$, was integrated in the DCS hardware.

6.2.2   The IBL Type-1 Services and Connectors

During the different steps of the production and QA, the stave readout and powering could be performed through the PCB-saver. Once a stave was integrated and the final services installed, the read-out had to be made through the Type-1 bundle carrying the stave signals out of the Inner Detector fiducial volume. Each Type-1 service with a total length of 4 m is composed of a cable board (connected to the i-flex) and an AXON connector.

Two different type-1 cables were installed with up to three temperature sensors, monitoring the type-1 bundle and the cooling pipe temperature. Additionally, one every three type-1 bundles where equipped with humidity sensors. Due to the different pin assignment in the type-1 connector for each DCS configuration, it was verified that any error on the switching settings on the connectivity-test to adapt to the correct DCS readout, only lead to a mis-reading, without damaging the DCS sensors nor the detector.

The AXON Connector

One of the most critical points during the service installation was the connection of the AXON connector (see Figure 6.5), a Micro-D connector (1.27 mm pitch) with twist pin contact technology. The AXON connector is terminating the power and DCS bundle at PP1 at about one meter from the IBL sealing location (PP0).

This connector was fabricated on a custom design complying with the IBL space requirements for the insertion of the package inside the existing Pixel subdetector. Due to radial space limitations no mechanical key features were made to guide the two connector shells to guarantee the pin connections. Only a flat key was designed on the PEEK[1] insert for the two connector genders. Very stringent tolerances were imposed to both the connector pins and insert. The custom-made connector with gold-plated pins has a non-standard gold-aluminium soldering to the type-1 data bundle.

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[1]PEEK: Polyether Ether Ketone
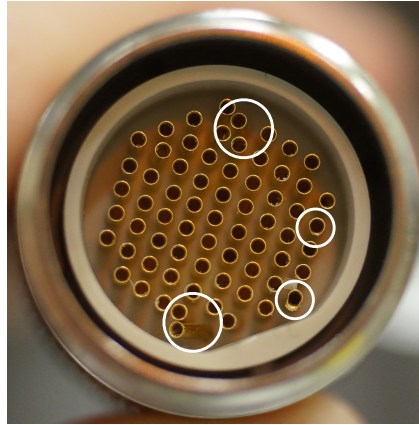
Figure 6.6 – AXON connector shoving severely deformed and bent pins (highlighted with circles).

During the first connections for the qualification of the delivered production prototypes, problems were met on few connectors where female pins were bent and damaged (Fig. 6.6). After reporting to the manufacturing company, several design modifications were implemented improving the clearance of the PEEK insert, limiting the risk of pin misalignment and damage.

In addition, to avoid any deformation of the AXON during the connectivity-test and final connection, a detailed QA was performed before and after each connection, ensuring a correct pin-to-pin alignment.

A picture was taken with a dedicated stand before each connection of the female gender (the most fragile part). The picture was analysed by means of a custom-made software based on the open source libraries Open CV [86]. As shown in Figure 6.7, each pin position was automatically identified by the software[2], and used as input for the fitting of the pins matrix position.

In order to reach a precision of $10\,\mu m$ in the reconstructed pins position, small picture variations (such as rotation and global scale) were corrected for. The rotation of the connector along its axes and with respect to the camera focal plane was taken into account by the software. This correction was performed by fitting the ideal pixel matrix using a MINUIT minimisation routine to the identified pins position. Thanks to the choice of the optics focal length and the small AXON size, the barrel distortion [87] could be safely neglected. Figure 6.8 shows an example of the pins deviation [3] for an individual connector while Figure 6.9 presents the summary for the 28 installed type-1 cables. All values lied within the mechanical accepted limit, determined by the male connector insert flench, shown schematically in Figure 6.10.

PCB-Saver Holder

Although the connectivity-setup aims to readout the staves after installation on the IPT through the Type-1 bundle, a holder for the PCB-saver was developed for debugging purposes. In case of communication problems with the stave, the PCB-saver provided an intermediate testing point to disentangle any possible issue coming from either the stave itself or the readout chain.

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[2]In case of a misleading recognition, a manual adjustment to individual points position was performed.

[3]The pin deviation is defined as the distance between the measured pin position and the theoretical pin position after the MINUIT minimisation of the pins position matrix.

(a)   (b)
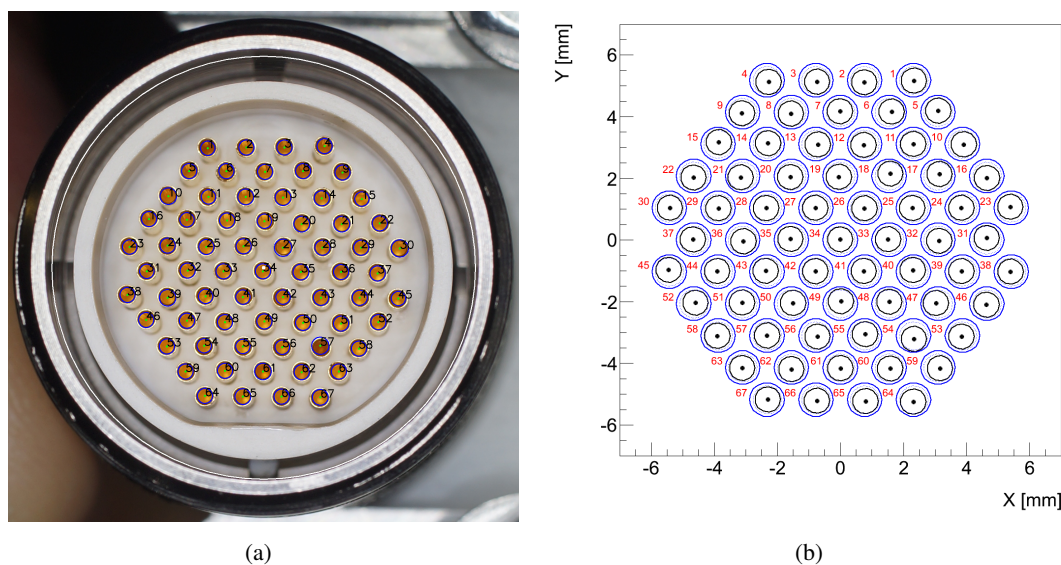
Figure 6.7 – AXON connector (left) showing the identified pins position. In blue the identified female pin radius is shown and its centre is represented in green. Right figure shows The matched pin matrix and the identified pins (black), using a MINUIT minimisation routine (right). Blue circles represent the male insert mechanical limit associated to each pin.
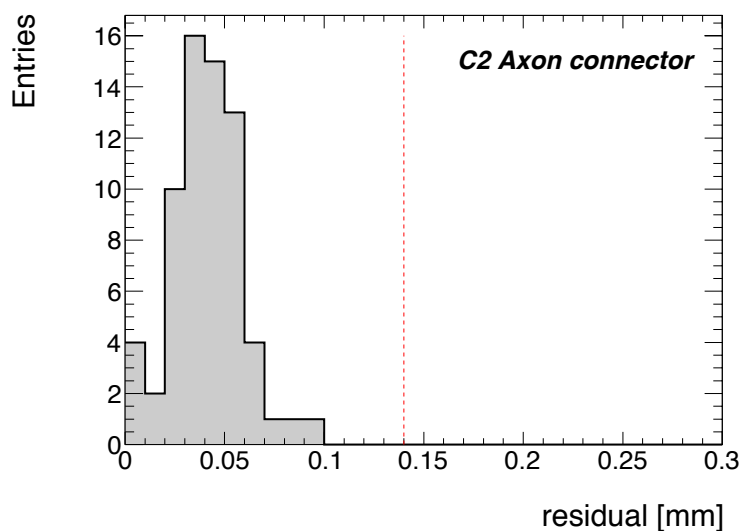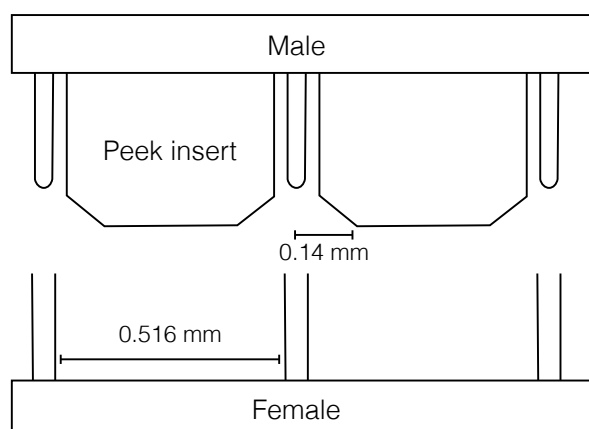

Figure 6.8 – Residuals distribution for the 67 pins of an AXON connector. The red vertical dashed line at 0.140 mm represents the mechanical accepted limit.
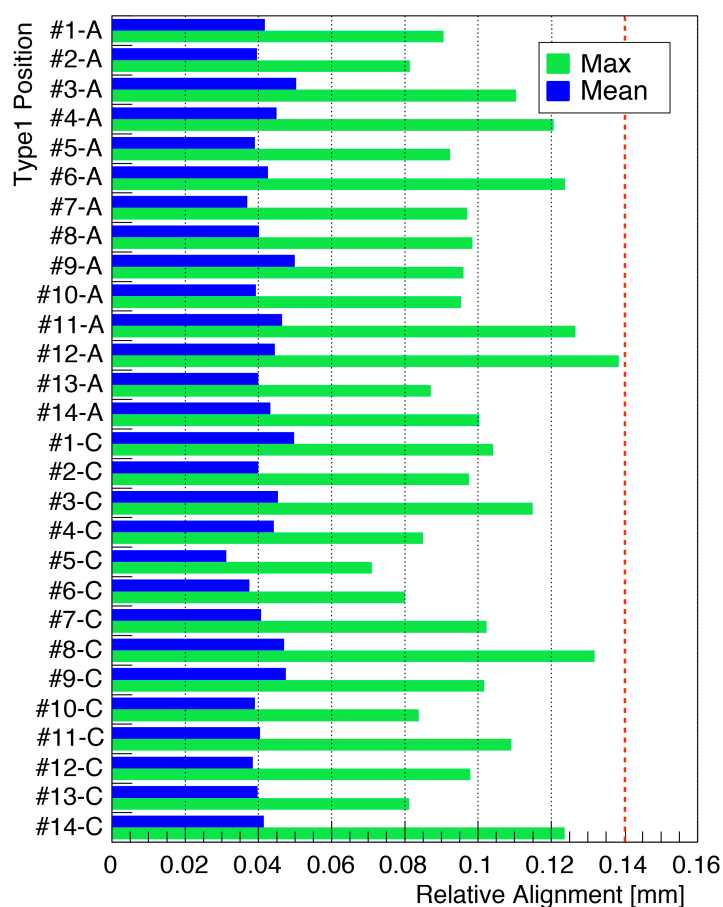
Figure 6.9 – Mean and maximum residual values for the 28 installed type-1 bundles. The vertical dashed line at 0.140 mm, represents the mechanical accepted limit.

Figure 6.10 – Schematic view of part of the male and female AXON connector, showing the PEEK insert and the 0.140 mm flench setting the maximum allowed misalignment.

As shown in Fig. 6.11, the PCB-saver holder is sitting on the dummy IST mechanical structure. The electrical connection with the stave is guaranteed by the intermediate flexes, avoiding any stress or damage to the stave-flex connectors.
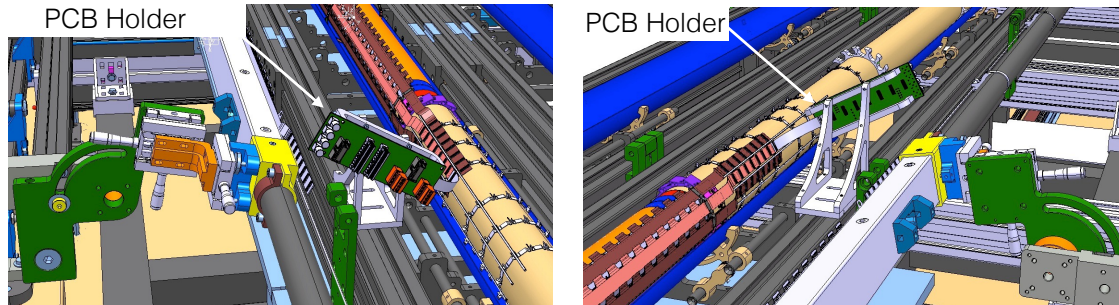
Figure 6.11 – PCB holder and installation on the integration tool.

6.2.3   Tests Performed and Results

The newly installed stave and its neighbouring were tested after each integration in order to make sure that no damage occurred during the process. This procedure led to a double test of each stave except for the first one that ended up being tested three times[4].

Staves were tested after integration and after the type-1 bundle was installed. The testing was performed on both sides in parallel after performing the connection to the AXON as explained in the previous section. The following tests were performed sequentially testing for different functionalities (see Section 5.4(f) for more details):

- *Digital Scan:* allowed to test the powering, the configuration and digital circuits of the FE.

- *Analog Scan:* allowed to verify the correct functioning of the pixel analog circuits.

- *Threshold Scan:* performed with and without HV, this test allowed to verify the configuration of each individual pixel by comparing the pixel threshold to that obtained during the stave QA. The difference between each pixel noise obtained with and without HV, allowed to detect disconnected bumps due to the sensor noise contribution difference.

- *IV scan:* measurements were performed up to 350 V allowing to track the evolution of the sensors breakdown voltage. In case of a breakdown voltage shift, a noise scan was performed with HV, looking for noisy pixels pointing to the origin of the breakdown.

The test results were compared with those obtained during QA (reference). An automatic comparison allowed to track new pixel failures in the digital, analog or threshold scan before a new stave was integrated.

Particular attention was paid to the results of the threshold scans. The average FE threshold values obtained with a stave tuning of 3000 electrons are shown in Fig. 6.12. The difference between the obtained equivalent noise and QA are plotted in Fig. 6.13 showing consistent results after loading. Time over Threshold values were also measured showing no discrepancies with respect to the QA as shown in Fig. 6.14.

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[4]Staves have been loaded onto the IPT starting from position 14 backwards to position 1, sequentially one position at a time.
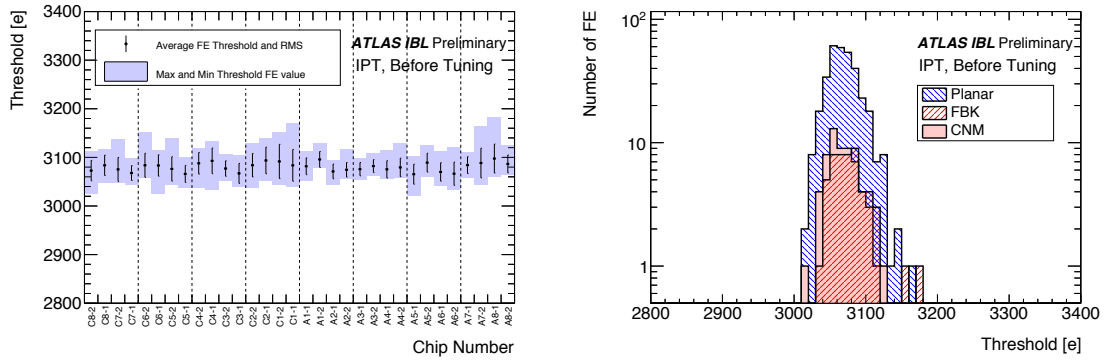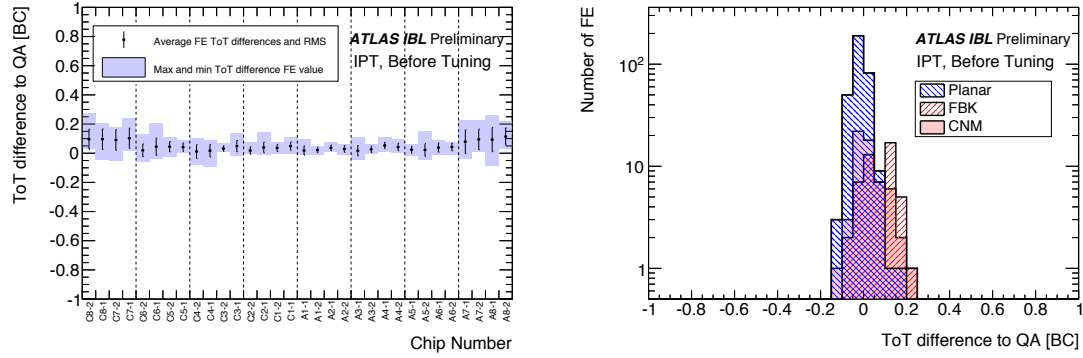
Figure 6.12 – left: average and RMS of the chip-to-chip FE threshold mean value for the 14 staves after integration around the IPT. Data was obtained using the QA configuration targeted to 3000 e and 10 ToT at 16 ke. Maximum and minimum FE threshold mean values of the 14 staves are represented for each chip position by the filled area. Right: FE threshold mean values distribution for each sensor technology.
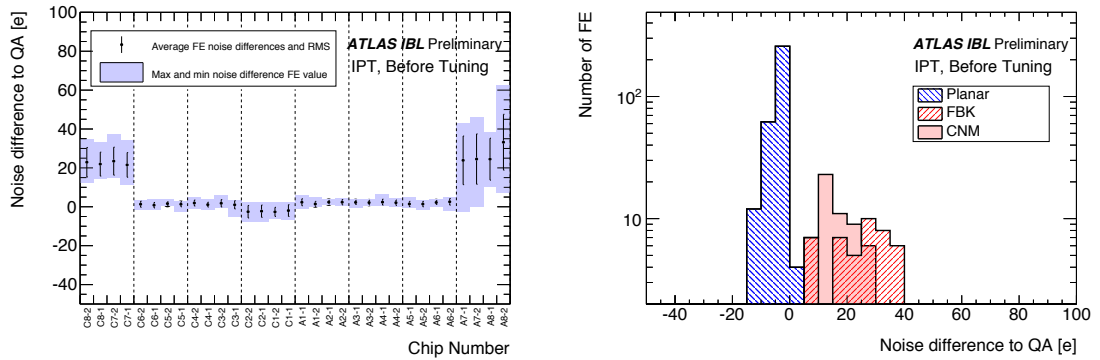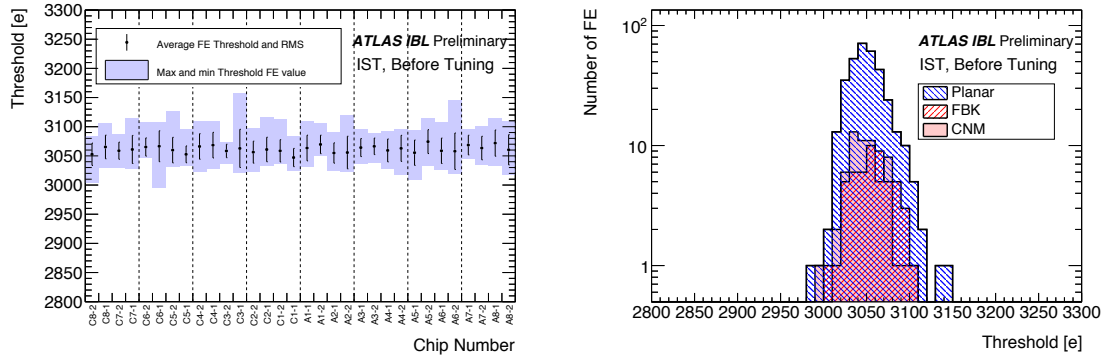

Figure 6.13 – Left: average and RMS of the chip-to-chip FE noise difference between the obtained results with the Connectivity Test minus the quality-assurance (QA) values for the 14 staves after integration around the IPT. Data was obtained using the QA configuration targeted to 3000 e and 10 ToT at 16 ke. Maximum and minimum FE noise mean values of the 14 staves are represented for each chip position by the filled area (most four outer chips per side, using 3D sensor technology, shown different noise behaviour). Right: FE threshold difference values distribution for each sensor technology.

In all cases, tests showed compatible results with the reference QA and no significant deviations were observed, confirming that no damage was caused to the staves during the loading procedure. Being the threshold scan the most inclusive test (involving most of the FE functionalities), results from other tests are not shown here.

After the closure of the IST around the staves and in order to check the correct functionality of all modules before service wrapping and lift to the pit, a reduced set of electrical tests was finally performed. This reduced set included an analog scan (without HV), an IV measurement and a threshold scan with HV. As shown in Figs. 6.15 and 6.16, no misbehaviour nor any significant difference have been observed with respect to QA, meaning that no damage occurred to the staves during the IST closure. This set of tests was the last one to be performed before the transfer of the IBL to the ATLAS cavern and thus before the insertion into the detector.

Figure 6.14 – Left: average and RMS of the chip-to-chip FE ToT mean values difference between the obtained results with the Connectivity Test minus the QA values for the 14 staves after integration around the IPT. Data was obtained using the QA configuration targeted to 3000 e and 10 ToT at 16 ke. Maximum and minimum FE ToT mean values of the 14 staves are represented for each chip position by the filled area. Right: correspondent FE threshold difference values distribution for each sensor technology.

Figure 6.15 – Left: Average and RMS of the chip-to-chip FE threshold mean value for the 14 staves after closing the IST. Data Taking was performed using the QA configuration targeted to 3000 e and 10 ToT at 16 ke. Maximum and minimum FE threshold mean values of the 14 staves are represented for each chip position by the filled area. Right: correspondent FE threshold mean values distribution for each sensor technology.
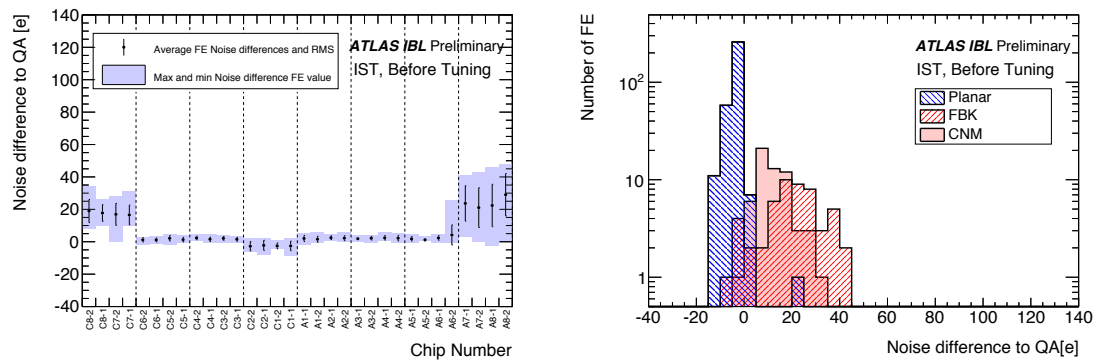
Figure 6.16 – Left: average and RMS of the chip-to-chip FE noise difference between the obtained results with the Connectivity Test minus the QA values values for the 14 staves after closing the IST. Data Taking was obtained using the QA configuration targeted to 3000 e and 10 ToT at 16 ke. Maximum and minimum FE noise mean values of the 14 staves are represented for each chip position by the filled area. Right: correspondent FE threshold mean values distribution for each sensor technology.

6.3 Detector Commissioning After Insertion in ATLAS

6.3.1 The ATLAS Infrastructure and First series of test on the IBL

After the insertion of IBL in ATLAS, the connectivity setup was only used for the staves read-out while the powering was provided through the ATLAS DCS infrastructure, thus avoiding an additional connection to the AXON.

One of the critical parameters to be monitored was the LV, to ensure that no over-voltage would be delivered to the FE regulators later-on. Particularly, due to the sense compensation circuit implemented in the final powering scheme[5], the behaviour of the LV power supply in case of broken sense wires was carefully reviewed.

Applied voltages to the IBL end of stave were measured in the pit thanks to a dummy type-1 service and stave-flex, for different powering configurations (open high and low sense wires). It was observed that in case of open sense wires, due to the voltage compensation, the applied voltage to IBL exceeded the maximum value allowed for the FE-I4 (2.5 V). In Figure 6.17, the measured voltage at the modules for a supplied voltage of 2.1 V (operational voltage) and for different testing scenarios are shown. With a standard powering at 2.1 V, the maximum accepted voltage of 2.5 V was exceeded in case of open sense wires. This combined with the observation during surface testing of open connection in the AXON due to non perfect tightened connectors, additional powering procedures were devised.
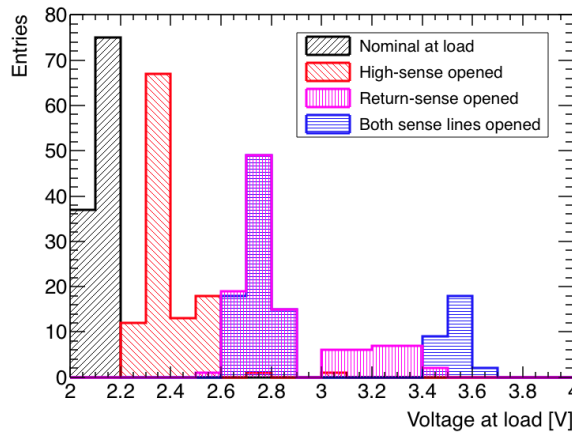
Figure 6.17 – Measured voltages at PP1 during the service testing for a set voltage of 2.1 V under different sense open lines scenarios. A dummy load was connected at PP1 simulating the type-1 bundle resistance.

Since IBL staves were directly connected to the type-1 services, any electrical measurement (such as phase reflexion for non terminated wires) couldn't be performed in order to detect defective connections. Therefore, the sense wires from IBL to an intermediate power station (located at PP2, see Figure 5.4(f)) were tested using a dummy board after the final AXON connection and before powering. Measured resistances are summarised in Fig. 6.18 showing no open sense lines.

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[5]The final LV powering scheme compensates for the voltage drop in the services thanks to the feedback readout of the sense wires.
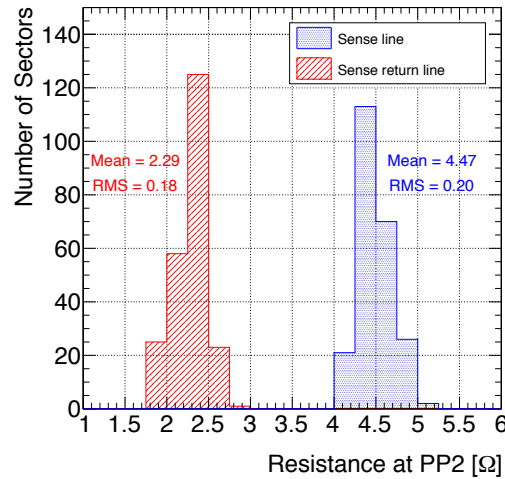
**Figure 6.18** – Measured sense and return sense resistances from PP2 to IBL.

Additionally, in order to prevent a FE over-voltage, the LV supplies were underpowered to guarantee the maximum output voltage of 2.5 V. An internal monitoring allowed to check the applied voltages (before voltage drop) during the powering. Unfortunately, a minimum voltage and current was needed to operate the monitoring, creating a potential over voltage risk. Safe operation windows were determined for different supply voltages and currents given the different scenarios. During the first turn on, IBL was powered with a set voltage of 1.7 V. All channels exceeded the minimum current consumption of 1A to operate the monitoring.

Before connecting the data bundles, a final electrical check was performed with the connectivity setup to assess the functionality of the detector. A reduced set of tests was performed consisting of a digital test and a threshold scan with HV as well as an IV. As shown in Figs. 6.19 and 6.20 for the threshold scan, all FE behaviour were compatible with the QA, showing no discrepancies. These results gave the green light to include IBL in the ATLAS readout system to start the detector calibration and commissioning.

6.3.2 Detector Commissioning with First Cosmic-Ray Data

The Pixel Detector, including now IBL, is responsible for track reconstruction, measurement of charge particle momentum and vertex determination. Being the sub-detector closest to the interaction point, and due to the small pixel size, any misalignments can affect detrimentally the performances of the Pixel Detector. Therefore, one of the very first steps during the commissioning of IBL is the alignment of its different constituents. The alignment is performed using the so-called Global χ^2 algorithm, based on the least square minimisation of the hit residuals taking into account their dependence on both alignment and track parameters. At first, the IBL detector is aligned as a whole (assuming a perfect geometry in the layer substructures, *i.e.* staves and modules) correcting for large displacements. Secondly, the IBL staves and modules are individually aligned correcting for local deformations and misplacements [88].

Right after integration, a first alignment of IBL was performed using cosmic-rays ($\sim$ 8 M events). It was observed that the staves exhibit a distortion of their shape with respect to the designed geometry. The distortion was found to depend on the operating temperature and on the
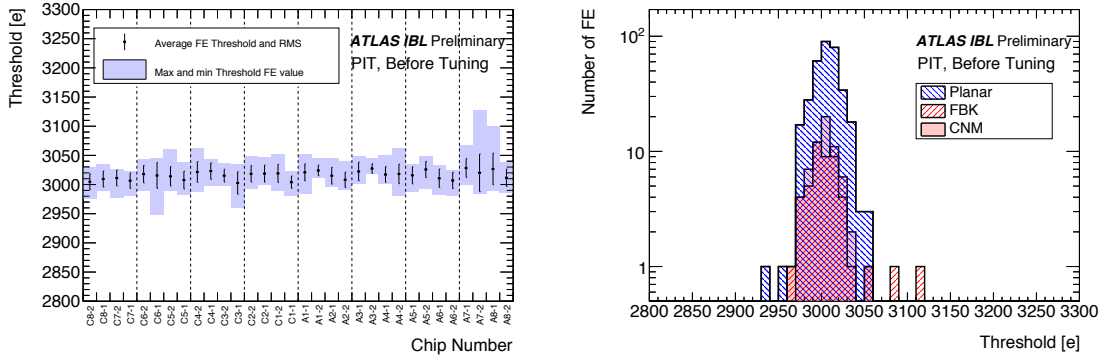
Figure 6.19 – Average and RMS of the chip-to-chip Front-End (FE) threshold mean value for the 14 integrated staves after installation in the pit (left). Data Taking was performed using the quality-assurance configuration file targeted to 3000 e and 10 ToT at 16 ke. Maximum and minimum FE threshold mean values of the 14 staves are represented for each chip position by the filled area. Correspondent FE threshold mean values distribution for each technology (right).
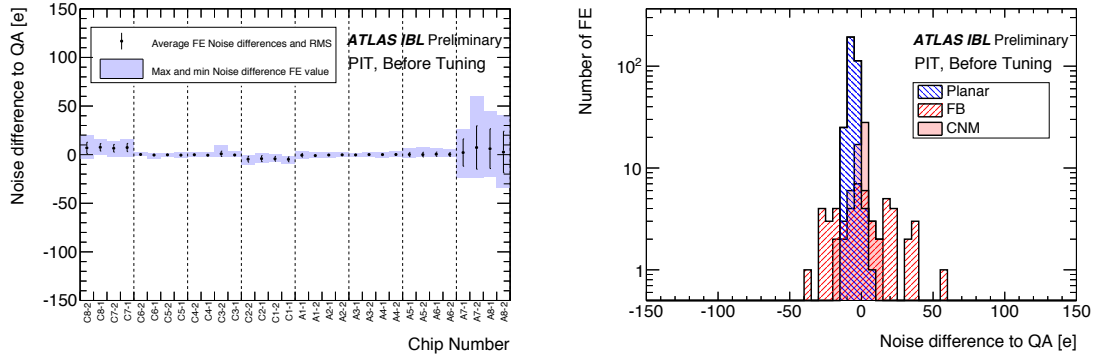
Figure 6.20 – Average and RMS of the chip-to-chip Front-End (FE) noise difference between the obtained results with the Connectivity Test minus the quality-assurance values for the 14 integrated staves after installation in the pit (left). Data Taking was performed using the QA configuration file targeted to 3000 e and 10 ToT at 16 ke. Maximum and minimum FE noise mean values of the 14 staves are represented for each chip position by the filled area (most four outer chips per side, using 3D sensor technology, shown different noise behaviour). Correspondent FE threshold mean values distribution for each technology (right).

mismatch between the CTE of the stave components (stave carbon-fibre and flex).The stave-flex, being mainly composed of copper and being glued to the stave carbon-fibre at room temperature, contracts when cooled down creating a bi-laminar effect.

The track-to-hit residual vector, $\vec{r}_{res}$, is used to quantify the distortion of the IBL. It is defined as:

$$\vec{r}_{res} = \vec{r}_{hit} - \vec{r}_{exp}$$

where $\vec{r}_{hit}$ is the vector of measurements of the hit position in the module and $\vec{r}_{exp}$ is the expected position according to the track fitting. Both are defined in the local coordinate system[6] of the mod-

---

[6]In the IBL module frame, the x_L and y_L local axes are defined in the detector plane with the x_L-axis pointing along the most precise measurement direction. The y_L-axis is pointing along the beam direction (z_G-axis in the global ATLAS coordinate system).

ule registering the hit. The schematic drawing of the local residual vector and the transformation from the local to the global coordinate system[7] are shown in Figure 6.21. Residuals are defined as being unbiased, *i.e.* the hit on a certain module is removed from the track fit for the residual calculation on that module.
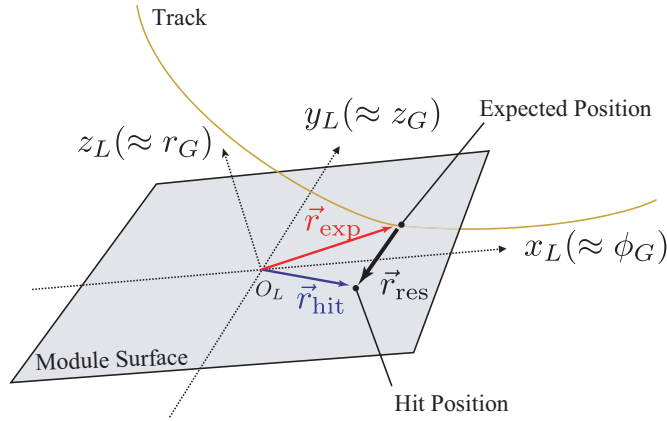
Figure 6.21 – The coordinate system of the track-to-hit residual vector of the IBL module (right). The two-dimensional local residual vector r_{res} is calculated in each module frame. The approximate mapping of the local coordinate system (indexed L) to the ATLAS global coordinate system (indexedG) is indicated.

The distortion effect is dominated by the temperature of the stave-flex. In order to appropriately study the stave behaviour during operation (*i.e.* under different power consumptions), a 2D model was built.

In order to obtain the thermal gradient in the stave, the model geometry shown in Figure 6.22 was considered, the values reported in Table 6.23 were used for the simulation. In addition, a boundary condition in the inner surface of the cooling pipe of $0°C$ was imposed. Figure 6.24 shows the obtained temperature distribution on the stave transverse plane. As expected, the stave-flex temperature was driven by the cooling pipe temperature, showing a thermal coupling of only 10% with the modules power consumption.

Additionally, a Finite Element Analysis (FEA) fully simulating all IBL staves and the barrel supporting structure was performed to corroborate the observed measurements. The simulation confirmed a stave bow toward the negative ϕ_G-direction (see Figure 6.21) in the ATLAS global coordinate system as observed in Figure 6.25. The predicted bowing is approximately parabolic in the azimuthal direction with maximum at the center of the stave. The FEA simulation also predicts radial distortions of the staves other than the region around the central ring, caused by the angle of the stave-flex with respect to the radial component.

In order to estimate the effect of the temperature on the IBL deformation, data were acquired at different temperatures. Each stave bowing was parametrised with the following parabolic function:

$$\Delta x_L(z) = B - \frac{M}{z_0^2}(z^2 - z_0^2) \tag{6.1}$$

---

[7]The ATLAS reference frame is a right-handed Cartesian coordinate system, where the origin is at the nominal p-p interaction point, corresponding to the centre of the detector. The positive x_G-axis points to the centre of the LHC ring, the positive y_G-axis points upwards and the z_G-axis along the beam direction.
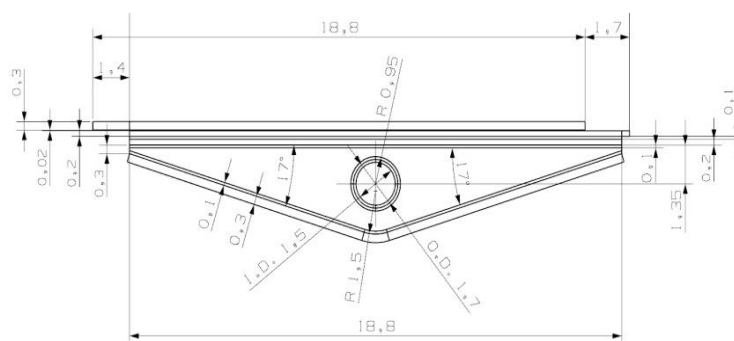
Figure 6.22 – IBL stave 2D geometry used for the thermal calculation. The fact that the thickness of the real Omega is not 0.3 mm has been corrected artificially through the increase of the thermal conductivity coefficient.

Component	Material	TCC [W/m K]
Face-plate & Omega	CF K13C/RS3	0.5
Cooling pipe	Titanium	16.45
Carbon Foam	KFoam	40
Cooling pipe Glue	Stycast glue	1
CF to Carbon foam	Epoxy glue	0.8
FE and sensor	Silicon	148

Figure 6.23 – Thermal Conductivity Coefficient (TCC) used for the 2D thermal simulation.
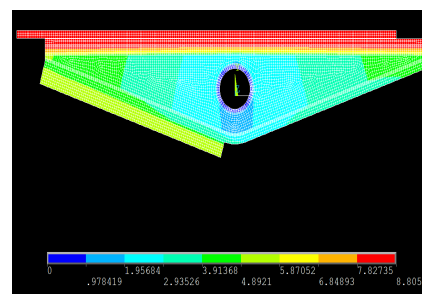
Figure 6.24 – Results of the 2D thermal simulation, with $0°$C temperature boundary condition on the cooling pipe and 0.5 W/cm^2 on the module surfaces.
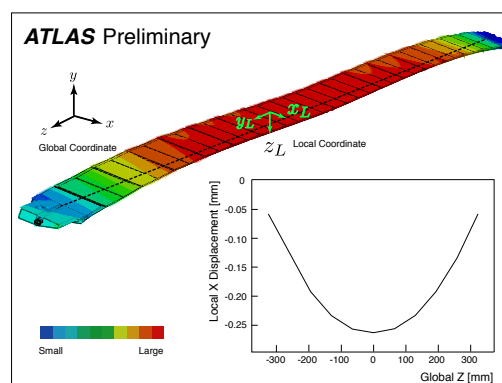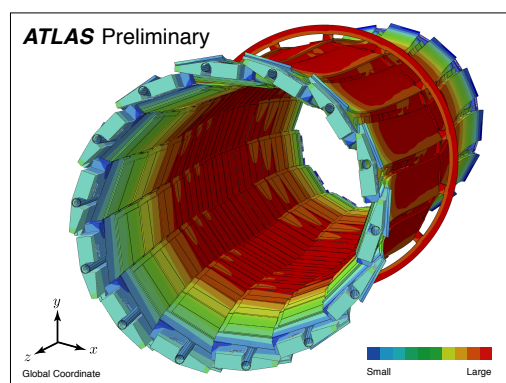
Figure 6.25 – Distortion of the full IBL package including the central ring, simulated by the 3D FEA (left) under a $\Delta T = -60\,°$C. The distortion is magnified by factor of 20 for a better visualisation. The color represents the relative size of the displacement. Detail of the distortion for a single stave (right). The graph in the insert shows the relative-displacement size in the local-x direction (x_L) as a function of the global z-position for the centre of the face plate (ϕ_0).

where $|z_0| \equiv 366.5$ mm is the fixing point of the stave at both EoS, B is the baseline which describes the overall translation of the whole stave and M is the magnitude of the distortion at the centre of the stave. For a given temperature point, and for all staves, B is set to a common constant because the end-blocks of each stave are fixed mechanically. M is the free parameter in the fit, which is used to quantify the size of the distortion.

The resulting fits for each measurement temperature are presented in Figure 6.26, showing the increased bowing with increasing temperatures. The dependence of the magnitude of the distortion with the temperature was found to be linear (Figure 6.27):

$$\frac{dM}{dT} = -10.6 \ \pm \ 0.70 \, \mu m/K \tag{6.2}$$

Given the deformation of $-10.6 \pm 0.70 \, \mu$m/K and the low thermal coupling (10%) between the power consumption and the stave-flex temperature, only significant changes in the FE power consumption need to be taken into account.

Based on a combination of DCS monitoring during the commissioning, engineering FEA simulations and the expected influence of the occupancy on the power consumption, it was found that over the course of a run the excursion of the stave-flex temperature does not exceed 0.2 K.

In order to assess the effect on the track reconstruction of varying temperature conditions during a run, a set of alignment constants was produced to mimic the IBL stave distortion (misalignment). Due to the bowing along the local x-axis, it is expected that the transverse impact parameter d_0 is the most sensitive track parameter. Figure 6.28 shows the d_0 distribution of muon tracks with respect to the beamspot as obtained from Monte Carlo simulations of $Z \rightarrow \mu^+ \mu^-$ events at $\sqrt{s} = 13$ TeV proton-proton collisions using the nominal, geometry and the distorted geometry. By comparing the mean values of both distributions, a bias of only ~ 1 μm is observed; this is small in comparison with the expected d_0 resolution, $\mathcal{O}(10 \ \mu m)$. In Figure 6.28, the full width at half maximum (FWHM) of the d_0 distribution includes the transverse size of the beamspot, $14 \ \mu$m $\times \ 14 \ \mu$m and does not change due to this distortion model.
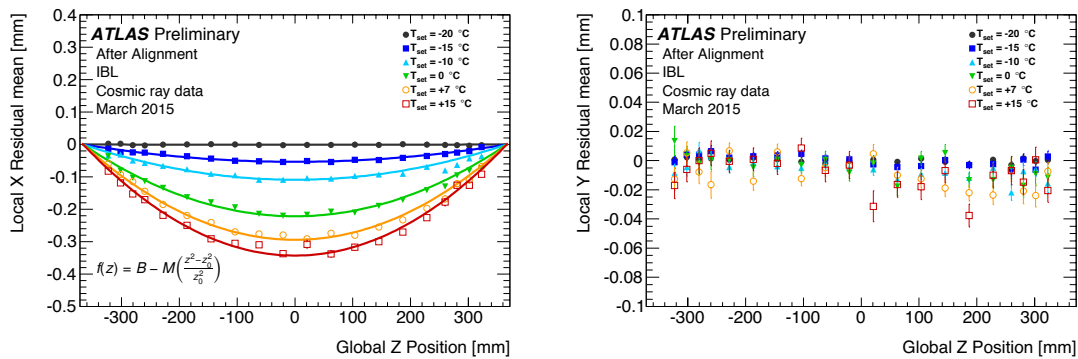
Figure 6.26 – The track-to-hit residual mean in the local-x (left) and the local-y direction (right). The residual mean is averaged over all hits of modules at the same global-z positon. The alignment corrections derived at -20 °C are applied to the local positions in the module frames. For local-x, each data set is fitted to a parabola which is constrained to match to the baseline $B = 0$ at $z = \pm z_0 = \pm 366.5$ mm (see Eq. 6.1).
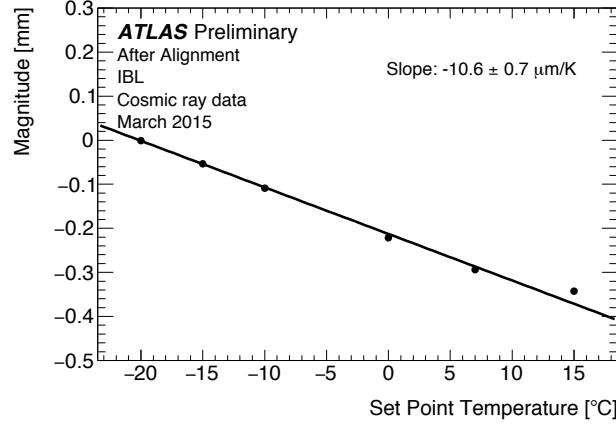
Figure 6.27 – The magnitude of the distortion as a function of the temperature set point. Each data point is a best fit of a parabola to the local-x residual mean as function of the global-z of the module position. The alignment corrections derived at $-20\,^\circ$C are applied to the local positions in the module frames.
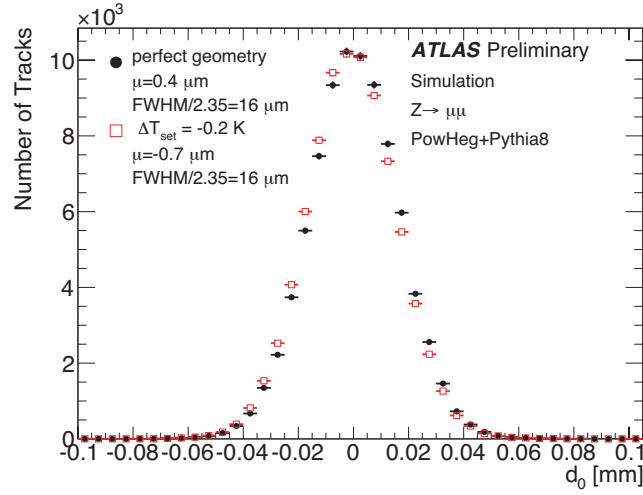
Figure 6.28 – Distribution of the transverse impact parameter d_0 of charged tracks with respect to the beamspot obtained from $Z \rightarrow \mu^+\mu^-$ events simulated in $\sqrt{s} = 13$ TeV pp collision. Solid circles show the nominal geometry and the open squares the distorted geometry corresponding to a temperature variation of the IBL of -0.2 K ($\sim 2\,\mu$m of displacement at the centre of the stave according to Eq. 6.2).

HV-CMOS Test-beam Data Analysis with the FE-I4 Telescope

7.1 Overview of the FE-I4 Telescope

During the R&D phase of a new pixel sensor technology for the HL-LHC, in addition to a complete electrical characterisation in the laboratory, it was essential to evaluate the sensor response to real particles. Thus, and in order to evaluate the detectors performance, test-beam measurements needed to be performed. For this purpose, the University of Geneva ATLAS group has designed and produced a tracking telescope (referred here as the "FE-I4 telescope") based on IBL modules, capable of acquiring data at very high rates.

7.1.1 Design and Capabilities

The FE-I4 telescope is a modular and compact telescope with a total length of 1200 mm. Two arms 400 mm-long allow the positioning of the telescope planes at different Z positions along the beam axis[1]. The standard telescope configuration is presented in Figure 7.1. It consist of 6 planes distributed in the arms (3+3). Two triggering scintillator planes can be installed at both ends for precise timing.

In-between the telescope's arms is installed a Device Under Test (DUT) box which is positioned using two micrometer stages along the X and Y axis directions. Via an external liquid-base cooling unit (chiller), the DUT box contact surface can be cooled down to $-50\,°C$ to test irradiated sample, thus avoiding any annealing [89]. The cooling system and DUT box provides a stable testing temperature as well as an easy operation with respect to more conventional coolings such as dry-ice.
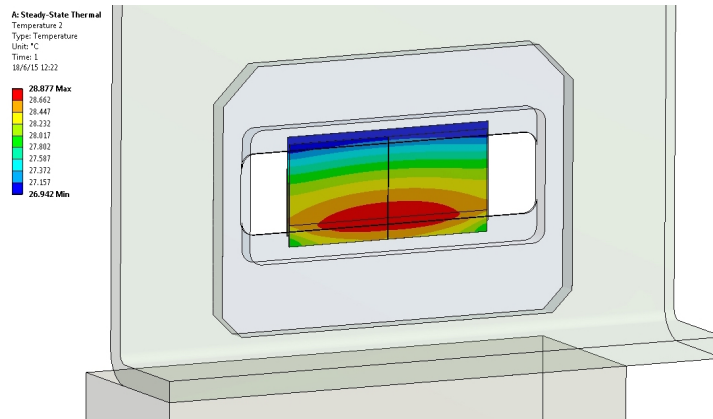
The Telescope Planes

Each telescope plane is composed of an aluminium frame, an IBL double chip module (section 4.2.2) and a module PCB adapter-board. The 4 mm-thick aluminium supporting-frame allows to easily position the modules on the telescope arms by machined rails. The sensors are directly

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[1]We use a right-handed Cartesian (X,Y,Z) global telescope coordinate system with the Z-axis pointing in the nominal beam direction and the Y-axis pointing downwards.
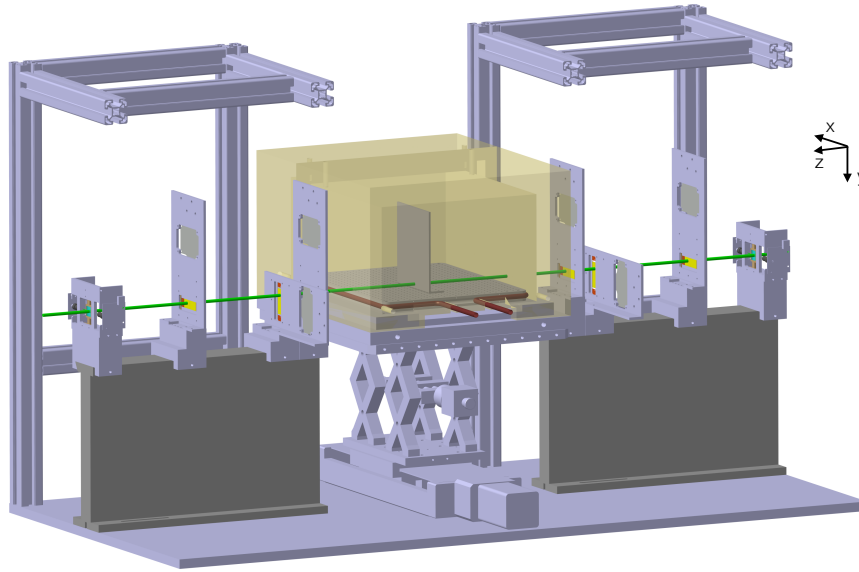
Figure 7.1 – View of FE-I4 telescope showing the two arms equipped with three planes each and the triggering scintillator planes at both ends. In each arm, the first and last planes are installed vertically while the central plane is installed horizontally (rotated).

Figure 7.2 – Finite element thermal simulation of an IBL module loaded on a telescope plane with a standard module power dissipation of 0.8 W/FE and ambient temperature of 25 °C. The plane frame is represented in transparent illustrating the module overlap with the frame as well as the recess.

mounted on the supporting-frame. In order to reduce multiple scattering by traversing particles, a 62×14 mm^2 opening was created in the frame, overlapping with most of the module active area. The direct contact of the module with the supporting-frame at both long edges, not only simplifies the mechanics but also allows to achieve a passive cooling for the IBL modules. Thermal simulations with a power dissipation of 0.8 W/FE, corresponding to the power consumption of the FE-I4, showed a maximal module temperature of 29 °C when both FEs are operated (Figure 7.2). To minimise the scattering effect in the region where the module and the frame overlap, a recess was performed, leaving a frame thickness of only 0.5 mm shown in Figure 7.2.

(a)

(b)

(c)

(d)
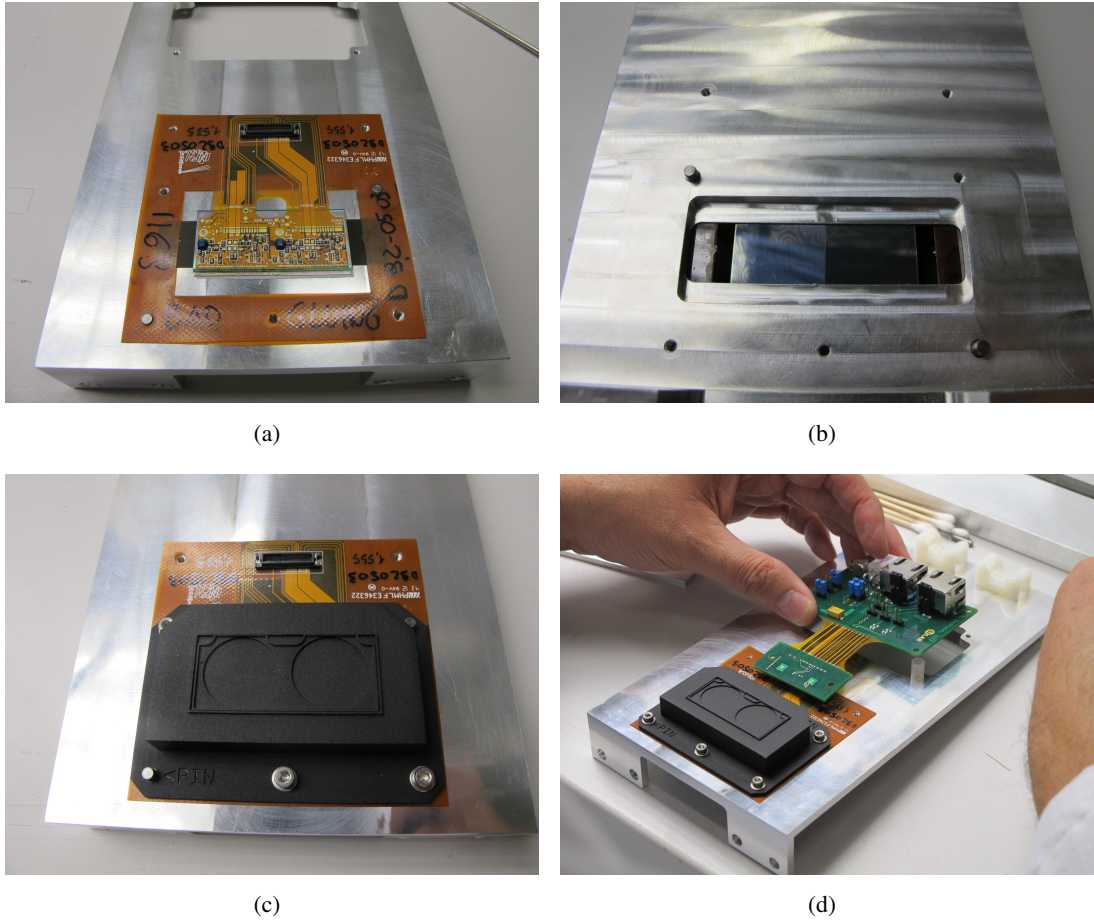
Figure 7.3 – Plane assembly process showing the module positioning on the aluminium supporting-frame a) and its back view revealing both FE and the frame recess b). The module fixation and protection is performed with a 0.4 mm-thick stereolithography cover c). The plane assembly is finalised with the connection of the module PCB adapter board to the module pig-tail Panasonic connector d).

All FE signals (data, clock and command) as well as the powering and HV are provided via the module PCB adapter card. By this means, the default module pigtail Panasonic connector can be used, strongly simplifying the planes assembly. Figure 7.3 shows the various steps of the assembly of the planes.

After the final installation of the IBL, due to the combined availability of a fast and compact readout system (connectivity setup), and the unqualified production modules[2], the usage of IBL modules for the telescope development was the most cost and time efficient solution. Therefore, the telescope planes are equipped with a 41.32×18.59 mm^2 silicon sensor with an asymmetric pixel pitch of $250 \times 50\,\mu$m^2. To obtain a similar telescope resolution in both the X and Y coordinates, the orientation of the modules is alternated between telescope planes as shown in Figure 7.1. The geometrical overlap between modules obtained due to the vertical and horizontal planes is reduced to a single FE as represented in Figure 7.4. Therefore, during operation, only one FE per module is used, centred with the beam axis thanks to the aluminium frame base.

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[2]Here, unqualified production modules refers to modules failing the IBL selection criteria of bad pixels.

The design of the plane frames enables not only the positioning and anchoring, but also their rotation along the X and Y-axis by means of pre-machined reference pins at $0°$ and $\pm15°$. Additionally, each of the FE can be centred with respect to the beam axis allowing the operation of only one FE.
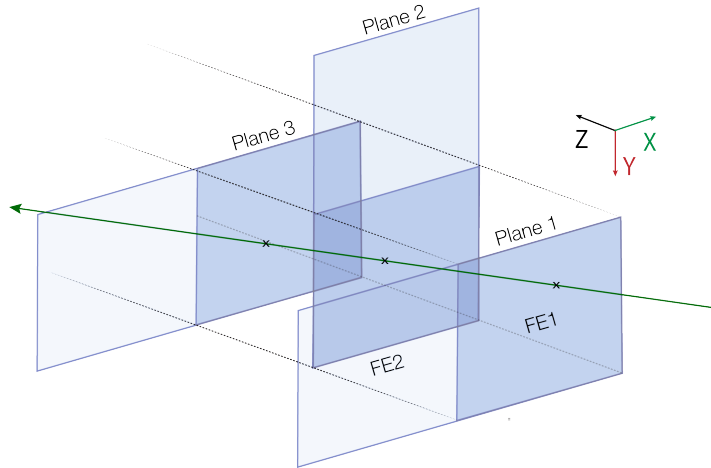
Figure 7.4 – A schematic view of a single arm of the telescope plane modules, showing the rotation between planes and the overlaid region. A particle track and the associated hits on the telescope planes are represented by the green arrow an the crosses, respectively.

7.1.2 Data Acquisition System

The FE-I4 telescope data acquisition relies on an adapted RCE readout system for its robustness and high speed parallel readout. With a single ATCA crate hosting four RCEs and the optical link to the HSIO board, up to 8 FE-I4 can be read-out in parallel fitting perfectly the FE-I4 telescope application. Having a telescope with a total of 6 active FE planes, up to 2 DUTs using FE-I4 as readout ASIC can be tested simultaneously with the same readout system, simplifying the data acquisition and analysis.

Trigger System

The telescope trigger system is centrally managed by the HSIO via two input LVTTL external signals and the onboard FPGA. Using the FE-I4 self trigger functionality (hitBus), a trigger pulse can be generated by the FE when a telescope plane has registered an event and be directly processed by the RCE. During standard operation, signals from the first and last telescope planes are used in coincidence (within 1 BC i.e. 25 ns). The FE-I4 pixel-mask was used in order to define a Region Of Interest (ROI) on the triggering planes. This allowed for a flexible and complex ROI definition online during data taking suitable for any DUT.

The self trigger approach simplifies significantly the trigger hardware by avoiding the need of external scintillators. Alternatively, two triggering scintillators planes, each composed of two scintillator layers, can be installed at both ends. The coincidence between two layers of each plane is then used to generate the LVTTL trigger input signal.

During data taking, up to 16 BC (400 ns) were readout consecutively after each trigger on the DUT making the module adjustment phase[3] easier and allowing for offline time studies on the DUT.

In order to improve the telescope performances, only 4 BC were readout on the telescope planes, reducing the data transfer to the readout system. Additionally, the RCE load was optimised using 3 telescope planes per RCE and one DUT per RCE[4]. A trigger rate of 20 kHz was achieved during data taking via the RCE readout time and load optimisation previously mentioned.

7.2 Data Reconstruction Software and Offline Analysis

7.2.1 Overview

The raw data from the FE-I4 telescope planes and the DUT have been reconstructed and analysed using Judith [90], a C++ software package for telescope data reconstruction originally developed for test-beam data analysis with heterogeneous reference detectors. The code package has been adapted for the FE-I4 telescope configuration and module specificities.

To obtain the particle trajectories by the reconstructed tracks from the single hits on the telescope planes, an alignment of each plane is performed before the track reconstruction. On a second step, the DUT synchronised data stream[5] is used to perform the analysis on the DUT, and the associated spatial and timing resolutions are reconstructed. The overall analysis process is schematically represented in Figure 7.5.
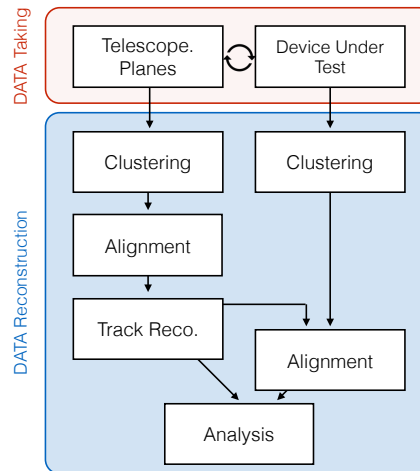
Figure 7.5 – Schematic representation of the test-beam data analysis flow for track reconstruction with the Judith software. In case of the use of two different DAQs, the data from the telescope and the DUTs are synchronised to eliminate event mismatches. Both data streams are then analysed in parallel. The telescope is aligned and tracks are reconstructed. The clustering is performed on the DUT allowing the alignment of the DUT. Finally the DUT analysis is performed, evaluating its performance in terms of efficiency and timing.

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[3]Due to the large readout window, planes desynchronisation of the order of 1 BC did not affect the detection efficiency, keeping all planes detection time within the readout window.

[4]This RCE-load optimisation was possible thanks to the reduced data transfer from the telescope planes (i.e. 4/16 BC readout window, ∼25%).

[5]In case the data taking was performed with two different DAQs, for the DUT and the telescope planes, a synchronisation of both data streams needs to be performed to detect missed triggers in either of the streams.

7.2.2   Clustering Algorithms

The first step in the data reconstruction is the clusterization, consisting on the association of mul-
tiple pixels which have recorded a signal into clusters, so that all pixels hit by the same particle
are grouped together.

   The clustering used in Judith is based on an iterative procedure. Starting from a single hit,
neighbouring fired pixels are associated to the cluster, and recursively neighbouring pixels are
added to the new cluster. Optionally, a maximum cluster size (number of pixels contained within
a single cluster) as well as a the maximum distance between two independent clusters to be joined
in one uni-cluster can be set in the algorithm. This process is performed for all hits, excluding hits
already associated to a cluster, avoiding double counting. If during the clusterization, a fired pixel
(or more) is not properly associated to the cluster, this is interpreted as if two (or more) particles
had crossed the sensor and therefore two tracks (or more) might be reconstructed.

   For clusters containing more than one pixel, a method to reconstruct the hit position is needed.
A straightforward method to reconstruct the cluster position is to compute the barycenter of the
hits in the cluster:

$$(x_{clus}, y_{clus})_{\text{digital}} = \left(\frac{\sum_{i=1}^{n} x_i}{n}, \frac{\sum_{i=1}^{n} y_i}{n} \right) = \frac{1}{n} \left(\sum_i x_i, \sum_i y_i \right)$$

   On the telescope planes, the integrated charge deposited on each pixel is accessible throughout
the ToT as measured by the FE-I4. This allows us to improve the cluster position resolution by
weighting the contribution of each hit by the associated deposited signal:

$$(x_{clus}, y_{clus})_{\text{analog}} = \left(\frac{\sum_i^{n} Q_i \cdot x_i}{\sum_i^{n} Q_i}, \frac{\sum_i^{n} Q_i \cdot y_i}{\sum_i^{n} Q_i} \right)$$

   In order to improve even further the resolution through the weighting procedure, one can take
into account charge sharing effects in between neighbouring pixels (η function). This technique
allows a finer resolution for double-hit clusters by taking into account the small inter pixel region
where charge sharing effects between both pixels allow to fire two neighbouring pixels.

   As shown in Figure 7.6 the cluster size for the telescope planes is dominated by single hits
clusters, representing more than 80% of the total number of clusters. The results presented in the
following sections are baed on digital clustering.
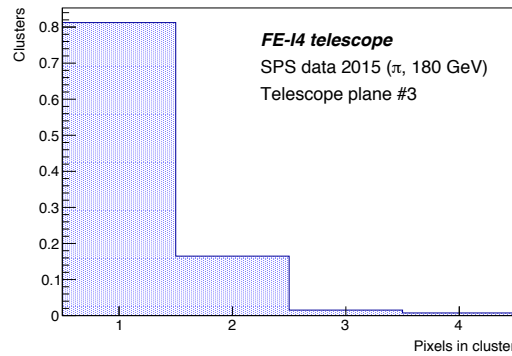
Figure 7.6 – Clusters sizes (number of hits per cluster) on a FE-I4 telescope plane. The distribution
has been normalised to unity.

7.2.3   Alignment of the Telescope Planes

The telescope planes are aligned in two steps. First, a coarse alignment is performed, correcting for X and Y displacements of the telescope planes. Taking the first plane as a reference, the successive planes are aligned with respect to the previous one. This first alignment is performed using the distribution of the distance between clusters on two planes on both the X and Y-axis (plane-to-plane cluster distances). By fitting both distribution with a Gaussian, a coarse alignment is obtained by correcting the planes position by the respective deviation from zero of the Gaussian mean. Although this method provides a robust and fast starting point, it however relies on the hypothesis that the beam is parallel to the telescope Z-axis. Therefore, an incident beam entering with an inclination with respect to the planes normal direction will result on an artificial shift of the telescope planes as explained in Figure 7.7.
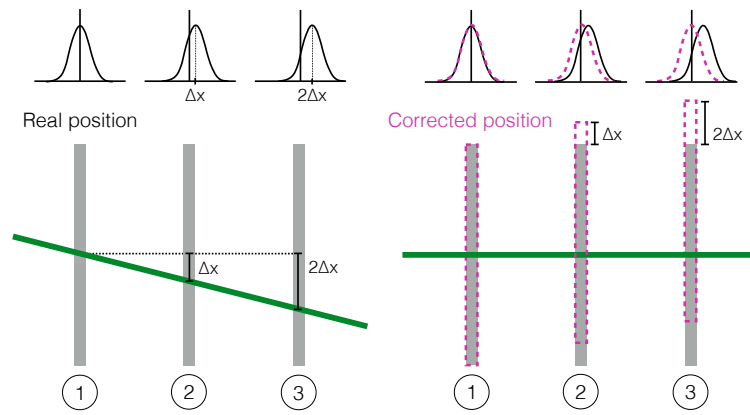
Figure 7.7 – Schematic representation of a particle beam (green) with an incident angle with respect to perfectly aligned telescope planes. The plane-to-plane cluster distances distributions before coarse alignment is shown (left). The situation after coarse alignment (right), shows that the telescope planes are artificially shifted (dashed pink lines) as a result of the coarse alignment.
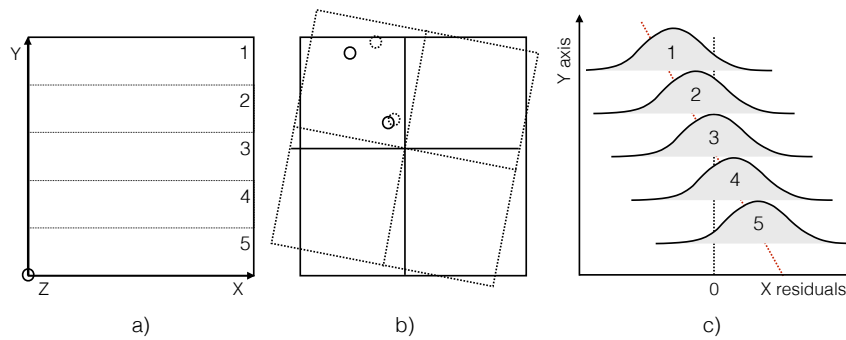
Figure 7.8 – Schematic representation of the fine alignment for the R_Z correction. In Figure a), the sensor is "sliced" in 5 sections along the Y axis. The latter corresponds to the number of slices which is a parameter that can be selected by the user during the analysis. In b), the predicted position of the sensor and the hits are represented with solid lines. Extrapolated hits and sensor positions are shown with dashed lines. In c), the Gaussian unbiased residuals distribution obtained in each of the five Y-slices are represented, as well as the linear fit to the values of the Gaussian distribution.
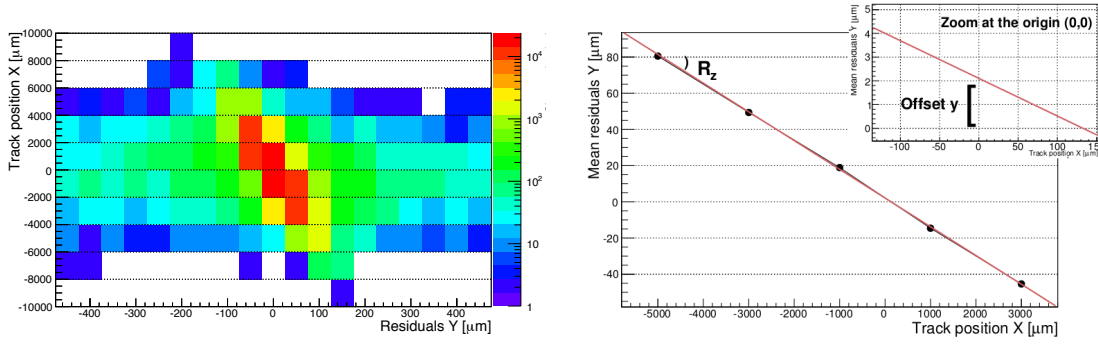
Figure 7.9 – Unbiased Y residuals distribution for each of the ten X slices (left). The mean value of each Gaussian fit for the slices and its linear fit in red (right) are shown. In order to guarantee the convergence of the alignment, slices with large fitted sigma and low χ^2 were removed from the linear fit.

A fine alignment is therefore performed subsequently to the coarse alignment. This correction is derived from the distribution of the unbiased residuals. The unbiased residuals are defined as the difference in distance between the track hits on both the X and Y axis and the extrapolated hit position obtained by the reconstructed track excluding the layer under study. Translations along the X and Y axis, as well as rotation along the Z-axis (R_Z) can then be corrected as explained below. The sensor on each plane is divided in slices along the X-axis (Figure 7.8 a), and the unbiased residuals distributions along the Y axes are computed. The distribution is each slice is fitted with a Gaussian function, each mean value providing a mean displacement of the Y-residuals per slice. A linear fit of the obtained X Gaussian means values allows the correction of the rotation and offset as shown in Figure 7.8 b. Example of the plots used during the alignment procedure are shown in Figure 7.9.

The fine alignment procedure typically converges to its final value after about 15 iterations for all planes as shown for X, Y and R_Z in Figure 7.10.

The induced error on the cluster position by the telescope plane alignment (σ_{a_p}) is defined as the quadratic sum of the translation ($\sigma_{a_p,translation}$) and rotation ($\sigma_{a_p,rotation}$) uncertainties. The translation uncertainty is estimated to be the RMS of the obtained correction for iterations larger than 20:

$$\sigma^2_{a_p,translation} = \sigma^2_{a_p,translation_x} + \sigma^2_{a_p,translation_y}$$
$$= (0.1636\ \mu m)^2 + (0.0138\ \mu m)^2$$
$$\sigma_{a_p,translation} \simeq 0.164\ \mu m$$

Since the convergence point is already reached by iteration 15 as shown in the example of Figure 7.10, the spread of the distribution reflects the uncertainty of the method.

Equivalently the rotation uncertainty is obtained by the RMS of the angular corrections (R_Z) multiplied by half the FE length ($\sim$20 mm):

$$\sigma_{a_p,rotation} = \sigma_{R_Z} \times 20000\ \mu m$$
$$= 2.3166651703 \cdot 10^{-6} \times 20000\ [rad \times\ \mu m]$$
$$\simeq 0.05\ \mu m$$

The total error on the cluster position for the telescope planes induced by the alignment of the telescope planes is therefore: $\sigma_{a_p} = 0.171\ \mu m$.

(a)   (b)

(c)
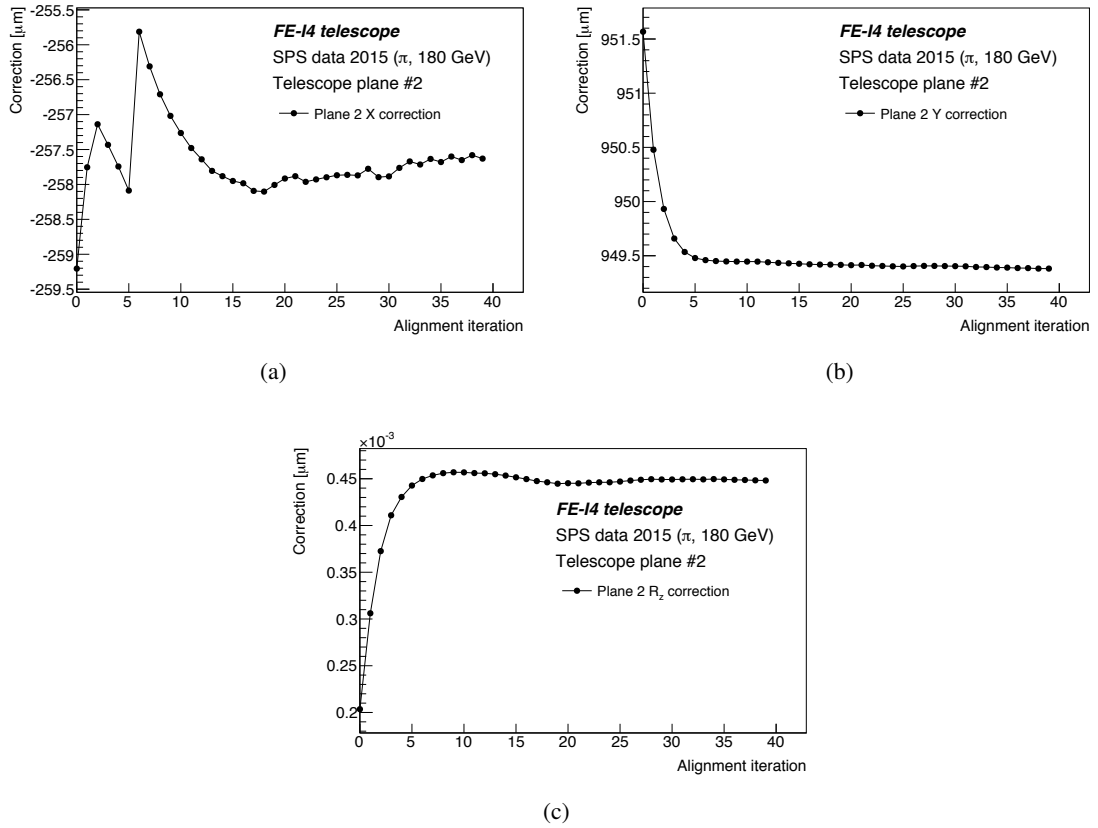
Figure 7.10 – Fine alignment corrections in X (7.10(a)), Y (7.10(b)) and R_Z (7.10(c)) obtained for the telescope plane 2 over 40 iterations.

7.3 Expected Performance of the FE-I4 Telescope within the Judith Framework

The expected telescope resolution, as for any other tracking detector, is a convolution of the number of measured space points, their resolution and the effect of multiple scattering. More precisely, for the FE-I4 telescope, the uncertainties are driven by the following contributions: the cluster resolution (σ_r), the multiple scattering (σ_s) and the alignment uncertainties.

7.3.1 Single Hits Resolution

The position resolution of a pixel detector is determined at the first order by the pixel size. The ideal single hit resolution (σ_r) of a pixel detector is a box-like response with width given by the pixel pitch (p). When a pixel detector is used for tracking purposes, that is subject to a uniform particle distribution, the measured position have a standard deviation:

$$\sigma^2 = \int_{-p/2}^{p/2} \frac{x^2}{p} dx = \frac{p^2}{12}$$

Therefore the statistical resolution of a pixel detector is $p/\sqrt{12}$ in each of the two spatial dimensions measured.

It is important to note that all the electric field lines in each pixel cell converge to the electrodes which motivates the assumption that the spatial resolution is determined by the pixel pitch rather than by the electrodes width. Since the IBL sensors used in the telescope have a full depletion at $\sim$60 V, the diffusion component and its influence on the detector resolution can be neglected.

The FE-I4 pixel pitch is $250\,\mu m \times 50\,\mu m$ $(x \times y)$[6], the single hit resolution is given by:

$$72.2\,\mu m \times 14.4\,\mu m\ (\sigma_{r,x} \times \sigma_{r,y})$$

If a digital clustering is used, the cluster resolution on each axis is determined by $p_{(x,y)}/\sqrt{12}$, where $p_{(x,y)}$ is the cluster size on each axis direction and cluster with multiple pixels have therefore larger uncertainties.

7.3.2 Multiple Scattering

Charged particles passing through matter interact with nuclei electrostatic field, causing repeated elastic Coulomb scattering. Since silicon nuclei have a mass (m_{Si}=26161.64 MeV/c^2) much greater than most of the incoming particles (m_π=139.5 MeV/c^2), the energy transfer is negligible but each scattering adds a small deviation to the incoming particle's trajectory.
During the data analysis, tracks are built starting from an initial hit on the "seed plane", defined as the first plane where a track can start and therefore where a hit is required). From the seed plane, the tracking algorithm finds recursively all clusters within a solid angle in the following planes, building all track candidates. Tracks without a hit on each plane are allowed by the algorithm, although the request of a minimum number of hits per track can be specified. Track candidates are fitted with a straight line (two degrees of freedom per coordinate, $t_{(x,y)} = a \cdot (x, y) + b$) and the track with the lowest fitted chi-square is retained. Although this technique can accommodate to some extent for multiple scattering (considering different values of the solid angle at the track reconstruction level), it leads in general to an increased χ^2 of the reconstructed tracks that were subject to a large multiple scattering. Therefore, a cut on χ^2 can be used to select only those tracks for which the multiple scattering did not have a large impact on the particle trajectory.

The particles deflection when encountering matter is well described by Rutherford's formula[91]:

$$\frac{d\sigma}{d\Omega} = \frac{z^2 Z^2 e^4}{16 E^2} \frac{1}{\sin^4(\Theta/2)}$$

where $\frac{d\sigma}{d\Omega}$ is the differential probability density of particles scattered per solid angle, Ze is the nuclear charge, ze the charge of the scattered particle, E its energy and Θ the scattering angle.

Since our telescope has a silicon thickness of $350\,\mu m$ per plane ($200\,\mu m$ of sensor + $150\,\mu m$ of FE), we only expect a small contribution from multiple scattering at each plane. Due to the deviations at small angles, the angular dispersion can be modelled with a Gaussian distribution function. The multiple scattering angle $\theta_{scattering}$ can be therefore defined as the RMS of the angular dispersion of incident particles after traversing x thickness of material [92]:

$$\theta_{scattering}[rad] = \frac{13.6}{\beta c p} z e \sqrt{x/X_0} \left[1 + 0.038 \ln \left(\frac{x}{X_0} \right) \right]$$

---

[6]Where (x,y) are the local modules coordinate system.

Accelerator	Particle	Momentum [GeV/c]	$\theta_{scattering}$ [mrad]	σ_s [μm]
PS	protons	15	0.01	1
SPS	pions	180	0.15	15

Table 7.1 – Test-beam accelerators facilities used at CERN and the particles present in the beams. The momentum, particle types, and the equivalent scattering angles ($\theta_{scattering}$) at each FE plane are reported, together with the expected error due to multiple scattering extrapolated for a plane-to-plane distance of 100 mm.
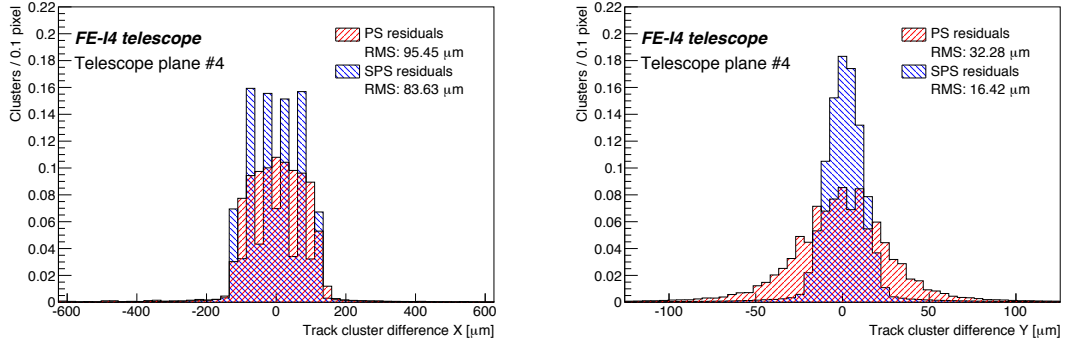
Figure 7.11 – Comparison of the PS and SPS hit to track normalised unbiased residual distributions for plane #4 showing the effect of multiple scattering in X (left) and Y (right) axis.

where p is the momentum, ze the charge of the incident particle, x the plane thickness and X_0 the radiation length. The X_0 of the material is an intrinsic property of the plane and can be approximated by the formula [3]:

$$X_0 = \frac{716.4A}{z(z+1)\ln(287/\sqrt{Z})}$$

$$X_{0,Silicon} = 9.36 \text{ cm}$$

Although the HV-CMOS analysis results presented in section 7.4.3 have been obtained with pions of 180 GeV/c at SPS, previous data were taken at PS with protons of 15 GeV/c. A comparison of the expected multiple scattering is shown in Table 7.1.

With a distance between the telescope planes of $\sim$100 mm and scattering angles at the SPS of the order of 0.01 mrad, the expected hit deviation[7]. Since the telescope single-cluster resolution ($\sigma_{r,x} \times \sigma_{r,y}$) is of 72.17 μm $\times$ 14.43 μm the multiple scattering can be safely neglected and straight tracks can be assumed at the SPS test-beam.

The impact of multiple scattering increases at low beam-energies. As can be seen in Figure 7.11, the measured unbiased Y-residual RMS at the SPS are of $\sim$84 μm and $\sim$16 μm in X and Y, matching the single hit resolution of $\sigma_{r,x}$ =72.2 μm and $\sigma_{r,y}$ =14.4 μm, and therefore excluding almost any multiple scattering as expected.

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[7]Since the track displacement due to multiple scattering increases linearly with the plane to plane distance [93] due to multiple scattering is of the order of 1 μm, low energy test-beam will have a smaller plane to plane distance (compact geometry) versus higher energy beams to maximise the telescope resolution.

(a)

(b)
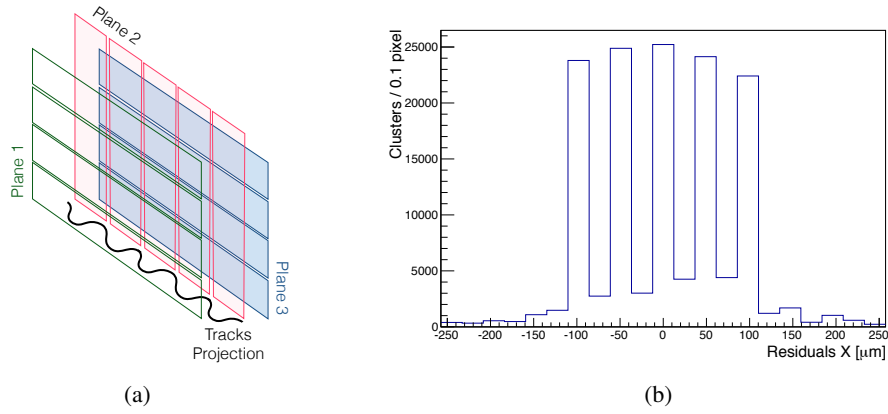
Figure 7.12 – Figure 7.12(a) shows a schematic view of the pixel stack of a telescope arm. The reconstructed tracks probability function along the X axis is schematically represented in black. Event simulation using the Allpix code [94] have been run to reproduce and understand such behaviour. Obtained unbiased residuals along the X axis (7.12(b)) show the $50\,\mu$m pattern arisen from the pixel geometry.

Due to the large pixel size in x and the small plane to plane distance, a clustering effect of the tracks every $50\,\mu$m can be observed, as shown in Figure 7.11(a). This effect arises from the rotated planes, where the high resolution $50\,\mu$m pixel space points dominates the track reconstruction. This effect is amplified in the X axis since only two planes provide a higher resolution measurement (rotated planes) and therefore can strongly bias the linear fit. This effect was reproduced by a simulation, the results of which are as shown in Figure 7.12.

The influence of the clustering effect on the telescope resolution and alignment has not been studied in this thesis.

7.3.3 Resolution of the Six-Plane FE-I4 Telescope

The telescope resolution, defined as the pointing resolution at the DUT location, has been estimated by the track linear-fit error propagation. As explained previously, the planes misalignment and multiple scattering uncertainties haven't been included in the cluster uncertainties. However, their contribution are absorbed in the fit parameter uncertainties[8].

In our case where each of the six planes provides a measurement on each of the coordinates, and given that the track has 4 variables to be determined, the number of degrees of freedom ($ndof$) of the track fit is:

$$N_{ndof} = (2 \times n_{planes}) - 4 = (2 \times 6) - 4 = 8$$

The distribution of the total $\chi^2/ndof$, calculated as a sum of the χ^2 in the horizontal and vertical planes can be seen in Figure 7.13(a), showing a most probable value consistent with one.
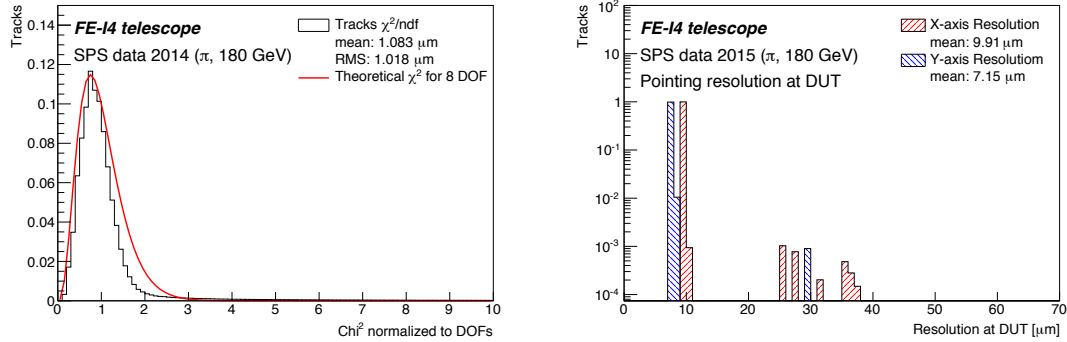
The telescope pointing resolution at a given position z along the beam-axis is given by:

$$\sigma^2_{(x,y)}(z) = o^2_{(x,y)} + z^2 s^2_{(x,y)} + 2zC_{(x,y)}$$

where $o_{(x,y)}$ is the track origin uncertainty and $s_{(x,y)}$ the slope uncertainties for x and y. $C_{(x,y)}$ is the covariance matrix of the track parameters.

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[8]The absorption of the alignment systematic uncertainties requires an uncorrelated systematics between data points.

The telescope pointing resolution for selected tracks passing the cuts in Table 7.2 at the DUT Z position for both axis is shown in Figure 7.13(b).

Figure 7.13 – $\chi^2/ndof$ for reconstructed tracks with six clusters (left). Theoretical $\chi^2/ndof$ for 8 degrees of freedom is overlaid showing reasonable agreement. Obtained telescope pointing resolution at DUT Z position during SPS test-beam (right). The obtained pointing uncertainties are obtained from the uncertainties on the fitted parameters (see text). Tracks containing multi-hit clusters present larger uncertainties as expected from the digital clustering.

Variable & cut
Maximum track slope in pixels per plane = 25
Minimum number of planes needed to form a track = 6
Maximum sigma deviation of a cluster from previous cluster = 50
Maximum χ^2 value of the accepted tracks = 2

Table 7.2 – Table summarising the main track parameters used during the track reconstruction and test-beam analysis.

7.4 High-Voltage CMOS Sensor Development

Due to the increasing surface and granularity of silicon detectors, new cost-effective technologies need to be explored for the future HL-LHC ATLAS upgrade. The High-Voltage CMOS (HV-CMOS) is a sensor technology under R&D, based on commercially available manufacturing processes that allow the implementation of low-cost, low material budget and high radiation tolerant detectors. The HV-CMOS characteristic with respect to standard detector diodes is that part of their electronics is embedded in the detector bulk, allowing an in-pixel signal processing, so called "Smart Diode" Array (SDA).

7.4.1 The High-Voltage CMOS Detector

The HV-CMOS sensor is based on a multiple-well structure (see Figure 7.14). A deep n-well acting as a charge collecting electrode is placed in the p-substrate and hosts the pixel electronics. The PMOS transistor are directly implemented in the deep n-well while NMOS transistors are embedded in secondary p-wells in the deep n-well. P-implants rings around the pixels provide a biasing grid for sensor depletion significantly simplifying the design (single-side process).
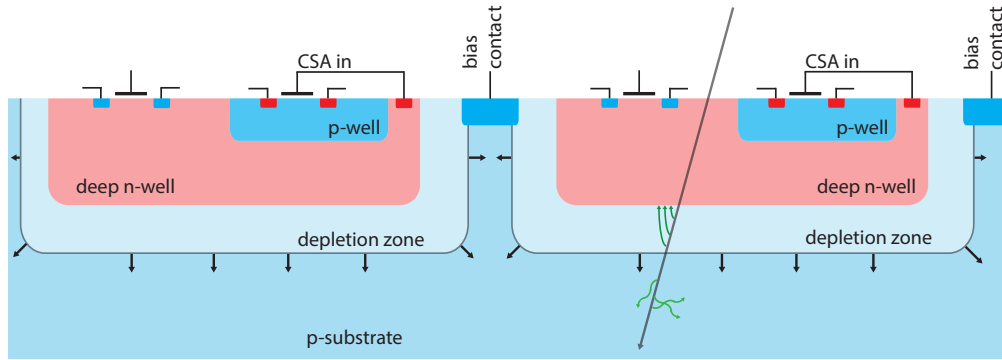
Figure 7.14 – Schematic view of the cross section of an HV-CMOS, showing two consecutive pixels. For each pixel a deep n-well (in light red) is implemented in the p-substrate (in light blue) and hosts the NMOS transistors. PMOS transistors are imbedded in the p-well (in blue), isolated from the bulk by the deep n-well. P-implant rings provide a biasing ring around individual pixels. An ionising particle particle is schematically represented with its charge deposition collected by drift in the depleted zone towards the deep n-well and by diffusion elsewhere.

In order to decrease the pixel capacitance induced by the large pixel size, a substrate with a resistivity of 20 Ωcm was used[9]. Standard 180 nm HV-CMOS process provides a technology suitable for the particle physics application, safely allowing bias voltages up to 60 V.

The use of a commercial available process allows a cost reduction with respect to a custom sensor design, from the achievable high volume production and the expected high yield.

7.4.2 The AMS 180 μm v4 High-Voltage CMOS Detector

The H18 process of the Austria Micro Systems (AMS) foundry provides 180 nm High Voltage CMOS technology. With its high level of digital integration (up to 118 kgates/mm^2) [95], it matches the embedded pixel electronics requirements.

The proposed hybrid detector uses the FE-I4 pixel readout electronics while replacing the standard diode-like pixel matrix sensor by an HV-CMOS SDA. In order to increase the detector granularity, each of the FE pixels reads-out up to three HV-CMOS pixels (sub-pixles). Discrimination between different sub-pixels can be achieved by their different signal amplitude (charge encoding) via the individual tuning of the charge amplification of the HV-CMOS pixels.

For research purposes, several prototypes have been studied. The results presented in Section 7.4.3 cover the latest HV-CMOS prototype version (as of the moment of writing), namely the so called HV2FEI4 v4. With a matrix size of 1.5×5.33 mm^2, the v4 contains four pixel flavours implementing various optimisations for testing purposes. Although four different pixels flavours were included in the v4 to test different amplification stages, low noise levels and discriminators, only *S-Time* and *Analog* pixels will be discussed.

The results presented in the following section are for the $S\text{-}Time$ pixels. The pixel matrix consists of 12×30 sub-pixels of $125\,\mu$m $\times\,33\,\mu$m consisting of a charge sensitive amplifier combined with a two stage discriminator (Figure 7.16). Since charge encoding was not feasible due to the limited tuning performance achieved with the current HV-CMOS, a sub-pixel encoding couldn't

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[9]Higher substrate resistivities are under consideration in order to increase the depletion region and thus improving the signal-to-noise ratio.
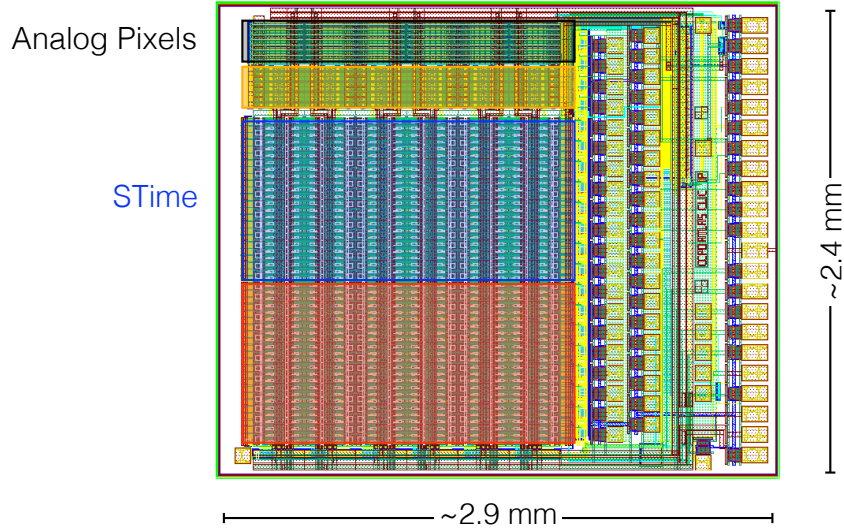
Figure 7.15 – Picture of the HV2FEI4 v4 overlaid with the different pixel flavours matrixes.
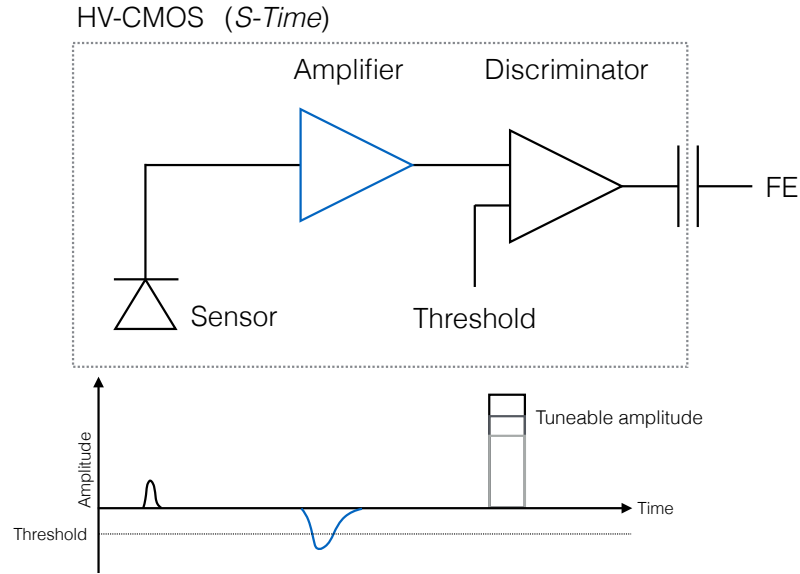

Figure 7.16 – Schematic representation of the $S\text{-}Time$ HV-CMOS embedded pixel electronics (top) and signals (bottom). The sub-pixel charge encoding can be achieved by the tuneable amplitude signal of the discriminator output.

be achieved during standard data taking throughout the FE-I4. Therefore, the following test-beam reconstruction and analysis was performed by merging FE pixels to match the HV-CMOS pixel unit cell, to a total of $6{\times}10$ units-cell ($250\,\mu\text{m} \times 100\,\mu\text{m}$), each composed of six sub-pixels. Sub-pixels inside each unit cell are connected by columns, read out by the FE pixels as can be seen in Figure 7.17.
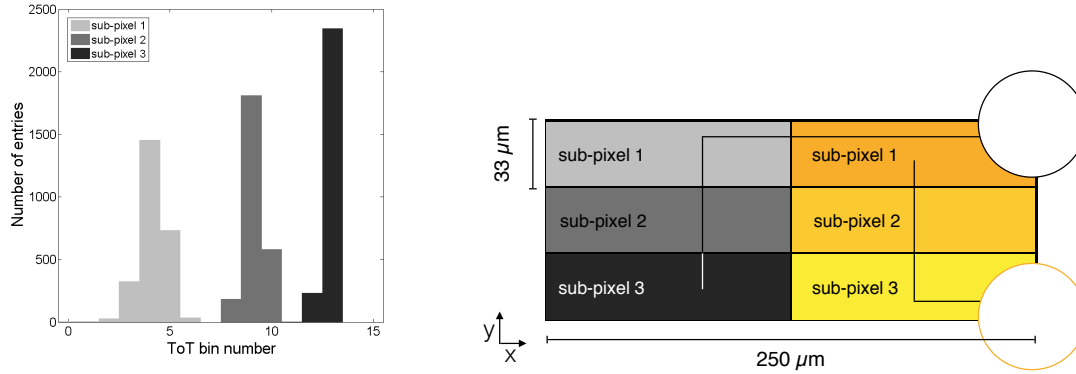
Figure 7.17 – Charge sub-pixel encoding of HV-CMOS pixel address using the embedded amplifier. The ToT spectrum of one FE-I4 pixel shows three distinct peaks corresponding to the three sensor sub-pixels connected to the readout pixel (left). In the right figure is shown a schematic drawing of the unit cell arrangement and signal routing of a v4 HV-CMOS.

In order to simplify the module assembly and to reduce even further the production cost, the sensor and the FE are capacitively coupled (Capacitive Coupled Pixel Detector, CCPD) by means of a layer of epoxy glue of approximately $5\,\mu$m-thickness avoiding the bump-bonding. This is achieved via the embedded electronics in the HV-CMOS pixels amplifying the signals (see Figure 7.18).
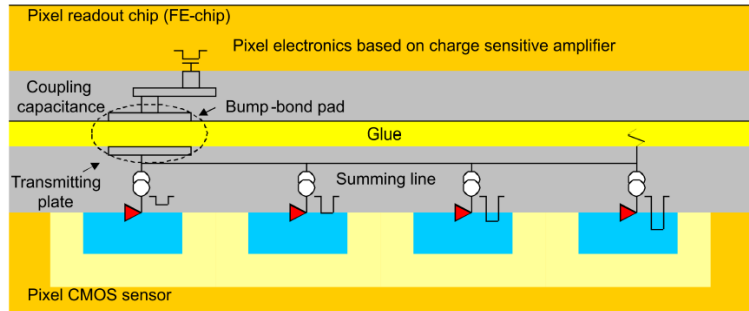
Figure 7.18 – Pixel cross section of a glued hybrid detector concept using capacitive signal transmission between combined HV-CMOS pixels and the FE electronics.

An HV2FEI4 glued to an FE-I4 and wire-bonded to the testing PCB is shown in Figure 7.19.

7.4.3   AMS 180 μm v4 Test-beam Results

The AMS HV-CMOS v4 (HV2FEI4 v4) was extensively tested during the November 2014 test-beam at the SPS H8 area (CERN) with a pion beam (Figure 7.20) of 180 GeV (max Δ p/p$\simeq \pm2\%$) and more than 6 billion triggers recorded. Two v4 samples were tested under a wide range of operation settings allowing the understanding of the HV-CMOS efficiency and time performance, an non-irradiated (**402**) and a neutron irradiated sample (**404**) to 10^{15} neq/cm^2.
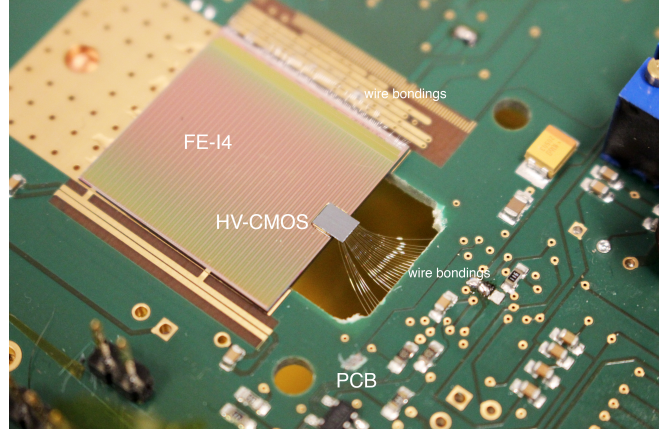
Figure 7.19 – HV-CMOS v4 sample glued to the large FE-I4 and wire bonded to the PCB.
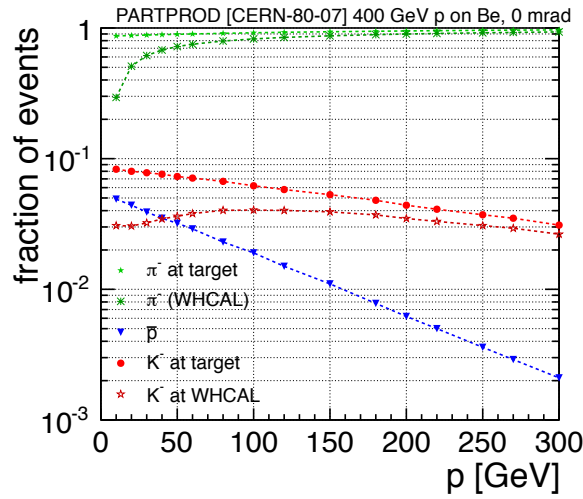
Figure 7.20 – Expected particle content for secondary beams produced from collisions of 400 GeV protons with a Beryllium target at 0 mrad production angle. The expected particle content at the DUT location measured thanks to the CALICE Tungsten Analog Hadronic Calorimeter prototype (W-AHCAL surface, z=605 m) is also given, taking into account in-flight decays of pions and kaons [96].

Detector efficiencies have been computed by matching the reconstructed tracks for each trigger to the DUT hits, as following explained. In order to cope with misalignment and track reconstruction uncertainties an acceptance region (d) was defined, such that the DUT hits within a given area surrounding the reconstructed track was associated to the particle (i.e. interpreted as a real particle hit). Due to the DUT unit cell geometry of $250 \times 100\,\mu\text{m}^2$ ($p_x \times p_y$)the acceptance region used for the cluster-to-track association was an ellipse given by:

$$d = \sqrt{\left(\frac{x_{track} - x_{cluster}}{p_x/2}\right)^2 + \left(\frac{y_{track} - y_{cluster}}{p_y/2}\right)^2}$$

where $x(y)_{track}$ is the interpolated track position at the DUT Z location and $x(y)_{cluster}$ is the DUT cluster position. In order to accommodate the alignment and track uncertainties a distance $d < 1.5$ pixels was required in order to have a HV-CMOS cluster associated to the telescope track[10].

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[10]This distance parameter d was optimised thanks to the efficiency study of an IBL module known to be efficient at

The efficiency ϵ for each individual pixel is defined as:

$$\epsilon = \frac{N_{matched}}{N_{total}}$$

where for a given pixel $N_{matched}$ is the number of matched clusters-to-tracks and N_{total} the total number of reconstructed tracks passing through it. The accuracy of this efficiency measurement relies on a low DUT noise occupancy, avoiding fake cluster-to-track association pulling up artificially the measured efficiency. Due to the small DUT size compared to the beam spot, a uniform pixel occupancy is expected and therefore pixels with an occupancy five times higher than the average were masked as noisy pixels.

The DUT alignment was particularly challenging due to the small DUT size and large pixel size of $250 \times 100\,\mu m^2$. Although the obtained x and y residual distributions of the analysed samples are centred at 0, the obtained RMS of $\sigma_{DUT,x} \approx 145\,\mu m$ and $\sigma_{DUT,y} \approx 85\,\mu m$ show significant discrepancies with respect to the predicted RMS from the unit cell sizes and the telescope pointing resolution as seen in Figure 7.21 (being the expected $\sigma_{DUT,x} \approx 80\,\mu m$ and $\sigma_{DUT,y} \approx 35\,\mu m$). The increased residuals RMS points to a misalignment between the DUT and the telescope, particularly to a rotation. In order to align the small DUT with higher precision, a new alignment algorithm based on Least Squares Fits would need to be implemented [97]. Due to time constraints, this new alignment procedure already under development hasn't been implemented in the analysis described here.
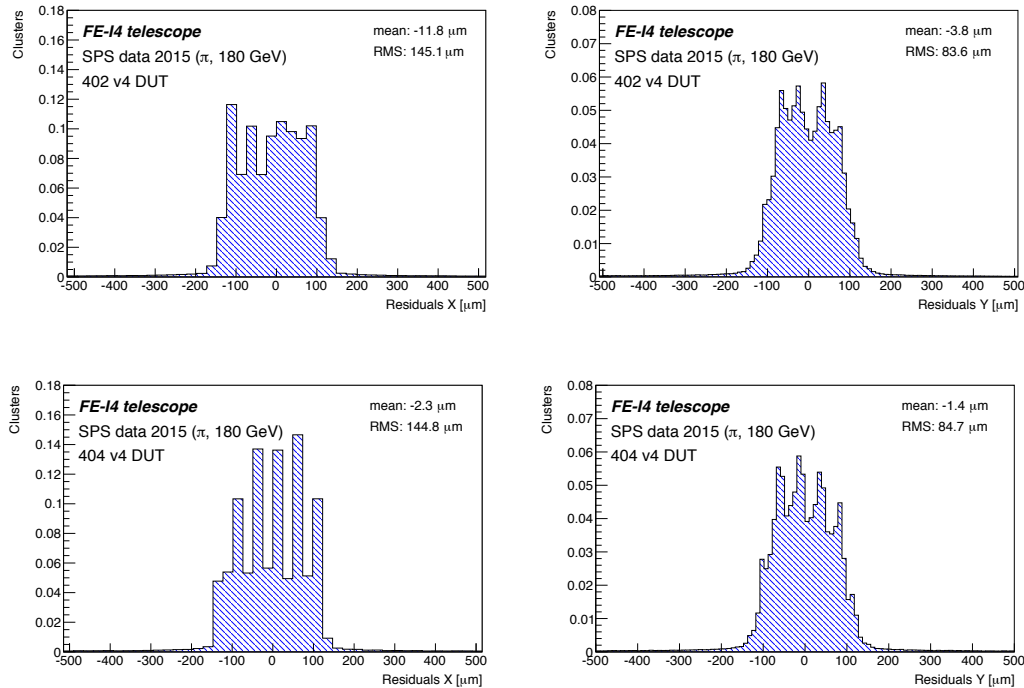

Figure 7.21 – Residual distributions on X (left) and Y (right) for the analysed HV-CMOS samples 402 (top) and 404 (bottom). The large RMS obtained with respect to predicted ones is due to the DUT misalignment described in the text.

99.9%. A cluster-to-track association distance of $d = 1.5$ was found to be the smallest working point without compromising the efficiency.
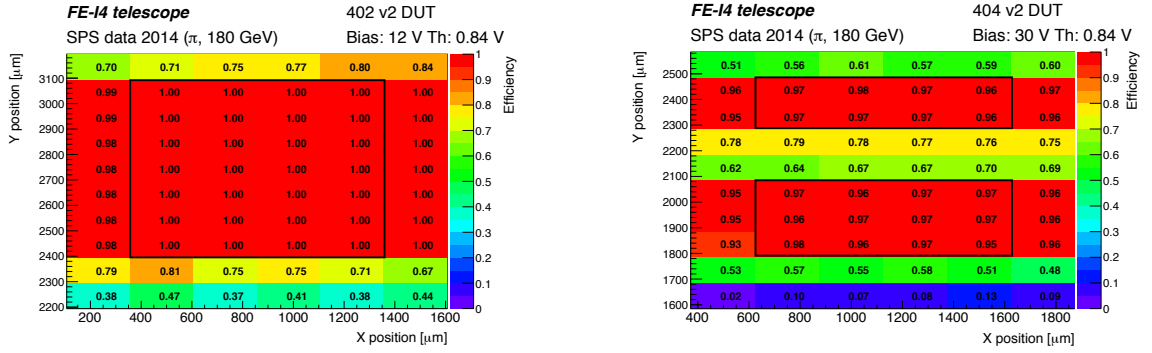
Figure 7.22 – Efficiency map of the HV-CMOS v4 *S-Time* pixels for non-irradiated (left) and irradiated to 10^{15} neq/cm^2 (right) samples. Global efficiencies (402: 99.7 % and 404: 96.2 %) are calculated in the highlighted regions, excluding edge pixels to cope with the reconstruction uncertainties. Although sample 404 was fully operational, during data taking two rows were mis-tuned and therefore excluded for the efficiency computation.
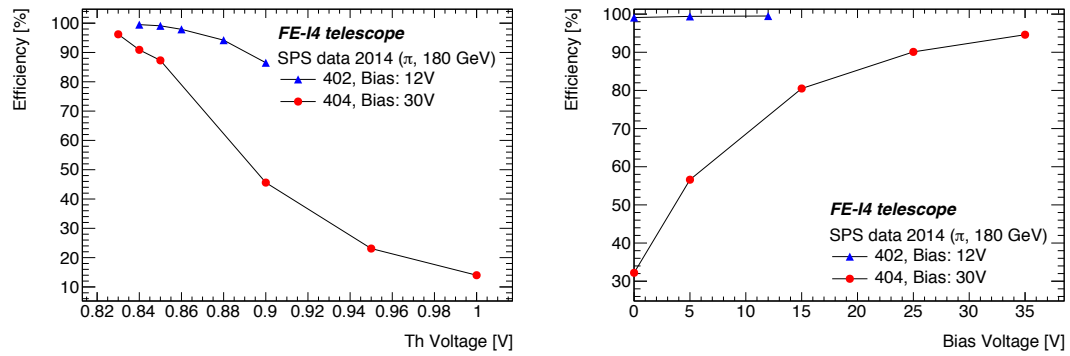
Figure 7.23 – Global efficiency as a function of the threshold (left) and bias voltage (right) for v4 standard pixel.

The efficiencies obtained for the standard v4 pixels before (402) and after irradiation (404) operated with a "noise tuning" of 0.84 V show a flat efficiency over the pixel matrix (Figure 7.22). The global efficiency[11] for the non-irradiated sample is 99.7 % at 12V bias voltage and 96.2 % after irradiation at 35 V bias voltage.

Bias and threshold scans have been performed as shown in Figure 7.23. The non-irradiated sample (402) shows high efficiencies even at very low depletion voltages, as expected from diffusion and the n-in-p build in voltage of the HV-CMOS diode. For the irradiated sample, due to the reduced diffusion component[12], mostly drifting charges are collected and therefore, the efficiency increases with the increasing depletion zone as can be seen in Figure 7.23. Due to a defect in the 404 sample, biasing voltages couldn't exceed 35 V and therefore the efficiency plateau wasn't reached.

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[11]The global efficiency is calculated as the average of the single pixels efficiency excluding edge pixels due to reconstruction ambiguities.

[12]As discussed in chapter 3, due to irradiation, defects induced in the silicon crystal act as charge traps capturing the slow diffusing carriers and largely reducing the diffusion component.

Thanks to the pointing resolution of the telescope and the high statistics, a sub-pixel resolution could be achieved merging the data from all pixels. Figure 7.24 shows the "in-pixel timing" defined as the average hit timing in BC units of 25 ns. As observed, the non-irradiated sample presents a double column structure with later events at the sub-pixels edges. After irradiation a uniform in-pixel timing is seen. The discrepancy between the two results points to the presence of a diffusion component before irradiation, where signals generated in the undepleted pixel boundaries (Figure 7.25) are collected by diffusion producing therefore slower and smaller signals. After irradiation, due to charge trapping, the diffusion component is strongly suppressed and therefore its effect is not longer visible.

Charge collection time via diffusion being of the order of the ns, the observed timing dependance indicates the presence of a time-walk on the HV-CMOS discriminator. The time-walk effect is schematically shown in Figure 7.26, where low amplitude signals (such as those produced by diffused collection) have later trigger time due to the slower discriminator raising time. The timing improvement at lower thresholds (Figure 7.27) indicates a time-walk effect. On top of the timing shift, it is particularly interesting to notice the decrease of the number of late hits (above 10 BC) for higher thresholds in the non-irradiated sample. This decrease confirms the presence of very low amplitude signals (i.e. late events) from diffusion that couldn't reach the higher thresholds.
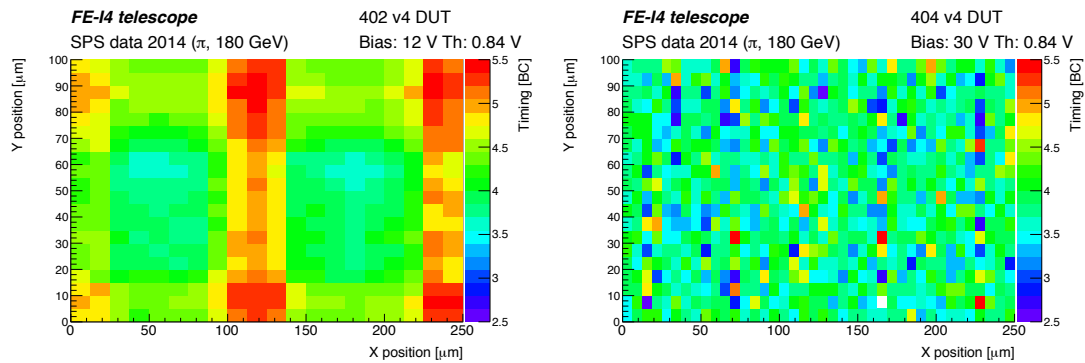

Figure 7.24 – In-pixel average timing (in ATLAS Lv1 bunch crossings of 25 ns) distribution for the non-irradiated (left) and the irradiated (right) samples. Edge effects before irradiation can be correlated to an undepleted bulk in the pixels edges.
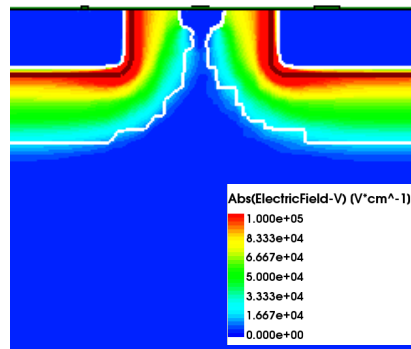
Figure 7.25 – Distribution of the absolute value of the electric field within pixels for a silicon substrate of 20 Ωcm and a HV bias of - 50 V. The boundaries of the depletion zones growing from each pixel electrode are indicated in white.
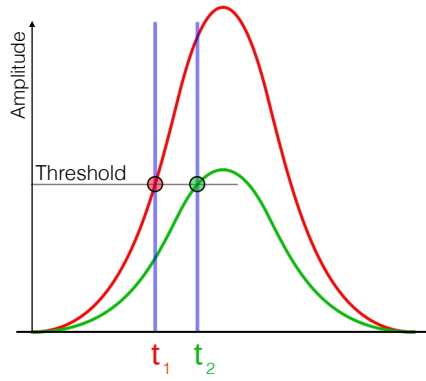
Figure 7.26 – Schematic representation of different amplitude signals and the time walk effect due to a simple threshold triggering in the discriminator
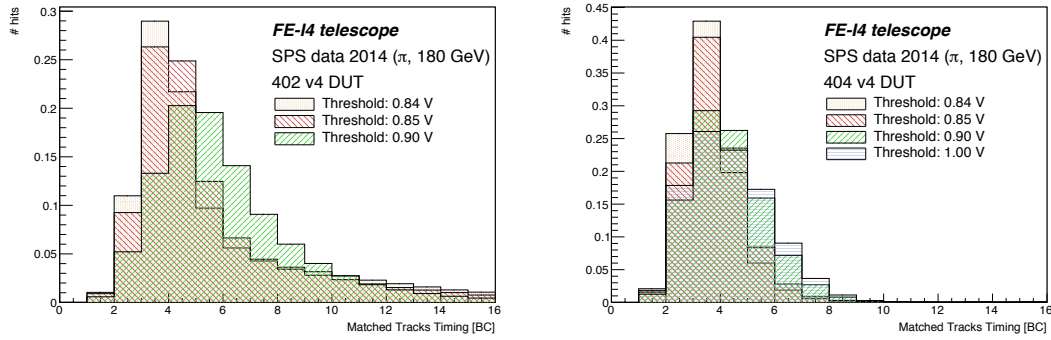

Figure 7.27 – Normalised occupancies as a function of the Lv1 trigger at different thresholds for non-irradiated (left) and irradiated (right) samples. Timing improvement at low thresholds indicate the presence of a time walk effect. The diffusion component is strongly suppress after irradiation as observed from the tail distribution difference between before (left) and after irradiation (right).

Additionally, in order to independently test the amplification stages of the HV-CMOS, the *Analog* pixels were tested. With a pixel size of $50 \times 250\,\mu m^2$, these pixels are composed of a two-stage amplification, providing the correct signal polarity to the FE without a discriminator (Figure 7.28). The output amplitude is therefore proportional to the collected charge, so is the measured ToT on the FE. This enabled the study of the dependence of the electronics as a function of the signal amplitude otherwise inaccessible due to the pulse shaping of the discriminators.

As observed in Figure 7.29 a clear dependence between the Lv1 timing and signal amplitude (ToT) is measured at the FE level for Analog pixels. This timing dependence, although present for standard pixels, is not correlated to the signal amplitude due to the presence of the discriminator at the HV-CMOS level (constant output signal). The FE-I4 being designed for LHC operation has a time-walk specification of $\sim 20\,ns$ (Section 4.2.1). Therefore the observed time-amplitude dependency is directly induced by the HV-CMOS amplification stage.

The timing performances are therefore found to be unsatisfactory in the v4 version, because of the HV-CMOS discriminator time-walk and the slow response of the amplification stages. Given the results shown in this thesis, a new HV-CMOS prototype version with a time-walk compensator and a fast amplifier has been produced and is presently under test.
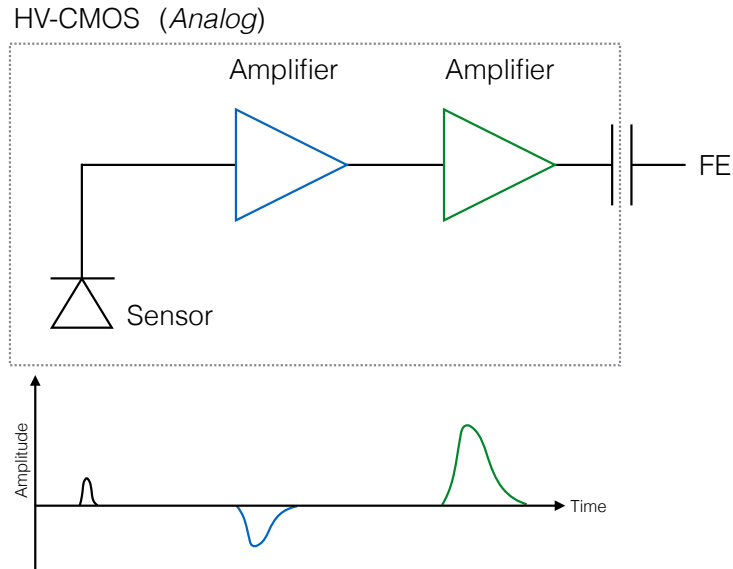
Figure 7.28 – Schematic representation of the *Analog* HV-CMOS embedded pixel electronics (top) and signal (bottom).
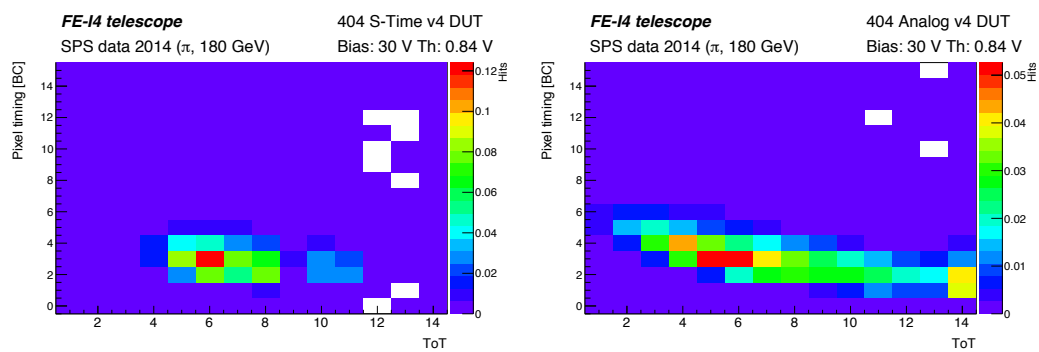
Figure 7.29 – Normalised distributions of the pixel timing versus ToT for *S-Time* (left) and *Analog* (right) pixels.

CHAPTER **8**

Conclusion

The IBL detector, required to guarantee the physics performances of the ATLAS pixel detector during the data-taking of the coming years. The IBL has been the first major ATLAS upgrade introducing several novel pixel sensor technologies at the LHC. With the introduction of the new 3D and planar slim-edge sensor designs, a new step-forward in high efficiency and radiation hard sensors has been achieved. Additionally to the sensor design, the new FE-I4 Front-End electronics had been installed to cope with the challenging occupancies expected during Run-II and the new pixel granularity of $250 \times 50 \, \mu m^2$.

The first part of this thesis is devoted to the work performed for the production of the IBL staves. With a major contribution to the stave loading and Quality Assurance performed at the University of Geneva, more than 450 modules had been tested for loading and a total of twenty staves were produced in the timeframe of one year. Additionally to the loading, a rework procedure was developed allowing the replacement of the modules and the rework of the staves, a critical step in order to guarantee fully functional staves. The staves loading and rework procedure success represents an important experience for future detector integration with "stave-like" structures, where modules need to be placed on the staves with limited replaceability.

Loaded staves were extensively tested at the University of Geneva and CERN following a stricts characterisation and qualification procedures. The obtained quality results outperformed the original IBL specifications. In total, fourteen staves were selected for final integration based on their ranking and with a final failing pixels fraction of 0.09 %. During its integration around the IPT, the detector behaviour has been monitored thanks to the developed connectivity test setup. This allowed to verify that no damage was produced to the detector at any step as well as the commissioning of the installed services. Due to the encountered connectivity problems with the AXON connector and their non rework-ability after installation, an additional Quality Assurance step was implemented. All connections performed after the Quality Assurance were tested successfully, a critical step for the detector installation. Finally, the first IBL test in the cavern was performed, delivering a fully functional detector for final commissioning within ATLAS.

The second part of this thesis focuses in the characterisation of new HV-CMOS v4 prototypes for the High Luminosity LHC. The FE-I4 telescope was designed and constructed by the University of Geneva group fully exploiting the acquired experience during the IBL construction

and became operational in less than six months showing high trigger rate capabilities and a very robust data-taking. The analysed data allowed the characterisation of HV-CMOS v4 irradiated (10^{15} neq/cm^2) and non-irradiated prototypes, with obtained efficiencies of 96.2% and 99.7%, respectively. The detailed studies of the sensor performances presented in this thesis allowed the implementation of new circuitry and various design optimisations for the new HV-CMOS prototype versions.

Modules Qualification

Test Name	Test Purpose	Test stage
Sensor current vs. applied bias voltage	Sensor operability and reference characteristics measurement	Q, F
Power-up test	Chip supply voltage and current test	W, Q, F
Shunt-LDO I/V scan	Shunt-LDO warm/cold calibration and functionality test	Q, F
Generic ADC test	Generic ADC warm/cold calibration and Shunt-LDO calibration verification	W, Q, F
Sensor bias ON	Ramp-up of sensor depletion bias	Q, F
Digital test (high threshold)	Pixel read-out chain functionality	W, Q, F
Module tuning	Multi-step threshold and feedback current adjustment (global and pixel level)	Q, F
Digital test (operation threshold)	Pixel digital read-out chain functionality	W, Q, F
Analog test (operation threshold)	Pixel analog read-out chain functionality	W, Q, F
Threshold and noise measurement	Threshold and noise (ENC) measurement	Q, F
ToT verification at the charge of $16\,000\,e$ (MIP)	Charge measurement verification	Q, F
Crosstalk test	High analog charge injection for inter-pixel crosstalk test	Q, F
t_0-tuning	Injection timing fine adjustment	F
In-time threshold measurement	Threshold for hit detection within single bunch crossing measurement	F
ToT calibration	Full range ToT to charge calibration	F
Noise occupancy measurement	Noise hit probability at operation threshold and noisy pixel masking	F
Source scan	^{241}Am high statistics source scan for bump connectivity test	F
Low threshold operability test	Noise occupancy as function of threshold measurement	F
Sensor bias OFF	Ramp-down of sensor depletion bias	Q, F
Threshold and noise measurement	Threshold and noise (ENC) measurement with undepleted sensor to detect bump failures	Q, F

Table A.1 – Test flow of the electrical test during wafer testing (W), after module assembly (Q) and the intense module functionality and performance validation test (F).

| **Mechanical issues**	
missing glue in wing area	100
re-bond of wire bonds (FE, bridge, HV)	10 times # of re-bonds 50
excess of glue on sensor edges	50
chip re-work	100
damage on module edges	50
Sensor Properties	
breakdown voltage change during assembly (yellow cut)	100
breakdown voltage change (red cut)	1000
non visible alignment marks	50
non visible alignment marks (> 2)	1000
Electrical Performance	
mean noise out of range (yellow cut)	50
width of tuned threshold distribution (yellow cut)	50
regulator output voltages out of range (yellow cut)	50
mean noise, threshold disp., regulator output (red cut)	1000
HV capacitor potting removed/thinned	30
Re-work of the reset capacitors	100
minimal operational threshold $> 1,500$e-	50

Table A.2 – Penalties in numbers of bad pixel for IBL modules.

Integrated Staves Test Results

Qualification and performances results of the fourteen loaded staves:
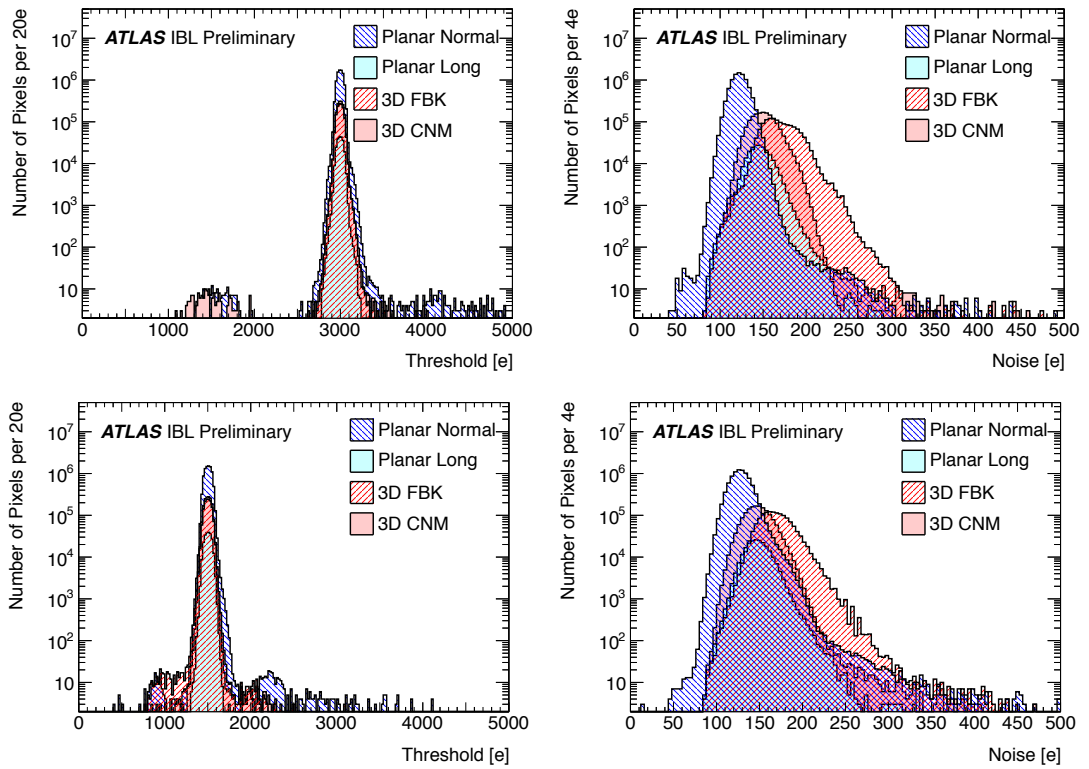
Figure B.1 – Threshold and noise distributions on integrated staves after tuning to a threshold target of $3000\,e^-$ at $20\,°C$ (top) and $1500\,e^-$ at $-12\,°C$ (bottom). The small peak around $2150\,e^-$ on the planar normal pixels is an artefact of one mask step in the threshold scan, where noisy pixels bias the s-curve. By redoing the threshold scan and injecting in less pixels per mask step, the incorrect measurement can be avoided, but for this particular chip it was not done due to time constraints. The bump around $300\,e^-$ on the 3D FBK noise is caused by a small noise on the HV line of the setup and the sensitivity of FBK modules to such noise.
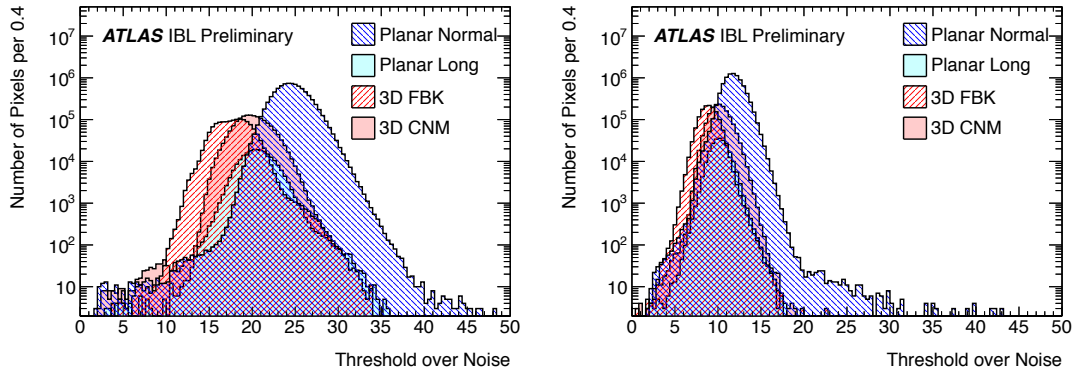
Figure B.2 – Threshold over noise distribution of pixels on integrated staves for 3000 e^- (left) and 1500 e^- (right) 1threshold tunings at 22 °C and −12 °C module temperatures, respectively.
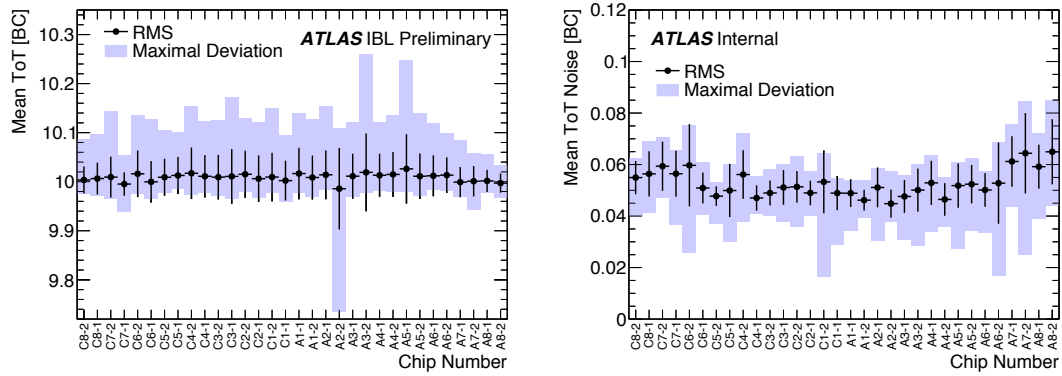
Figure B.3 – Modules average (left) and noise ToT (right) distribution on integrated staves as a function of chip number. Noise ToT is defined as the RMS of the obtained ToT distribution after 50 injections.
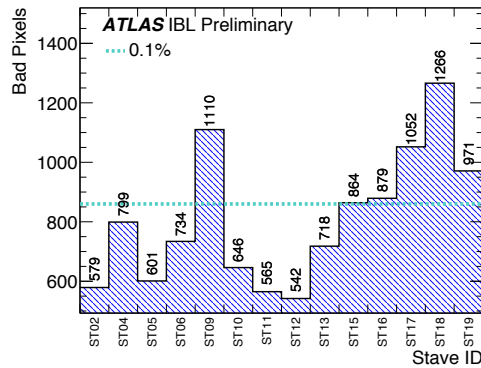
Figure B.4 – Number of bad pixel per stave for all integrated staves. Bad pixels fraction of 0.1% and 0.2% are shown in dashed lines.

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