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Implementation of the first level trigger for the auger observatory surface array

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Abstract. The surface array of the Pierre Auger Observatory will consist of 1600 water Cherenkov detectors spread over 3000 km^2. The remote location of the water tanks and the consequent lack of affordable conventional AC power sources or communications links necessitates reliable low power electronics and trigger logic at each tank. Trigger algorithms, operating within each surface detector, have been developed to suppress lower energy cosmic ray showers and retain the high energy showers of interest. A design approach using both programmable logic devices (PLDs) and custom application specific integrated circuits (ASICs) has been utilized to address delivery schedule, power consumption, functionality, and cost goals. This paper discusses the trigger algorithms and describes the implementation of those algorithms in PLDs and ASICs. Experience in the field is discussed.

1 Introduction

The Pierre Auger Observatory surface array will consist of 1600 water Cherenkov detectors spread over 3000 km^2 (Dova, 2001). Each detector station contains a tank of pure water (Escobar, Filevich, and Mazur, 2001; Salazar, Nellen, and Villaseñor, 2001), instrumented with low power electronics (Suomijärvi, 2001) powered by solar panels. The station electronics communicates with the observatory campus via a custom radio network (Clark and Nitz, 2001).

Cherenkov photons produced when cosmic ray secondaries in the shower front traverse the water are recorded by three downward facing photomultiplier tubes (PMTs) situated at the top of the water. A low and high gain signal from each PMT is sent to front end electronics, which conditions the signals before digitizing them. Each 25 ns the outputs of 6 10-bit analog to digital converters (ADCs) are presented to the trigger/memory circuitry. The high and low gain outputs have a factor of 32 gain difference, which increases the nom-

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inal dynamic range to 15 bits.

The trigger/memory circuitry evaluates the high gain output of each PMT every 25 ns for interesting trigger patterns, stores the data in buffer memory, and informs the detector station micro-controller when a trigger occurs.

The station controller reads triggered events from the trigger/memory circuitry. It sends trigger packets, and when requested, event data to the observatory campus via the wireless network.

A hierarchical event trigger is used (Nitz, 1997) to select events of interest and reject uninteresting events, while keeping within the rate constraints imposed by the station micro-controller, the communications link bandwidth, and the central data acquisition system. The trigger/memory circuitry generates a first level trigger based upon hardware analysis of the high gain PMT channel waveforms. The station controller imposes additional constraints in software to generate a level 2 trigger. A level 3 trigger is formed at the observatory campus based upon the spatial and temporal correlation of the level 2 triggers. Once the data has been read from the detector stations, additional constraints are applied in forming a level 4 trigger at the campus.

2 Level 1 Trigger Philosophy

The goal of the first level trigger is to trigger efficiently on UHE cosmic ray air showers of $> 10^{19}$eV, while simultaneously rejecting lower energy showers and minimizing composition dependent trigger biases, within a rate constraint of 100 Hz.

Two principle characteristics of the shower waveforms are employed in the level 1 trigger: 1) On average, for any fixed number of Cherenkov photons detected, those from higher energy showers will be more dispersed in time than those from lower energy showers; and 2) the Cherenkov signals from electrons and photons in the shower are (usually) smaller than those of muons. The first property is a reflection that a fixed energy contour will be farther from the shower core in
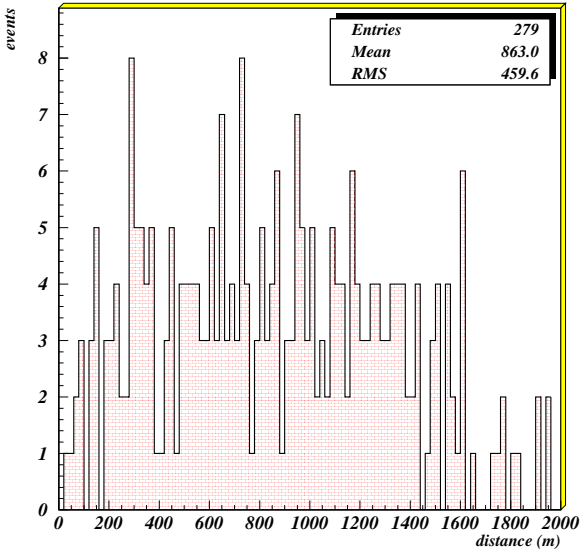
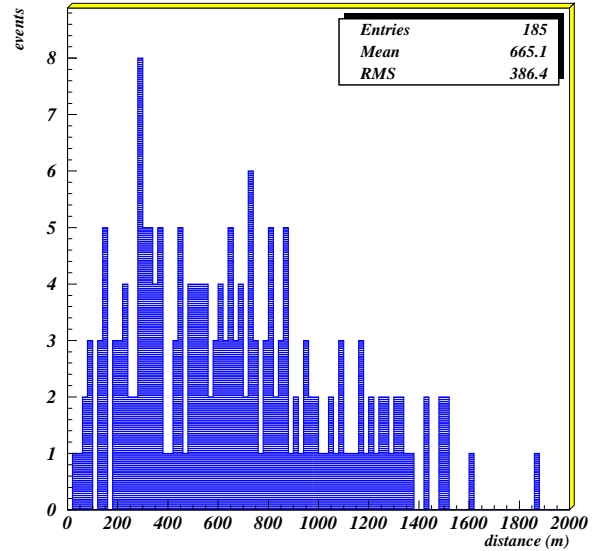**Fig. 1.** Distance to core of AGASA events, low threshold, wide occupancy

Fig. 2. Distance to core of AGASA events, high threshold, low occupancy.

a larger energy shower. The second reflects that the typical energy of muons at the observation level is higher than that of photons and electrons.

Thus we arrive at 2 basic conditions for our shower trigger. Requiring that the observed signal be extended in time will bias the trigger against lower energy showers. Employing a low pulse height threshold will minimize composition bias by reducing the trigger dependence on muon content, since the muon content is strongly correlated with the primary composition.

However, the time dispersion of the signals is reduced for inclined showers, and we must be careful not to reject them in our desire to be insensitive to lower energy showers.

We have implemented a basic shower trigger which incorporates these features as follows. A running sum is kept of the number of 25 ns time bins that the high gain PMT signal is above a specified threshold, within a sliding window of specified width. If this sum exceeds a specified number, a trigger is generated.

Multiple instances of the trigger allow one to formulate a final level 1 trigger which encompasses various shower types of interest.

The trigger conditions have been studied both via simulation and by analysis of data taken with an Auger test tank situated in the AGASA array (Ghia and Navarra , 2001). The simulation studies are described in Ref. (Meyhandan, Matthews, and Nitz, 2001).

The test tank was triggered by AGASA, and the reconstructed parameters of each shower (energy, core position, etc.) have been provided by the AGASA collaboration. For each event, a 50 μs waveform, with a sampling rate of 100 MHz and a resolution of 8 bits, was recorded from each

PMT by a digital oscilloscope. 29 days of data, containing 1513 non-zero traces were analyzed. This data was filtered through a 20 MHz RC filter, re-sampled at 40 MHz, and normalized to simulate the Auger electronics.

After this processing, an ADC channel corresponds to ≈ 0.6 photo-electrons, and a vertical muon has a peak pulse height of ≈ 12 channels in each PMT, similar to the conditions we expect in the Auger array .

Using the recorded data, the trigger rate was studied as a function of the width of the sliding window, n_w, the fixed threshold, t_h, and the number of bins required for a trigger, n_b. Two of the 3 PMTs were required to meet the trigger conditions. This was first done using background data (with no corresponding AGASA trigger), and for each choice of n_w and t_h, a value n_b was identified which produced a trigger rate of ≈ 20 Hz. Trigger conditions selected from this "equal background rate" set were then applied to the shower data set for those events where the reconstructed primary energy was $> 10^{18}$ eV.

Two of these examples are shown in Figs. 1 and 2. Both cases are for $n_w = 240$ bins (6 μs). Fig. 1 uses a threshold $t_h = 2$ ADC channels per PMT, and $n_b = 15$ bins. Fig. 2 uses $t_h = 20$ ADC channels, and $n_b = 4$ bins. The low threshold, extended signal trigger conditions displayed in Fig. 1 selects events where the tank is farther from the core of the shower, as desired.

3 ASIC implementation

The baseline design for the Auger surface detector level 1 trigger uses an application specific integrated circuit (ASIC), fabricated in a 0.35 μm CMOS process. In order to progress
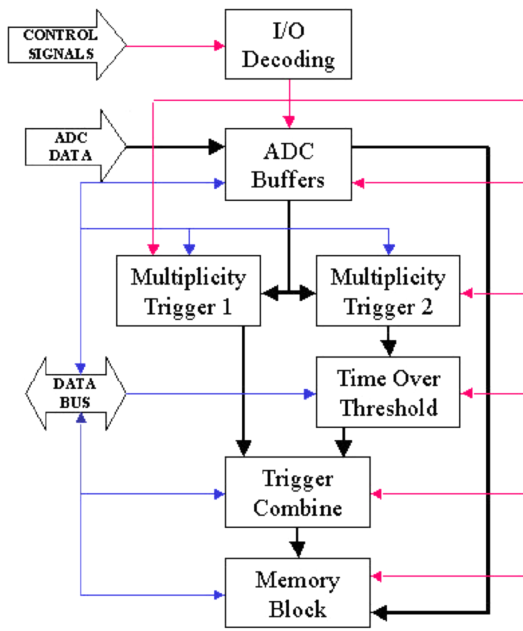
Fig. 3. Block diagram of Phase 1 trigger ASIC.

towards the final design, the design has been partitioned into 3 phases, each of which includes sufficient functionality to be a useful trigger/memory circuit.

3.1 Phase 1

The phase 1 implementation contains the essential trigger and shower memory buffers. The block diagram of this ASIC is shown in Fig. 3.

The module *I/O Decoding* interfaces to the station microcontroller bus, an IBM PowerPC 403GCX. The 60 bits of ADC data from the 6 ADCs are registered in the module *ADC Buffers*. This module buffers the ADC data, or optionally, replaces it with test data from a set of register/counters.

The 30 bits of ADC data from the 3 low gain channels are stored in a 1024 word circular memory buffer in module *Memory Block* until a shower trigger occurs. The 30 bits of data from the 3 high gain channels are also stored in a circular memory buffer, but in addition, they are fed to the trigger modules *Multilplicity Trigger 1* and *Multiplicity Trigger 2*.

The *Multiplicity Trigger* modules apply a trigger condition on each time bin. A register for each PMT contains a threshold level for that PMT. An 8 bit mask enables a specified set of patterns of PMTs meeting the threshold requirement. In addition, the sum of the pulse height in a selected set of the PMTs is compared against another threshold. The final trigger output of the module can be selected to be either the logical AND or the logical OR of the pattern and sum triggers.

The output of the first *Multiplicity Trigger* module is sent directly to the master trigger control module, *Trigger Combine*. The trigger output of the second *Multiplicity Trigger* module is sent to the *Time Over Threshold* module.

The *Time Over Threshold* module keeps a running count of the number of trigger signals from the *Multiplicity Trigger 2* module within a 256 bin sliding window (n_w above). If this count exceeds the value n_b specified in the "TOT THRES" register, *Time Over Threshold* outputs a trigger signal to *Trigger Combine*.

Trigger Combine accepts trigger signals from *Multiplicity Trigger 1*, *Time Over Threshold*, and an external input, not shown in Fig. 3. If the corresponding trigger has been enabled in the "TRIGGER MASK" register, a final trigger is issued.

The circular buffers are allowed to continue accumulating data until the position of the trigger within the 1024 word buffer meets the condition specified in the "PRE TRIGGER" register. At this point an interrupt signal is sent to the station controller. This signal is also used by the time tagging system to register the event time. The active set of memory buffers is closed, and storage of data continues uninterrupted in a second set of buffers (providing the station controller has emptied the previous event from those buffers).

Data is transferred from the trigger/memory chip memory buffers into the station controller memory via a direct memory access (DMA) operation initiated by the station controller.

The layout of the phase 1 ASIC is shown in Fig. 4.

3.2 Phase 2

The phase 2 chip implements the features of the baseline design which were not included in the phase 1 chip. It is designed to be operated in conjunction with a phase 1 chip to provide the full baseline design functionality.

The primary additional function in the phase 2 chip is the muon buffers. These buffers serve two purposes: 1) To collect a large sample of single muons for calibration and monitoring; and 2) to provide information about muons on the edges of an air shower, beyond the set of stations with a shower trigger.

They record the ADC signals from the 3 high gain PMT channels in a 1024 word "muon" buffer when those signals meet *Multiplicity Trigger* conditions. Each trigger causes a burst of 4 time bins to be recorded. In addition, a time stamp is recorded for each burst. With a relatively high threshold setting, this trigger will record mostly single muons, which occur at a rate of $\approx$3 kHz.

A special feature of the muon buffers is a second set of thresholds, which are activated for a specified interval (1-1023 bins) after each muon trigger. It is planned to use this feature for calibration purposes to temporarily lower the threshold in order to enhance the detection of decay electrons from stopped muons.

When a muon buffer fills, an interrupt is sent to the station controller and the time tagging system registers the time of buffer closure. Data storage continues uninterrupted in a second muon buffer, while the station controller initiates a DMA transfer of data from the first buffer. With an average muon having 4-8 bins above threshold, each buffer will take
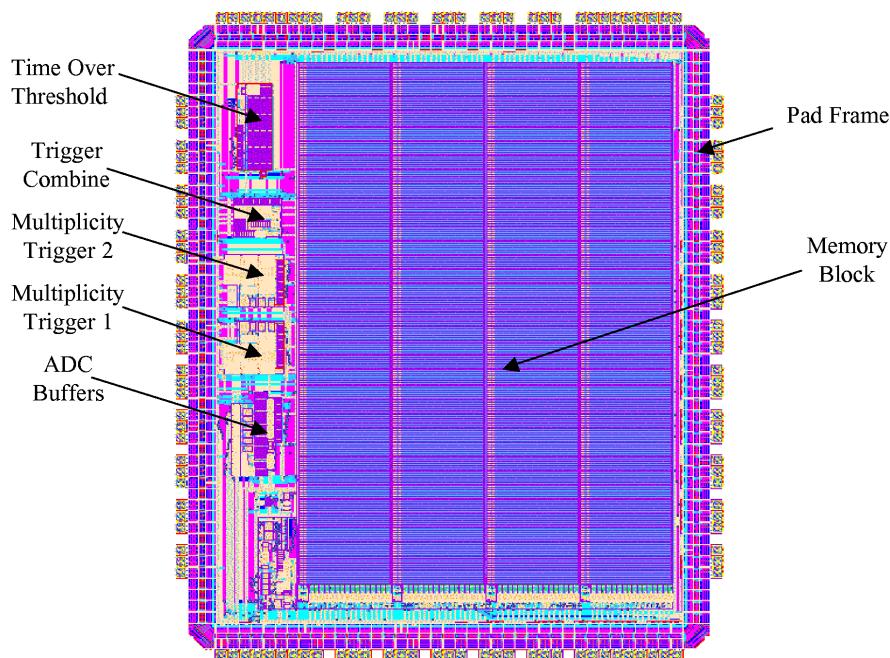
Time Over Threshold

Trigger Combine

Multiplicity Trigger 2

Multiplicity Trigger 1

ADC Buffers

Pad Frame

Memory Block

Fig. 4. Layout of the phase 1 trigger ASIC. The layout is 4.11 mm wide and 5.19 mm high. It has been produced using a 0.35 μm CMOS process and is packaged in a PGA-132 ceramic package.

40-80 ms to fill.

Additional new functions included in the phase 2 chip include a set of scalers to monitor rates in the PMTs, and a "random" trigger initiated by the station controller for diagnostics.

Finally, the phase 2 chip includes 2 instances of an enchanced version of the *Time Over Threshold* module, which allows the width of the sliding window n_w to be specified, in multiplicative increments of 2, from 2 to 256 bins.

3.3 Phase 3

The phase 3 chip integrates the phase 1 and 2 chips into a single chip. Depending upon the results of the evaluation of the first batch of prototype phase 1 chips, we may skip phase 2 and proceed directly to phase 3.

4 PLD implementation

Development of an ASIC is not a quick or easy process. We have thus pursued in parallel a backup implementation of the trigger/memory circuitry based upon progammable logic devices (PLDs) and commercial memory chips. The PLD implementation is discussed in Ref. (Szadkowski and Nitz, 2001).

5 Status

PLD trigger boards have been constructed and have been deployed in the Auger Engineering Array. The first iteration of phase 1 ASIC prototype chips has been received and is under study.

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