Proceedings of ICRC 2001: 865 © Copernicus Gesellschaft 2001

ICRC 2001

Frontend Electronics of the Telescope Array Detector

M. Sasaki[1], T. Aoki[1], Y. Arai[2], M. Fukutomi[3], K. Hashimoto[4], K. Honda[5], F. Ishikawa[1], M. Jobashi[1], N. Manago[1], M. Masuda[1], M. Sakai[3], Y. Tanaka[3], Y. Tsujikawa[6], and the other Telescope Array collaborators

[1]Institute for Cosmic Ray Research, Univ.Tokyo, Kashiwa, Japan
[2]High Energy Accelerator Research Organization, Tsukuba, Japan
[3]Department of Electrical Engineering, Nagasaki Institute of Applied Science, Nagasaki, Japan
[4]Faculty of Education and Human Science, Yamanashi University, Kofu, Japan
[5]Faculty of Engineering, Yamanashi University, Kofu, Japan
[6]Faculty of Science, Konan University, Kobe, Japan

Abstract. We report the design the frontend electronics of the Telescope Array (TA) detector and the status of the prototype test.

1 System requirement and overview

The Telescope Array detector (Sasaki et al., 1997)(TA Design Report, 2000) will be built to record the passage of extremely high energy cosmic rays through the atmosphere via air fluorescence with huge detection aperture. The strength and duration of the air-fluorescence pulse depends largely on the geometry of the event. The recording of the signal time profile becomes increasingly important for events with a long duration, for which most of the information to determine the geometry (particularly the direction) is included in the time information. Therefore the continuous digitization and recording of the signal wave form is much preferred compared to the analog integration of the signal with a fixed gate width, or a fixed time constant.

We performed a Monte Carlo study to estimate a required dynamic range of the electronics. In Fig. 1, we show scatter plots of the maximum number of photoelectrons contained in 200 ns gate time v.s. its impact parameter for the 10^{21} eV proton air-shower events.

The rate of events in which at least one of the PMTs exceeded the ADC dynamic range of 12 bits (16 bits) is roughly 30% (10%) assuming a LSB of digitization is taken equal to one photoelectron in 200 ns. The difference between 12 bits and 16 bits increases as we tighten the event selection cut. If we require more than 10 PMT hits with more than 2 σ significance level above the background, the overflow rates are 12% and 58% for 16-bit and 12-bit dynamic range respectively. This concludes the dynamic range of 16 bits is needed for the ADC system to be unsaturated up to 10^{21} eV event. The requirement can be alleviated if we take a LSB sensitivity to be at significantly lower level, say at the level of the night sky background (∼30 photoelectrons in 200 ns). But the monitoring of the background level will be unreliable for such a system, and a signal separation from the background will be much deteriorated for the online and offline analysis.

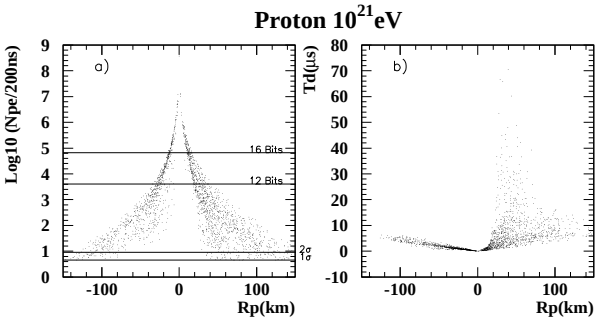

Fig. 1. Maximum number of photoelectrons per 200 ns time bin for one PMT versus impact parameter R_P of the event (left). Signal duration versus R_P for the same PMT (right). The sign of R_P distinguishes between going (plus) and coming (minus) tracks of observed air-shower events with respect to a detector station.

The duration of the signal for the PMT with the highest number of photoelectrons is plotted in Fig. 1 against the impact parameter of the event. It indicates some events can generate fluorescence signal as long as 70 μs. An elaborate and flexible algorithm will be required online and offline to identify a signal and maximize the signal to noise ratio (S/N). We checked that the 25.6 μs time window is practically sufficient for the signal finding for the triggering purpose. The necessary time depth for the event recording can be determined for each event by the DSP software.

A good S/N will allow us to trigger and analyzed lower energy and more distant events. As a result, we will be able to decrease the threshold energy for detection down to 10^{16} eV, which is about an order of magnitude smaller than that of Fly's Eye. Here the D is a mirror diameter and d is a

Correspondence to: M. Sasaki
(sasakim@icrr.u-tokyo.ac.jp)

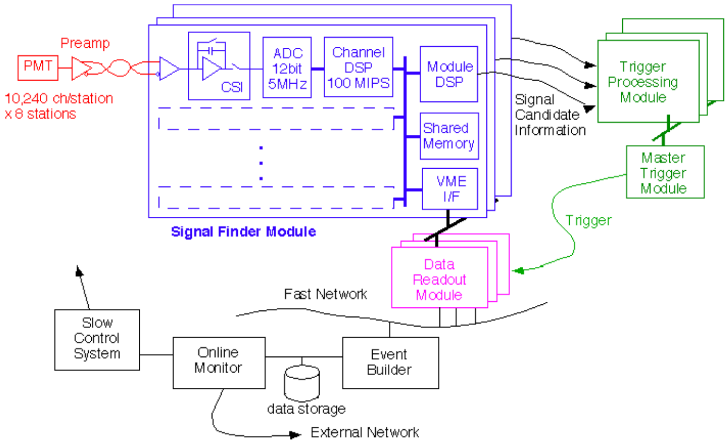

Fig. 2. Block diagram of the TA online system.

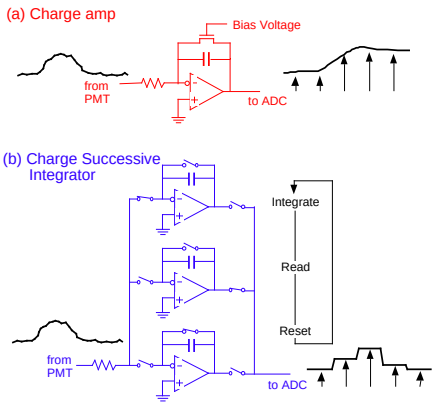

Fig. 3. Schematics of Charge Successive Integrator.

PMT diameter. This would allow us to study cosmic rays in this energy region and specifically opens up a possibility of detecting the neutrinos from AGN.

Monte Carlo studies indicate that many showers that trigger one station will also be seen by several neighboring stations. Even if the neighboring telescope does not see enough of the light to trigger on that shower, there will be information present useful for the stereo reconstruction of the event. The system of broadcasting triggers seen by one detector to its neighboring detectors will be thus important. When a trigger occurs in one detector, the data of its neighboring detectors will be examined and any hits found will be written into the data stream.

A design of the TA signal digitization, trigger and data acquisition was drawn to satisfy above conditions (see Fig. 2). Its main features are summarized below;

1. AD conversion with 12-bit resolution and 5 MHz continuous sampling using a pipelined ADC chip.
2. 16-bit dynamic range using H/L 2-range scheme at the front-end charge sampling LSI (custom development). Here LSB sensitivity is taken equal to one photoelectron in 200 ns time window.
3. on-flight software recognition of fluorescence signal by the DSP attached to each channel.
4. generation of trigger in 3-dimensional space; XY (camera) coordinates and T (time) coordinate by software.
5. exchange of trigger information between stations (inter-site trigger).

2 Front-end Electronics System

The front-end electronics for TA is one of the most critical elements to achieve a large aperture of the detector and lower threshold of cosmic ray primary energy.

In the pioneering work of the Fly's Eye detector, analog sample-and-hold circuit with a slow AD converter (Baltrusaitis et al., 1985) was adopted. In the subsequent HiRes detector, 8-bit flash ADC was introduced with additional analog sum measurements to circumvent the effect of over range (Boyer et al., 1995).

A new pipelined ADC technology and a wide spread of digital video system enable us to use a fast and wide dynamic range ADC for all channels. The pipelined ADC is fabricated in a CMOS process, and it has superi or characteristics of low power, low cost and high speed. A 12-bit 5-MHz sample ADC is commercially available in less than $5.

While the fast ADC system could give us more information on air shower, it increases data size almost 100 times. Thus a large bandwidth is required in data acquisition system. Furthermore, to maximize the merit of the fast digitization, it is indispensable to process the data in real time to increase signal to noise ratio. This is particularly important in the fluorescence measurement since the signal wave form varies greatly depending on the zenith angle and the impact parameter.

To process the digital data in real time, a large processing power is required. Fortunately, recent progress in digital products introduces high-performance, low-cost Digital Signal Processors (DSPs). There are several DSPs, performances of which are more than 100 MIPS and the price is about $6. By using these DSPs we will be able to search optimal signal width for fluorescence signal in real time.

2.1 Charge Integration

A charge integration method is essential in designing a calorimetric measurement.

To implement the frontend electronics design, we are developing a Charge Successive Integrator (CSI) LSI. (Fig. 3). It has 3 or 4 rotating capacitances which serves for the in-

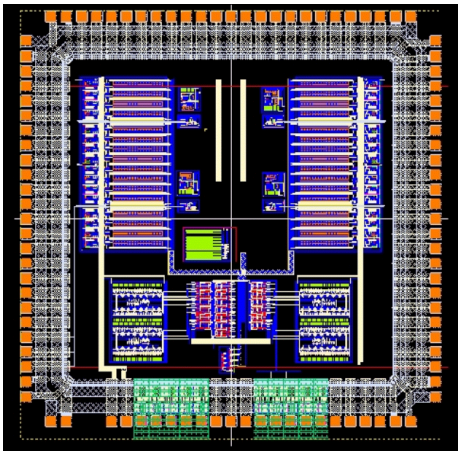

Fig. 4. Layout of the test CSI cell designed in 0.6 μm CMOS technology.

tegration, signal output to ADC, and reset successively for each 200 ns. Required signal range for the CSI (and PMT) is summarized in the following lists. Here we use a PMT amplification of 8×10^4, which is followed by a preamplifier circuit with the gain of 4, and 52 pF storage capacitance for the CSI. The LSB in the low range (a unity gain before CSI) corresponds to 1 photoelectron in 200 ns. The maximum signal corresponds to 65,536 (=2^{16}) photoelectrons in 200 ns and is detected in the high range (a gain of 1/16 before CSI).

- **Least count sensitivity:** A 10 ns wide (square) pulse from PMT has a (peak) current of 5.2 μA and a total charge of 52 fC. This is equivalent to 1.2 mV of stored voltage on the CSI capacitance (low range used).
- **Full scale sensitivity:** 65,536 photoelectrons in 200 ns corresponds to 16.8 mA current from PMT for the same duration. The total charge from PMT is 1.7 nC and this becomes 5.0 V on the CSI capacitance (high range used).
- **Night sky background:** We assume 30 photoelectrons in 200 ns. This is equivalent to a continuous current of 8 μA from PMT and 38 mV stored on the CSI capacitance (low range used).

The CSI will be fabricated in a CMOS technology. In this technology the value of the capacitor matches in 0.1% level, and no correction will be necessary. But the area of CSI-VLSI limits the integration capacitance less than ~200 pF. A test CSI chip using a 0.6 μm single-poly, triple-metal CMOS process was fabricated (Fig. 4) at Rohm Co. through VLSI Design and Education Center (VDEC, Univ. of Tokyo) multi project ware service. The prototype CSI chip includes two range of circuit.

2.2 Pipelined ADC

Recent progress in digital video system brings a new high-speed, large dynamic-range, low-power, low-cost ADC. Tech-

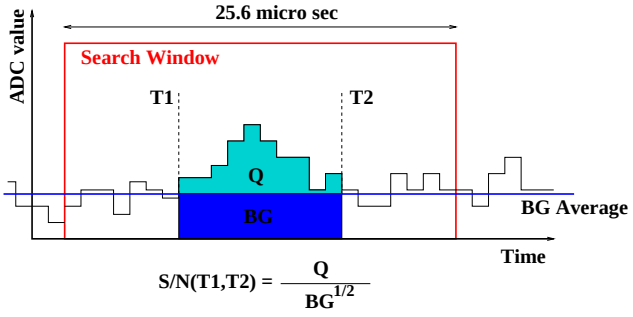

Fig. 5. Signal finding algorithm.

nique used here is called pipelined ADC. The ADC has many pipelined stages, and digitization of only one or two bit is done at each stage. This ADC is fabricated in similar process used in CMOS digital LSIs and there are very little analog elements in the chip. A digital error correction technique is usually employed to achieve a high precision. We are presently using Burr-Brown ADS803 and its power consumption is only 115 mW. The ADC has 12-bit dynamic range and 5 MHz-conversion rate.

2.3 DSP

The ADC converts a PMT signal continuously at 5 MHz frequency, and 12-bit data together with additional information such as a range and an overflow bit are successively stored into the memory of dedicated DSP. A high-performance DSP is needed to run a signal finding algorithm in real time on the stored data. We are presently using a TMS320C549 DSP from Texas Instruments. This DSP runs at 100 MHz, and many operations can be performed in one cycle. The C549 has 3 internal data bus and one program bus, and consists of 6 stage pipelines. It contains 32k word internal memory that is enough for our application. The DSP consumes only 100 mW/chip. Since the ADC generates 12-bit data every 200 ns, there are 20 cycles for one data in average. We set 25.6 μs time window for finding a signal. Since this window has 8.5 μs overlap with the next window, a total of ~1,700 DSP cycles (17.1 μs) can be executed for 128 data words (25.6 μs) to identify the fluorescence signal.

An example of signal finding algorithm at DSP is illustrated in Fig. 5. The program looks for a set of signal edges T1 and T2 which maximize the S/N or $Q/\sqrt{BG}$. According to a Monte Carlo study, the charge resolution by this algorithm is 50 % for 10 photoelectrons (Q=10) and 20 % for 50 photoelectrons.

3 Signal Finder Module

A Signal Finder Module, which contains the front-end CSI, ADC and DSP, has been prototyped as the 3rd version (Proto-3) (see Fig.6).

The schematics of the module is shown in Fig.7. The module is implemented in a 9U VME board and contains 16 chan-

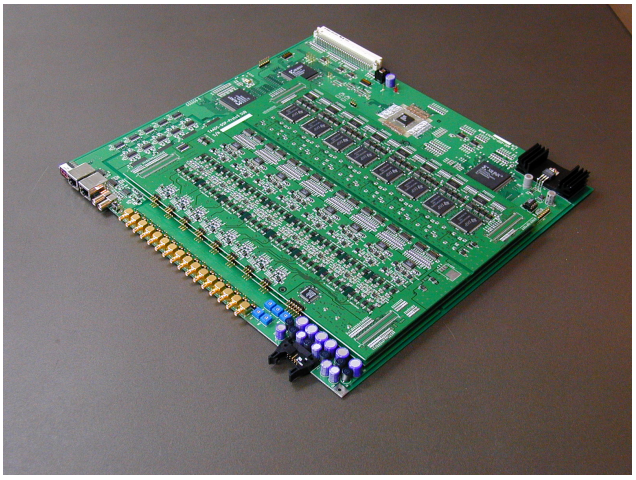

Fig. 6. Proto-3 module of signal finder. The height of the module is 9U but the depth of the module is extended to 50 cm.

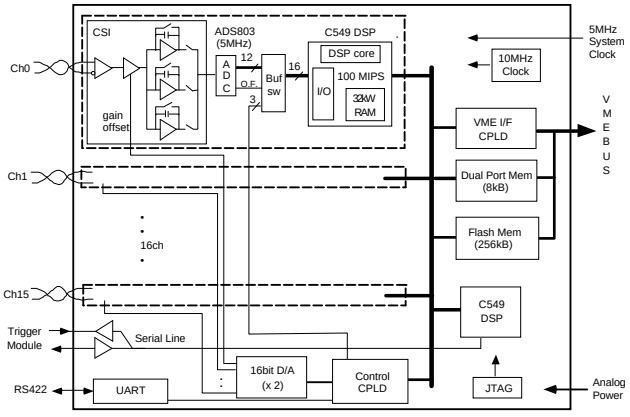

Fig. 7. Block diagram of the 16-ch prototype Signal Finder module. The module is implemented in a 9U VME board.

nels. The gain and offset of each channel can be corrected before the CSI with 16-bit DAC. The single range hybrid version of CSI is used for the present prototype (3rd version) with the 2-range scheme implemented.

Data transfer between the ADC and the DSP internal memory will be done through an 8-bit host port interface of the DSP with a maximum speed of 20MB/s. ADC data are automatically transferred to internal circular buffer without DSP intervention. The size of the circular memory is 2k words, thus the data can be stored in the memory up to 400 μs (200 ns $\times$2 kW). For the intersite trigger which requires a longer latency than 400 μs, a data copy operation is required to the external memory.

Between the ADC and the host port, 12-bit data and an overflow bit are transferred. In addition, 2 bits are transferred to a 2-bit counter, which is used to check the data sequence. Last one bit is reserved for data flow control which is used in DSP software. This is realized by two 8-bit data transfer cycles.

All the individual DSPs are controlled by another DSP, which collects the processed information (T1, T2, Q and S/N, etc.), and send them to the Track Finder trigger module through its serial lines at 50 Mbps. An easy-to-use commercial PC tool can be connected to the module via JTAG boundary scan port for debugging and monitoring of the DSPs. A dual port memory of 8 kB is used to exchange the data between the module and a VME master module. A Flash memory of 256 kB is included to store program and parameters. The whole system can be synchronized by using an external system clock of 5 MHz.

Sixteen modules of Proto-3, which corresponds to 256 input-channels, has been made and tested. The output noise fluctuation of CSI amplifier followed by the pipelined ADC is less than 2 photoelectrons, which is less than half of intrinsic night sky background fluctuation of $\sqrt{30} = 5.5$ photoelectrons in a PMT every integration time of 200ns. The ch-by-ch variation of the noise fluctuation is examined to be small. The noise originated from the Proto-3 circuit can be neglected. Also the signal finding algorithm and data flow control among 16 DSPs on a module has been developed using assembler language dedicated to C549 DSP. We confirmed that the signal finding and data flow control can successfully work without any dead time on the way of the online data aquisition. Detailed results on trigger efficiency using the developed signal finding algorithm are shown elsewhere(Sasaki et al., 2001).

References

M. Sasaki *et al.*, Proc. 25th ICRC, **5**, 369 (Durban, 1997).
The Telescope Array Project: Design Report. July 2000. http://www-ta.icrr.u-tokyo.ac.jp
R. M. Baltrusaitis *et al.*, Phys. Rev. D **31**, 2192 (1985).
J. Boyer *et al.*, Proc. 24th ICRC, **3**, 429 (Rome, 1995).
M. Sasaki *et al.*, Proc. 27th ICRC, **HE7.1** (Hamburg, 2001).