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A PLD implementation of the Pierre Auger Observatory first level trigger

Z. Szadkowski[1,2], **D. Nitz**[1], **and The Pierre Auger Observatory Collaboration**[3]

[1]Physics Department, Michigan Technological University, Houghton, MI 49931, USA
[2]University of Łódź, Pomorska 151, 90-236 Łódź, Poland,
[1]Observatorio Pierre Auger, Av. San Martin Norte 304, (5613) Malargüe, Argentina

Abstract

A surface detector trigger for the southern hemisphere Pierre Auger Cosmic Ray Observatory implemented using Altera™ programmable logic devices (PLDs) is presented. The ultra large-scale integrated circuit (ULSI) technology of the APEX™ family allows the trigger logic to be implemented using only one PLD chip. Digitized waveforms produced by the passage of an extensive air shower front through a surface detector are stored in the internal PLD memory. While awaiting a trigger the first 256 64-bit words of the waveform (from 6 10-bit analog to digital converters) are stored in a circulating memory. Upon determination of a trigger, an additional 512 words are recorded. The size of the internal memory in the PLD allows two buffers to be implemented. When one buffer is full it is transferred to the detector station micro-controller via direct memory access. The other buffer remains active to record another shower waveform. Such a solution minimizes dead time. Additional logic implemented in the PLD records single muons. A reduced threshold interval following the detection of a muon-like signal enhances the capture of the signal from stopped muon decay. The memory size required for the muon buffer exceeds the capacity of the internal PLD memory. An external memory chip is added for this memory. More than 40 trigger boards have been fabricated and installed in the surface detectors of the Auger Engineering Array.

Correspondence to: zszadkow@mtu.edu

1. Introduction

The Pierre Auger Observatory, which investigates cosmic rays > 10^{19} eV, consists of two types of detectors: fluorescence detectors registering the nitrogen fluorescence from the showers and a surface detector investigating Cherenkov light generated in highly purified water in large closed cylindrical tanks (Escobar, Filevich and Mazur, 2001; Salazar, Nellen, and Villaseñor, 2001). An extremely low flux of particles requires a huge detector area. The surface detector in the Pierre Auger Observatory consists of 1600 tanks spread over 3000 km^2 (Dova, 2001). Three photo-multipliers (PMTs) in each tank detect the Cherenkov light. Afterwards the PMT signals are analyzed by rather sophisticated electronics (Suomijärvi, 2001). Analog signals given by the PMT are converted into digital form in 10-bit ADCs. To provide a high dynamic range of data for analysis, signals from the PMTs are amplified in two separate channels with different gains. High-gain channels are intended for normal work with small signals (far showers), however low-gain channels provide data for analysis when the high-gain channels are close to saturation. Such an approach allows obtaining a 15-bit dynamic range using 10-bit ADCs covering different ranges of energy.

The main goal of the surface detector trigger is to extract event-like signals from the stream of data. The time spectrum of signals given by PMTs is relative wide. Very short, as well as long-tailed signals can appear. The frequency of digitalization should be high enough not to lose short signals. In the surface detector, 40 MHz has been chosen, as a compromise between efficiency and cost. The data is digitized and

the triggers operate at the same 40 MHz frequency. Three PMTs, each with two different gain channels of 10-bit ADCs, result in a 60-bit data bus.

The final chip including all trigger logic will be implemented in an application specified integrated circuit (ASIC). However, as the procedure of ASIC preparation and fabrication is long, temporarily the PLD trigger will be installed in the detectors. They provide an important backup solution for the ASIC design.

2. Triggers

Five triggers are implemented. The first trigger is periodic, interrupting the micro-controller at a programmable time (typical 0.1 s). The second one is an external trigger designated for tests and future use. The third and fourth triggers are connected to the fast channel and the fifth to the slow channel (Nitz 1997). In both channels data is written temporarily into a memory buffer. Afterwards data from the memory buffer can be transmitted to the micro-controller while additional data is simultaneously being recorded in the second buffer. Such an approach of switching buffers reduces dead time when the time interval between following triggers is small. In the fast channel, data is sequentially written in a circulating buffer. When a trigger appears, data in the buffer is frozen and data starts to be written into the next buffer. In the slow channel data is stored only after a trigger. Additionally, time stamps are inserted into data stream.

The Pierre Auger Observatory will be operating for ~20 years. It is important to minimize the number of chips for long-term reliability (Szadkowski, 2001). The PLD design discussed here achieves that objective. The Altera^{TM} programmable logic devices (PLDs), based on ultra large-scale integration (ULSI), allow the trigger logic to be implemented in one PLD chip. The chip EP20K200RI240-2 from the APEX^{TM} family has been used. This chip has sufficient capacity to implement sophisticated logic (equivalent to 200000 elementary gates) and in addition contains internal memory in Embedded Array Blocks (EABs), which has been used as buffer memory for the fast channel. The size of the EABs allows two 64-bit wide 768-word buffers (256 words before a trigger and 512 words after) to be implemented. The fast channel trigger logic uses only 23% of the chip resources. In the same chip, the slow channel trigger logic is also implemented. However, for the slow channel, additional external memory is needed. The trigger logic for both channels use 43% of the chip resources. The register performance of the PLD chip has been tested in simulation at 60 MHz. The chosen chip is an industrial temperature version, which can operate from –40 ºC up to 85 ºC. In spite of the industrial temperature version of the chips not being the fastest in the family, the speed of the chosen chip is high enough for all the implemented logic. For the external slow memory, the IDT70V3569S6DRI chip has been used. It is high-speed 3.3V 16k*36bit synchronous pipelined dual port static RAM in the industrial temperature version. This temperature version is the slowest one available. However the guaranteed 83 MHz pipelined operation is sufficient. The size of the external memory allows two slow buffers storing 2048 32-bit words to be implemented. Slow data are written into the external memory via the PLD, however they are read by the micro-controller via direct memory access.

In the fast channel, two types of triggers are implemented: single time bin and a moving window of successive time bins. The single time bin trigger is generated when the ADC data from the high-gain channels is over the specified threshold. The window trigger is generated when the time bins in the scanning window contain more events over threshold than a specified value. Data from low gain channels do not affect the triggers in either case.

In the slow channel, a trigger is generated when the ADC data exceeds the threshold. Afterwards the threshold decreases and remains low for a specified time. Data over the threshold are only written into memory as blocks of 4 time bins. To identify the slow data in time, time stamps are inserted into beginning of each block of slow data over the threshold. 30-bits of data are stored. The two bits in the 32-bit bus not used by the data are implemented as time stamp and PMT threshold indicators. When the low threshold expires, but the data is still over the high threshold, the data is written continuously. No additional time stamp is inserted. However, the threshold indicator records threshold changes.

All values necessary to generate triggers, thresholds, size of windows, etc., are stored in registers and can be modified online by the micro-controller.

3. Conclusions

The first stage of the Pierre Auger Observatory is the Engineering Array (EA) consisting of 40 surface detector tanks and two fluorescence detector cameras. In both detectors, many particular details can be implemented in different ways, so the EA is mainly a test facility to verify and to optimize among the variants of optics, electronics and mechanics. For the EA, more than 60 boards of the PLD based trigger have been fabricated. Starting in June 2001, 40 trigger

boards are being installed on tanks in the EA. The algorithms of both the fast and slow triggers implemented into the PLD have been completed. However changes and additions are still possible.

References

Dova,T. for the Pierre Auger Collaboration, *Overview of the Pierre Auger Observatory*, Contribution to this conference.

Escobar,C., Filevich, A., and Mazur P. for the Pierre Auger Observatory Collaboration, *Surface Detector Construction and Installation at the Auger Observatory*, Contribution to this conference.

Salazar, H., Nellen, L., and Villaseñor L. for the Pierre Auger Observatory Collaboration, *Surface Detector Calibration for the Auger Observatory*, Contribution to this conference.

Suomijärvi, T. for the Pierre Auger Observatory Collaboration, *Surface Detector Electronics for the Pierre Auger Observatory*, Contribution to this conference.

Nitz, D. for the Pierre Auger Observatory Collaboration, *Triggering and Data Acquisition Systems for the Auger Observatory*, Xth IEEE Real Time Conference, Beaune, France, 1997.

Szadkowski, Z., *Second level trigger in the Pierre Auger Fluorescence Detector*, Nuclear Instruments and Methods A, 2001 (in publication).

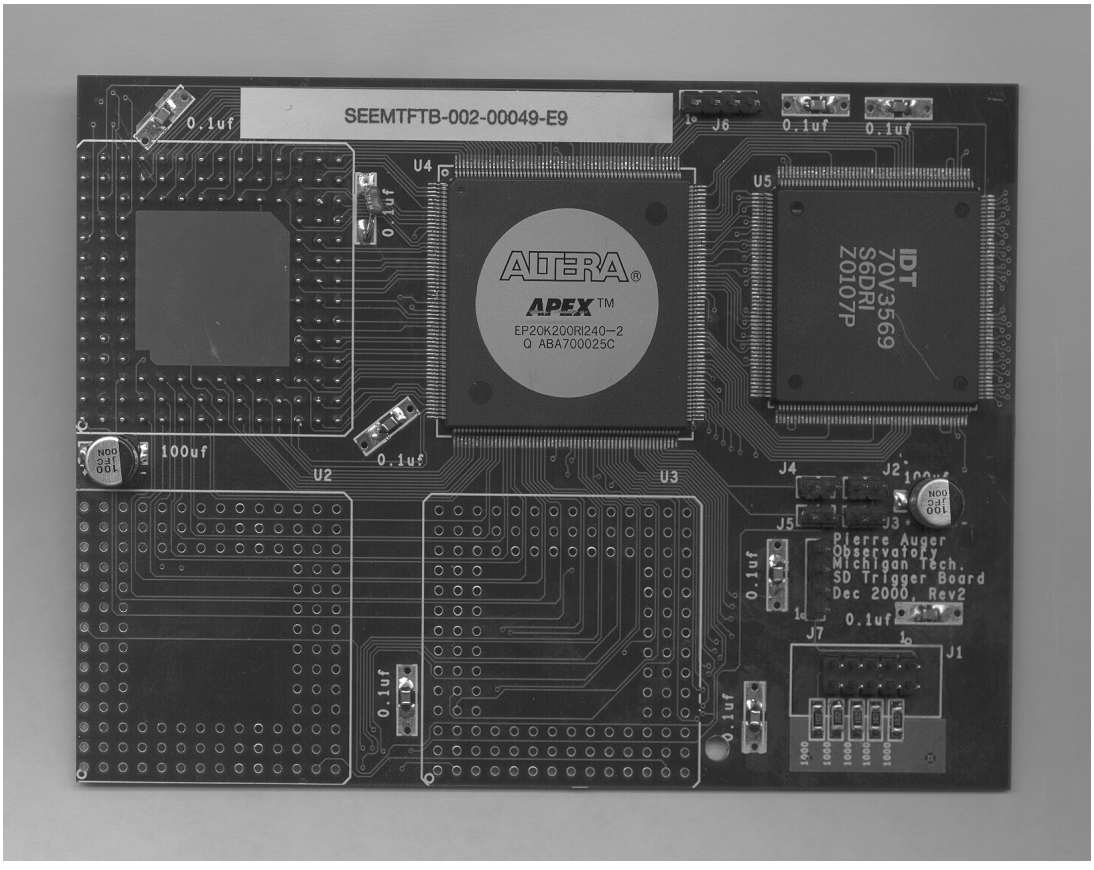

Fig.1. PLD trigger board.