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Time of Flight read out system of the AMS-02 experiment

V. Bindi[a,b], D. Casadei[a,b], G. Castellini[a,c], F. Cindolo[a], A. Contin[a,b], F. Costa[a,b], F. Giovacchini[a,b], G. Laurenti[a], G. Levi[a,b], F. Palmonari[a,b], L. Quadrani[a,b], C. Sbarra[a], L. Villa[a,b], W. Wallraff[d].
(a) INFN, Sezione di Bologna, Viale Berti-Pichat 6/2, 40127 Bologna, Italy
(b) Physics Department, Bologna University, Via Irnerio 46, 40126 Bologna, Italy
(c) IFAC-CNR, Via Panciatichi 64, 50127 Firenze.
(d) I. Physikalisches Institut, RWTH, D-52056 Aachen, Germany
Presenter: V.Bindi (bindi@bo.infn.it), ita-bindi-V-abs1-HE15-oral

The AMS-02 detector is a space cosmic-ray spectrometer to be operated without human intervention for at least three years on the International Space Station. The Time-of-Flight (TOF) system front-end electronics gives the fast trigger to the spectrometer, digitizes 68 time and 144 charge channels at a speed up to 10 KHz with a total power of 100 W, and must be operational between -30° and 50 °C in space. Based on the previous experience of the AMS-01 experiment, the general design for long term operation is reviewed.

1. Introduction

The AMS-02 detector is a superconducting magnetic spectrometer that will operate on the International Space Station without human intervention for at least three years [1]. The time of flight (TOF) system of AMS-02 is composed of four scintillator planes with 8, 8, 10, 8 counters each, read at both ends by a total of 144 phototubes. The TOF system of AMS-02 is completely designed and built at the INFN Laboratories in Bologna, Italy. Its main goals are to provide the fast trigger to AMS readout electronics, and to measure the particle velocity, direction, crossing position and charge. The TOF performances are reported in reference [2].

After the successful operation of AMS-01, the detector has been redesigned to increase the maximum detectable rigidity up to 1 TV, by using a superconducting magnet which will provide a maximum field of about 0.8 T. The main differences with respect to the TOF system of AMS-01 are due to the very strong magnetic field and to the more severe weight and power limits. AMS-02 will operate in space with a pressure of about 10^{-9} atm, a temperature between -30° and +50 °C, in a radiation-hard environment. Hence the apparatus and the electronics have been developed considering these extreme conditions. To reduce the risks, the AMS-02 electronics components are space qualified and radiation tolerant, and all the TOF and ACC (the AntiCoinCidence system) boards are doubly redundant.

All Front-End (FE) and Data Acquisition (DAQ) boards of ACC and TOF, with the exception of the Scintillator Front End Charge boards (SFEC), are distributed among four crates (S-crates) [3]. Each S-crate contains the same number and type of boards:

1. one Scintillator Data Reduction redundant unit called SDR2, which collects data from the FE boards and sends them all slow-control commands;
2. four Scintillator Front End TOF redundant boards called SFET2, which provide the time measurement and the signals for the trigger generation;
3. one Scintillator Front End ACC redundant board called SFEA2, which provide the signal for the veto of the trigger:
4. one redundant Scintillator Pre-Trigger board called SPT2, which implements pre-trigger combinations of logical signals coming from SFET2 and SFEA2 modules, and sends the results to the trigger boards using LVDS connections.

Only the SFEC boards, which are placed inside the TOF enclosing box and perform the redundant charge measurement via the dynode signals, are not doubled.

The SFET2, SFEA2 and the SPT2 boards are connected to the SDR2 through dedicated serial lines and communicate using a custom protocol (called TOFwire), whereas digitized charge data follow separate links. To ensure the complete double redundancy of the S-crate, there is no connection between the two halves of the same board and during the normal conditions, at any given time, only half of the crate is powered.

2. The time measurement

When a charged particle crosses a scintillation counter, the photomultiplier tubes (PMTs) produce a current pulse proportional to the emitted light. Every couple of anodes signals from the PMTs produces a signal that goes to the SFET2 where it is split in two paths: the bigger fraction is necessary for the time measurement, and the smaller one is used for the charge measurement inside the SFET2 (Figure 1).

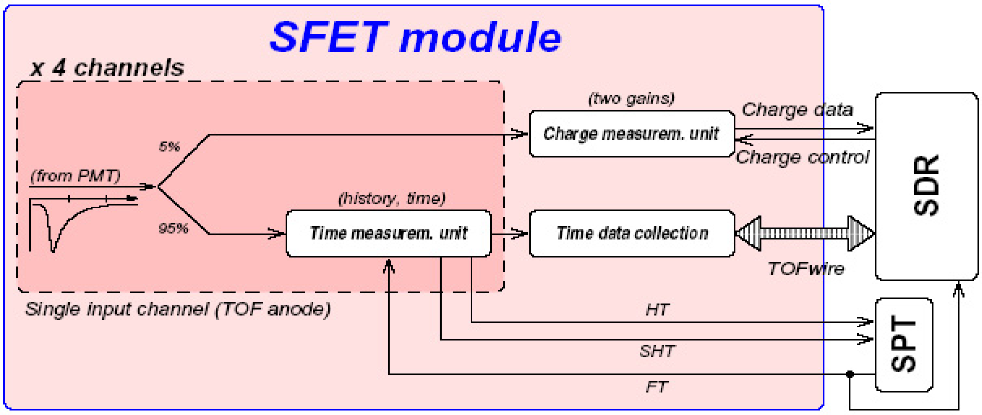

Figure 1. Anode signals received by the SFET module are split in two paths. The bigger fraction is used for the time measurement: the analog signal is compared to fixed thresholds

The signal used for the time measurement is compared to three fixed thresholds, called "low threshold" (LT, roughly 20 mV), "high threshold" (HT, 60 mV), and "super-high threshold" (SHT, 350 mV) (Figure 2). The digital signals produced by the comparators will be used to start the time measurement (LT), to send "charged particle" signal to the trigger logics (HT), or to send a "big charge" signal to the trigger logic (SHT). In addition, LT and HT are used by the LeCroy MTD 135 TDC inside the SFET2, that has two independent 16 fronts deep buffers per channel: the "time" and "history" buffers. The first one stores the four fronts of the time expansion and freezes them; the latter is used to flag (eventually discard) events with other particles crossing the detector since 13.5 μs before the FT to 7.5 μs after it.

The time expansion technique is the following: in order to measure the time Δt elapsed between the LT and the fast trigger (FT) (time "4-3" Figure 2), a capacitor is linearly discarged during this time. Upon the FT arrival, it starts discharging linearly on a circuit with a longer characteristic time. The triangular shaped voltage law of the capacitor is compared with a fixed threshold, and the "expanded time" is given by the delay between the last crossing point and the LT ("4-1" in Figure 2). If M is the ratio between "3-1" and "4-3", the total time "4-1" is equal to $(M+1)\Delta t$. . If the intrinsic TDC resolution is σ_{TDC} and the fluctuations on M are negligible, the final time resolution after the time expansion is $\sigma \approx \sigma_{TDC}/M$. Any instability of the time expansion factor M will result in a higher σ_{TDC} and special effort is devoted to avoid this problem.

The SFET2 receives 4 anode channels and consists of two identical SFET modules, for redundancy. Each module is composed by an Actel A54SXA32 and two Actel A54SXA08 programmable chips. The latter control 4 TDCs (one for each channel) and 5 DACs which set the LT HT e SHT thresholds. The TDC data are collected by the A54SXA32, which sends them to the SDR2 board using the TOFwire protocol. The SFEA2 is a simplified version of the SFET2, adapted for the ACC anode signals. The ACC signals are split in two parts: the lower fraction is used to measure the charge, whereas the higher one is compared to a threshold. If this pulse is over the threshold, a TDC keeps track of the crossing time and the SFEA2 sends a logic signal to the boards for the trigger generation.

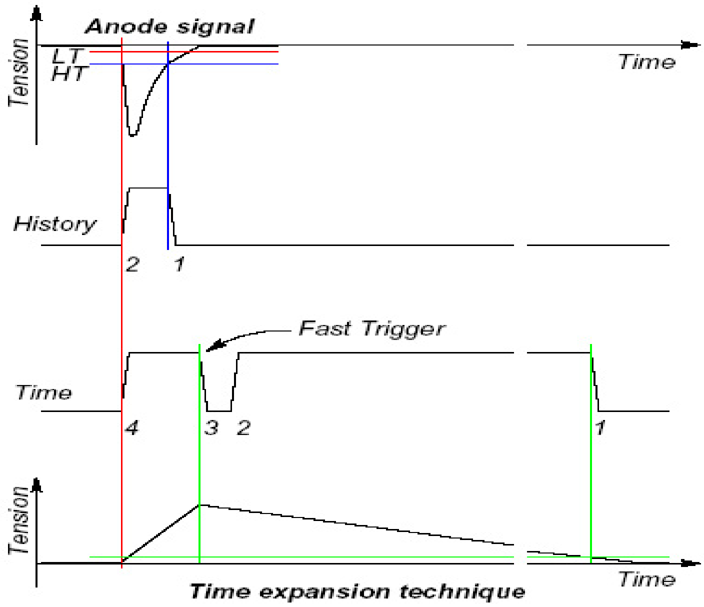

Figure 2. The time expansion technique.

3. The charge measurement

The charge measurement is done by SFET2 and SFEA2 using the anodes signals. The dynodes are read by the SFEC boards. In both cases the charge measurement is made by a special chip (called AICPPP) built for this particular purpose by the AMS-RICH collaboration [4].

This chip has an architecture based on a spectrometry chain. This method gives a voltage signal proportional to the charge of the input pulse. The circuit integrates 16 identical channels. The analog output of each channel is memorized into the track-and-hold and the 16 outputs are sequentially sent to a serial ADC via a multiplexer in order to reduce the number of input/output pads (Figure 3). In order to increase the resolution for small signals, an amplifier with a 5× gain has been added at the output. A switch selects the gain G1 (8.8 fC/ch on the ADC) or gain G5 (1.76 fC/ch) outputs. The spectrometry chain consists of a charge integrator followed by a first-order high-pass filter with a pole-zero cancellation followed by a 5th low-pass filter (Figure 4). The result is a quasi-gaussian shaped pulse. The peak amplitude is directly proportional to the total charge.

The circuit has been implemented into CMOS 0.6 µm technology. Special attention was paid to minimize the noise coupling from the digital part to the analog one. The circuit is optimized in order to have the power consumption as small as possible.

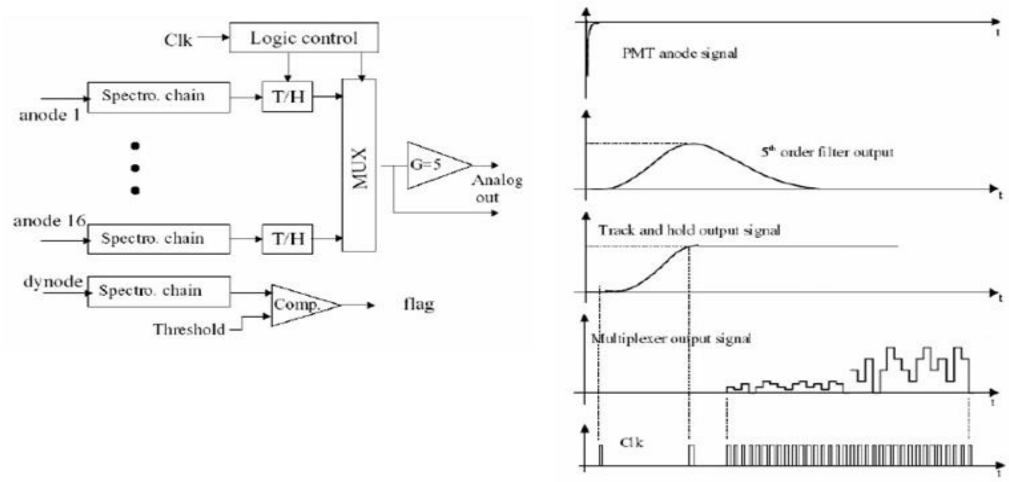

Figure 3. On the left is represented the circuit architecture and on the right the circuit chronograms [4].

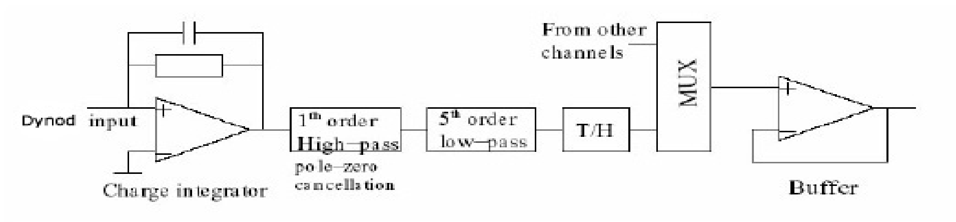

Figure 4. Single channel architecture [4].

There are two versions of the analog chip for negative and positive inputs. Each SFET2 and SFEA2 board has one AICPPP for the anode charge measurement whereas SFECs have two chips, for the positive signals coming from the PMT dynodes. The output of each AICPPP is sent to one AD7476 Analog Devices serial ADC, which is read by the Actel A54SX08A. The SFEC board is very similar to the charge measuring part of SFET2 and SFEA2, the only difference being the presence of two AICPPP and two AD7476, whose data are sent to the SDR2 via independent LVDS lines.

4. Acknowledgements

We wish to thank the many organizations and individuals listed in the acknowledgments of ref [5]

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