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Low Power Front-End Electronics for the BESS-Polar Time-of-Flight Counter and Aerogel Cherenkov Counter

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The BESS experiment has measured cosmic-rays at low geomagnetic cutoff for more than a decade and has found suggestive and important results. To study these phenomena further, we planned a long duration flight in Antarctica to accumulate statistics with an instrument built specifically for that purpose. To adapt to the particular requirements of the Antarctica flight, we developed low-power Front-End-Electronics (FEE) using techniques originally developed for space instruments at Goddard Space Flight Center. A Digital Signal Processor (DSP) was resident on each FEE board and controlled each board independently to maximize the data throughput rate. The power consumption of the time-to-digital converter was about 0.5 W per channel and data processing time of one event was less than 30 microseconds. The data obtained by the FEE were sent to an event-builder subsystem board which converted the data format to be handled by a USB 2.0 controller chip. A CompactPCI embedded computing system gathered these data through USB 2.0 ports and built the complete event data including the tracking information. The event data were recorded on an array of hard disk drives (HDD) with total capacity of 3.6 terabytes. This system was flown nearly 9 days over Antarctica successfully recording cosmic-ray events.

1. Introduction

The Balloon-borne Experiment with a Superconductiong Spectrometer in Antarctica (BESS-Polar) is part of a US-Japan cooperative balloon program in the field of particle astrophysics that aims to study elementary particle/antiparticle phenomena in the early history of the Universe [1]. The detector systems of the BESS-Polar experiment are evolutionary developments of those used in the previous BESS experiments [2], and improved to adapt to a long duration flight in Antarctica. Observation conditions were similar for the BESS experiment. The trigger rate varied depending on the solar activity from 1.5kHz to 2.5kHz and typical event data size was about 2 kbytes. For the BESS experiment, standard CAMAC and VME systems were used for the data acquisition system (DAQ). Since the DAQ system in the BESS detector was not fast enough to process data to yield an acceptable dead time, an intelligent second-level trigger system was introduced to reject the background events using only hit pattern information from scintillation counters and drift chambers. For the BESS-Polar flight, a new DAQ system was developed in order to process and record all data during the flight without any onboard event selection. Also to adapt to the need to operate with a solar power system in Antarctica flight, low power consumption was pursued. The low-power FEEs for the BESS-Polar Time-of-Flight Counter (TOF) and Aerogel Cherenkov Counter (ACC) [3] are described in this paper.

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2. System architecture and Performance

Figure 1 shows the BESS-Polar DAQ system. The T0 trigger is generated by the trigger board with the coincidence of hits in the top and the bottom or middle TOF counters. Once T0 trigger is generated, the trigger board is locked until the trigger board receives a "Ready" signal from all FEEs. To minimize the dead time caused by the event processing, each FEE sends the "Ready" signal to the trigger board independently just after it finishes digitization. The dead time can be kept under 10% if each of the FEEs finishes this process within 50 microseconds. For the FEEs of TOF and ACC, a Digital Signal Processor (TMS320VC5402 [4], Texas Instruments) is resident on each board and controls each board independently to maximize the data throughput rate. The data from up to three FEEs board are gathered in the event-builder subsystem board, a so call MU2 board, and converted to a USB 2.0 signal using a USB Microcontroller (EZ-USB FX2 CY7C68013 [5], Cypress). Then the MU2 board sends the data to the CompactPCI embedded system. The event is built in the system together with the drift chamber data (digitized by the FADC) and recorded to the HDD.

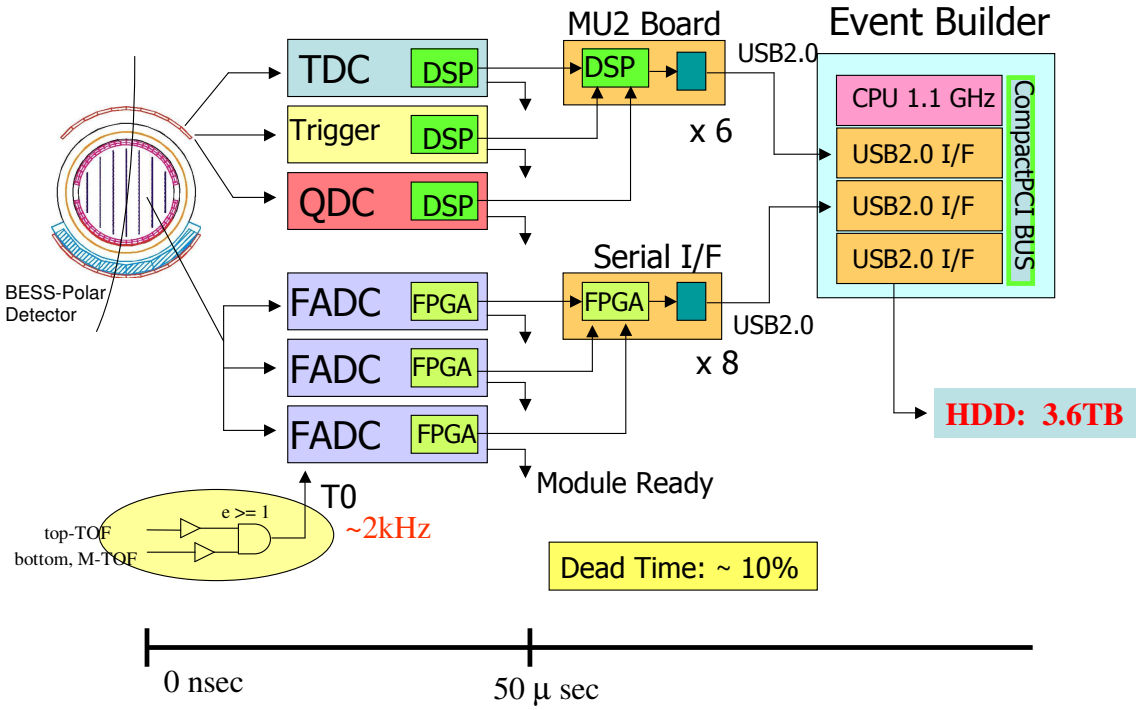

Figure 1. A block diagram of the BESS-Polar DAQ system.

The time-to-digital converter (TDC) boards incorporate fast discriminators and common-stop time digitizers to detect signals from the top and bottom TOF and middle TOF (MTOF) and measure their arrival times. The output pulses from the discriminators are also fed into the trigger. The TDCs have a full range of 150 nanoseconds and a resolution of better than 43 picoseconds for measured times up to 100 nanoseconds. For the top and bottom TOF, PMT anodes are coupled directly to the TDCs. For the MTOF, dynode signals are coupled to the TDC through an inverting amplifier with a gain of ten and a bandwidth of more than 1 GHz.

Figure 2 shows the block diagram of the TDC board's digital section. The program for the DSP is burned onto

a FLASH ROM (28F160B3, Intel) using the DSP emulator (XD510 USB JTAG Emulator, Spectrum Digital, Inc.) through a JTAG port. The DSP is booted at power-on time by reading the program from the FLASH ROM and initializing the board [6]. The data digitized at the analog section is read by the DSP through the FPGA (EPM7256AET, ALTERA). The DSP packs the data of 12 channels and sends them to the MU2 board. The event processing time for one event is about 30 microseconds. Figure 3 shows a photo of the actual TDC board. Careful use of ECL components only where absolutely required for timing performance resulted in a power consumption of less than 0.5 W per channle for the TDC. It corresponds to 1/3 of the previous BESS TDC.

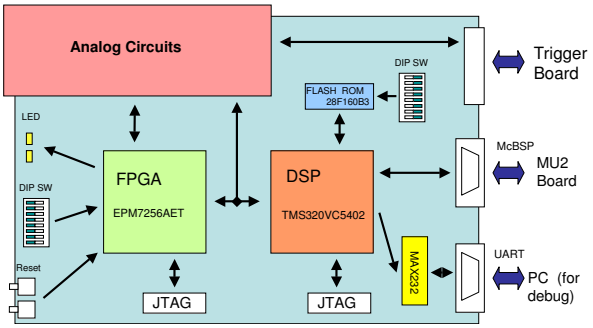

Figure 2. A block diagram of the TDC board (digital section)

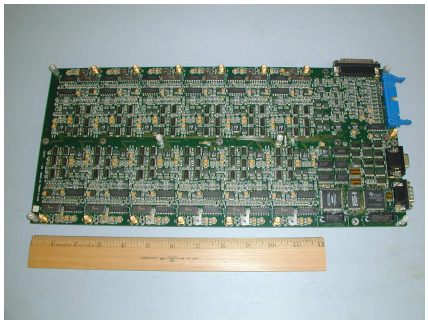

Figure 3. A photograph of the TDC board with ruler.

Figure 4 shows a linearity test result of the TDC board using Phillips Scientific PS7120 (a precision charge and time generator). The result showed good linearity over all TDC channels.

The charge-to-digital converter (QDC) measures the integral charge of PMT signals from the ACC, TOF and MTOF. The QDCs can be set to measure negative charge pulses from the PMT anodes (ACC and MTOF) or positive pulses from the PMT dynodes (TOF). The full-scale ranges of the QDCs is tailored to match the needs of individual detectors and are set at 250 picocoulombs for the ACC, 1000 picocoulombs for the outer TOF, and 2000 picocoulombs for the MTOF. Sixteen bit digitizers are used and in bench tests using a precision charge pulser, the QDCs have demonstrated a good linearity and a resolution of better than two bits (LSB). With a PMT of flight event rate, the effective dynamic range is 12 bits mostly due to a recharge time constant of the PMT base. The power consumption of the QDC is about 0.16 W per channel. It corresponds to 1/2 of the previous BESS QDC.

The trigger board receives the discriminator outputs from the TDC boards, generates a T0 trigger based on a programmable coincidence and distributes the T0 trigger to all FEEs. Also a periodic T0 trigger is issued, using the internal clock, to evaluate the FEEs performance during the flight. Since FEEs send the data to the event builder independently, the trigger board distributes an 8-bit event number in order to synchronize each data segment of one event in the FEEs. A scaler on the trigger board counts the discriminator outputs from each channel on the TDC boards. These scaler values are sent as monitor data to the ground in every 15 seconds. Any noisy PMTs can be removed from the coincidence pattern by command from the ground.

The event-builder subsystem board (MU2 board) acts as a mediator between the FEEs and the CompactPCI embedded system. Up to three FEEs are connected to one MU2 board through Multichannel Buffered Serial Ports (McBSPs), then connected to the CompactPCI embedded system through USB 2.0.

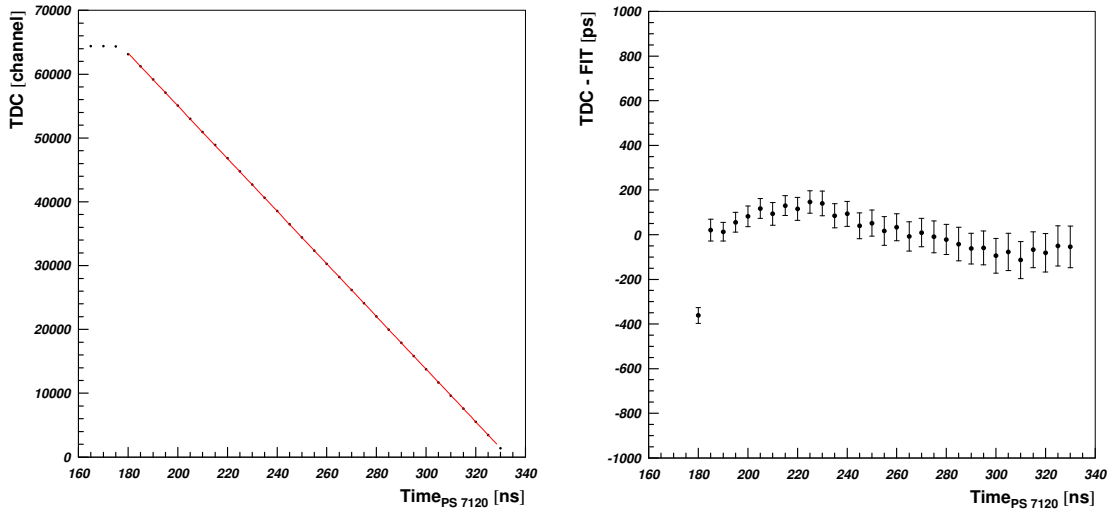

Figure 4. A linearity test result of the TDC board. The left side is a plot of TDC channel versus input delay time (offset is about 180 ns) using the PS7120 with fitted line (2.42 ps/channel). The right side shows the deviation from the fitted line. The error bar represents the time resolution for a given delay.

3. Summary

We have developed FEEs for the BESS-Polar TOF and ACC adapted to the new DAQ system. Pursuing a low power consumption, we have realized less than 0.5 W per channel for the TDC board and 0.16 W per channel for the QDC board. These correspond to 1/3 of the previous BESS TDC and 1/2 of the previous BESS QDC respectively. These systems were flown nearly 9 days around Antarctica successfully recording 900 million cosmic-ray events [7].

4. Acknowledgments

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