ICRC'07

Mérida, México

4th generation of the 1st level surface detector trigger in the Pierre Auger Observator

Z. SZADKOWSKI[1,2]

[1]*Department of Experimental Physics, University of Łódź, Pomorska 151, 90-236 Łódź, Poland.*
zszadkow@kfd2.phys.uni.lodz.pl

Abstract: Huge progress in electronics and new challenges and expectations on physics caused a considering of higher sampling rate and of new types of triggers, which now could be easily implemented into modern FPGA and which were unattainable in currently used FPGA in the Auger South. Much higher sampling rate would significantly improve an analysis accuracy of very inclined and horizontal showers, interesting as potentially generated by neutrinos For currently used sampling rate of 40 MSps the FADC traces for these showers show almost instantaneous jump from the noise level to the maximal value corresponding to the narrow muonic front generating sharp short signals in the PMTs. Various analysis based on rising times of FADC-traces in a trigger region are limited by poor time resolution, if the signal changes in a maximal way in the single time bin. New FPGA with much more resources and newer architecture allows implementing sophisticated signal processing algorithms, e.g. spectral triggers. The paper describes a proposal of the new generation of the Front-End-Board equipped with the powerful FPGA Stratix II and dual-FADCs working parallel in a interlaced mode with an effective sampling rate of 160 MSps.

Introduction

The Pierre Auger Observatory is the international experiment for research on ultra-high energy cosmic rays (UHECR) above 10^{19} eV and currently the world largest hybrid experiment. Hybrid techniques: the detection of particles at ground in water Cherenkov detectors (WCD) and measurements of correlated fluorescence light generated in the atmosphere by the Extensive Air Showers, gives an unique possibility cross-calibration and measurement uncertainties reduction. The surface array on a triangular 1.5 km grid will finally contain 1600 surface detector stations distributed over 3000 km^2 on Southern hemisphere (Argentina, under construction since 2000, 1400 tanks already deployed with full operational electronics) and 4000 WCD distributed over 10000 km^2 on Northern Site (Colorado, deployment planned since 2008).

Each surface array station is a solar powered water Cherenkov detector, instrumented with low power electronics and communicates with the Central Data Acquisition Station (CDAS) via a custom radio network. Low gain and high gain (32 times larger) signals from three downward facing 9" PMTs are sent to the front-end electronics and via a 5 pole anti-aliasing filter with a cutoff at 20 MHz, digitized at 40MHz by 10-bit FADC. 300 MB/s samples stream is next processed in the trigger/memory system (TMS) [1].

The TMS analyses on-line the ADC-traces looking for interesting trigger patterns, stores the data in buffer memory, and interrupts the detector station micro-controller in case a trigger occurs. Full data package is transmitted on the CDAS request. A hierarchical event trigger has been implemented to select only interesting events and reject "noise" events in order not to exceed the rate constraints imposed by the station micro-controller, the communications link bandwidth, and the CDAS.

The TMS was originally planned as an ASIC, containing all functions in a single chip, together with the memories for fast and slow channels. Fast channels are designed for shower profile investigations; slow ones for investigation of the muon component and for calibrations. Incessant development of Field Programmable Gate Arrays (FPGAs) allowed using commercial chips and implementing advanced algorithms in them. The flexibility of the FPGA configuration reduced the risks

if some bugs were not found; algorithms were not fully optimized and allowed easier modifying them in the future if some new measurements were necessary.

The physics imposed a data recording of FADC-traces of selected events in all 6 channels with ca. 20μs. This time corresponds to duration of signals coming from the showers. A profile describing a shower FADC traces should show its most significant structure as precisely as possible. It should present not only data, since a trigger appears, but also data before a trigger to have a complete view of timing/amplitude dependence. The FPGA offers Embedded System Blocks (ESB) working in a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Each ESB can be configured in any of the following sizes: $128 \cdot 16$, $256 \cdot 8$, $512 \cdot 4$, $1,024 \cdot 2$ or $2,048 \cdot 1$. Larger memory blocks can be established by combining multiple ESBs. 19.2μs at 40 MHz sampling corresponds to 768 samples. The 768-word buffer has been divided into two different-task sub-buffers. The 1st sub-buffer is a circulating one; it permanently monitors incoming data and freezes them, when a trigger appears. The 2nd sub-buffer next receives data after a trigger and allows completing a full profile.

The 1st generation of the trigger based on the Altera® APEX™ EP20K200RI240-2 chip supported by a dual-port RAM IDT70V3569S5DRI (storing data for the slow channel) has been successfully used for the TMS in the Auger Engineering Array. However, the cost of the FPGA chip significantly exceeded the expected budget. The APEX™ chip allowed implementing fully fast buffers into the internal FPGA memory. The slow buffer was implemented as an external dual-port RAM [2].

The 2nd generation of the trigger based on a cost-effective ACEX® family, which offered inexpensive chips with sufficient resources of logic elements, but unfortunately insufficient internal memory. The signal path had to be split into two parallel paths performing synchronously. Two ACEX® chips were sufficient to perform all APEX tasks. The high gain fast channel was performed by ACEX_A, the low-gain fast channel by ACEX_B respectively. The slow channel remained almost the same and has been implemented into ACEX_A.

Triggers were generated from only 30-bits of high-gain channel in ACEX_A and next were transferred by additional I/O chain to ACEX_B to synchronously record data for low-gain channel. An additional I/O chain is necessary to reduce an influence of propagation times from inside the chip to the chip pins and next to the internal structure of the next chip. However, such a dual chips design requires additional mechanism of synchronization. Some parts of the code had to be duplicated into the adjacent chip. The Altera® ACEX® chips EP1K100QI208-2 reduced significantly the total cost, but at the expense of splitting signal processing into two parallel working chips that were synchronized with additional glue logic [3]. Ca. 800 Front-End-Boards equipped with ACEX® chips have been deployed in the Auger South array [3].

3rd generation of triggers based on newer architecture FPGA chips Altera® Cyclone™ EP1C12Q240I7 allowed merging functions of both ACEX chips again into a single FPGA [4] and improving the reliability of the TMS due to better FPGA network optimization as well as allowing implementation of new algorithms [5]. The 2nd half of Auger South array is equipped in the Cyclone™ chips.

4th generation of the Front-End-Board

Resources utilization in ACEX® chips reached 70% and 50% respectively. Practically there is no room to add new algorithms. Cyclone™ chips utilize 50% resources and there is a possibility to implement new algorithms, however still with 40 MHz sampling rate.

The new proposal AMIGA (Auger Muons and Infill for the Ground Array) is to show that the addition of a small area of SD stations with nearby buried muon counters at half or less 1.5 km spacing would allow a dramatic increase of the physical scope of the Auger Observatory, reaching lower energies at which the transition from galactic to extragalactic sources is expected. The infill array will require an addition of 66 surface detectors [6]. Huge progress in electronics and expectations on physics give a good opportunity to implement much newer advanced electronics, which will be also a test platform for the Auger North.

Higher sampling rate requires faster FADCs. However FADCs with a sampling rate above 100 MSPS are very power consuming. Also a PCB design is critical to transfer several tens bits from FADCs to FPGA with so high frequency. Practically, it is simpler to use dual FADCs working with interleaving mode e.g. AD9216 with 10-bit resolution and 105 MSPS speed or AD9248 with 14-bit resolution and 65 MSPS. Interleaving mode, when two clocks shifted on half of the period drive two FADCs, gives an effective sampling rate 210 MSPS and 130 MSPS respectively. AD9216/9248 are pin-to-pin compatible and allow preparing an universal PCB designed both for Auger TMS and also for radio detection purposes. In order to be compatible as much as possible with the currently used CDAS format, 10-bit sampling is kept, however the sampling is increased by the factor of 4 to 160 MSPS. 19.2μs investigating window would require 4 times longer data package. Because of bandwidth limitation the data size may be limited to 1536 words, which corresponds to an interval 9.6μs, sufficiently long for large part of events.

New PMTs configuration in planned tanks for Auger North, needed wider dynamic range of measured analog signals require higher FADC resolution 12- or 14-bits. The new PCB takes into account various possibilities of applications.

The selection of the new FPGA for the 4th generation of a trigger is a compromise between the speed, performance and the cost. Cost-effective Altera® families Cyclone II™ or Cyclone III™ would be good candidates however the speed seems to be not enough. The registered performance for the currently used AHDL code implemented into Cyclone II™ EP2C35F484I8 is merely on the level 100 MHz, less than for EP1C12Q240I7 from Cyclone™ family. Cyclone III™ chips with sufficient resources and industrial temperature ranges are expected on the market too late. Additionally the current status of the timing model is "preliminary". Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible. The preliminary status of the timing model does not allow selecting yet the Cyclone

III™ family as the successor of the Cyclone™ chips from the 3rd generation of the trigger, although big capacity and cost- efficiency is worth taking into account for the final design of the Auger North. Finally we decided on smaller chip from powerful Stratix II™ family EP2S15F484I4.

The Stratix II FPGA family is based on a 1.2-V, 90-nm, all-layer copper SRAM process and features a new logic structure that maximizes performance. EP2S15F484I4 offers 408 kbits of on-chip, TriMatrix memory for demanding, memory intensive applications and has 12 DSP blocks for efficient implementation of high performance filters and other DSP functions. DSP blocks can implement up to either eight full-precision 9x9-bit multipliers, four full-precision 18x18-bit multipliers, or one full-precision 36x36-bit multiplier with add or subtract features. DSP blocks significantly support new type of triggers based on the FFT [5] or DCT [7]. Stratix II devices support various I/O standards along with support for 1-gigabit per second (Gbps) source synchronous signaling with DPA circuitry. They offer a complete clock management solution with internal clock frequency of up to 550 MHz and up to 12 phase-locked loops (PLLs) as well as they are the industry's first FPGAs with the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm to protect designs. The adaptive logic modules (ALM) provide advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

Much bigger internal memory allows fully implementing the slow channel into the FPGA and removing the external dual-port RAM. Two DMA modes for fast and slow data transfered from the FPGA and dual-port RAM respectively to the micro-controller has been reduced to the single DMA mode at the expense of an additional stage in the hierarchical multiplexer in the FPGA output system. Previously used additional external

IDT70V3569S5DRI is the high-speed 16kx36 synchronous pipelined dual-port static RAM. Its capacity allowed buffering slow data in two buffers with a length of 8192 32-bit words each. Slow data were transferred to the μC via DMA and were used for calibration. The calibration process required a lot of data, which were analyzed in the μC after multiple DMA transfers. Actually, the size of the buffer is not critical. Shorter buffer requires more DMA transfers. The single calibration cycle takes ca. 1 minute. Splitting a DMA transfer on shorter DMA cycles does not affect on the calibration accuracy. Fast channel needs 96 kbits of the memory for the standard data length. For 160 MSPS data rate and 9.6μs investigating interval 192 kbits is needed. There is still more than 192 kbits free for the slow channel, which allows building a single slow 32-bit buffer with a length of 6144 words. The slow buffer has been implemented into the FPGA as the FIFO.

Still a lot free logic elements in the EP2S15F484I4 chip enable a change of the concept of the slow calibration channel. Currently the FPGA supports only a delivery of the calibration data for the μC. Full calibration calculations are the task of the relatively slow μC. Afterwards new calculated conditions (thresholds) are sent back to the FPGA. More natural and much more effective is to establish a full calibration process as the autonomous task of the FPGA adding the NIOS processor as the calculation unit. Currently used FIFO as the slow buffer could be used as an operational memory directly for NIOS microprocessor-type calculations.

Summary

Being developed the new Front-End-Board based on the new FADCs with the 105 MHz clocks working in the interleaving mode and supporting effective sampling rate of up to 210 MSPS together with the powerful Stratix II^{TM} EP2S15F484I4 as the single trigger/memory chip is designed for the ca. 100 surface detectors in the Infill Array (66 additional + ca. 34 regular tanks).

A flexibility of internal PLL configuration and the clocks control in the FADCs gives a possibility to sample the analog signal effectively by 4 FADCs with 4 clocks shifted to each other at $\frac{\pi}{2}$. With 14-bit resolution of AD9248 and final sampling rate 250 MSPS the FEB will be a good platform to apply its on the radiodetection, where both high sampling and high resolution are the factors [8]. Four clocks sampling requires merging two dual-FADCs to a single process. Effectively the FEB will be able to process three independent analog channels.

Acknowledgements

References

[1] Pierre Auger Collaboration, "Properties and Performance of the Prototype Instrument for the Pierre Auger Observatory", *Nucl. Instr. Meth.* **A523**, pp. 50-95, 2004.

[2] Z. Szadkowski, D. Nitz," Implementation of the first level surface detector trigger for the Auger Observatory Engineering Array", *Nucl. Instr. Meth.*, **A545**, pp. 624-631, 2005.

[3] Z. Szadkowski, "The concept of an ACEX® cost-effective first level surface detector trigger in the Pierre Auger Observatory", *Nucl. Instr. Meth.*, **A551**, pp. 477-486, 2005.

[4] Z. Szadkowski, K-H. Becker, K-H. Kampert, "Development of a New First Level Trigger for the Surface Array in the Pierre Auger Observatory based on the Cyclone^{TM} Altera® FPGA", *Nucl. Instr. Meth.*, **A545**, pp. 793-802, 2005.

[5] Z. Szadkowski, "16-point Discrete Fourier Transform based on the Radix-2 FFT algorithm implemented into Cyclone^{TM}FPGA as the UHECR trigger for horizontal air showers" *Nucl. Instr. Meth.*, **A560**, pp. 309-316, 2006.

[6] Auger Muons and Infill for the Ground Array, Design Report, Auger Collaboration Meeting, 22-28 Apr, 2007, Malarge, Argentina.

[7] Z. Szadkowski, "16-point DCT as the spectral 1st level surface detector trigger in the Pierre Auger Observatory", submitted to *Nucl. Instr. Meth.*, 2007.

[8] 4th Auger Radio Workshop, March 1-2, 2007, Forschungszentrum Karlsruhe, Germany.