

Electronics and data acquisition system of the extensive air shower detector array at the University of Puebla

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Abstract: Field programmable gate arrays (FPGAs) are playing an increasing role in DAQ systems in cosmic ray experiments due to their high speed and integration and their low cost and low power consumption. In this paper we describe in detail the new electronics and data acquisition system based on FPGA boards of the extensive air shower detector array built in the Campus of the University of Puebla. The purpose of this detector array is to measure the energy and arrival direction of primary cosmic rays with energies around 10^{15} eV. The array consists of 10 liquid scintillator detectors and 6 water Cherenkov detectors (of 1.86 m^2 cross section), distributed in a square grid with a detector spacing of 20 m over an area of 4000 m^2 . The electronics described also makes use of analog to digital converters with a resolution of 10 bits and sampling speeds of 200 MS/s to digitize the PMT signals. We also discuss the advantages of discriminating the PMT signals inside the FPGAs with respect to the conventional use of dedicated discrimination circuits.

Introduction

The hybrid extensive air shower detector array at UAP (EAS-UAP) was designed to measure the lateral distribution of secondary particles for EAS in the energy region of 10^{14} - 10^{16} eV. These measurements allow a determination of the arrival direction, energy and mass composition of the primary cosmic ray for energies around the "knee" of the spectrum. Identification of the primary cosmic rays at these energies are expected to contribute to the understanding of the origin of the "knee" [1], whose nature remains a puzzle despite the fact that it was discovered 48 years ago [2].

The EAS-UAP array (19°N , 90°W , 800 g/cm^2) consists of 6 water Cherenkov and 18 liquid scintillator detectors distributed on a square grid with spacing of 20m, as shown in Fig. 1. For a detailed description of the experimental set up and preliminary results see [3-5].

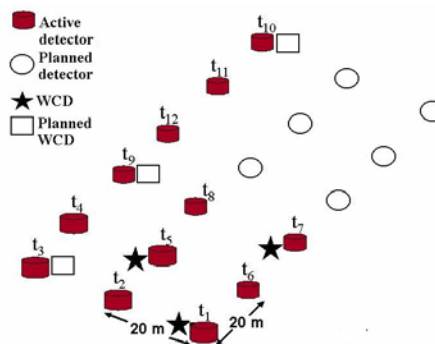


Figure 1: EAS-UAP array located on the Campus of the University of Puebla. Stars represent Cherenkov detectors filled with 2230 l of water and the cylinders represent scintillation detectors filled with 130 l of liquid scintillator.

In this paper we describe the new electronics system based on modern electronics based on field programmable gate arrays (FPGAs) that we have made to replace the old data capture system.

Present DAQ System

Figure 2 shows a photograph of the present control room of the EAS-UAP. The DAQ system is based on commercial CAMAC and NIM electronics modules in combination with several digital oscilloscopes to capture and process the signals from the PMTs of the water Cherenkov and liquid scintillator detectors.



Figure 2: Photograph of the present control room of the EAS-UAP detector array.

Figure 3 shows a print-out of the EAS-UAP DAQ program in which several traces from the PMTs of the detectors are visible. These traces are taken with 4 digital oscilloscopes and allow us to extract fine details of the temporal structure of the signals which can be used to implement methods to classify the muon/EM contents of extensive air showers [6-8]. Figure 4 shows a screen print-out of the EAS-UAP event display illustrating hits on the water Cherenkov (blue) and liquid scintillator (red) detectors.

The main reason behind the implementation of the present DAQ system was the fine detail on the the signals acquired with commercial digital oscilloscopes with typical sampling speeds of 1 GS/s. However, the transfer rates to move the signal traces from the oscilloscopes into the DAQ PC were very slow through a GPIB bus (about 1 event per second).

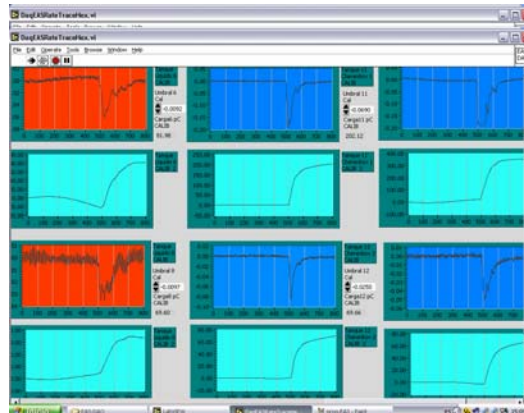


Figure 3: PMT traces from the EAS-UAP detectors as recorded by digital oscilloscopes in the present DAQ program.

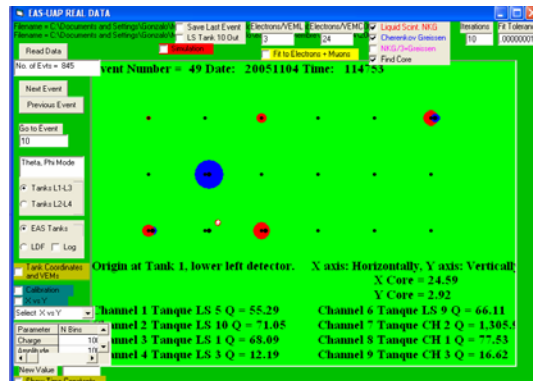


Figure 4: Screen print-out of the EAS-UAP event display illustrating hits on the water Cherenkov (blue) and liquid scintillator (red) detectors.

New DAQ System

Modern electronics based on on-chip fast analog to digital converters (ADCs) and powerful digital signal processors (DSPs) are ideal to be the basis of custom-made DAQ systems which are much more flexible, faster and much cheaper than the traditional DAQ systems based on modular electronics. We took advantage of these recent developments, in particular in the area of very high integrated circuits in the form of ADCs and FPGAs: at the heart of the new system there is an ADC daughterboard running at 200 MS/s, see Fig. 5. This custom-made board contains two parallel-interface 10-bit

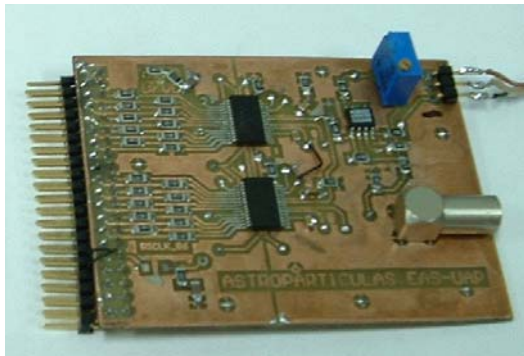


Figure 5: ADC daughterboard running at 200 MS/s. The two 10-bit ADC chips have a maximum conversion rate 100 MS/s.

ADC chips (AD9214) running at 100 MHz. They are clocked at the rising and falling edge of a 100 MHz clock on the motherboard to achieve the 200 MS/s sampling rate.

The control of the data acquisition process is done by an FPGA (Spartan 3 from Xilinx) on the motherboard whose firmware is custom-made using FIFO memories programmed on the FPGA with VHDL. Figure 6 shows a schematic diagram of the FPGA-based motherboard.

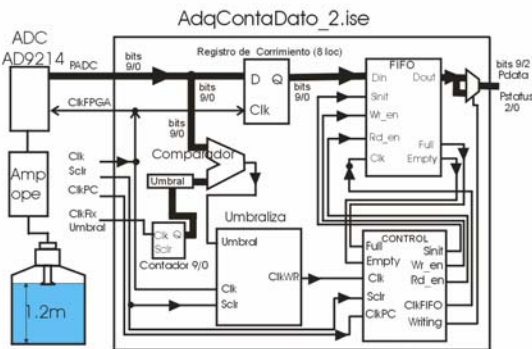


Figure 6: Schematic diagram of the new DAQ system of the EAS-UAP based on an FPGA-based motherboard.

Precision Timing

Each event is tagged with precise GPS time using a GPS embedded receiver with 1 PPS (one pulse per second) synchronized with the atomic clock on the GPS satellites within a corrected uncer-

tainty of 50 ns (Motorola Oncore UT+ module), as shown in Fig. 7.



Figure 7: Embedded GPS receiver used to attach a precise time tag to each event that passes the L2 trigger at the EAS-UAP array.

In addition to using the ADC motherboards described to digitize the signals of the PMTs, and the FPGAs to control all the digital operations of the DAQ system, including precise time to digital conversion, we are doing R&D on the use of the FPGAs to discriminate the analog signals. This is possible by using the low voltage differential signal (LVDS) standard for the inputs of the FPGA [9]. Figure 8 shows a daughterboard used to convey the analog outputs from the PMTs into the LVDS inputs of the FPGA.



Figure 8: Daughterboard used to provide a reference signal for each analog output of the PMTs and to convey the LVDS-like pair of signals into the LVDS inputs of the FPGA.

Conclusion

We have described the new DAQ system for the EAS-UAP air shower array. This new system takes advantage of the recent progress on on-chip fast ADCs and the ever faster and more powerful FPGAs. We have achieved “single channel” sampling rates of 200 MS/s at 10 bit by combing these modern advanced with the flexibility provided by on-chip programming using VHDL. The use of cheap GPS embedded receivers allows us to attach a precise time tag to each L2 trigger event for further off-line analyses.

Acknowledgements

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