Fast monolithic silicon pixel detectors in SiGe BiCMOS

The path to picosecond time resolution

LORENZO PAOLOZZI – DPNC SEMINAR

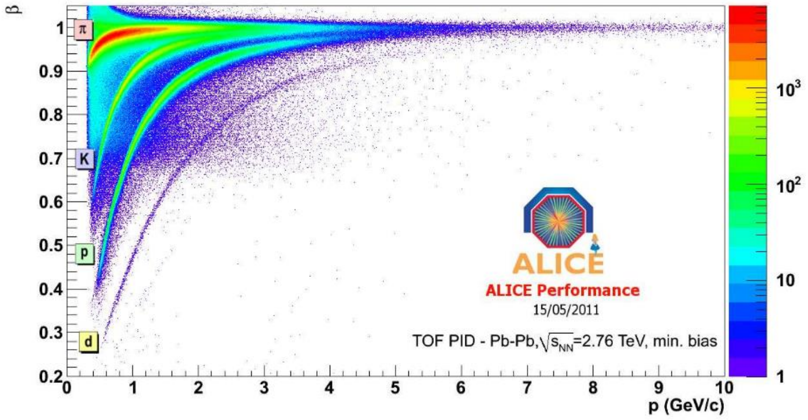
CERN
UNIVERSITÉ DE GENÈVE

Summary

1. **Precise timing in HEP and medical physics applications.**
2. Fast silicon pixel sensors in SiGe BiCMOS.
3. 4D tracking with monolithic silicon pixel sensors.
4. R&D at the University of Geneva.
5. The path toward picosecond time resolution.

Precise timing measurement in HEP

Particle identification



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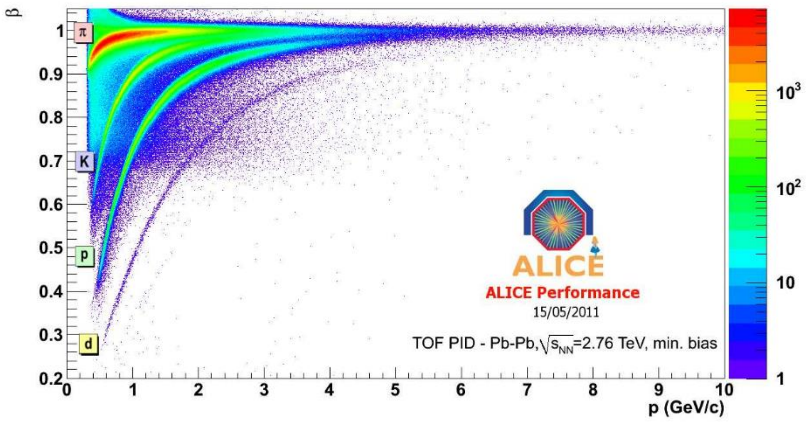
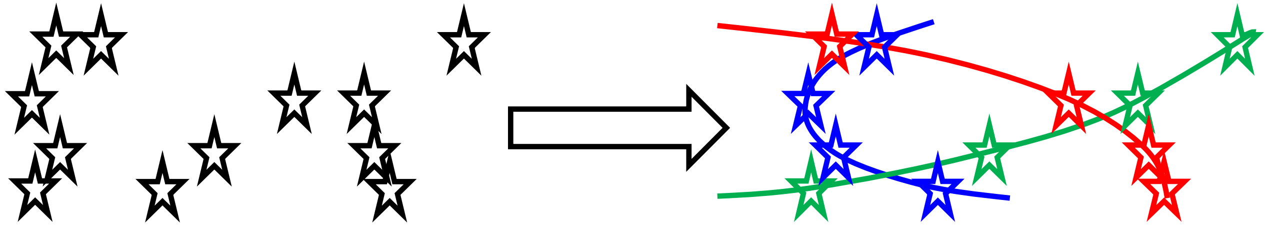


Support to fast tracking



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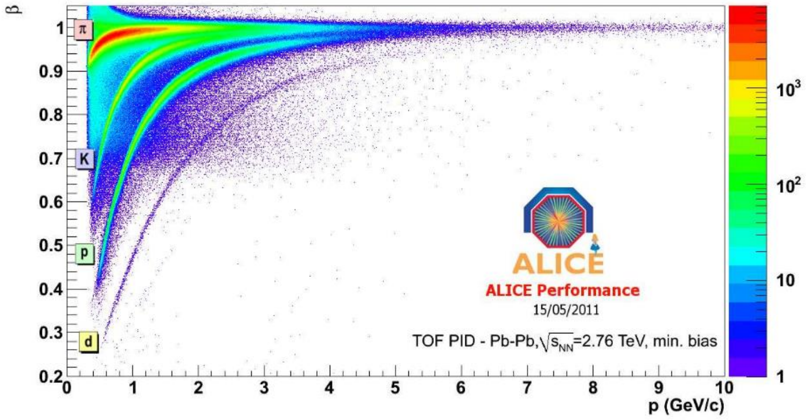
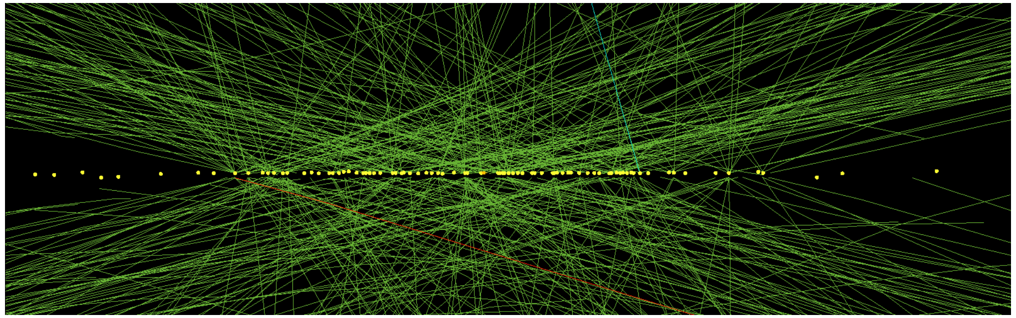


Pile-up suppression



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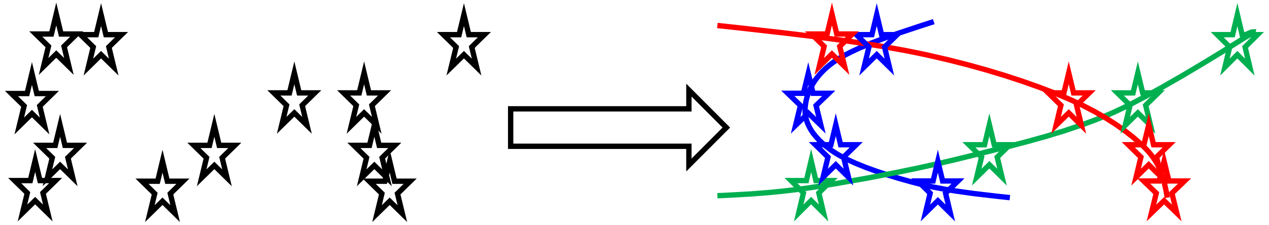
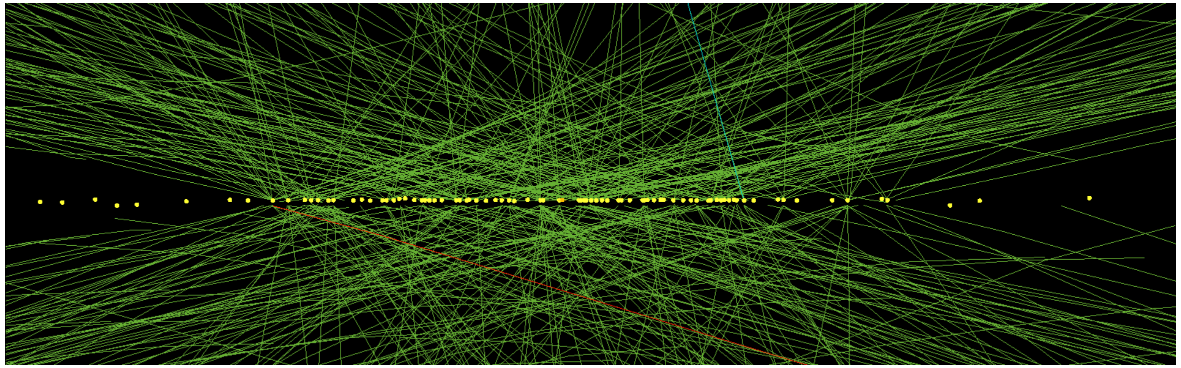


4D tracking for pile-up suppression

Hartmut F-W Sadrozinski *et al* 2018 *Rep. Prog. Phys.* **81** 026101

Without timing information



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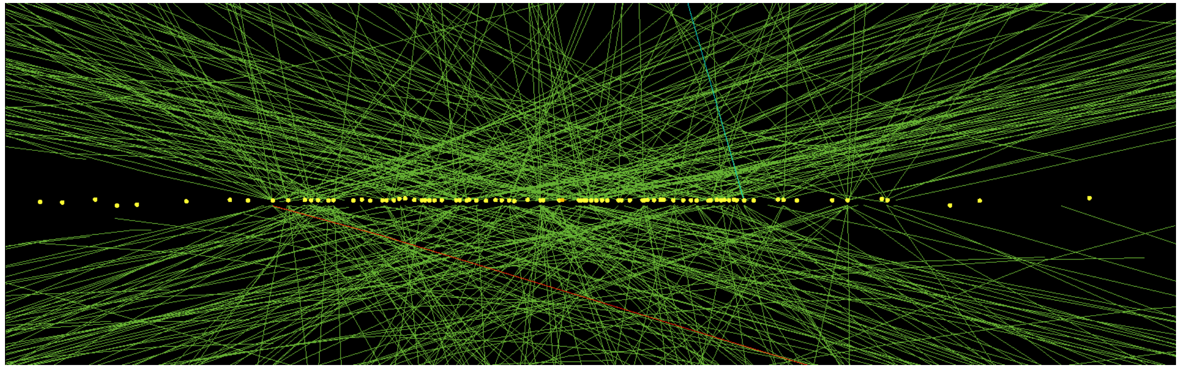

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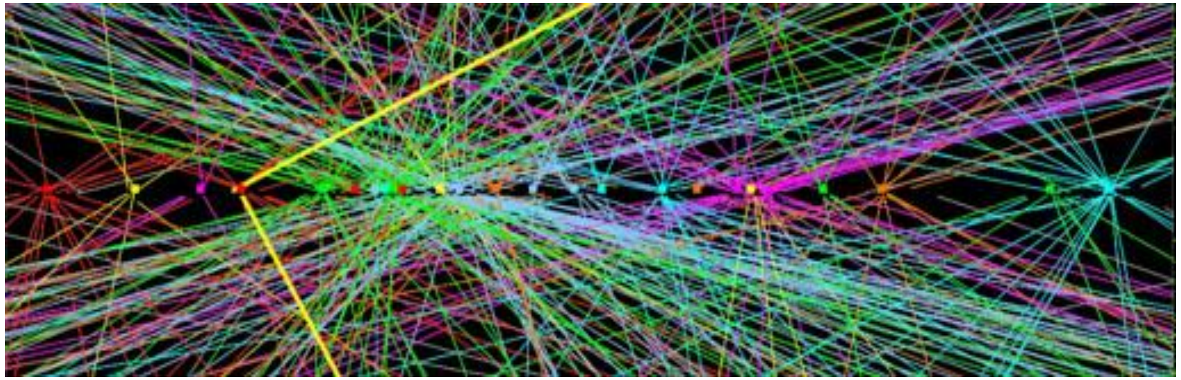

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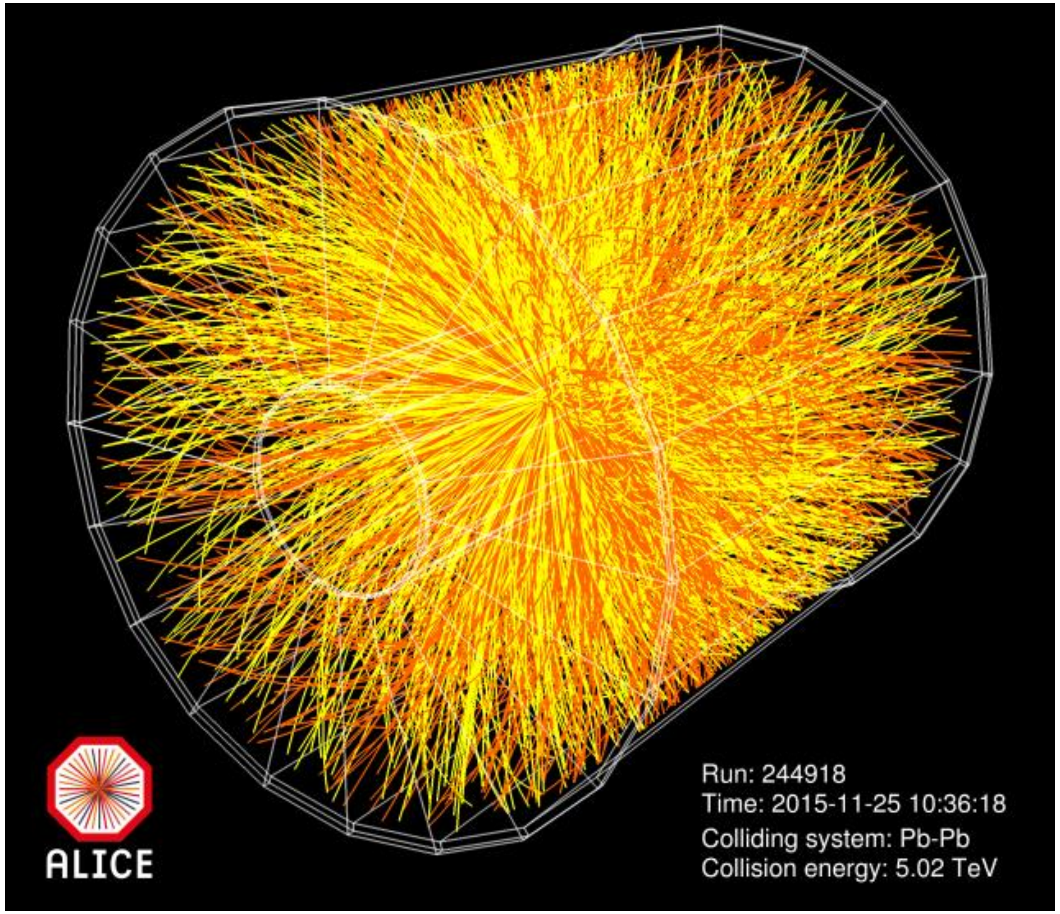
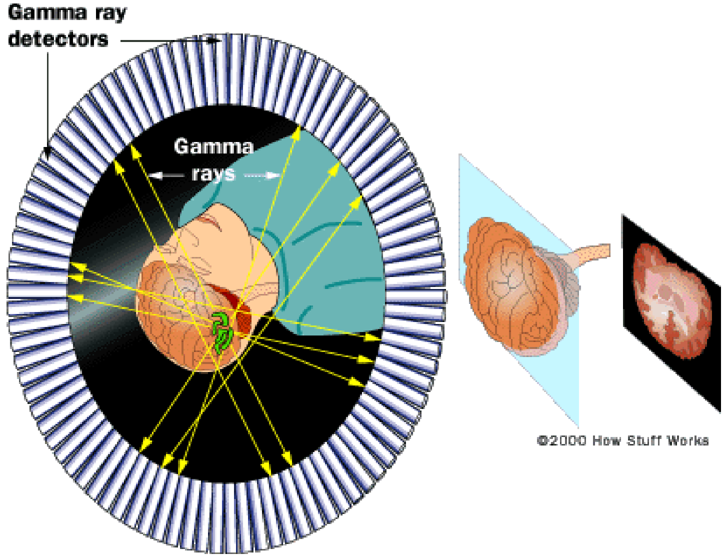
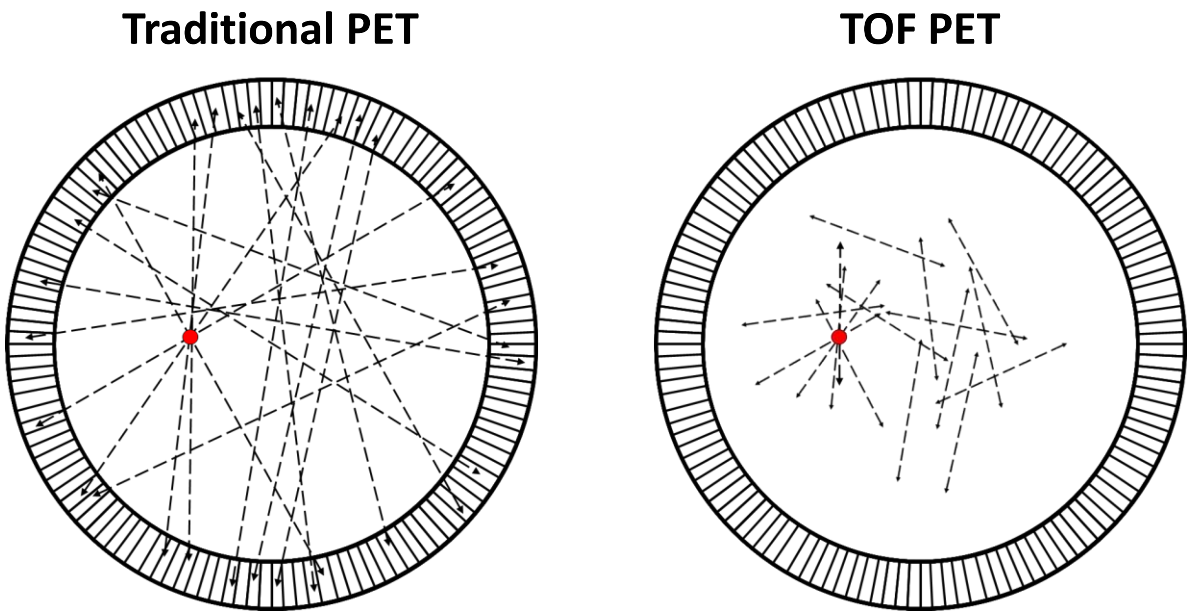


4D tracking for **ultra high-resolution medical imaging**

Positron Emission Tomography (PET)





- Improve signal-to-noise ratio.

- New possibilities in medical research.
- Greatly reduce radioactive dose in clinical PET.

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Precise timing measurement with silicon detectors

What are the main parameters that determine the time resolution of semiconductor detectors?

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$

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Precise timing measurement with silicon detectors

What are the main parameters that determine the time resolution of semiconductor detectors?

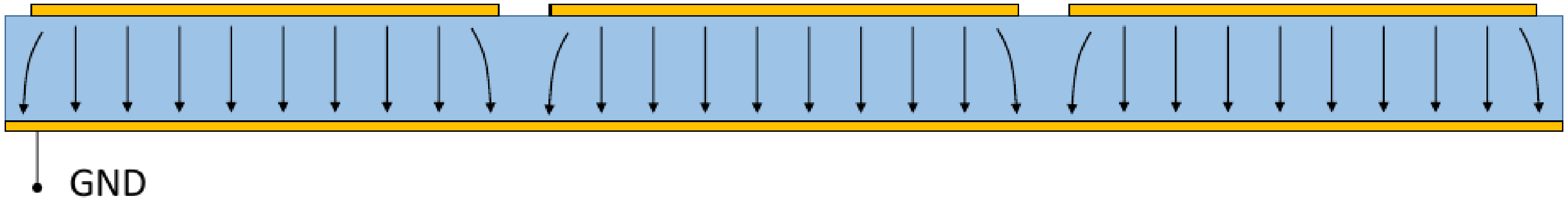
- Geometry and fields
- Charge collection noise
- Electronic noise

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$

1. Geometry and fields

Sensor optimization for time measurement means:
Sensor time response **independent** from the particle trajectory



→ "Parallel plate" read out: wide pixels w.r.t. depletion region

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

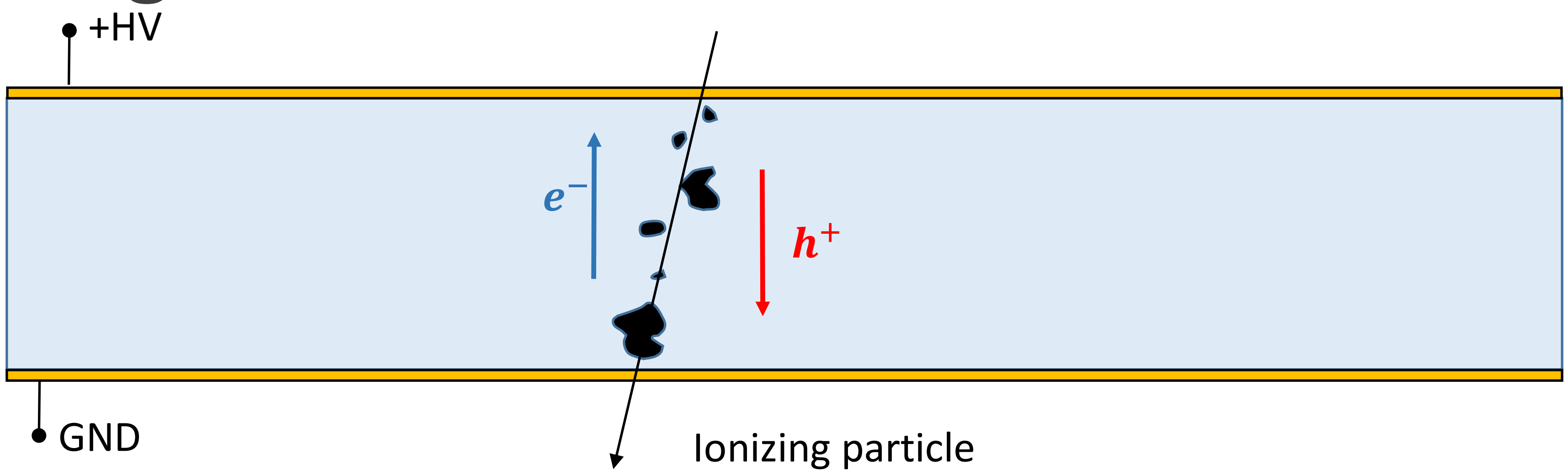
Scalar, saturated

Scalar, uniform

Desired features:

- Uniform **weighting field** (signal induction)
- Uniform **electric field** (charge transport)
- Saturated charge **drift velocity** (signal speed)

2. Charge-collection noise

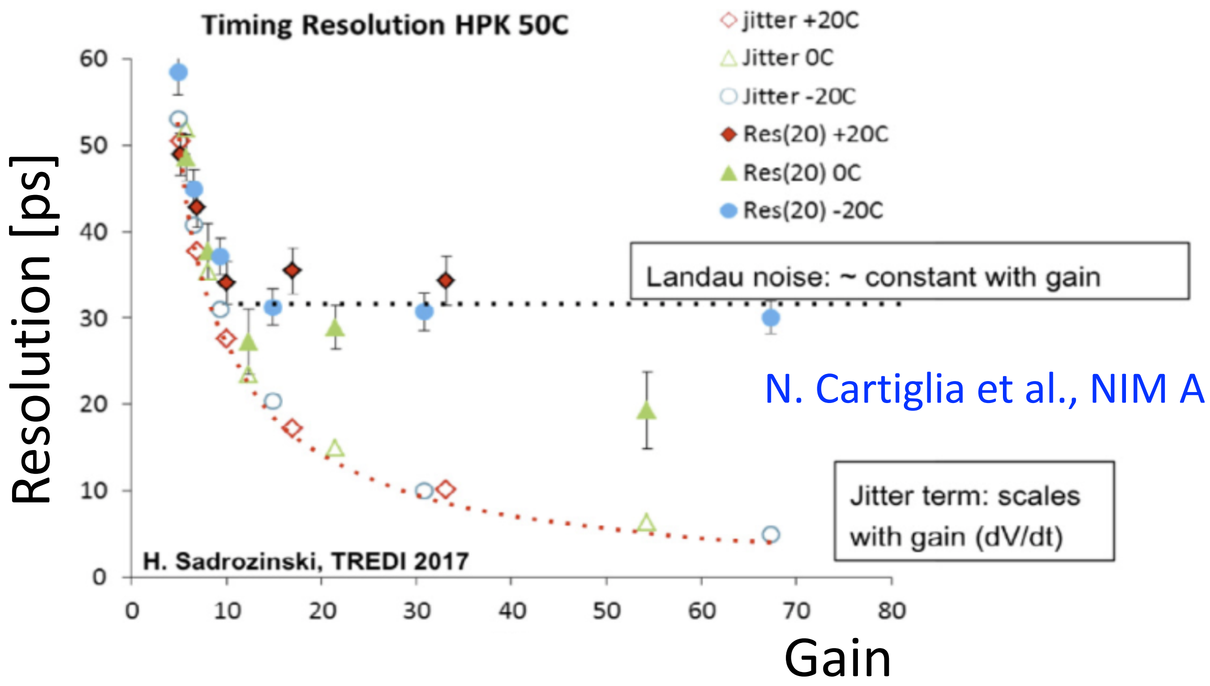


is produced by the **non uniformity of the charge deposition** in the sensor:

$$I_{ind} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

When **large clusters** are absorbed at the electrodes, their contribution is removed from the induced current. The **statistical origin** of this variability of I_{ind} makes this effect irreducible in PN-junction sensors.

2. Charge-collection noise



N. Cartiglia et al., NIM A 924 (2019) 350-354

Charge collection noise represents an intrinsic limit to the time resolution for a semiconductor PN-junction detector.

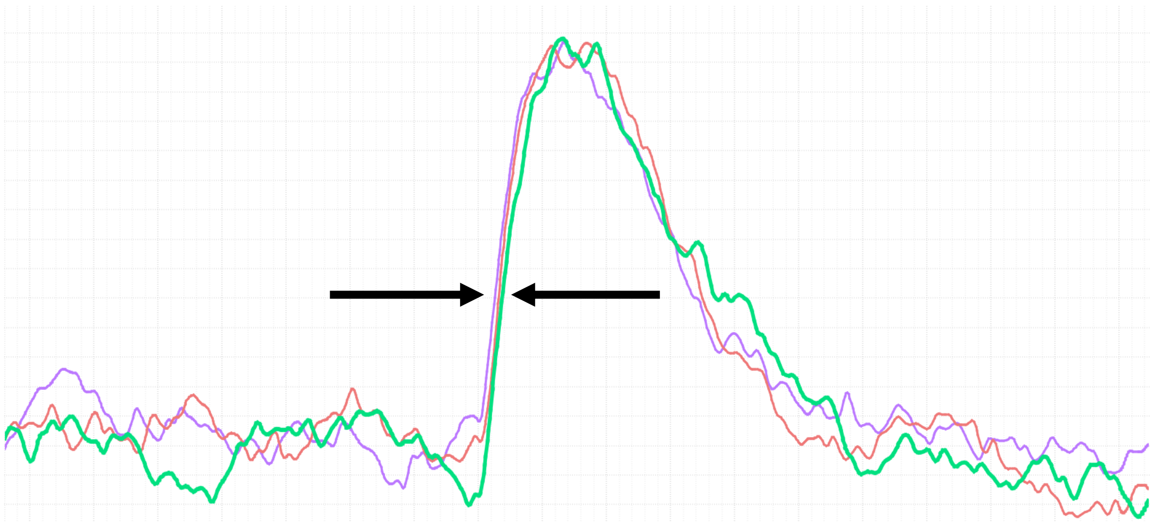
~30 ps reached by present LGAD sensors.

Lower contribution from sensors without internal gain

3. Electronic noise

Once the geometry has been fixed, the time resolution depends mostly on the **amplifier performance**.

Time jitter



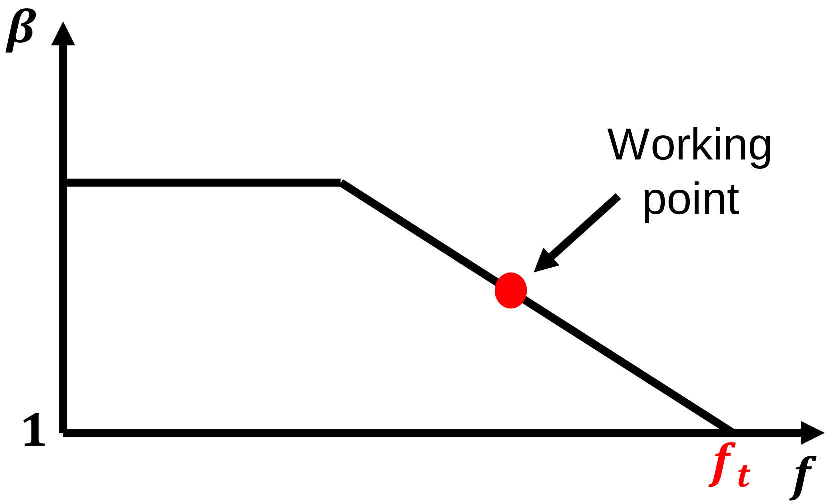
Fast integration

Reduce ENC: electronic performance

$$\sigma_t = \frac{\sigma_V}{dV/dt} \cong \frac{ENC}{I_{Ind}}$$

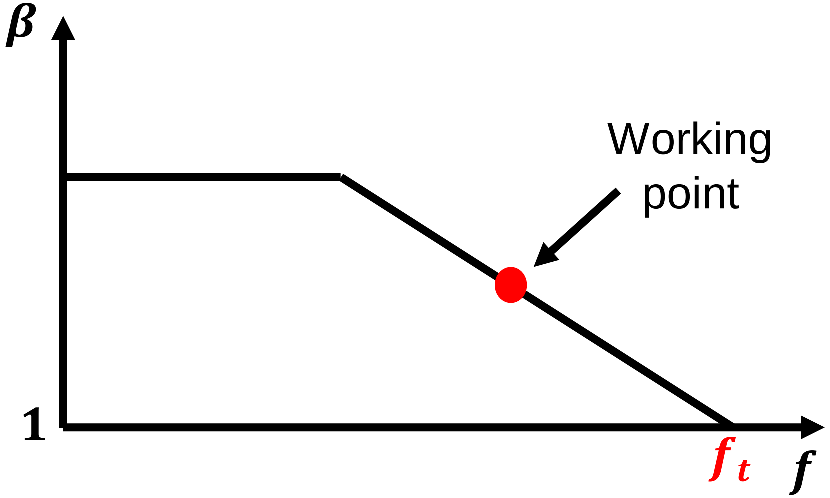
Increase signal: Avalanche

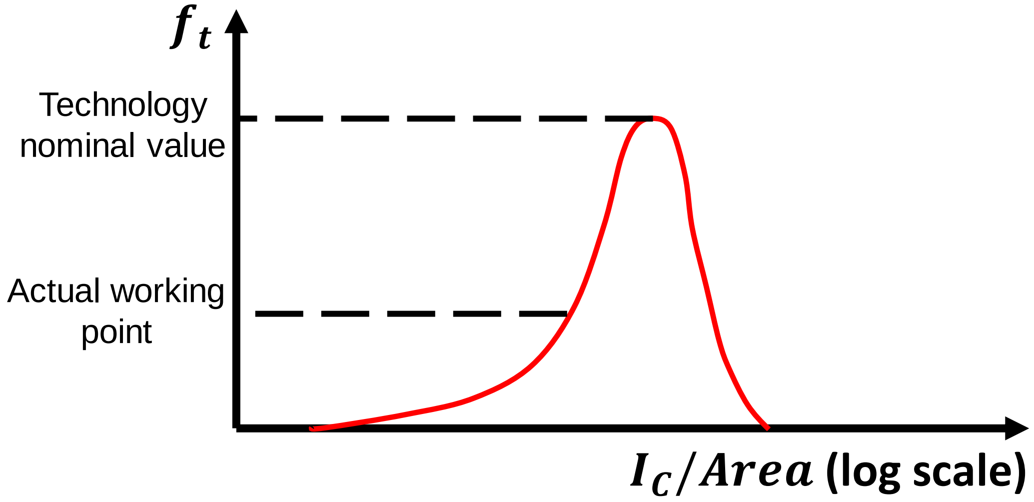
Current gain and power consumption



	$f_t = 10\ GHz$	$f_t = 100\ GHz$
β_{max} at $200\ MHz$	50	500
β_{max} at $1\ GHz$	10	100
β_{max} at $5\ GHz$	2	20

Current gain and power consumption





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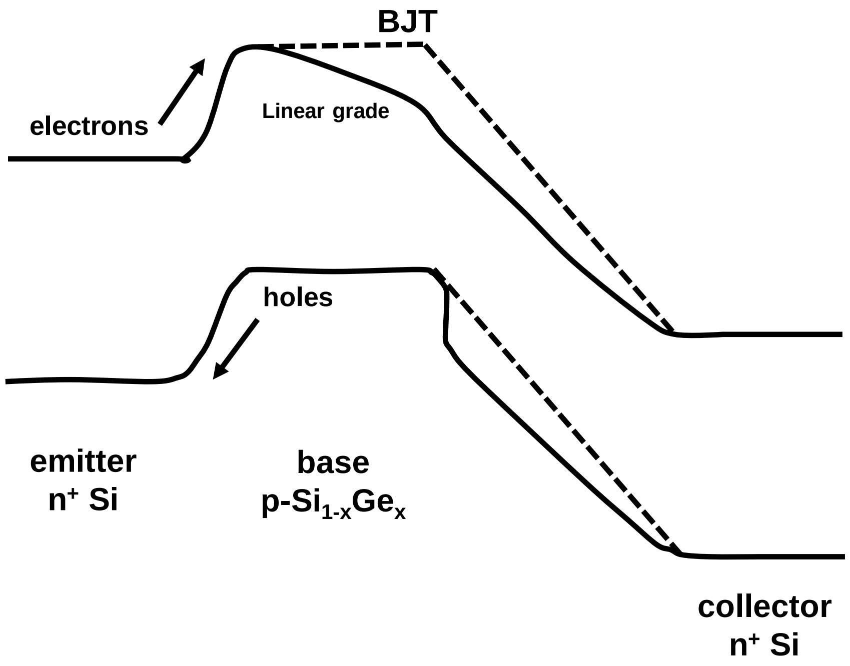
Trade-off: **ENC/σ_t** ⇔ **Power Consumption**

$f_t > 100\ GHz$ technologies are necessary for fast, low-power amplification.

SiGe HBT technology for fast amplifiers

In SiGe Heterojunction Bipolar Transistors (HBT) the **grading** of the bandgap in the Base changes the **charge-transport mechanism** in the Base from **diffusion** to **drift**:



Grading of germanium in the base:
field-assisted charge transport in the Base,
equivalent to introducing an electric field in the Base

$\Longrightarrow$ short e$^-$ transit time in Base $\Longrightarrow$ very high β

$\Longrightarrow$ smaller size $\Longrightarrow$ reduction of R_b and very high f_t

Hundreds of GHz

SiGe BiCMOS: A commercial VLSI foundry process

source: https://towerjazz.com/technology/rf-and-hpa/sige-bicmos-platform/

Some applications

- Automotive radars (27/77 GHz)
- Satellite communications
- LAN RF transceivers (60 GHz)
- Point-to-point radio (V-band, E-band)
- Defense
- Security
- Instrumentation

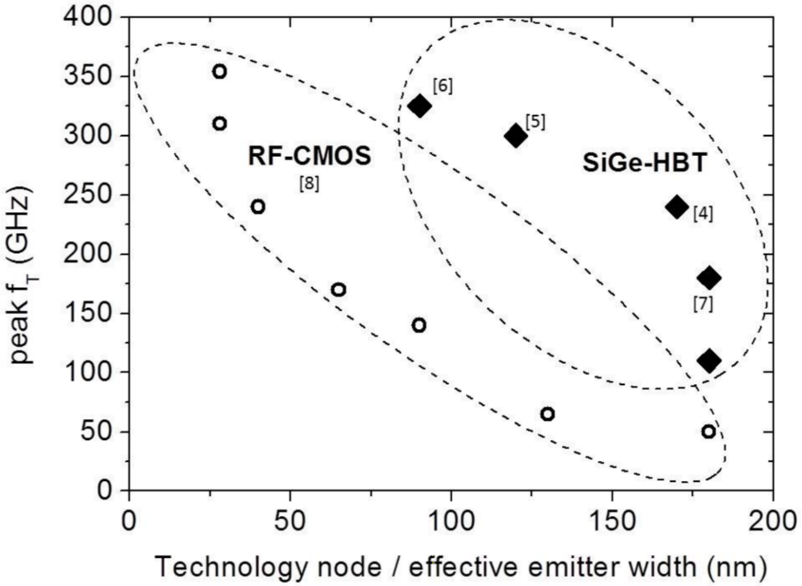
A **fast-growing technology: f_{max} = 700 GHz** transistor recently developed (DOT7 project, IHP microelectronics)

Some characteristics of SiGe

• Integrated in CMOS platforms	⟹	SiGe-HBT AND Si-CMOS
• Vertical transport device	⟹	Not as dependent on lithography as CMOS
• Cryogenic compatible	⟹	Silicon-based device operating at < 1 K
• Inherently rad. hard	⟹	Good radiation tolerance with standard processing
• High output current drive	⟹	Tolerance to parasitics

A comparison with CMOS technologies

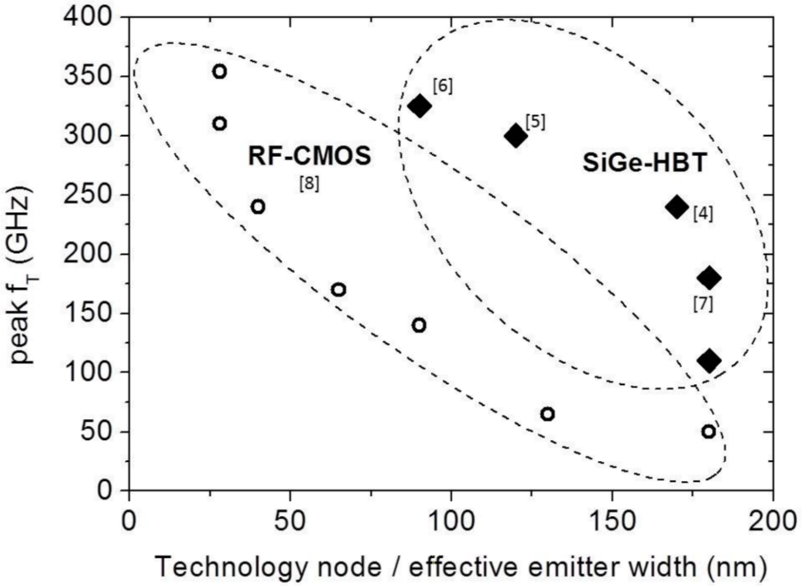
Intrinsic performance



A. Mai and M. Kaynak, SiGe-BiCMOS based technology platforms for mm-wave and radar applications.
DOI: 10.1109/MIKON.2016.7492062

A comparison with CMOS technologies

Intrinsic performance



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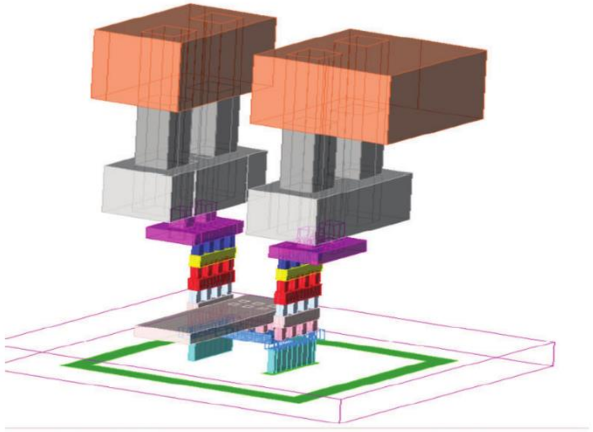
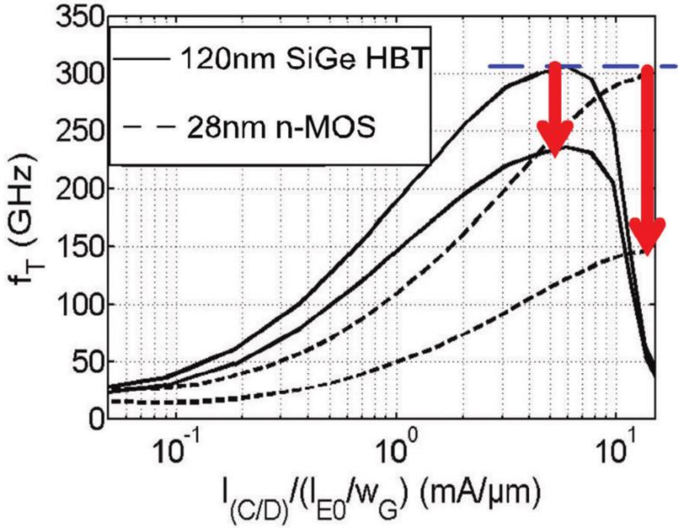
Robustness to parasitics

M. Schröter, U. Pfeiffer and R. Jain, Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling and Circuit Applications.





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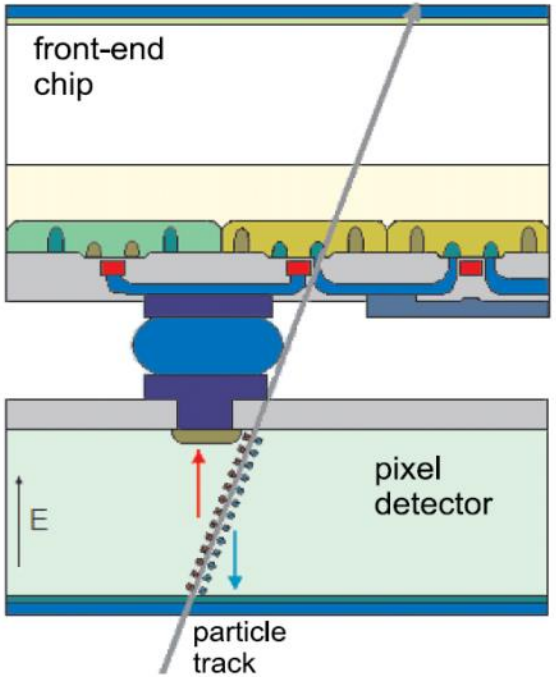
Monolithic silicon pixel detectors

Hybrid pixel detectors

Complementary Metal-Oxide-Semiconductor (CMOS) ASIC

Pixelated silicon Sensor



Pros: easier optimization of sensors and electronics
Cons: generally high production costs

Michael Moll. An introduction to silicon detectors with focus on high energy physics applications. SIM-Détecteurs 2014, September 2014, LPNHE Paris.

Monolithic silicon pixel detectors

Hybrid pixel detectors

Complementary Metal-Oxide-Semiconductor (CMOS) ASIC

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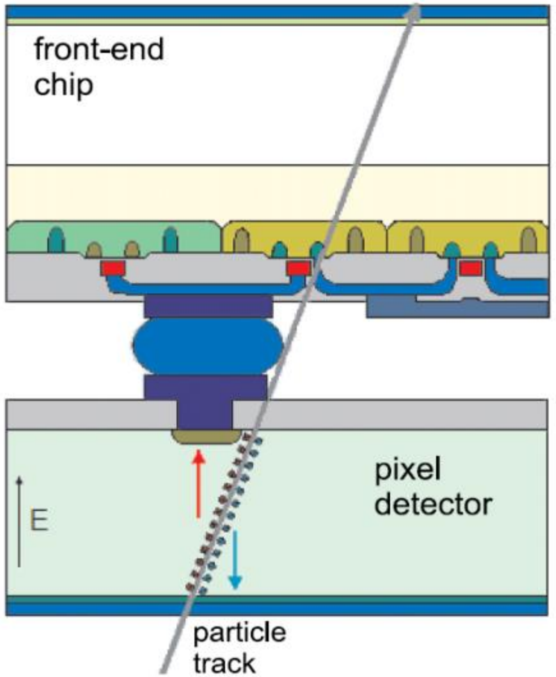

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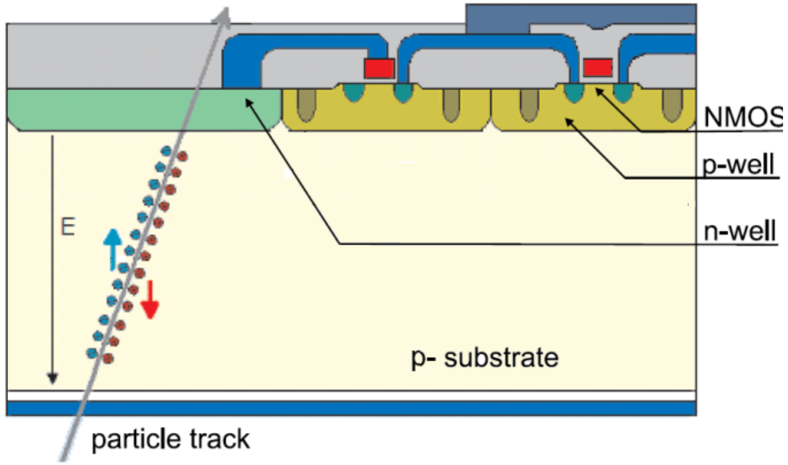
Monolithic pixel detectors

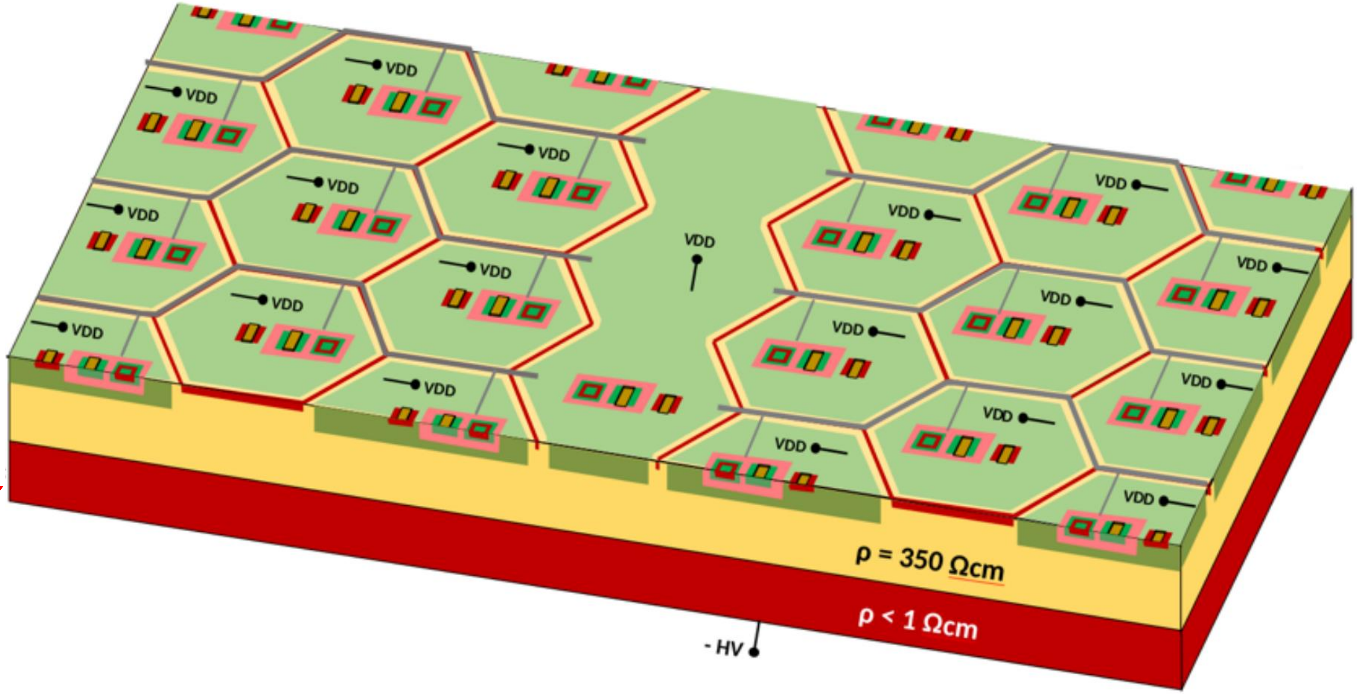
Sensor integrated in CMOS ASIC



Pros: lower production costs
Cons: more complex design

Michael Moll. An introduction to silicon detectors with focus on high energy physics applications. SIM-Détecteurs 2014, September 2014, LPNHE Paris.

Our recipe for monolithic design for 4D tracking



1. heavily P-doped substrate.

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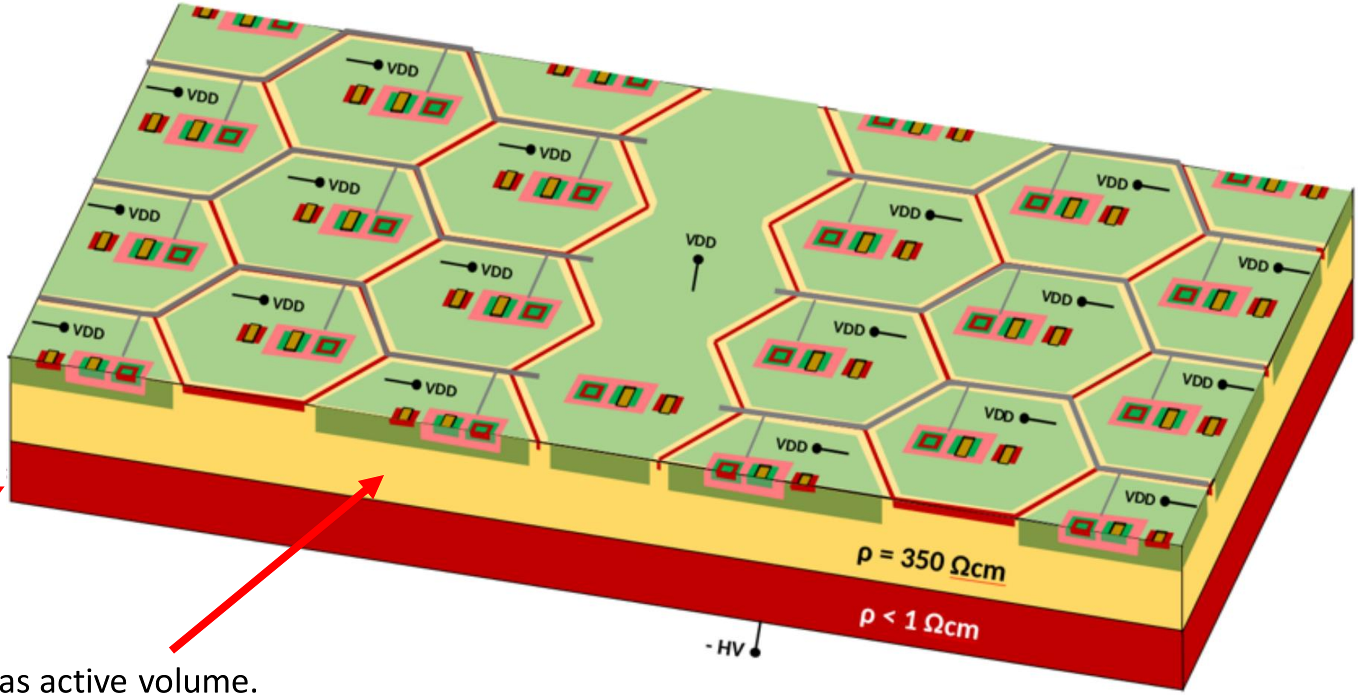

1. heavily P-doped substrate.

2. High resistivity epitaxial layer as active volume.

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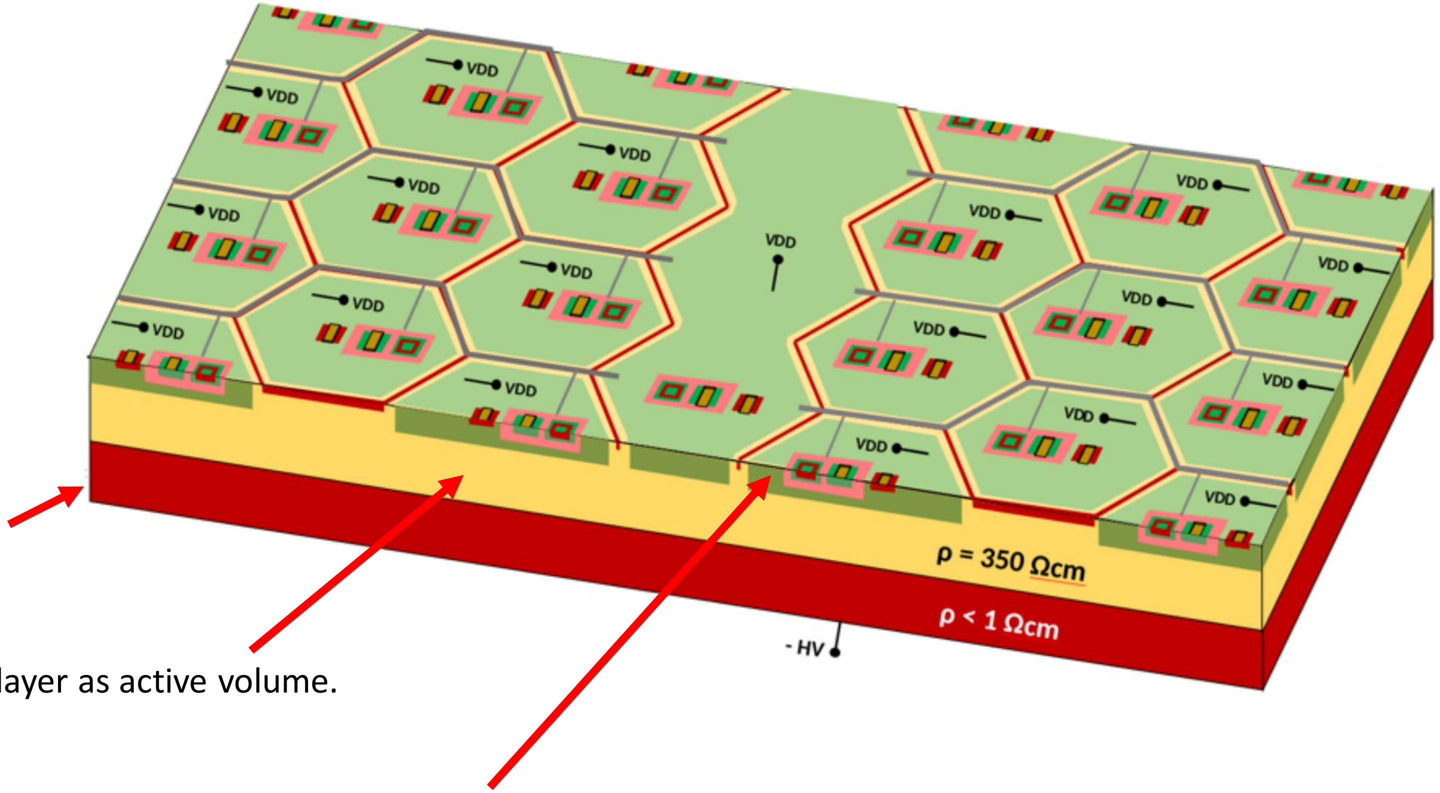

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3. Electronics inside the guard-ring, isolated from substrate using deep n-well.

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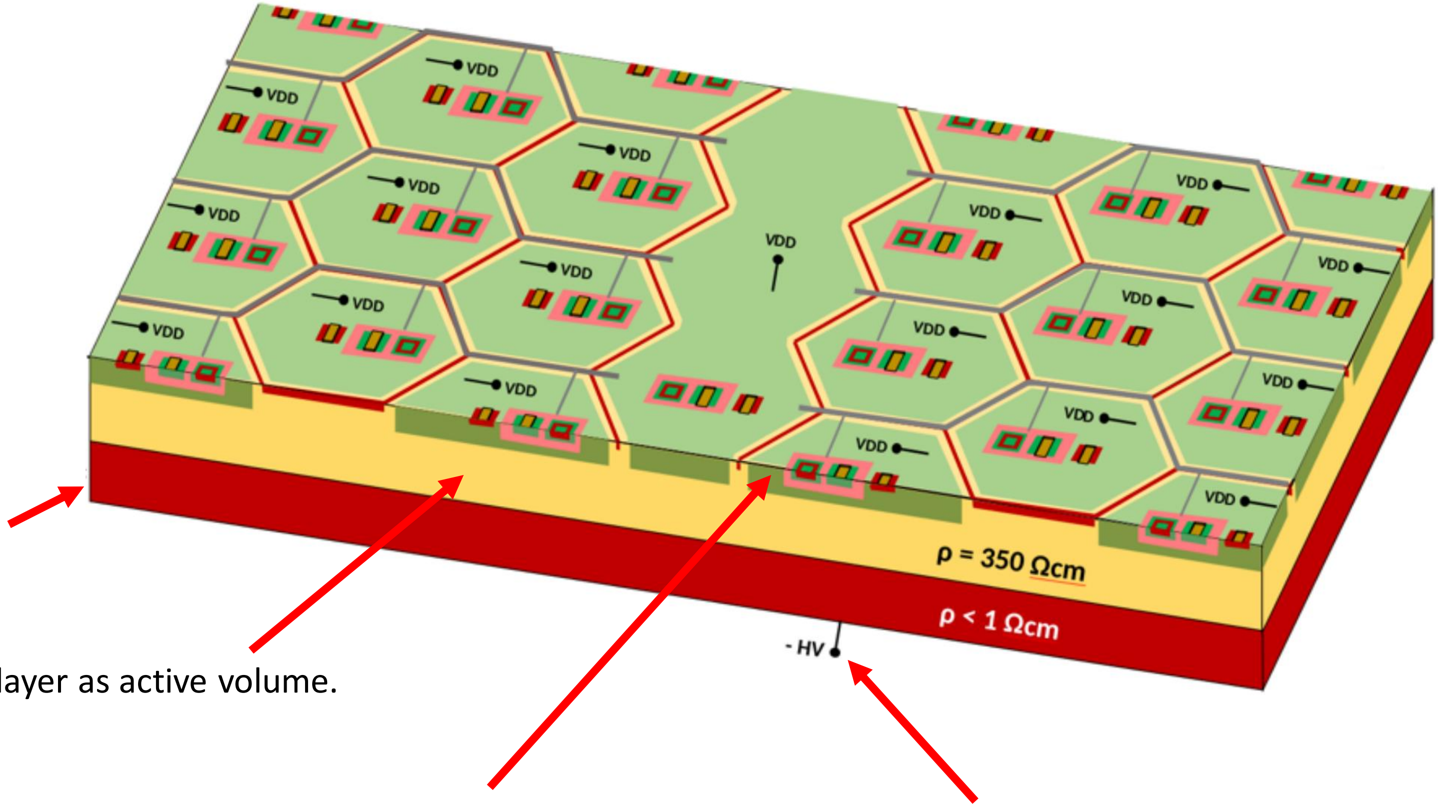

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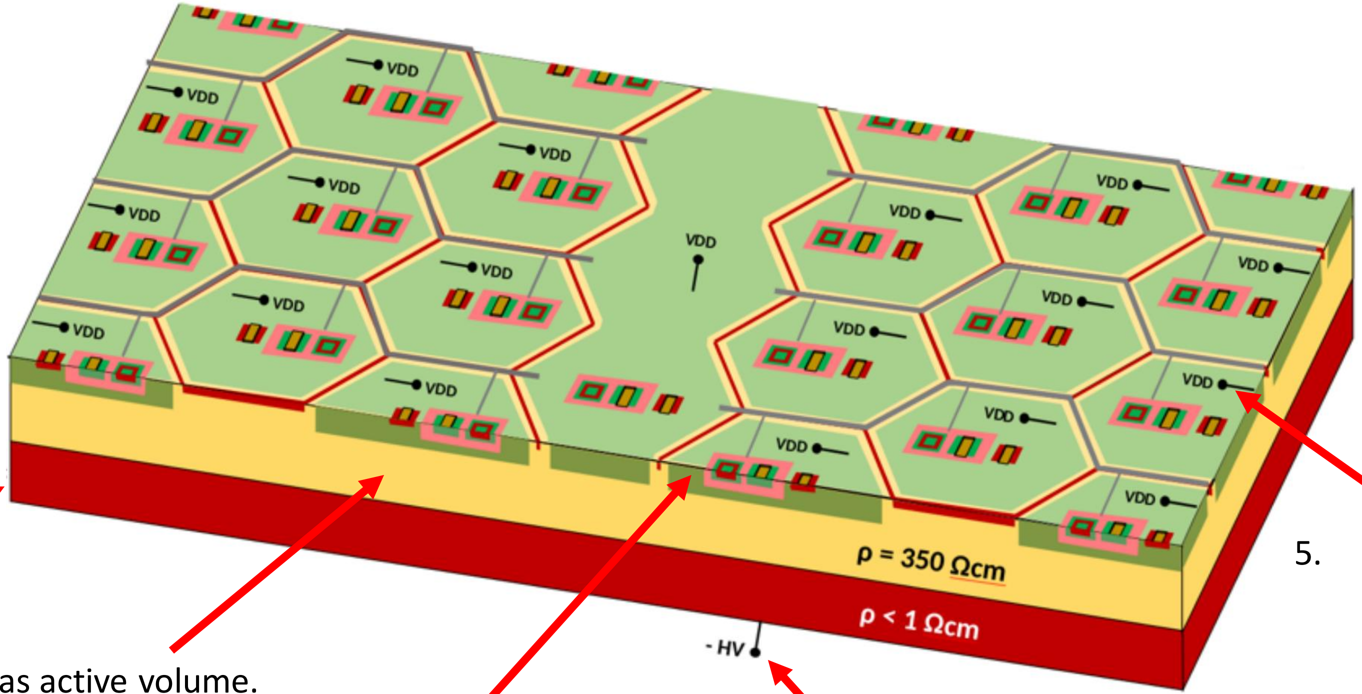
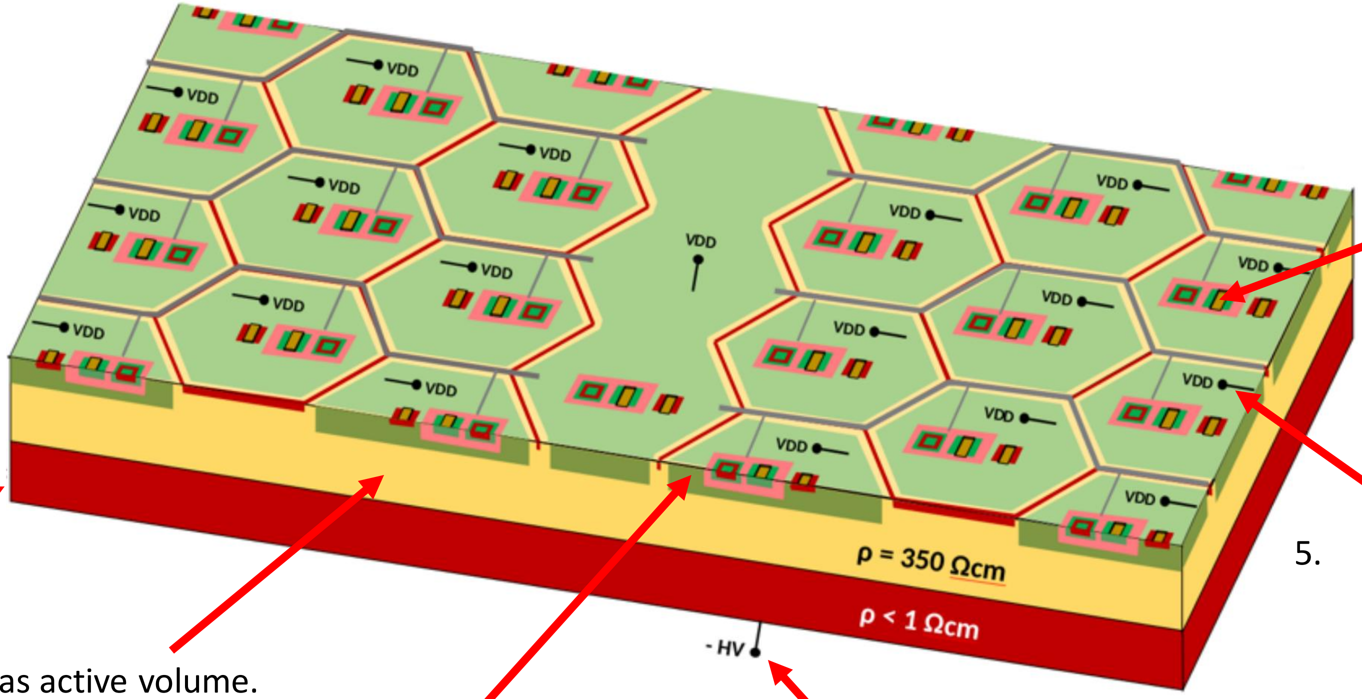


1. heavily P-doped substrate.
2. High resistivity epitaxial layer as active volume.
3. Electronics inside the guard-ring, isolated from substrate using deep n-well.
4. Negative High Voltage applied to the substrate.
5. Pixel and electronic deep n-wells are kept at positive low voltage.

Our recipe for monolithic design for 4D tracking



6. Analogue electronics in pixel.

1. heavily P-doped substrate.

5. Pixel and electronic deep n-wells are kept at positive low voltage.

2. High resistivity epitaxial layer as active volume.

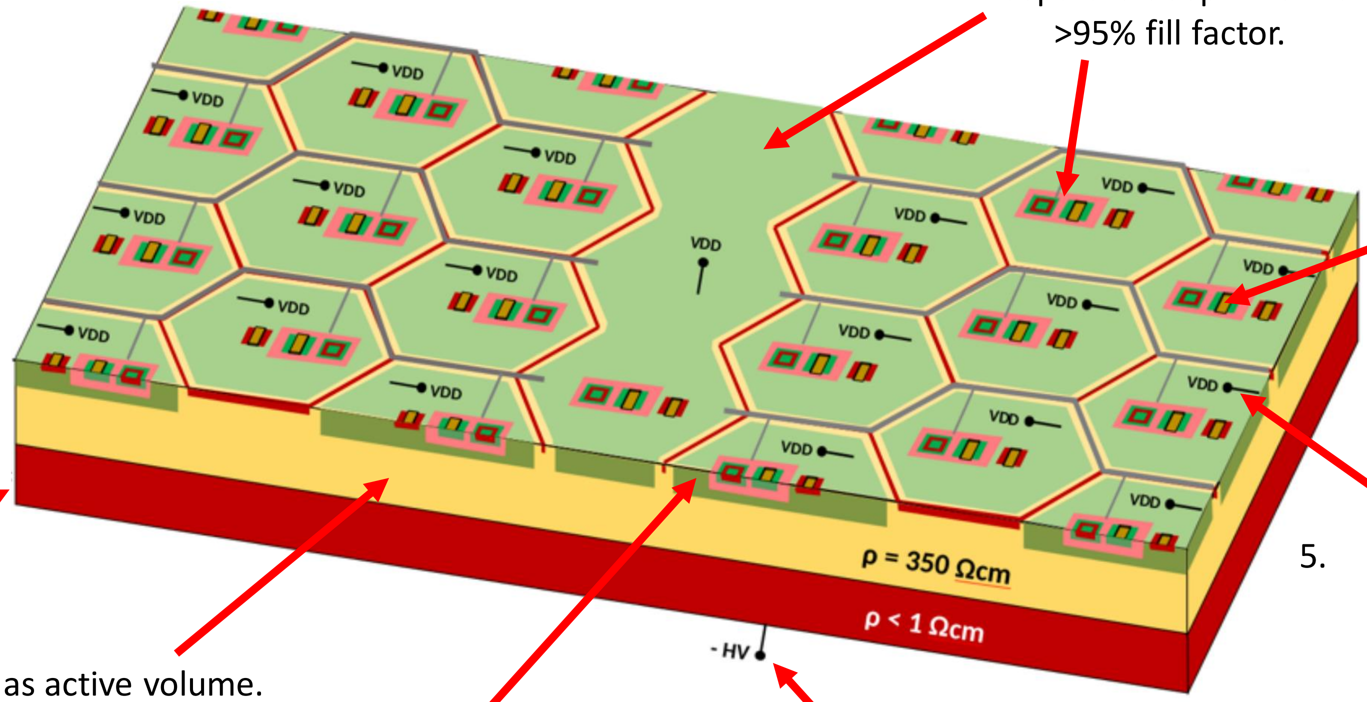
3. Electronics inside the guard-ring, isolated from substrate using deep n-well.

4. Negative High Voltage applied to the substrate.

Our recipe for monolithic design for 4D tracking

7. Digital electronics can be placed in pixel or in a separate deep-nwell to improve noise robustness.
   >95% fill factor.

6. Analogue electronics in pixel.



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SiGe group at UniGe

Giuseppe Iacobucci
- Project P.I.
- System design

Lorenzo Paolozzi
- Sensor design
- ASIC design
- System design

Roberto Cardella
- Sensor design
- ASIC design
- Laboratory test

Yana Gurimskaya
- Radiation tolerance
- Laboratory test

Fulvio Martinelli
- ASIC design

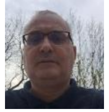
Magdalena Munker
- Sensor design
- Laboratory test

Mateus Vicente
- System design
- Laboratory test

Stefano Zambito
- System design
- Laboratory test

Stéphane Débieux
- Board design
- RO system

Yannick Favre
- Board design
- RO system



Didier Ferrère
- System integration
- Laboratory test

Sergio Gonzalez-Sevilla
- System integration
- Laboratory test

Rafella Kotitsa
- Sensor simulation

Chiara Magliocca
- Laboratory test

Matteo Milanesio
- Laboratory test

Théo Moretti
- Laboratory test

Antonio Picardi
- Analog electronics
- Laboratory test

Jihad Saidi
- Laboratory test

Main research partners:

Roberto Cardarelli
INFN Rome Tor Vergata
University of Geneva

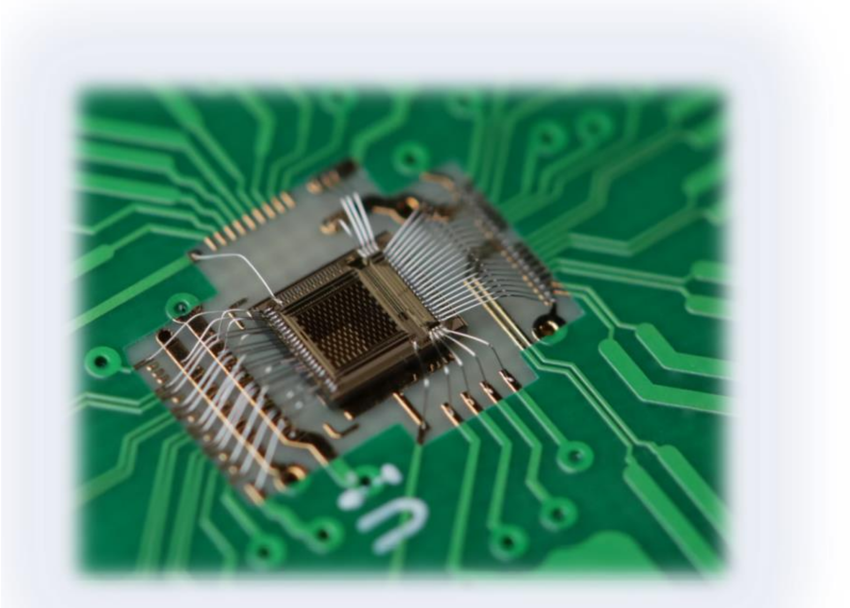
Holger Rücker
IHP Mikroelektronik

Marzio Nessi
CERN & UNIGE

Mehmet Kaynak
IHP Mikroelektronik

Ivan Peric
KIT

Bernd Heinemann
IHP Mikroelektronik



SG13G2 technology from IHP Microelectronics

Exploit the properties of state-of-the-art SiGe Bi-CMOS transistors to produce an **ultra-fast, low-noise, low-power consumption** amplifier

Leading-edge technology: **IHP SG13G2**

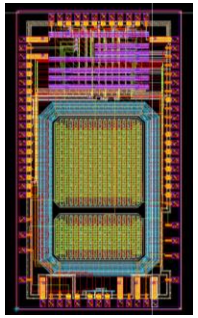
130 nm process featuring SiGe HBT with

- Transistor transition frequency: $f_t = 0.3\,THz$
- DC Current gain: $\beta = 900$
- Delay gate: **1.8 ps**

innovations
for high
performance
microelectronics

Leibniz-Institut für
innovative Mikroelektronik

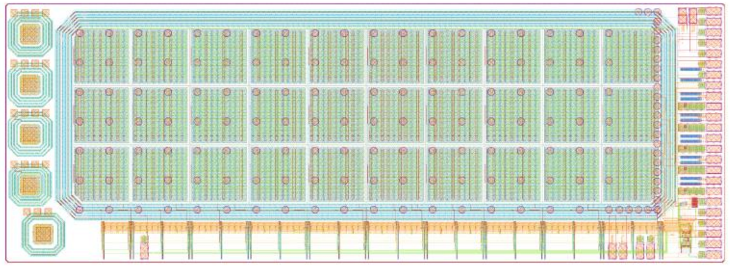
2016



200 ps

- 1 and 0.5 mm^2 pixels
- Discriminator output

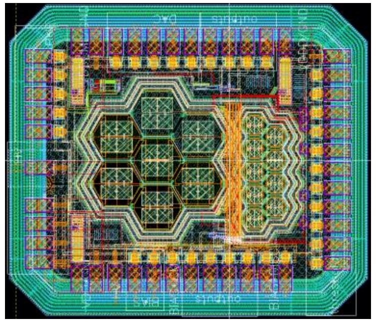
2017



100 ps

- 30 pixels 500×300 µm^2
- 100 ps TDC + I/O logic

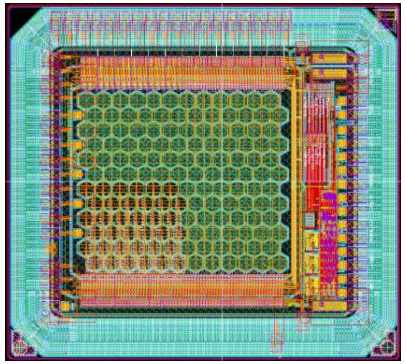
2018



50 ps

- Hexagonal pixels 65 µm side
- Discriminator output

2019

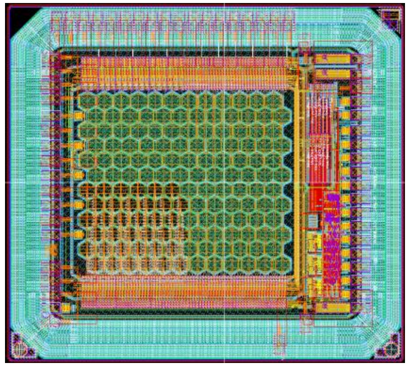


ATTRACT

36 ps

- Hexagonal pixels 65 µm side
- 30 ps TDC + I/O logic
- Analog channels

2021

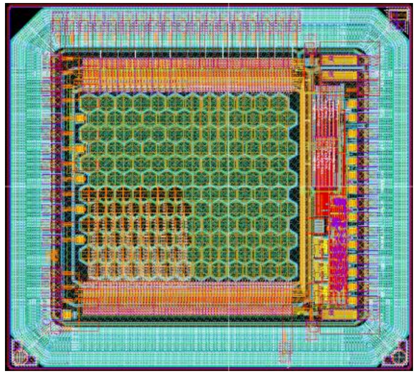


ATTRACT PicoAD

<20 ps

- Hexagonal pixels 65 µm side
- 30 ps TDC + I/O logic
- Analog channels

2021



Monolith

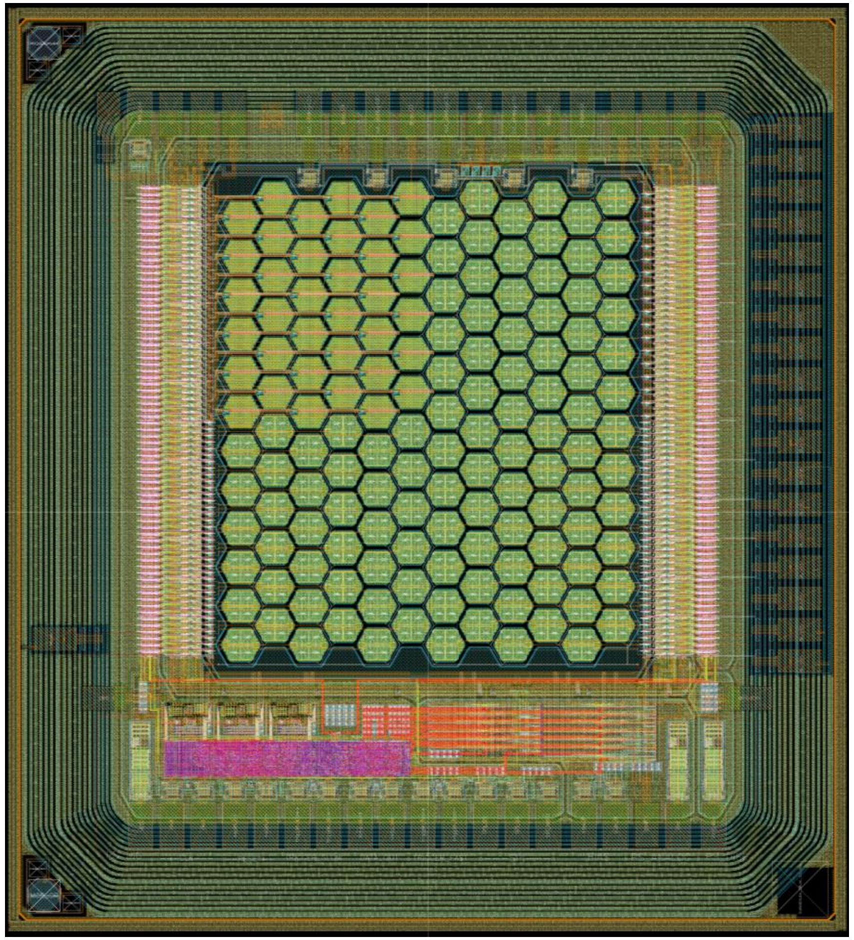
- Hexagonal pixels 65 µm side
- 1 ps TDC + I/O logic
- Analog channels

2021

FASER

- Hexagonal pixels 65 µm side
- 1.5 cm long columns

The “ATTRACT” prototype

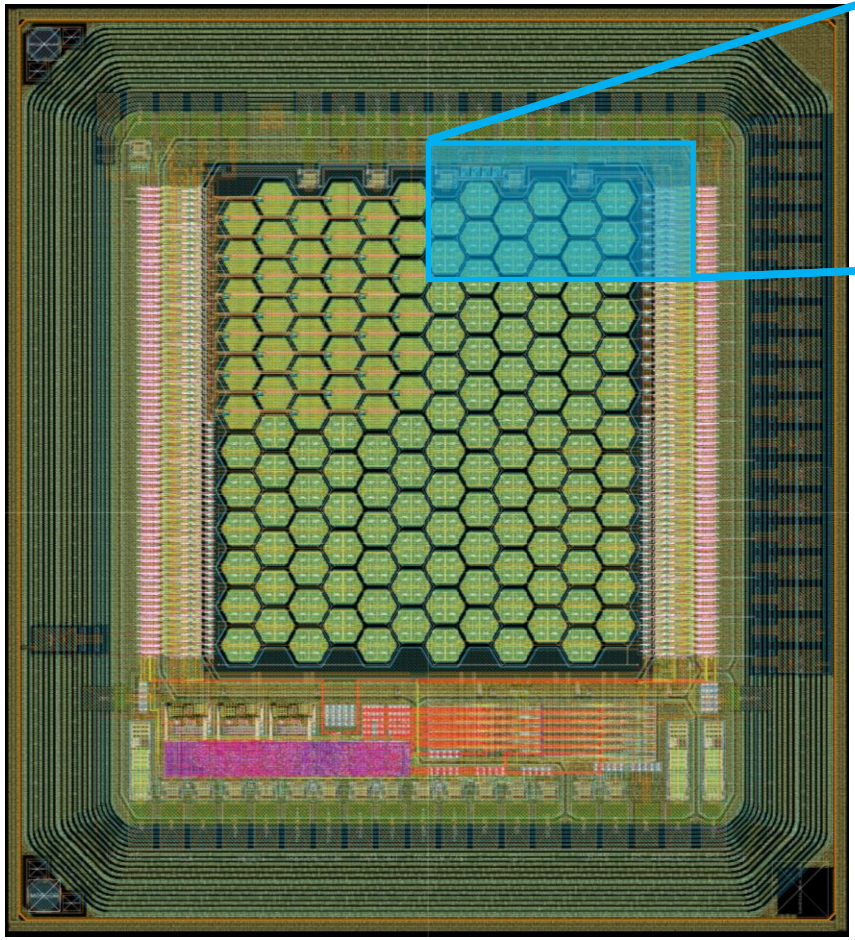


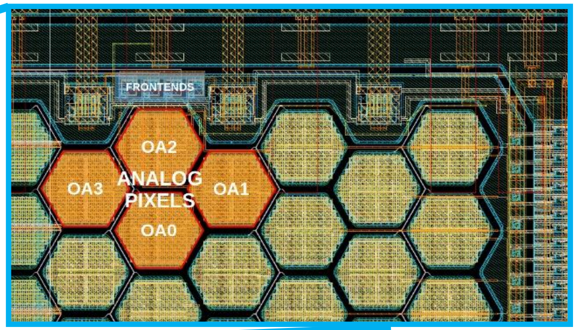
1. Active pixel
   - Front end in pixel
   - HBT preamp + driver (in pixel) + CMOS discriminator (outside pixel)
2. PET-project version:
   - HBT preamp + CMOS discriminator
3. Limiting amplifier:
   - HBT preamp + HBT limiting amplifier
4. Double threshold:
   - HBT preamp + two CMOS discriminators

MPW submission in 2019 funded by H2020 ATTRACT

G. Iacobucci et al 2022 JINST 17 P02019

The "ATTRACT" prototype

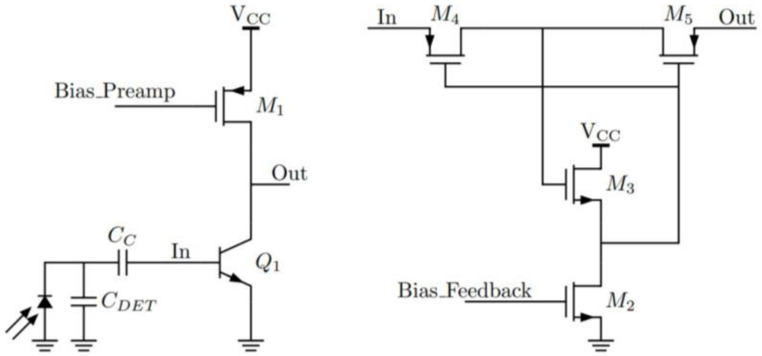




UNDER TEST HERE

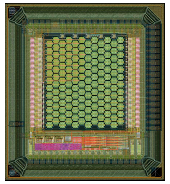
Analog Channels:

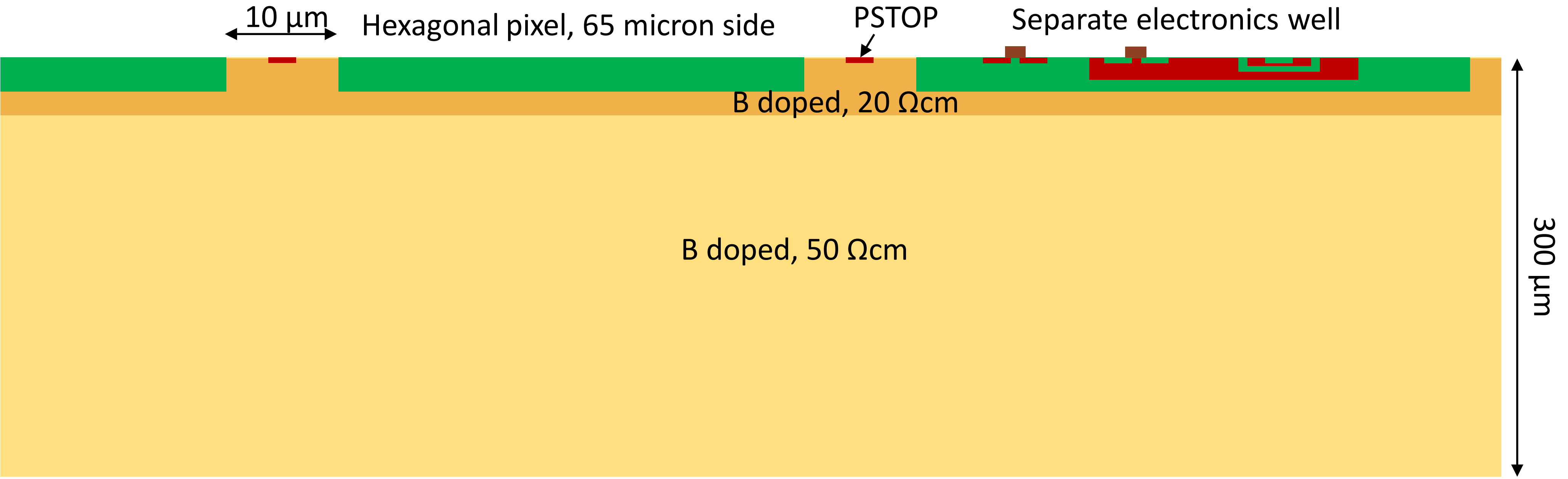
- HBT preamp + two HBT Emitter Followers to 500Ω Resistance on pad.



G. Iacobucci et al 2022 JINST 17 P02019

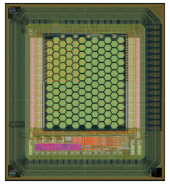
The "ATTRACT" prototype





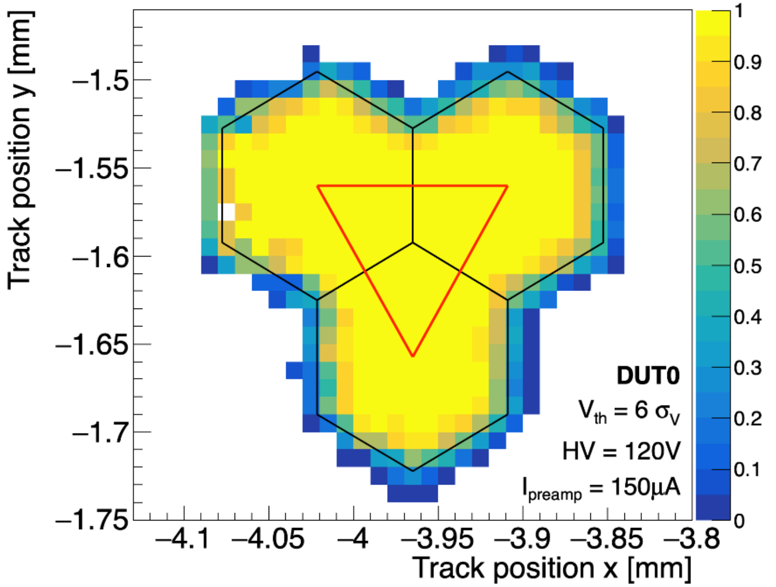
- Negative HV applied to substrate from backside and from top.
- All pixels and electronic nwells at positive low voltage.
- Typical HV: -140 V corresponds to a depletion layer of 24 µm.
  ⟹ Typical signal charge for a MIP: ~1450 electrons.

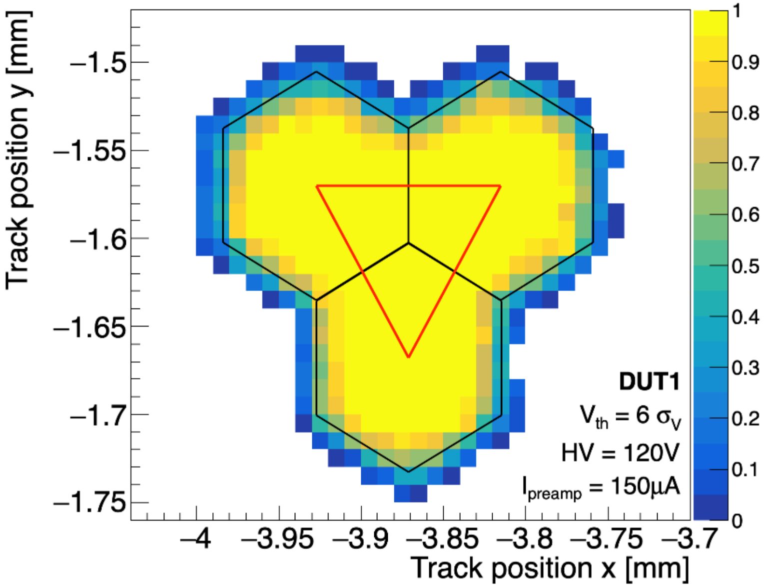
ATTRACT prototype - efficiency



CERN SPS 180GeV pion beam
FEI4 Telescope ($\sigma_x \sim 10\mu m, \sigma_y \sim 15\mu m$)

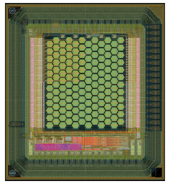
$I_{preamp} = 150\mu A$
$V_{th} = 6\sigma_V$
$HV = 120\ V$

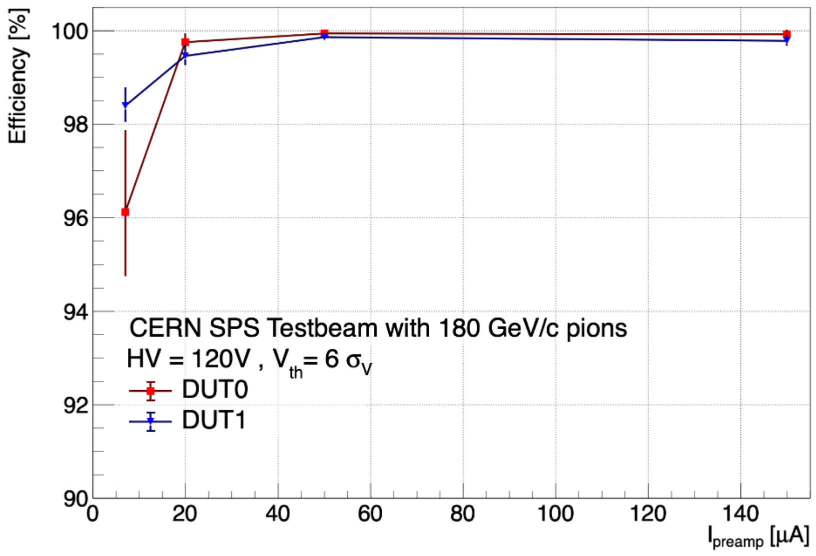


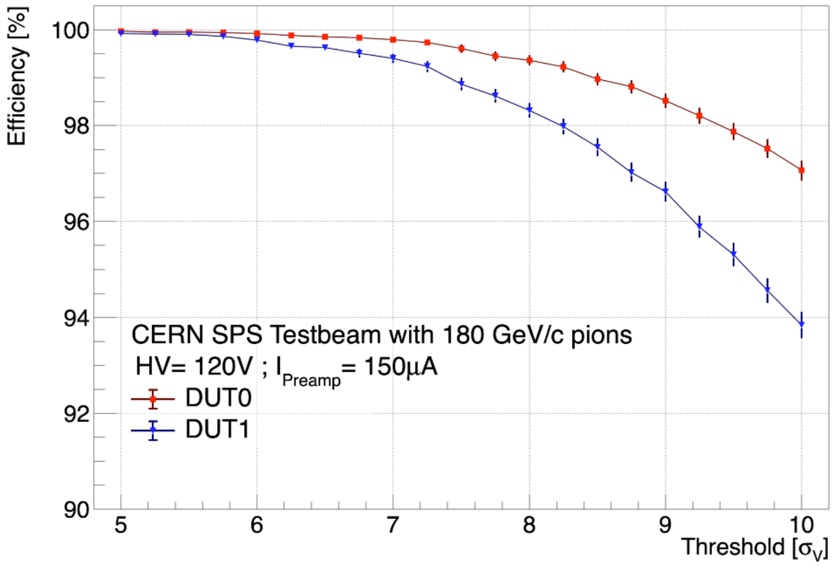


To get rid of the effect of the telescope precision, we can use the bins of the area inside the red triangle, that represents the entire pixel area in the right proportions.

ATTRACT prototype - efficiency

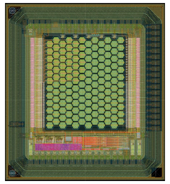


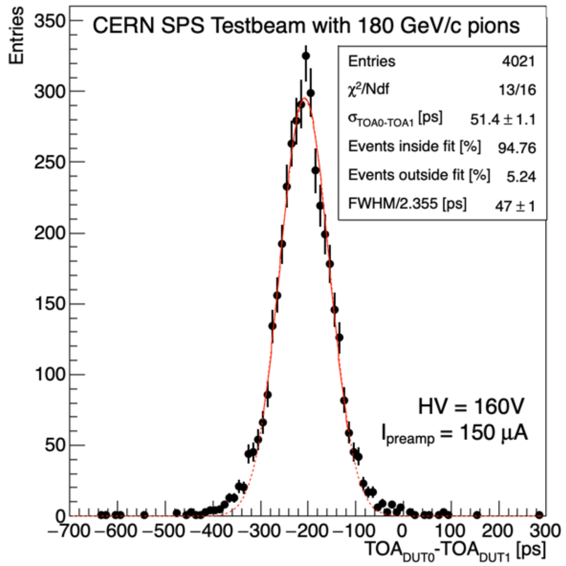


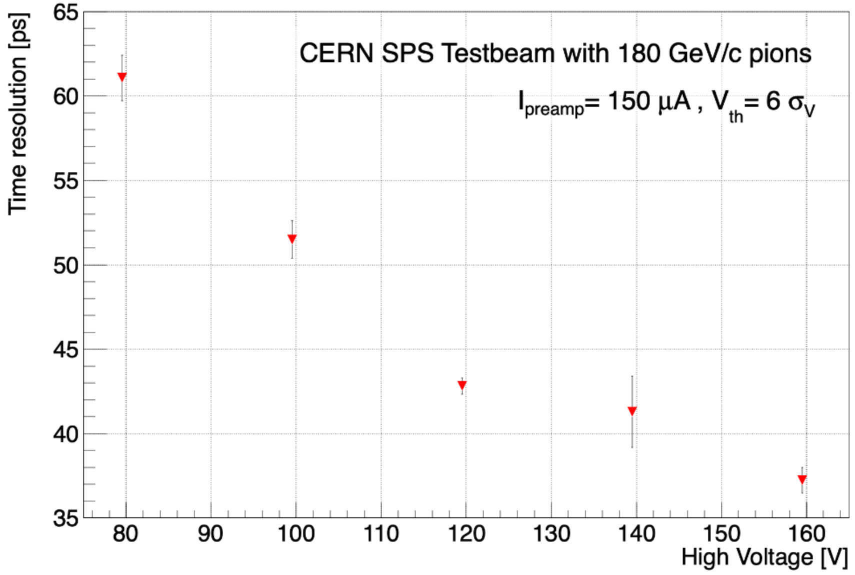


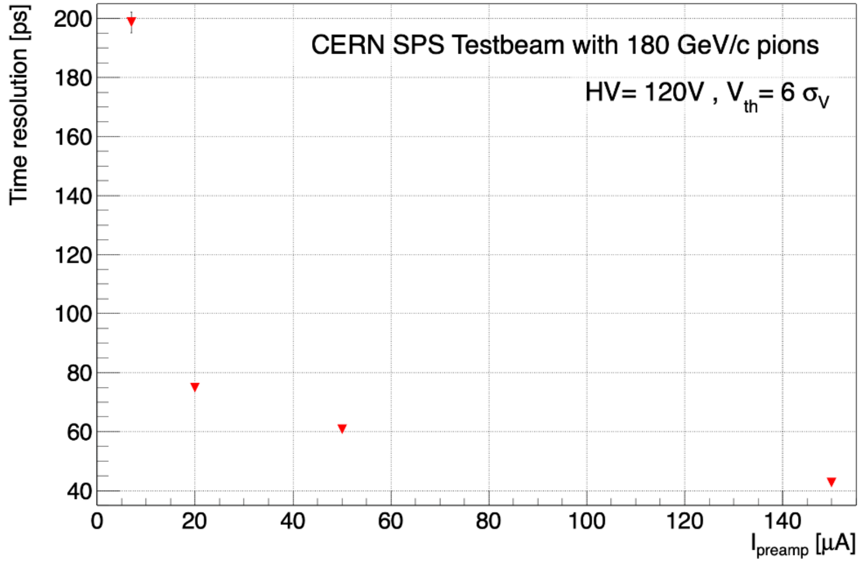
Efficiency measured at HV = 120 V				
I_{preamp} [μA]	7	20	50	150
Efficiency DUT0 [%]	$96.1^{+1.4}_{-1.7}$	$99.75^{+0.12}_{-0.17}$	$99.94^{+0.03}_{-0.05}$	$99.91^{+0.05}_{-0.08}$
Efficiency DUT1 [%]	$98.4^{+0.3}_{-0.4}$	$99.45^{+0.2}_{-0.2}$	$99.86^{+0.05}_{-0.07}$	$99.78^{+0.08}_{-0.11}$

ATTRACT prototype – time resolution









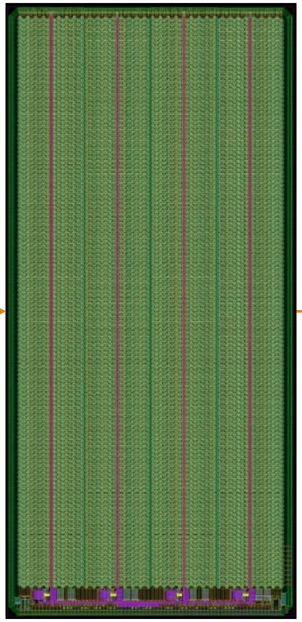
$$\sigma_t = \frac{\sigma_{TOA1-TOA2}}{\sqrt{2}} = 36.4\ ps$$

Time resolution **without avalanche gain**

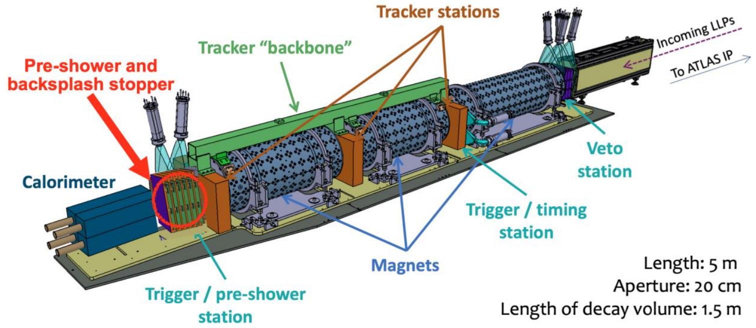
$$\sigma_t = \frac{\sigma_V}{dV/dt} \cong \frac{ENC}{I_{Ind}}$$

Direction of the R&D

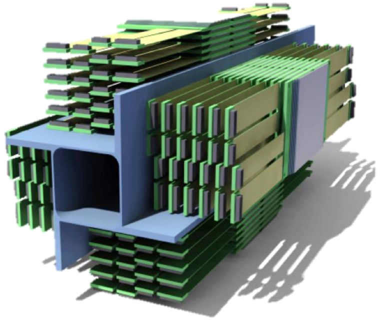
Large area chip



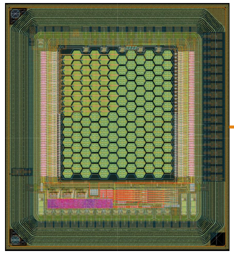
HEP



Medical Applications

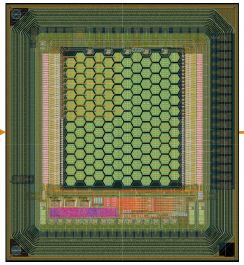


ATTRACT prototype



Picosecond time resolution

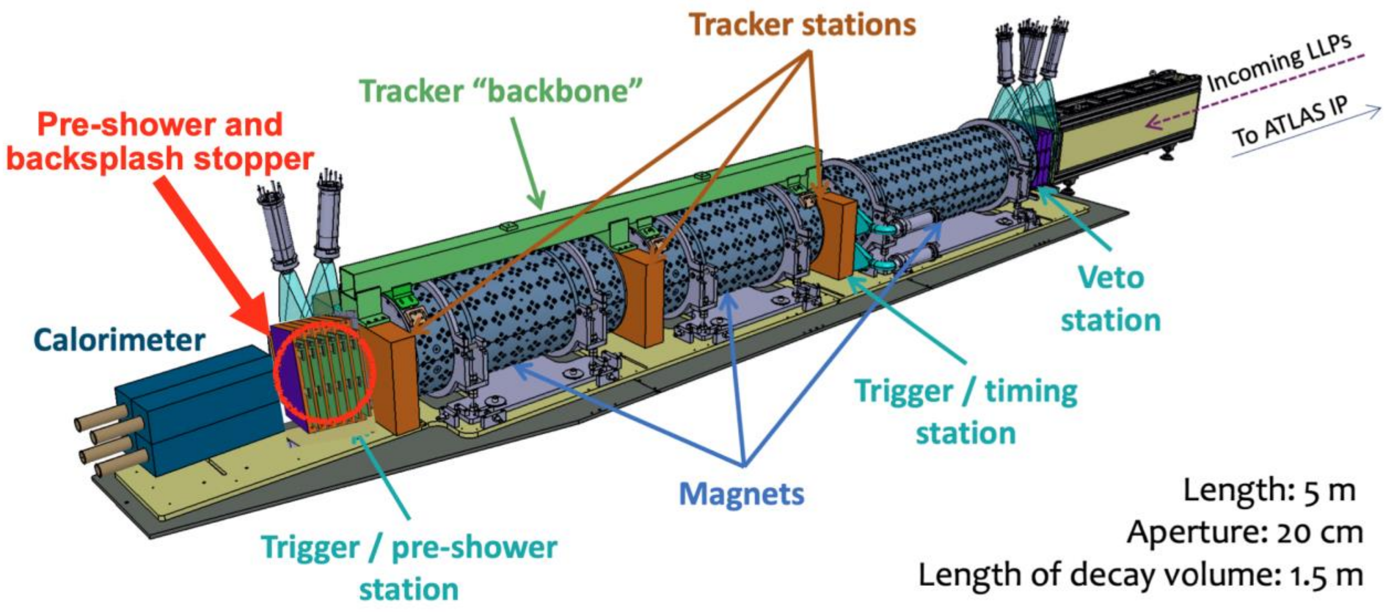
+ Avalanche gain



…

High-granularity pre-shower detector for FASER

Current pre-shower:
2 layers of tungsten (1X0) + scintillating detectors ⟹ No XY granularity.

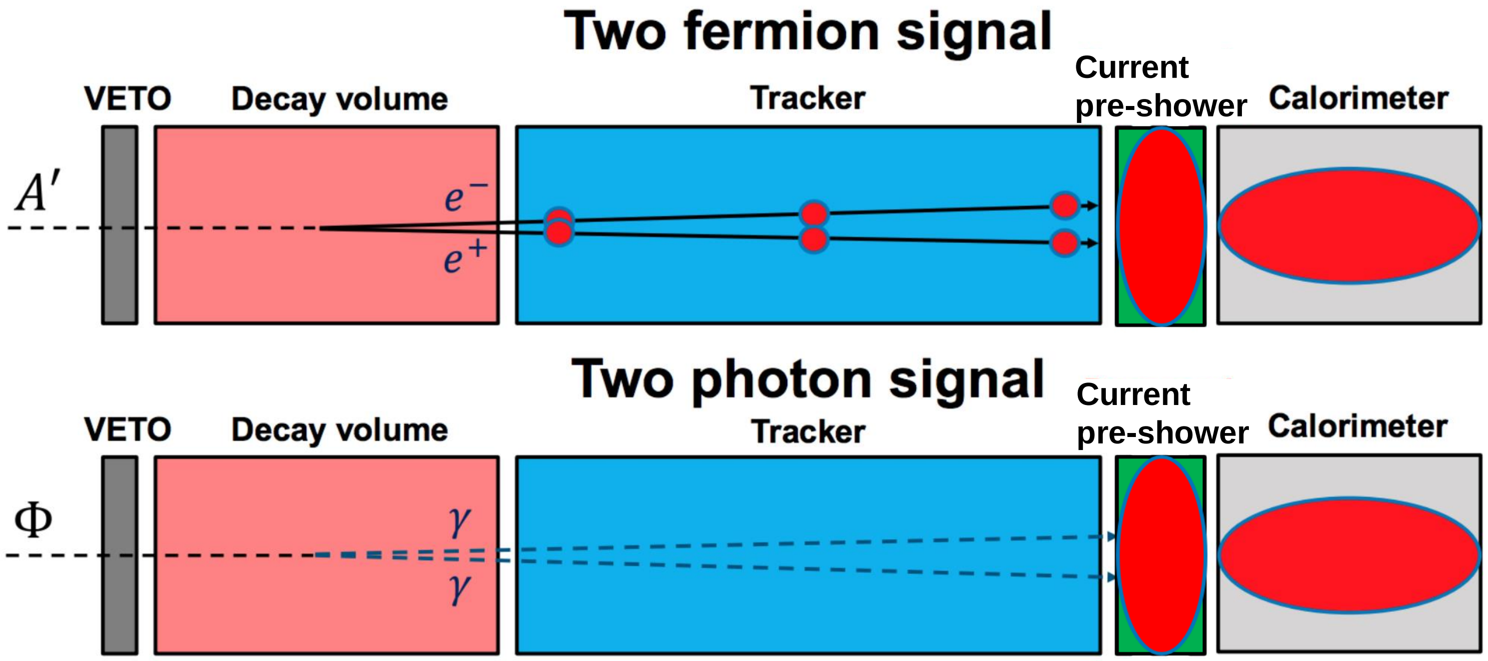


The project:

- **A high-granularity/high dynamic range pre-shower** based on monolithic silicon pixel sensors.
- Discriminate **TeV scale electromagnetic showers**.
- Targeting data taking in 2024/26, during LHC run 3 and during HL-LHC.

The goal of the new pre-shower

- The goal is to have independent measurement of two very collimated photons.



The goal of the new pre-shower

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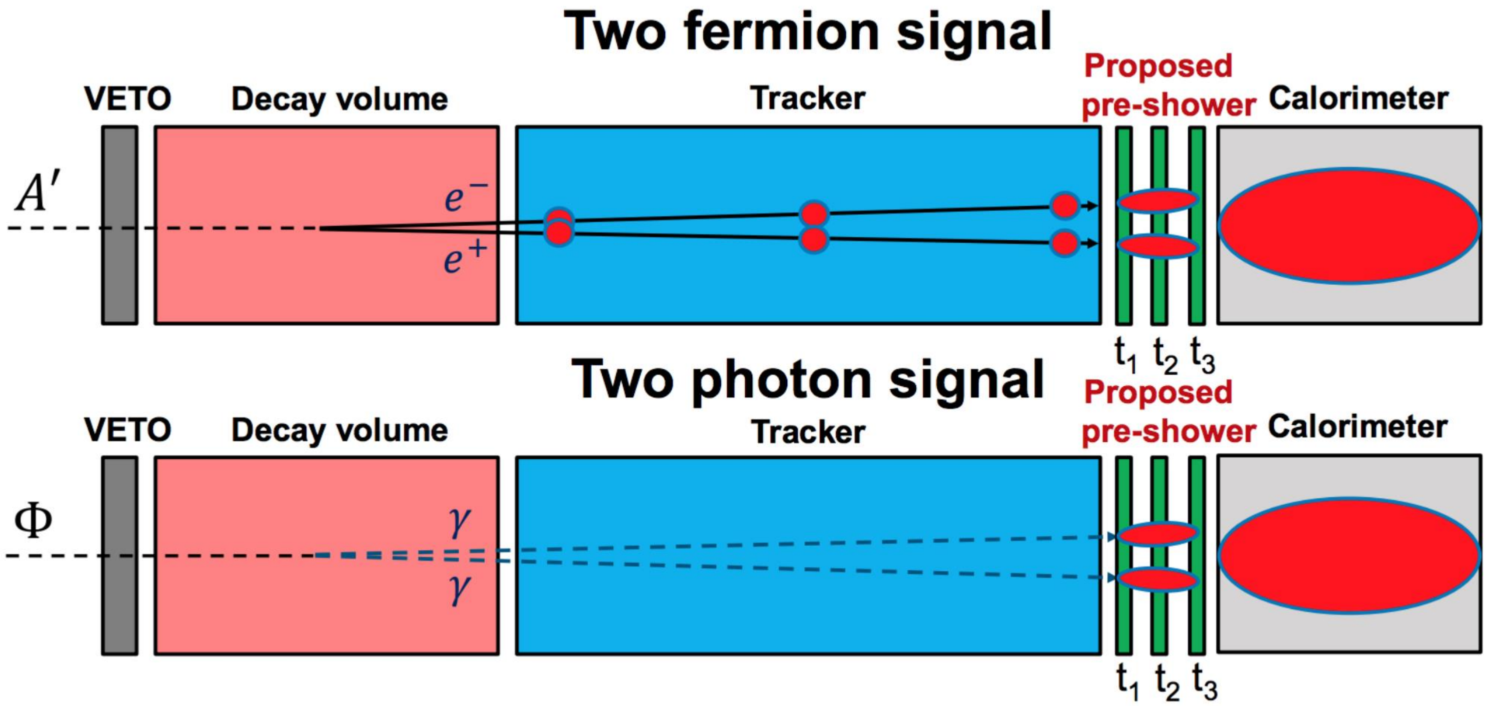
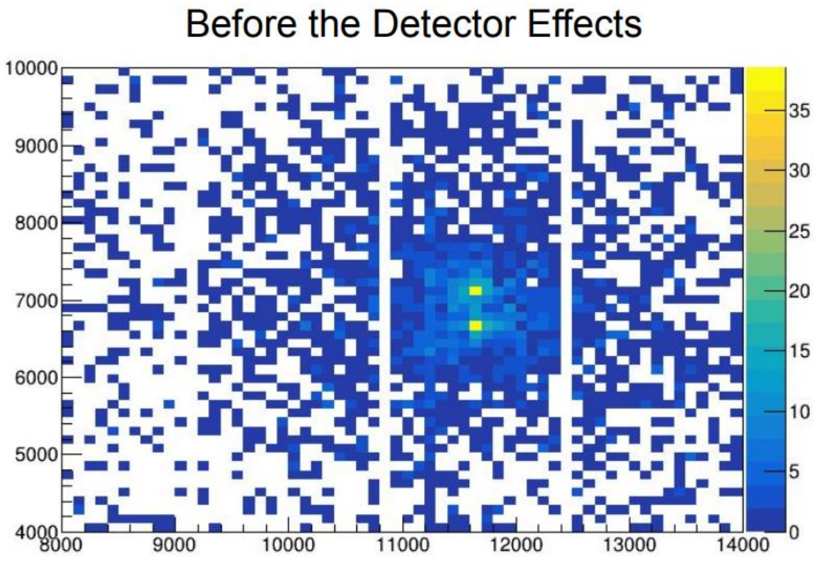
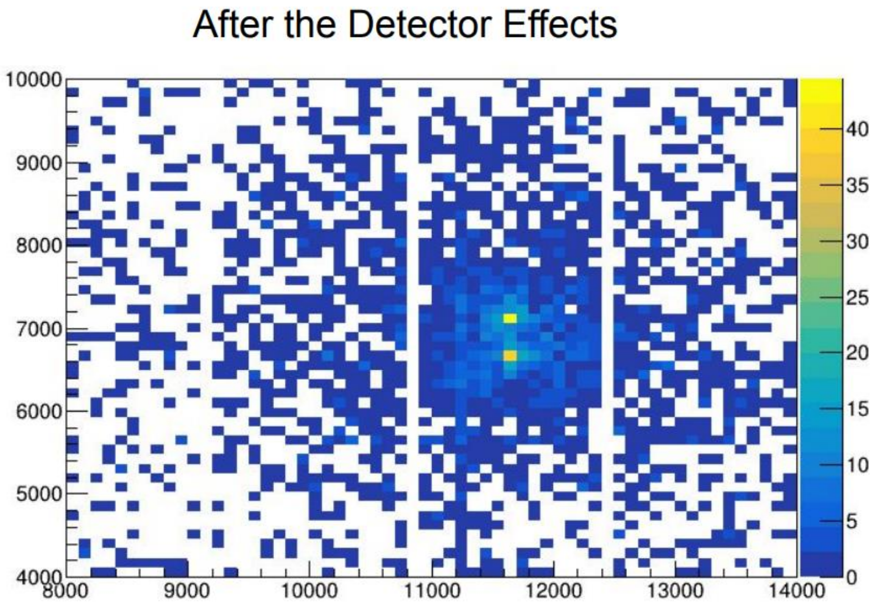


The FASER pre-shower

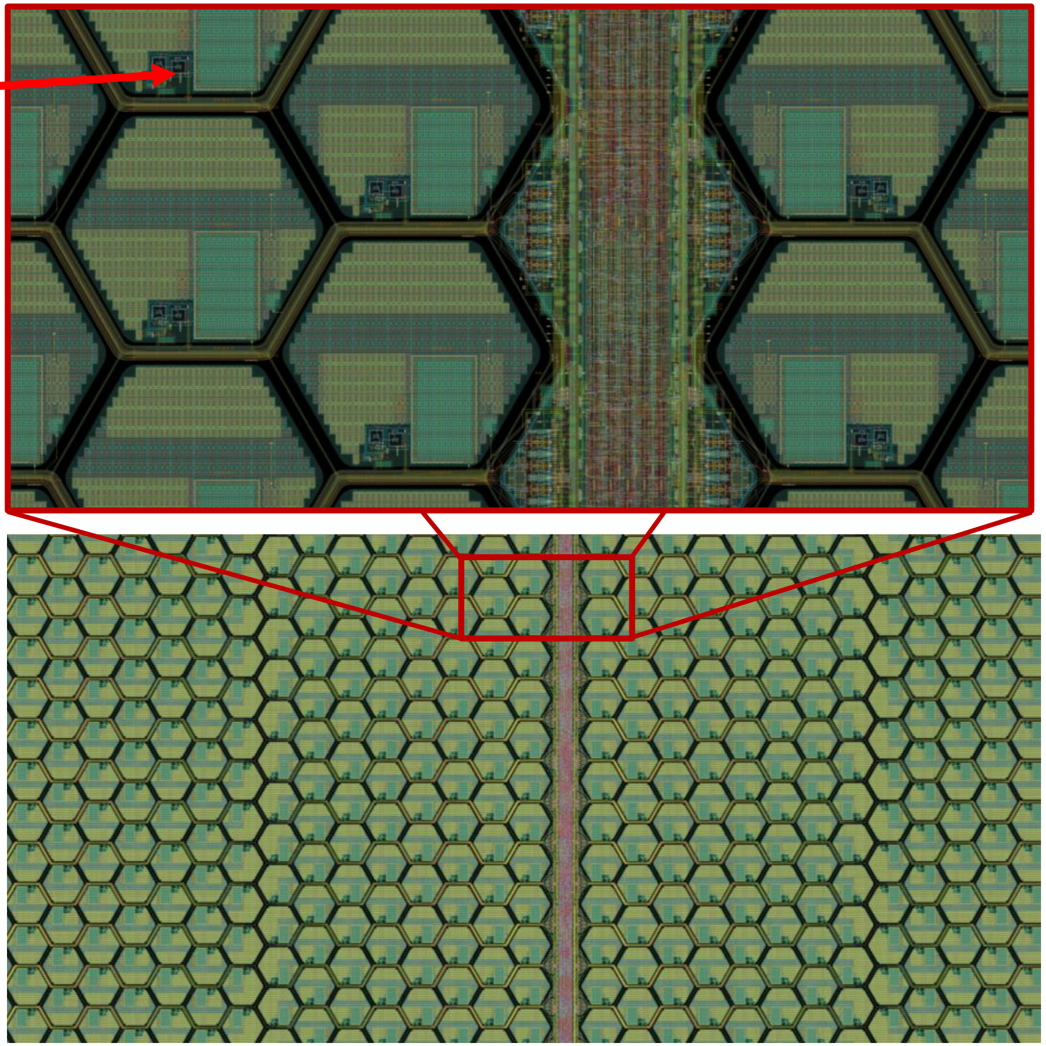
One Event - Hitmap - Chip 405 -2 photons - 1 Tev each - 500 µm Distance - After the Detector Effects





Monolithic layout

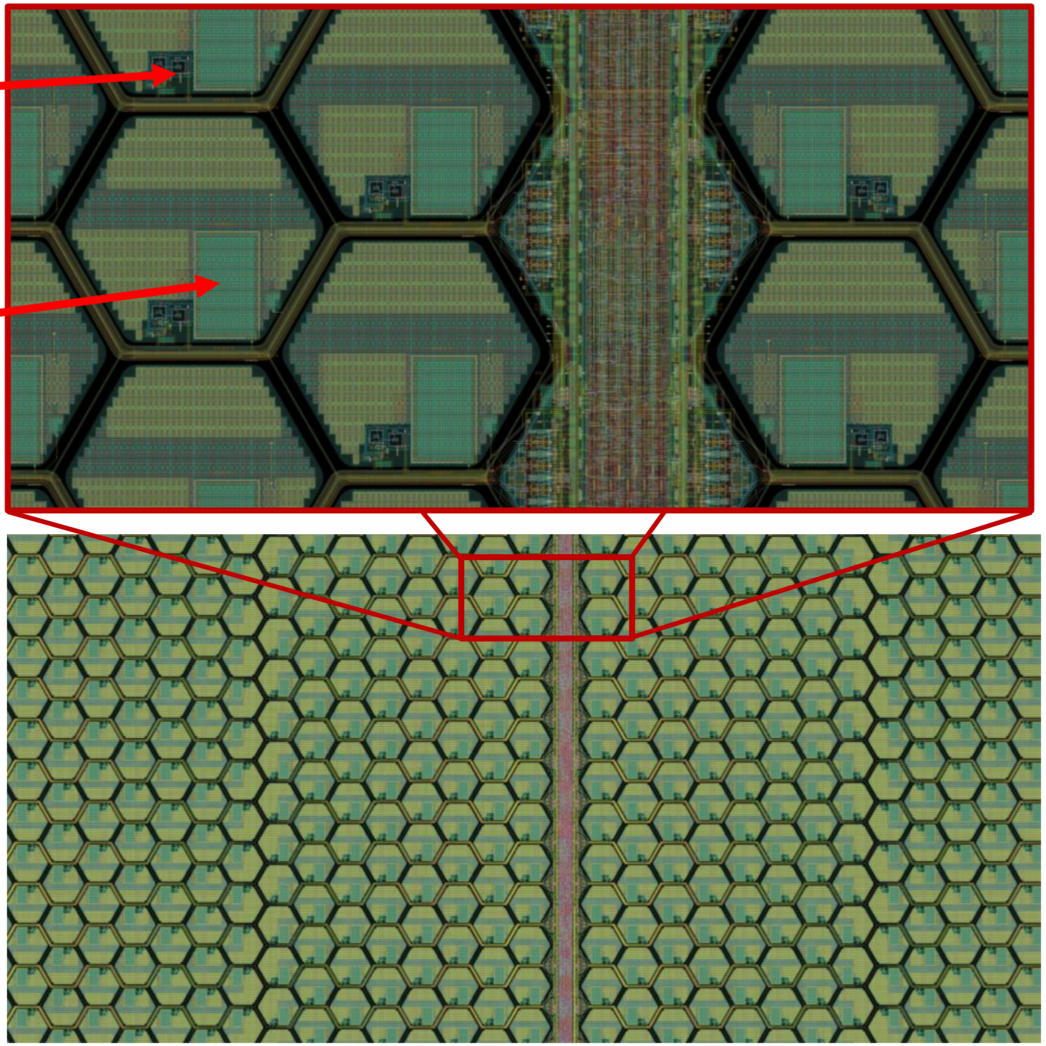
Analog front-end in pixel.



Monolithic layout

Analog front-end in pixel.

Metal-Insulator-Metal capacitor in pixel to store the signal charge



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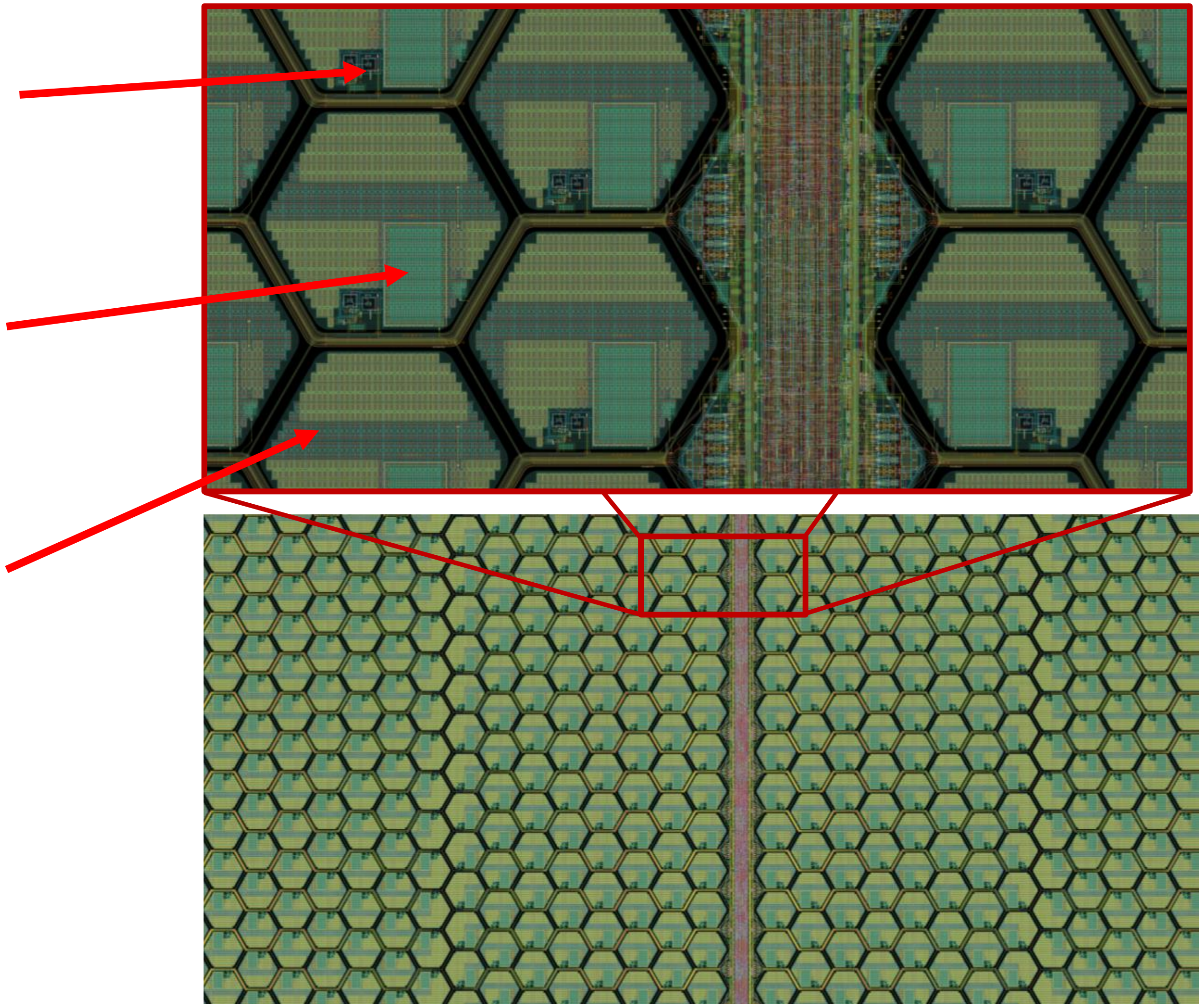
Metal-Insulator-Metal capacitor in pixel to store the signal charge

PMOS matrix used as coupling capacitor.



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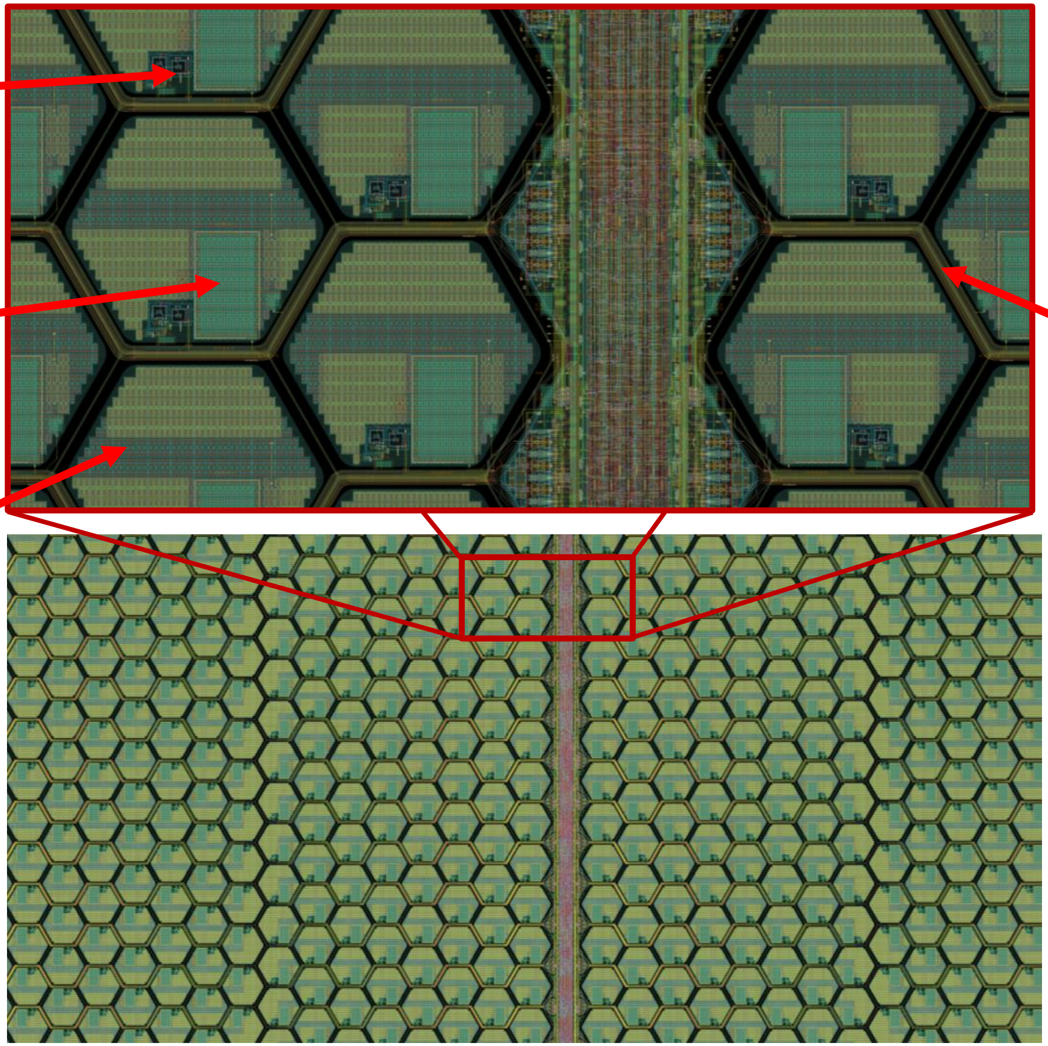


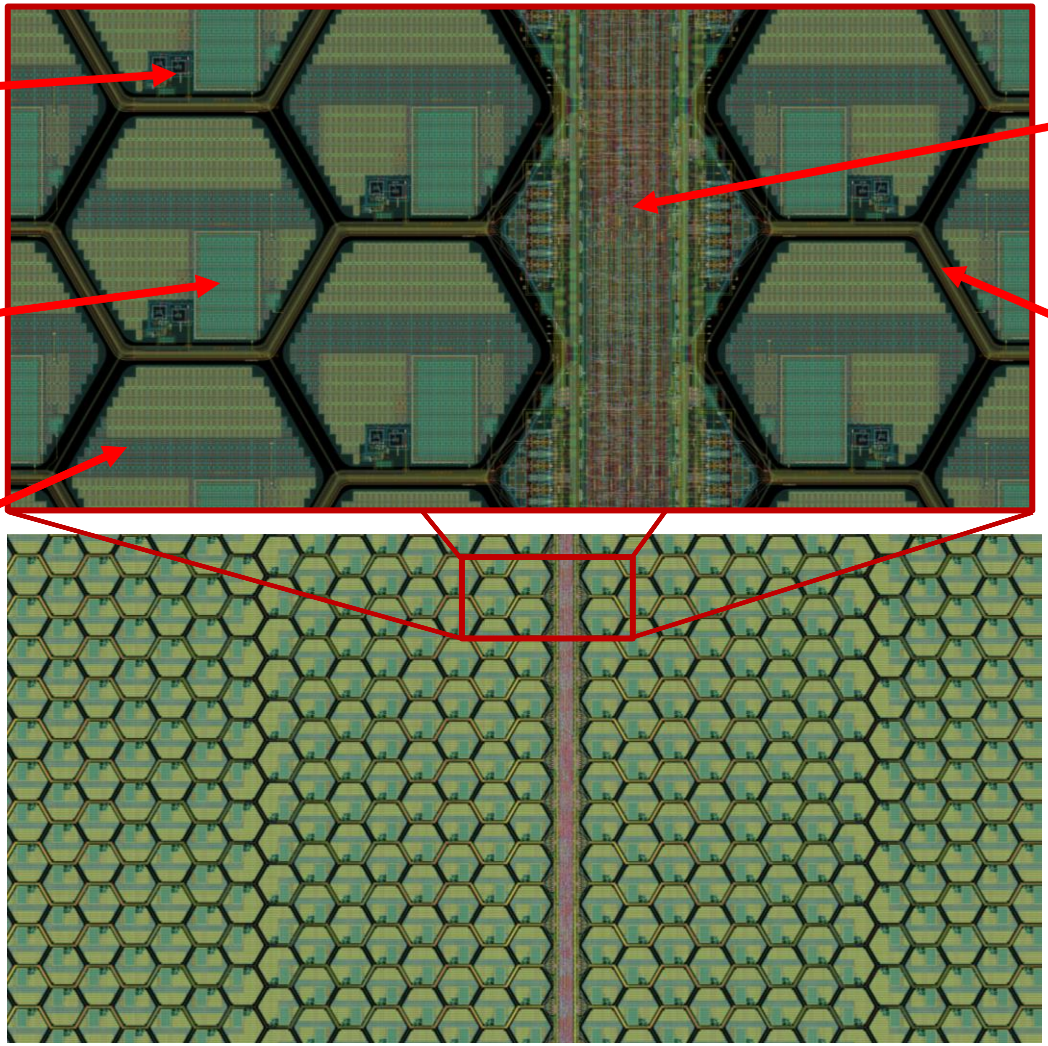
Signal routing after amplification stage requires shielded bus to avoid cross-talk to pixels.

Monolithic layout

Analog front-end in pixel.

Metal-Insulator-Metal capacitor in pixel to store the signal charge

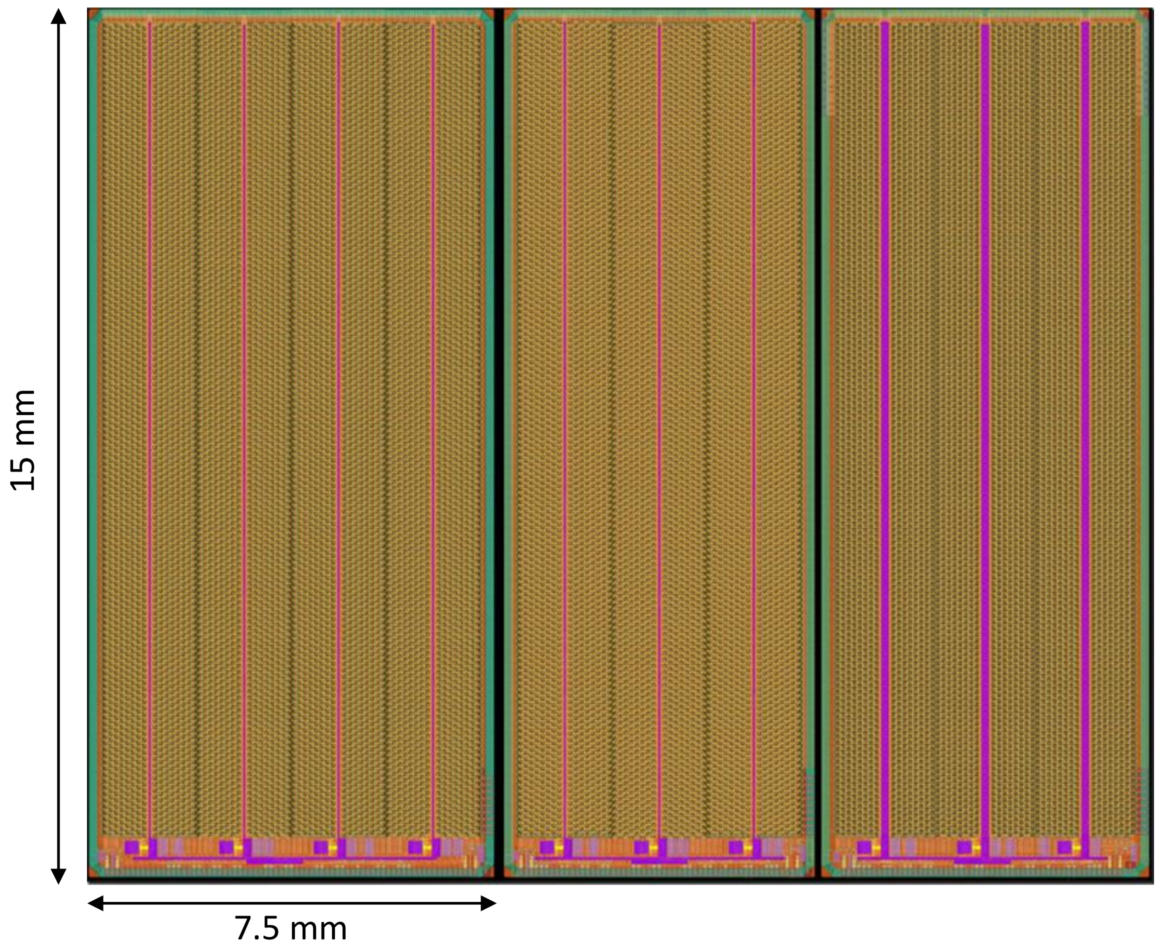
PMOS matrix used as coupling capacitor.



Digital electronics in separate well.

Signal routing after amplification stage requires shielded bus to avoid cross-talk to pixels.

Pre-production ASIC



- Large area, fully functional prototype.
- Two alternative test layouts with 3 columns.
- Tests will start in May 2022.

100µPET project

The **100µmPET** project: **molecular imaging with ultra-high resolution**

First silicon small-animal scanner prototype

SNSF SINERGIA four years project (from 2021 Q2)

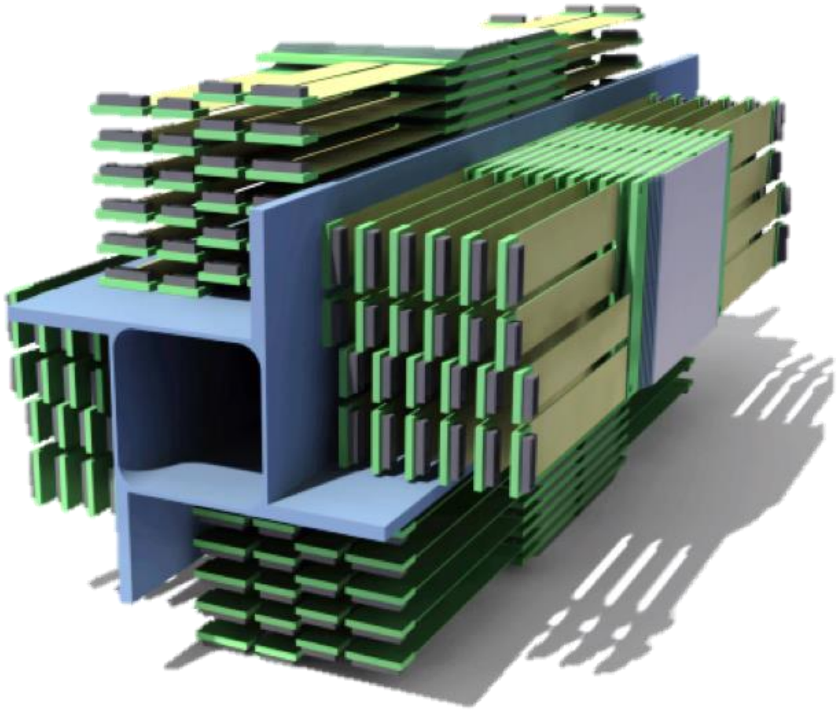
FNSNF SWISS NATIONAL SCIENCE FOUNDATION

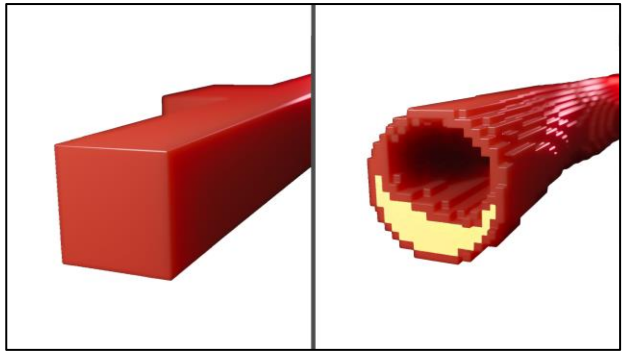
Sinergia

UNIVERSITÉ DE GENÈVE FACULTÉ DES SCIENCES

HUG Hôpitaux Universitaires Genève

EPFL

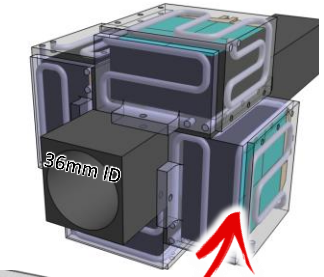


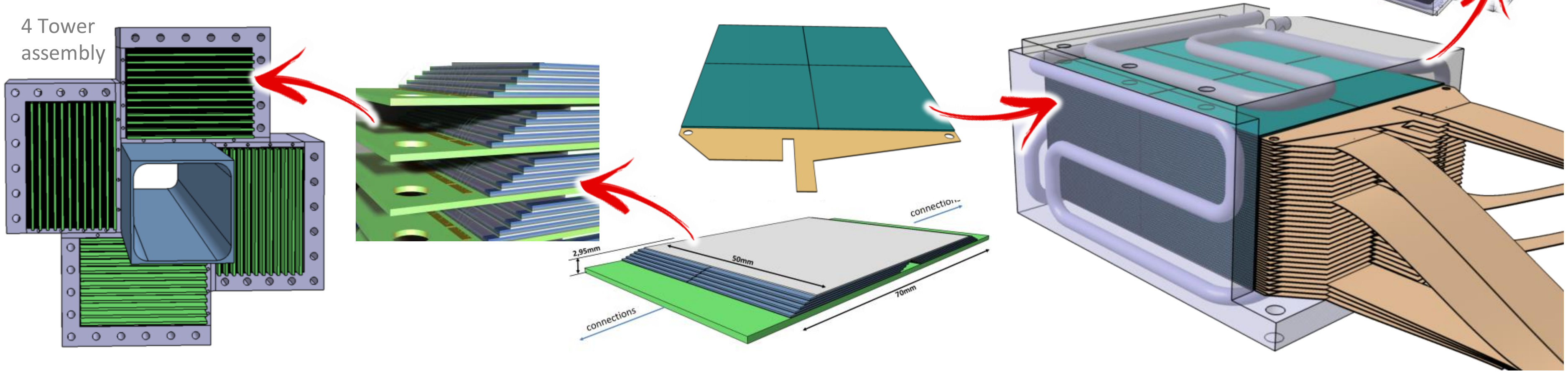


With today's PET technology, small blood vessels can only be visualized in their entirety (A). The proposed new PET technology will allow the study of changes in the lining of small blood vessels, such as atherosclerotic plaques (B).
Images: © Xavier Ravinet - UNIGE

100μPET application

- **Monolithic 100μPET detector ASIC**: 2.5 x 3 cm^2 active pixel matrix; 100 μm pixel pitch; 250 μm thick silicon sensor
- Single silicon detection layer composed by 2x2 chips assembled, covering about 30 cm^2!
- 4 “towers” compose the scanner. **60** detection layers on each tower **= 960 chips.**
  - Large number of services and interconnections, requiring **innovative** design.
  - **Two possible designs** under study
    - **5 silicon detector layers** stacked on a **PCB**, staggered for **wire-bonding**. **12 modules** are stacked in a tower
    - **1 detection layer** (2x2 chips) are interfaced to a **FPC** via [ACF bonding](). **60 FPCs** are stacked in a tower

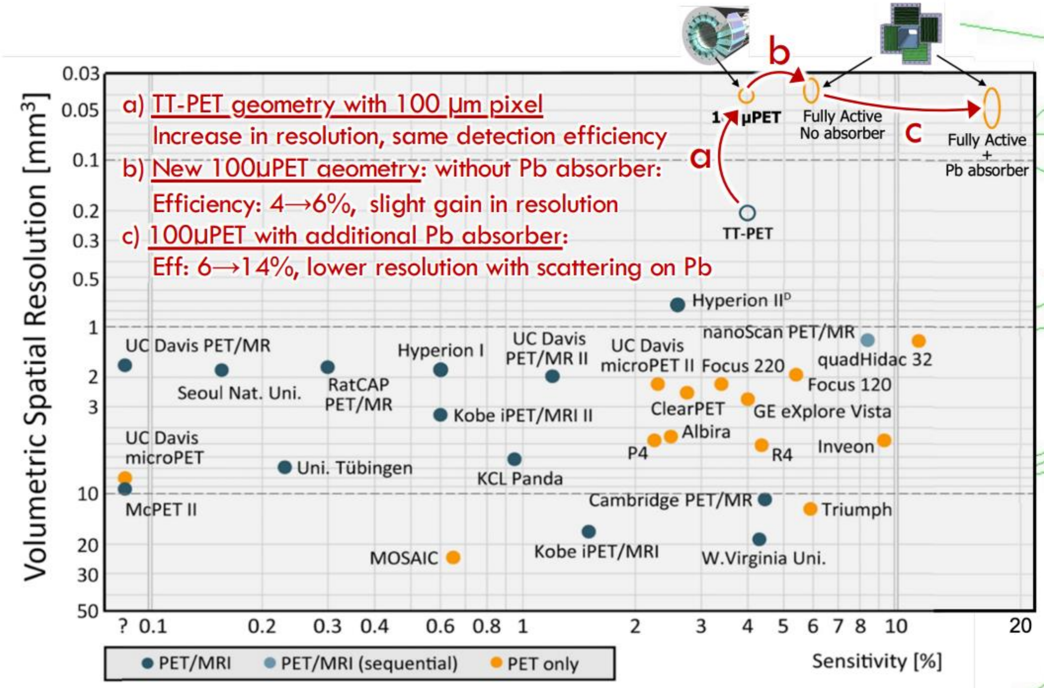


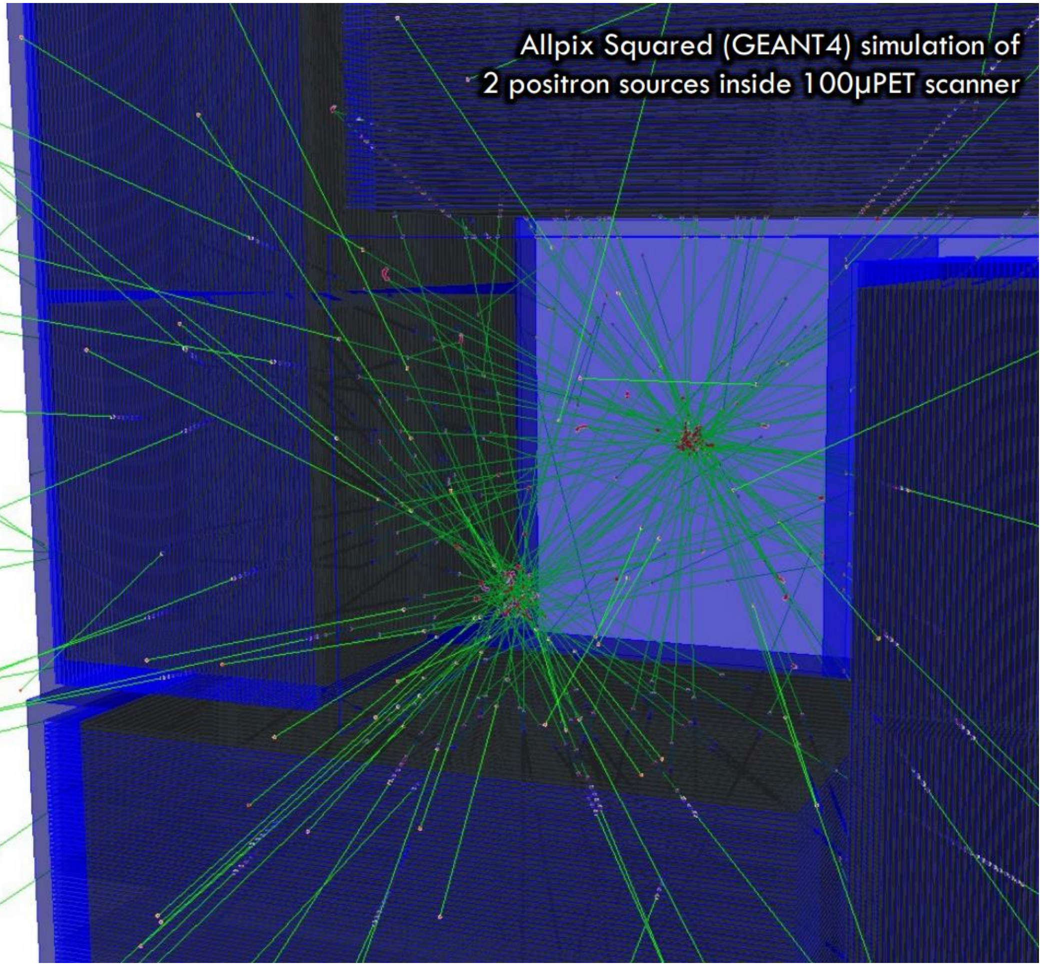


100μPET application

Monte Carlo simulations has shown a disruptive jump in the scanner's <u>resolution</u> and <u>sensitivity</u>

- Efficiency can be increased with absorber layers
  - It is a compromise **between efficiency** and **resolution**





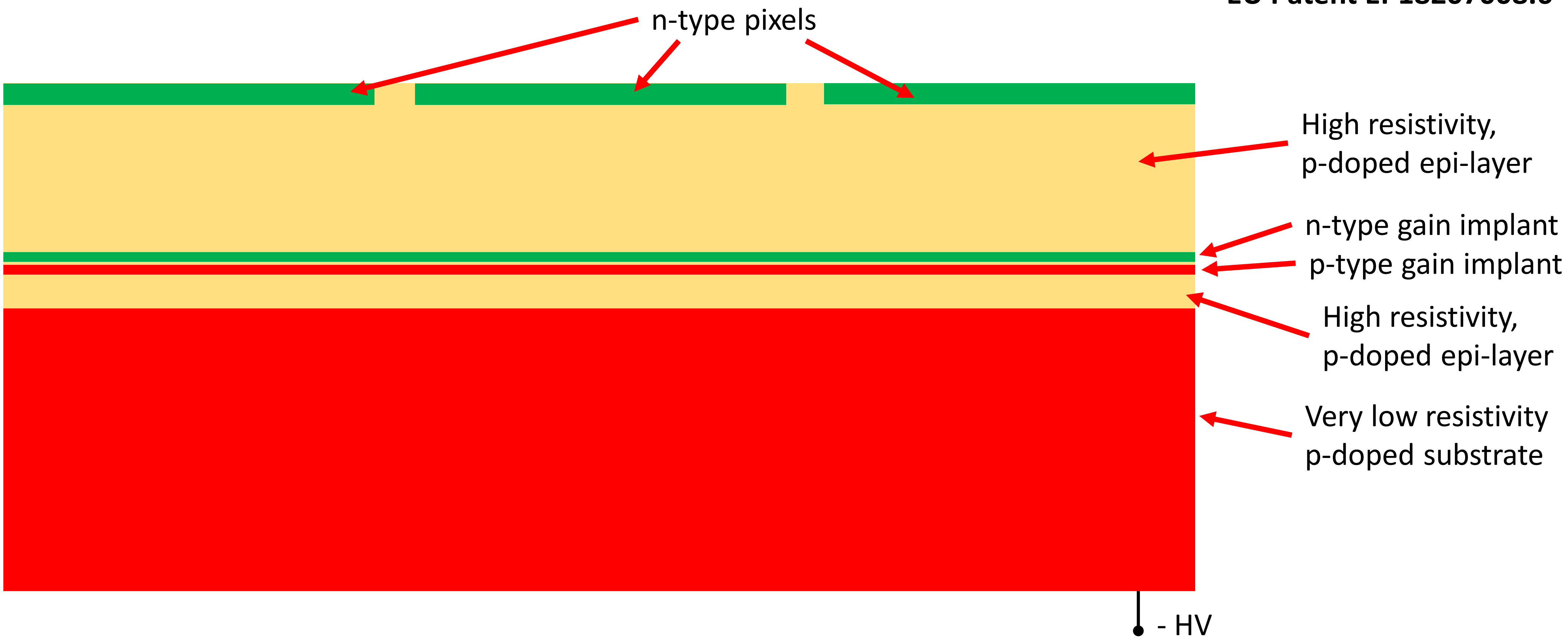
Summary

1. Precise timing in HEP and medical physics applications.
2. Fast silicon pixel sensors in SiGe BiCMOS.
3. 4D tracking with monolithic silicon pixel sensors.
4. R&D at the University of Geneva.
5. **The path toward picosecond time resolution.**

PicoAD: The PicoSecond Avalanche detector

- **Multi-Junction, pixelated avalanche detector.**

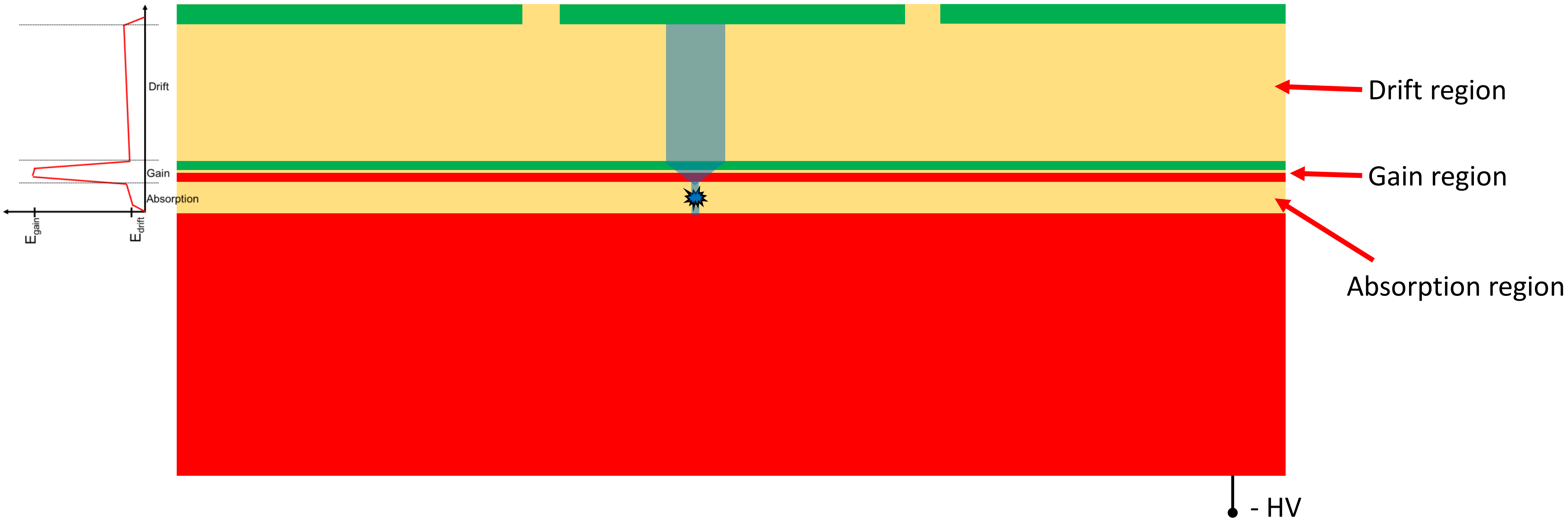
EU Patent EP18207008.6



PicoAD: The PicoSecond Avalanche detector

- **Multi-Junction, pixelated avalanche detector.**

EU Patent EP18207008.6



PicoAD: The PicoSecond Avalanche detector

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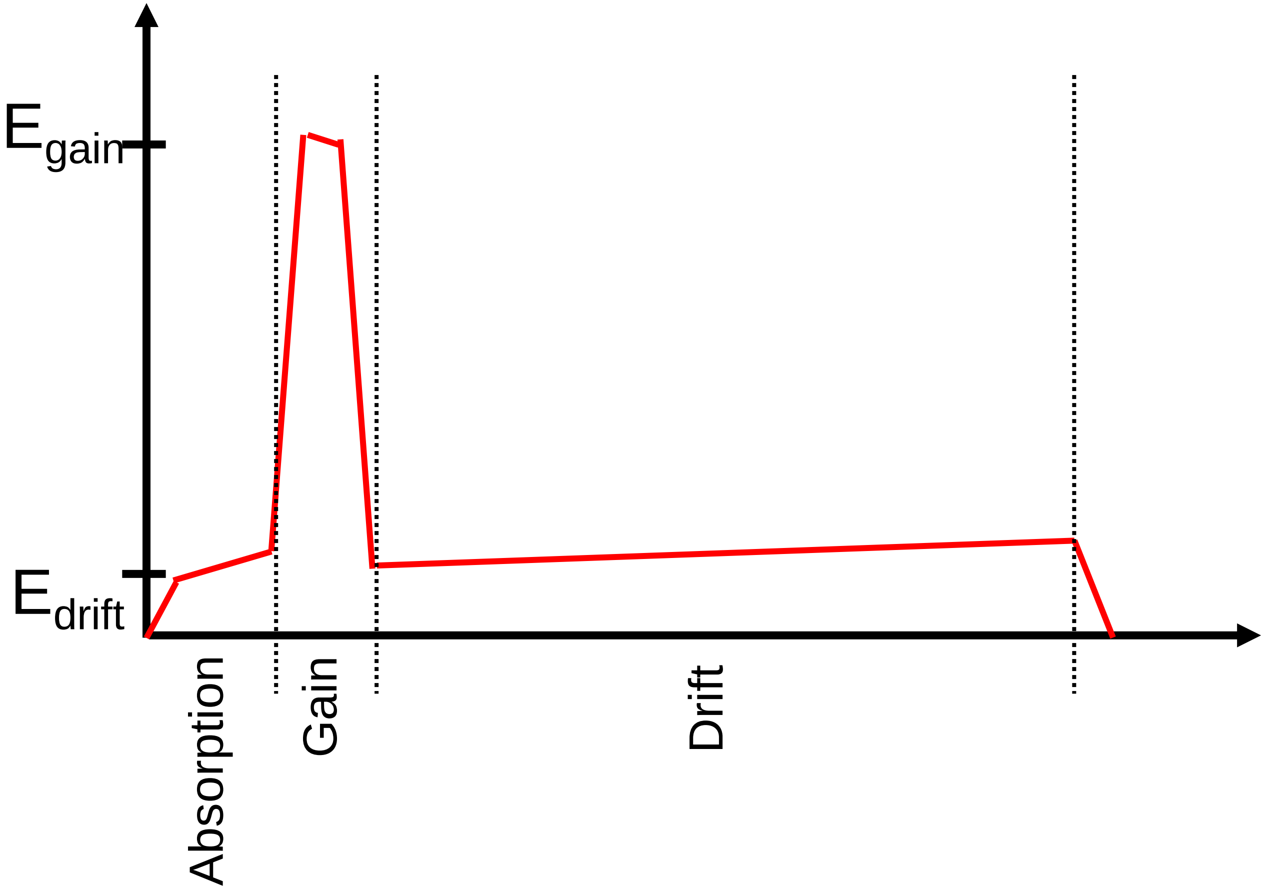
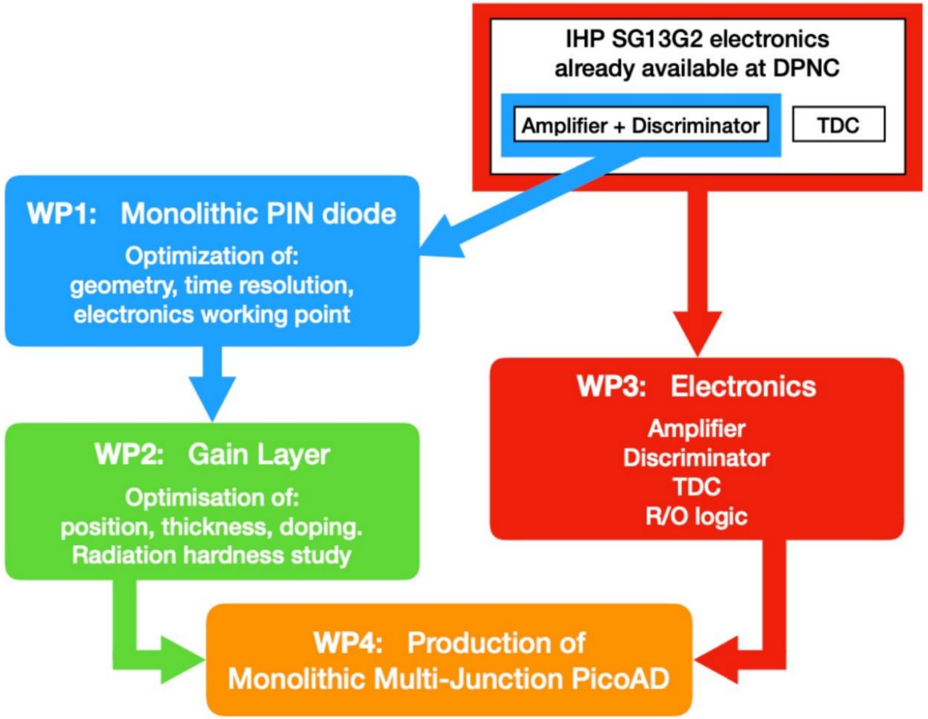
EU Patent EP18207008.6



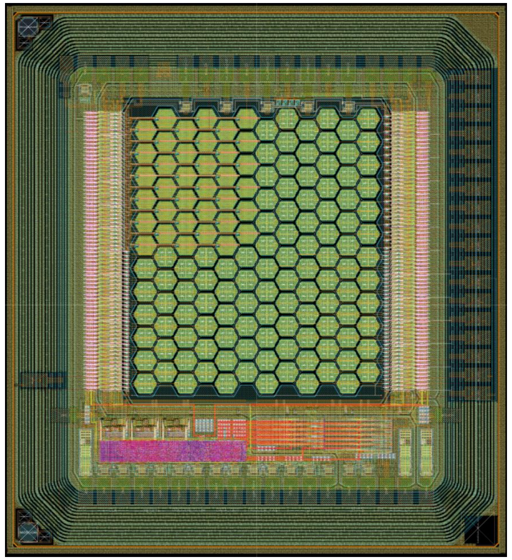
- The introduction of fully-depleted multi-pn junctions allows to **engineer the electric field**.
- New device with unique timing and reliability performance.
- Gain with 100% fill-factor.
- Geant4 + Cadence simulations estimate ~**2ps time resolution** contribution from the sensor.
- Requires low-noise, ultra fast electronics to be fully exploited.

MONOLITH ERC project

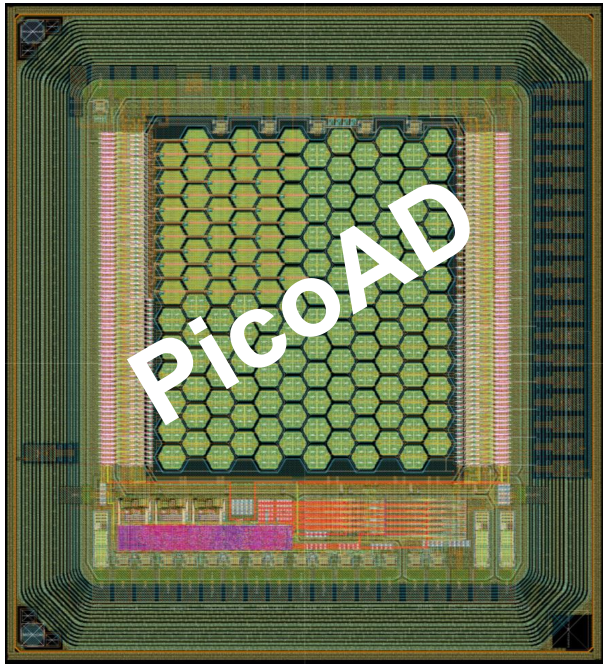
A monolithic silicon sensor able to measure precisely the 3D spatial position of charged particles while providing at the same **picosecond time resolution** using the novel **Picosecond Avalanche Detector (PicoAD)** concept.



PicoAD +



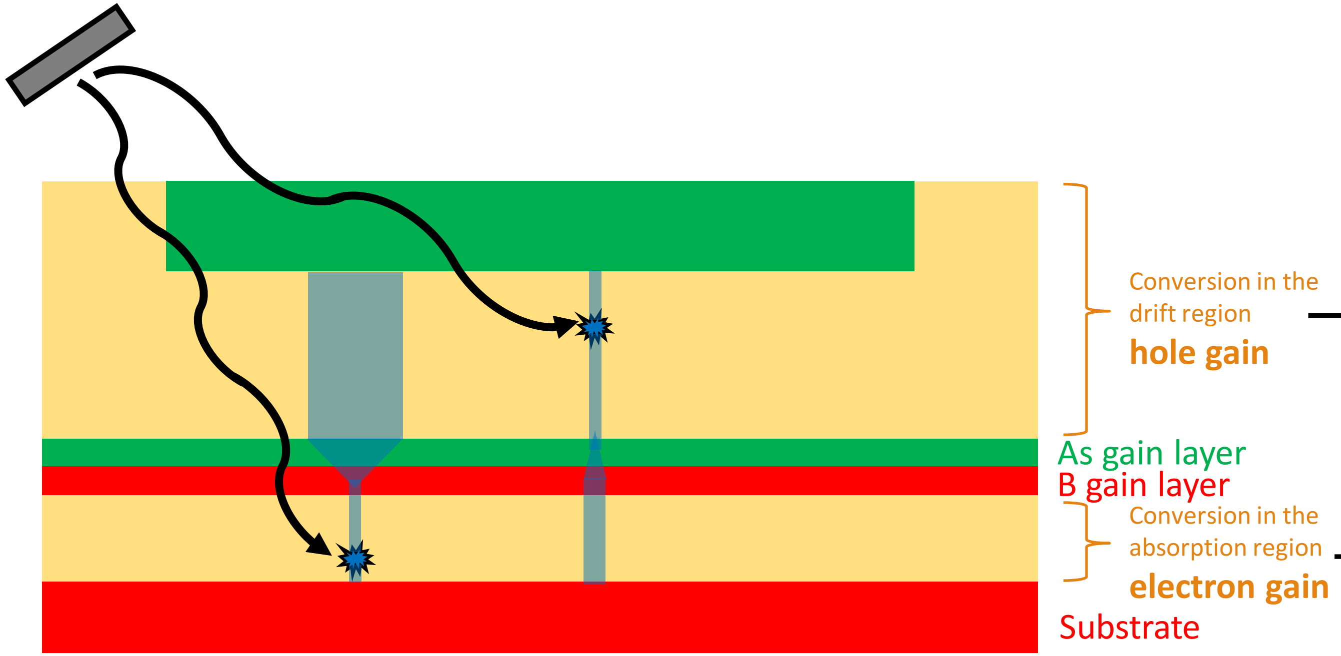
PicoAD proof-of-concept prototypes



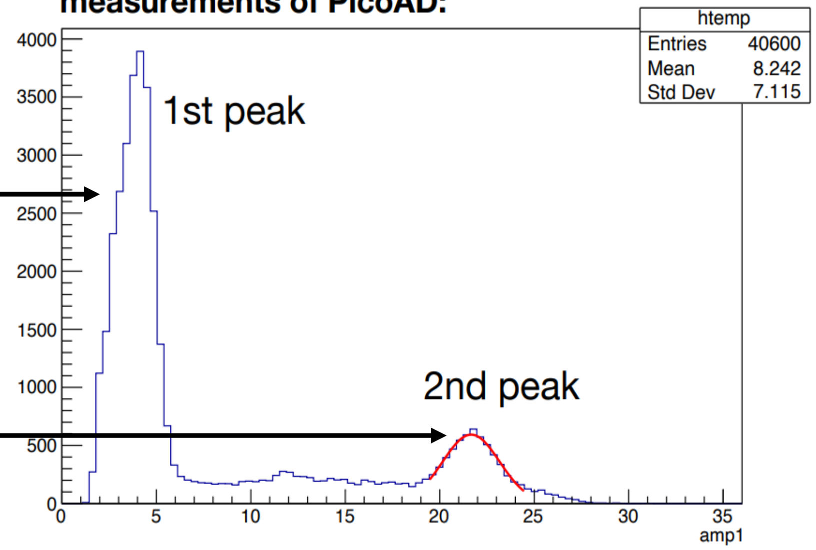
- Integrated in a special wafer for the ATTRACT prototype.
- Process design in collaboration with IHP.
- 15 µm total epi layer.
- Special wafers funded by INNOGAP.

PicoAD: First prototype test with Fe-55 source

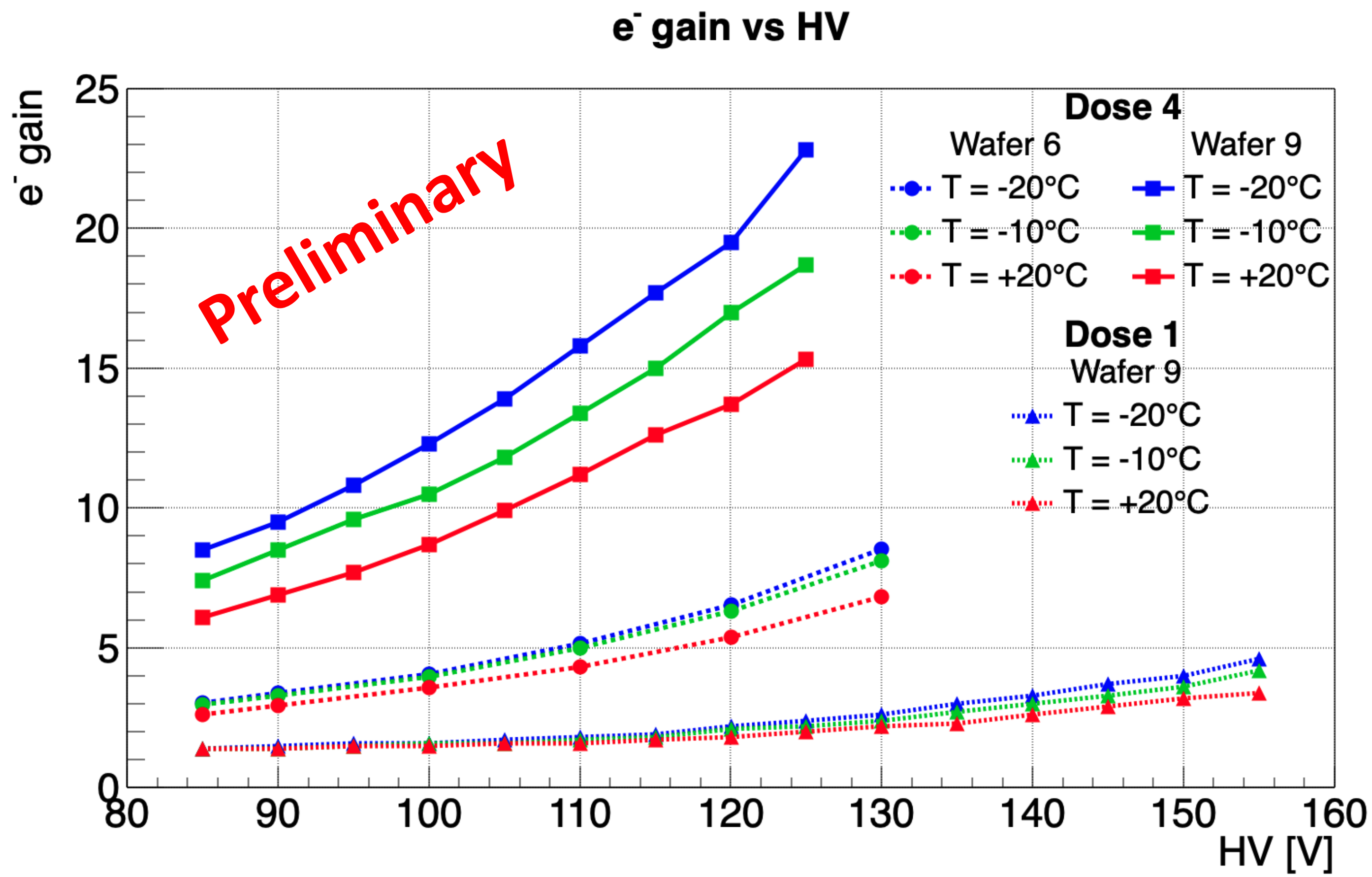
Fe-55 X-ray source: point-like charge deposition inside the sensor



Typical spectrum from 55-iron measurements of PicoAD:



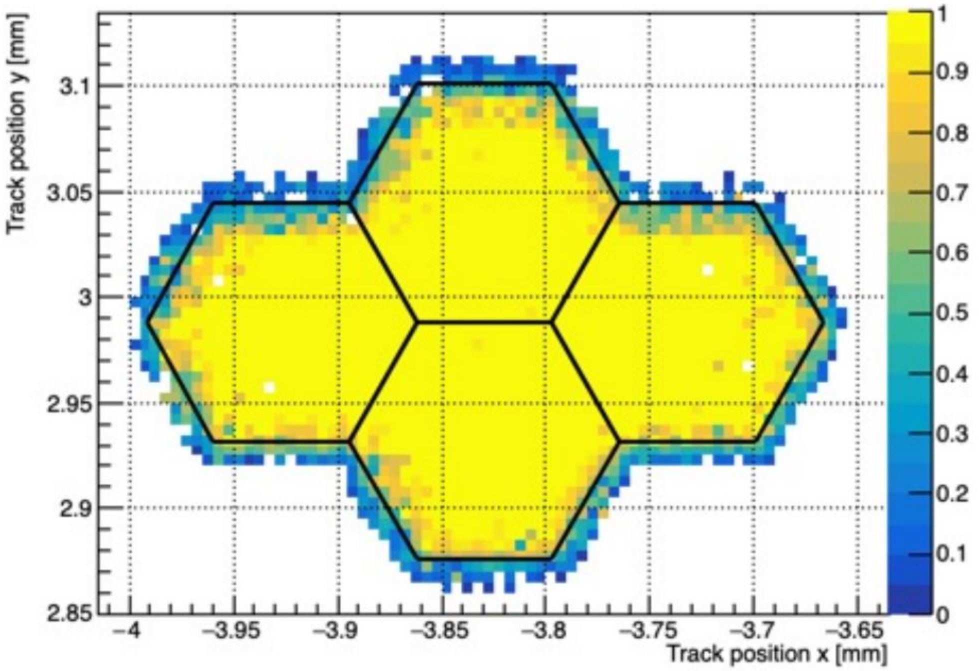
PicoAD: First prototype test with Fe-55 source

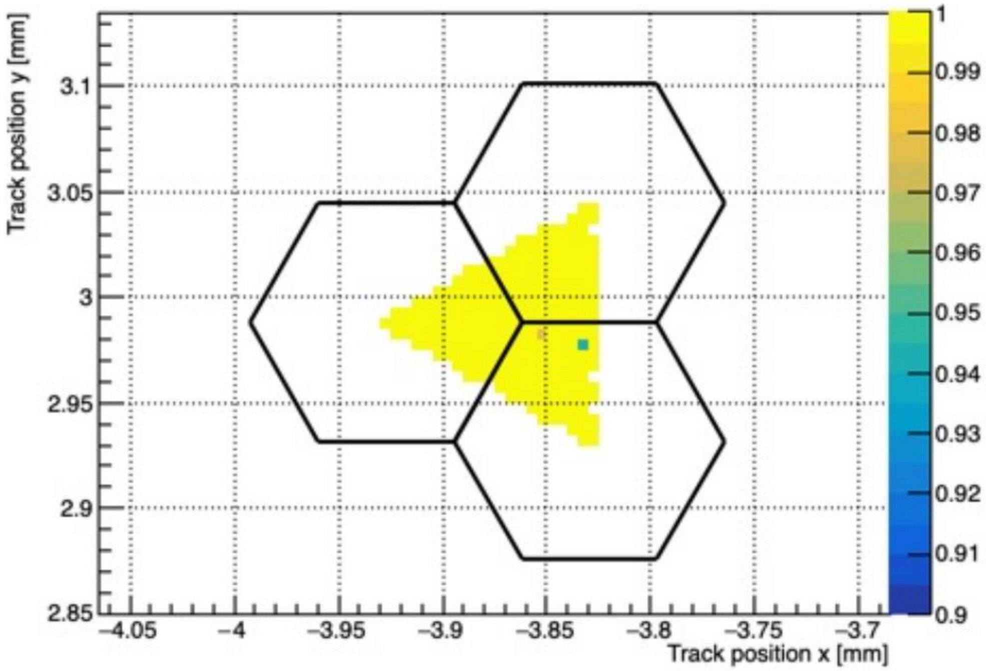


PicoAD prototype: Efficiency

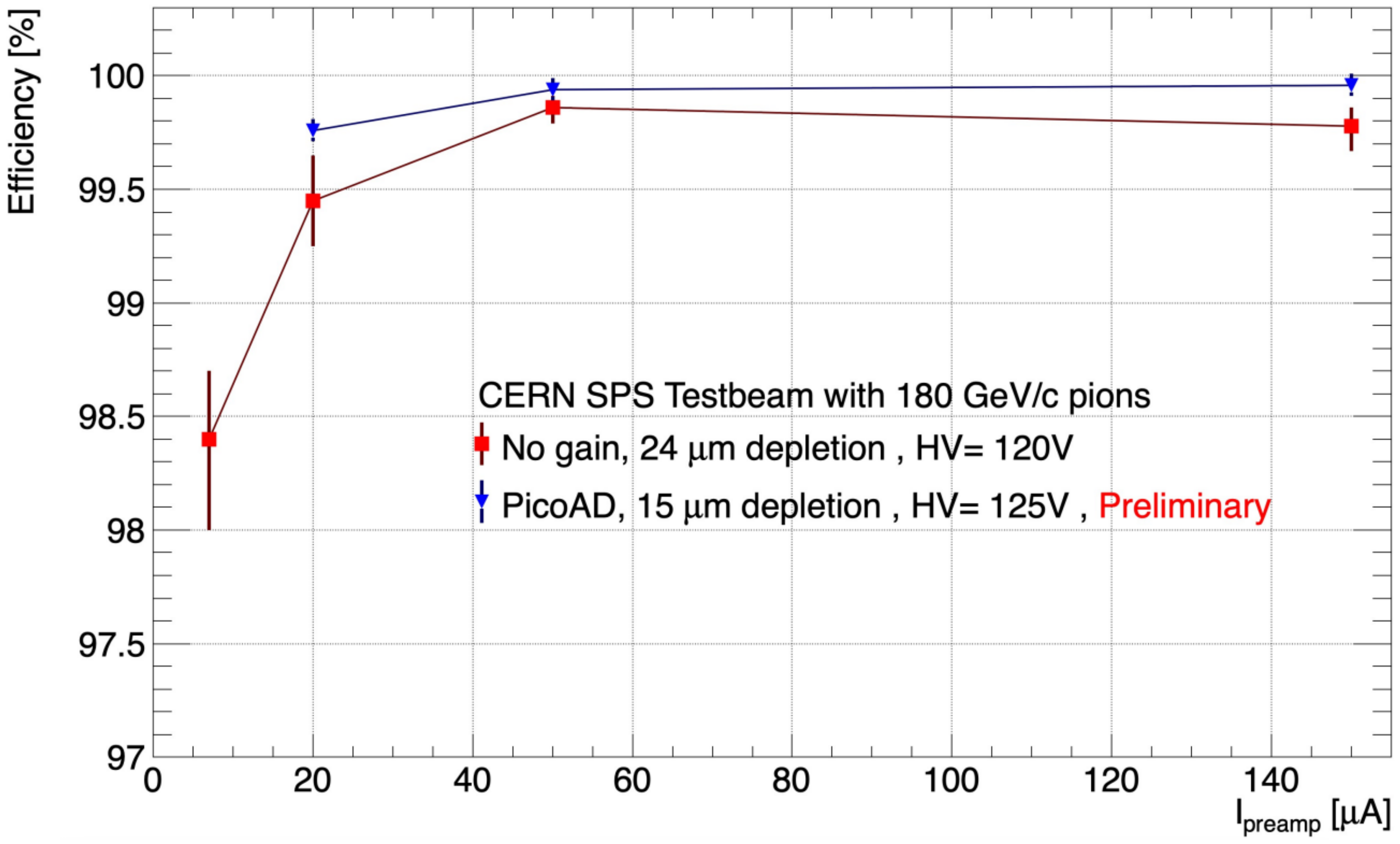
CERN SPS 180GeV pion beam
FEI4 Telescope ($\sigma_x \sim 10\mu m$ $\sigma_y \sim 15\mu m$)

I_{preamp} = 150 μA
V_{th} = 6 σV
HV = 120 V



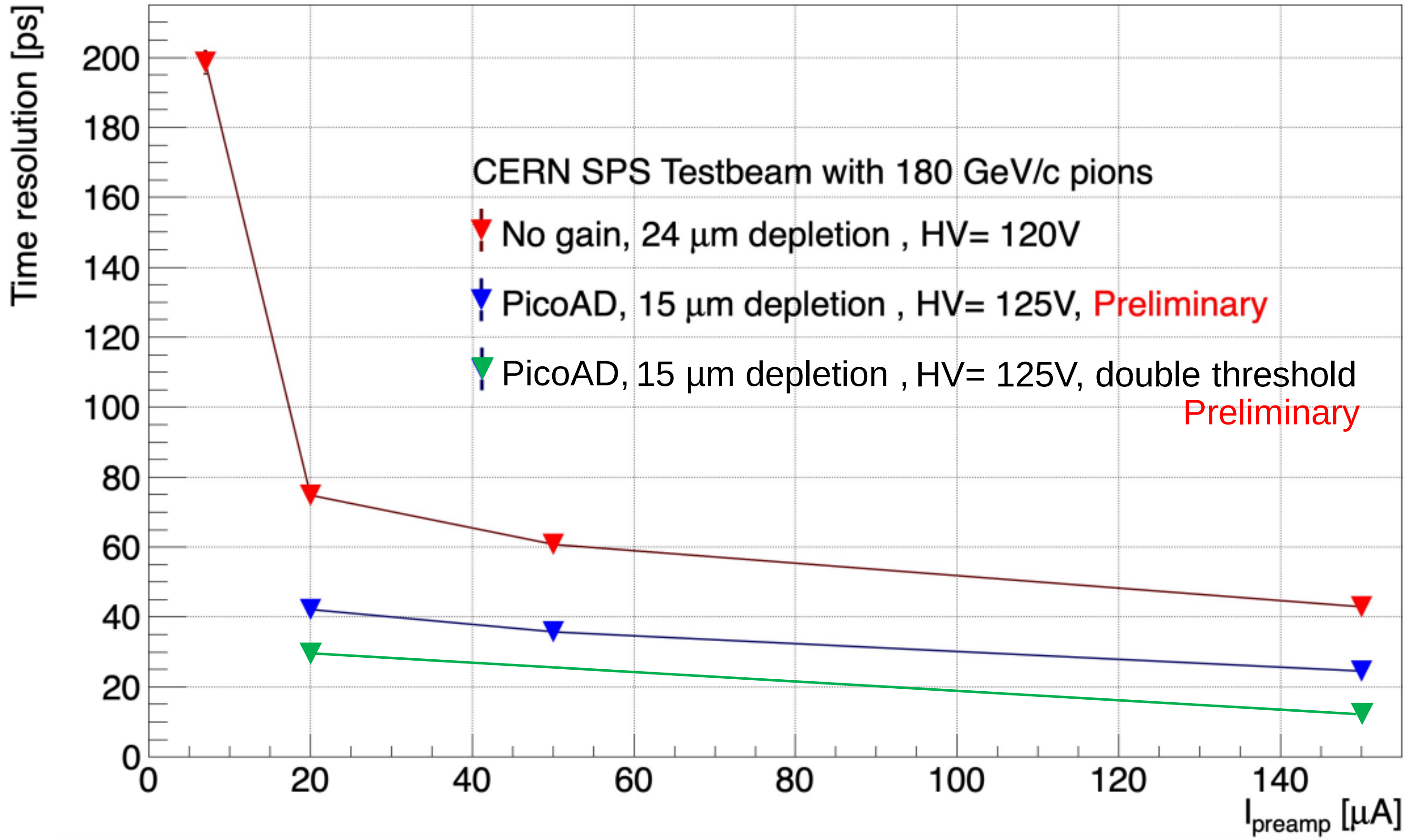


PicoAD prototype: Efficiency

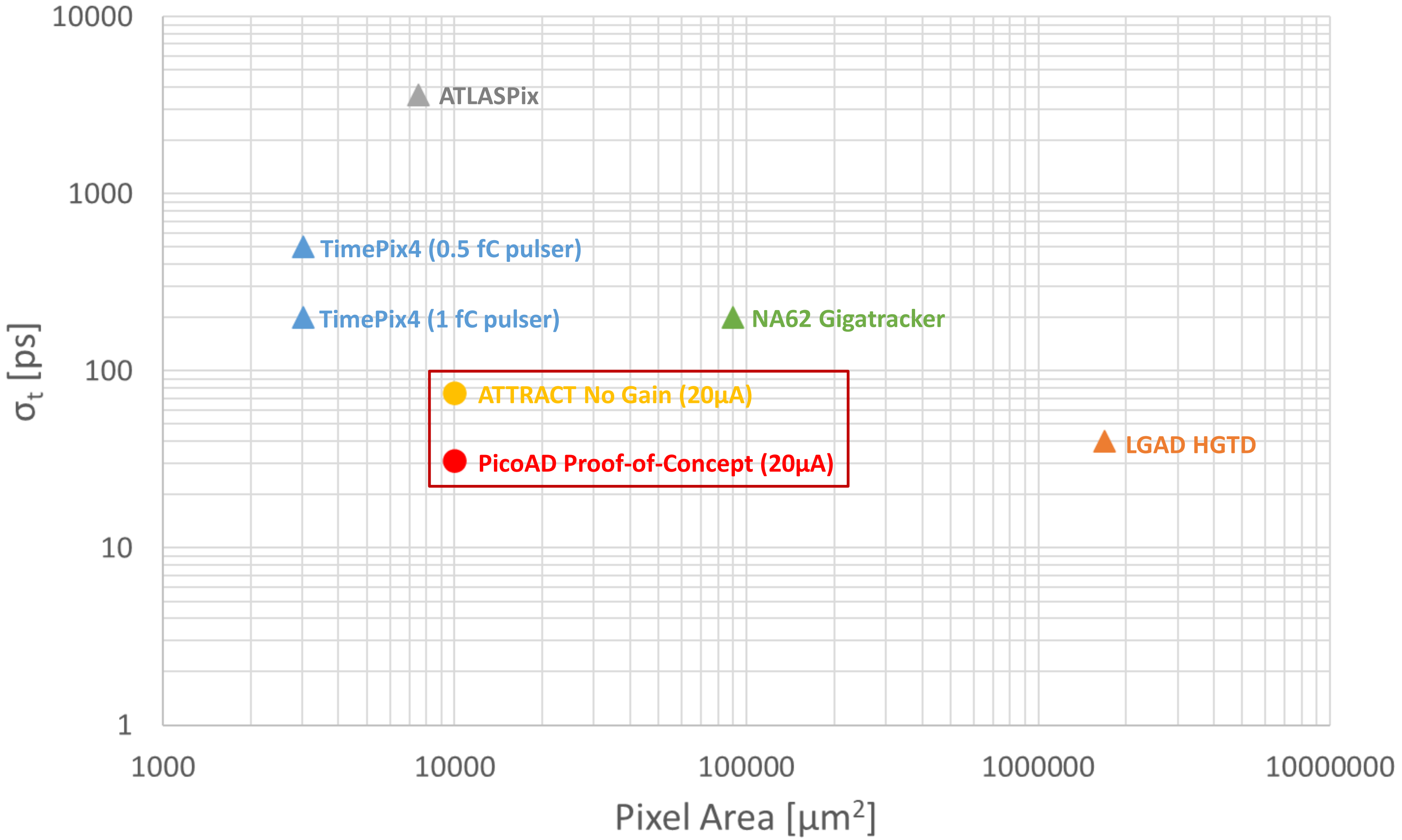


Reduced depletion thickness and still **better results**

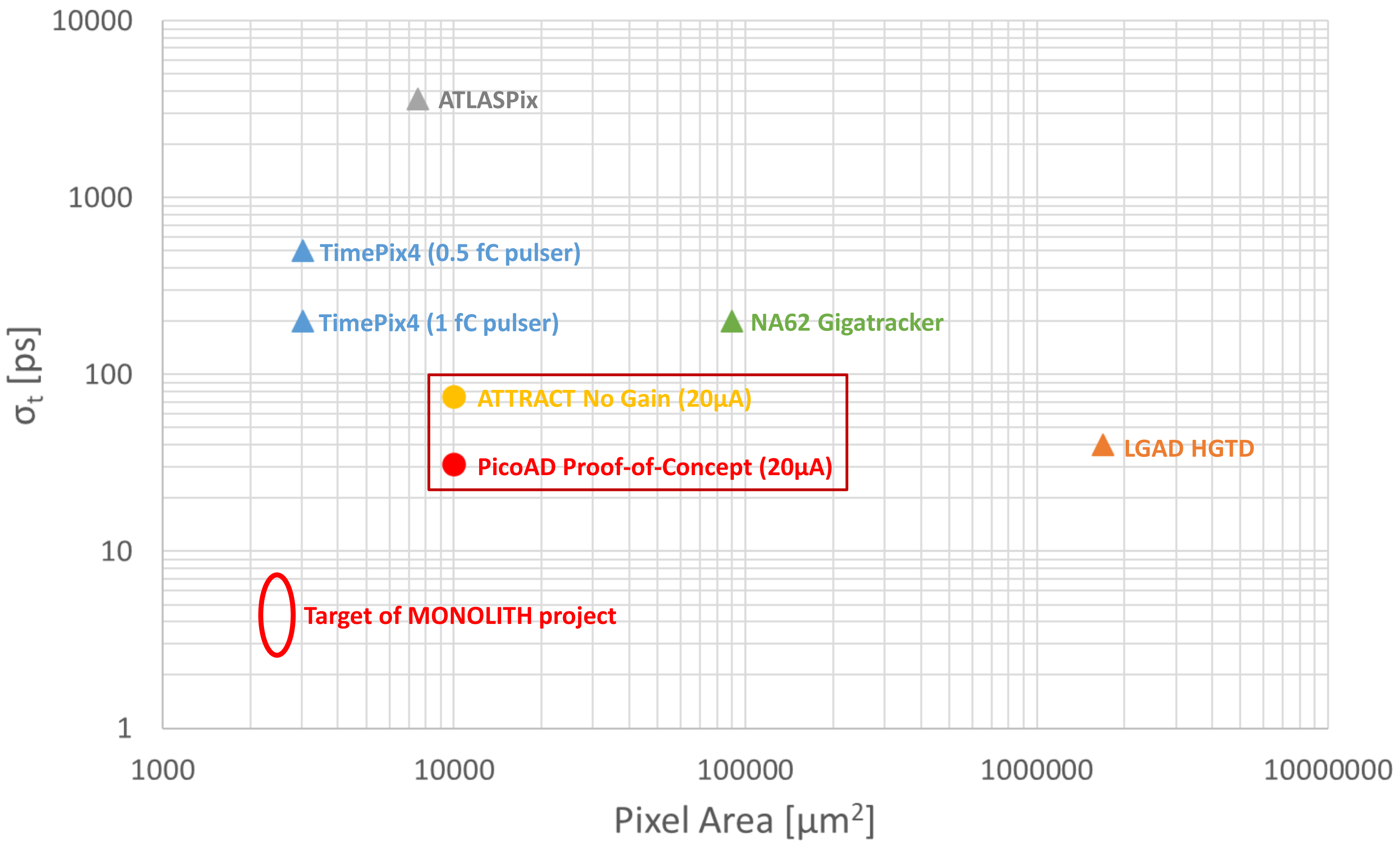
PicoAD prototype: Time resolution



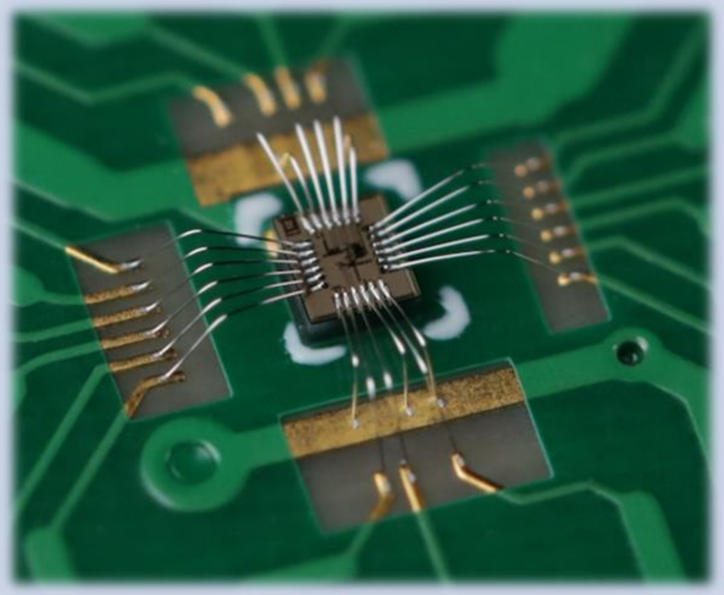
Comparison of time resolution



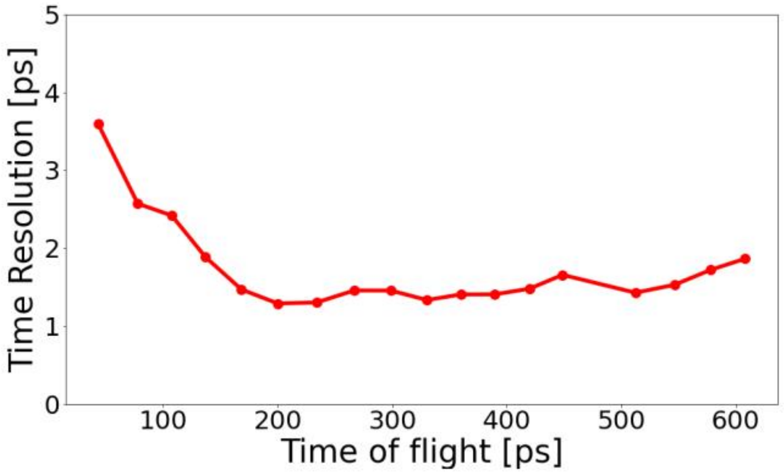
Comparison of time resolution



Picosecond TDC



Picosecond TDC test chip



Integrate in MONOLITH p1 Prototype
Soon to be tested
Improved version submitted in July 2021.

CONCLUSIONS

- SiGe BiCMOS proved the feasibility of a monolithic integration of silicon pixel sensors for ionizing radiation for **large area detectors with state-of-the-art space-time resolution**.

- Previous prototypes showed **36 ps time resolution without avalanche gain**.

- A **full-reticle chip will be produced** for the new FASER pre-shower and the 100µPET scanner, targeting ~100 ps time resolution.

- The development of a **4D detector with picosecond time resolution** is in progress with the MONOLITH project. State-of-the-art space and time resolution are possible in a single device.

Main publications and patents

Articles:

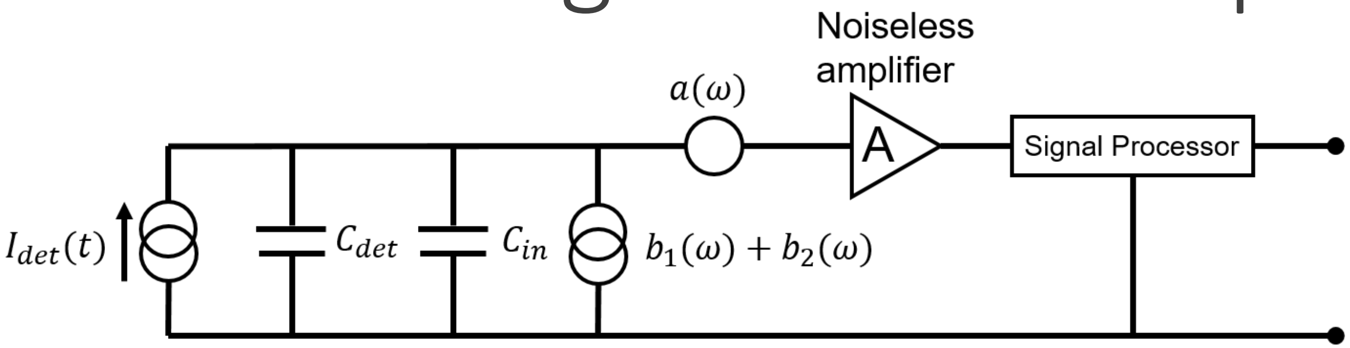
- ATTRACT prototype without gain: JINST 17 (2022) P02019, https://doi.org/10.1088/1748-0221/17/02/P02019
- Small-area pixels power consumption: JINST 15 (2020) P11025, https://doi.org/10.1088/1748-0221/15/11/P11025
- Hexagonal small-area pixels: JINST 14 (2019) P11008, https://doi.org/10.1088/1748-0221/14/11/P11008
- TT-PET demonstrator chip testbeam: JINST 14 (2019) P02009, https://doi.org/10.1088/1748-0221/14/02/P02009
- TT-PET demonstrator chip design: JINST 14 (2019) P07013, https://doi.org/10.1088/1748-0221/14/07/P07013
- First TT-PET prototype: JINST 13 (2017) P02015, https://doi.org/10.1088/1748-0221/13/04/P04015
- Proof-of-concept amplifier: JINST 11 (2016) P03011, https://doi.org/10.1088/1748-0221/11/03/P03011

- TT-PET engineering: arxiv:1812.00788
- TT-PET simulation & performance: arxiv:1811.12381

Patents:

- PLL-less TDC & synchronization System: EU Patent EP18181123.3
- Picosecond Avalanche Detector: EU Patent EP18207008.6

Equivalent Noise Charge: device comparison

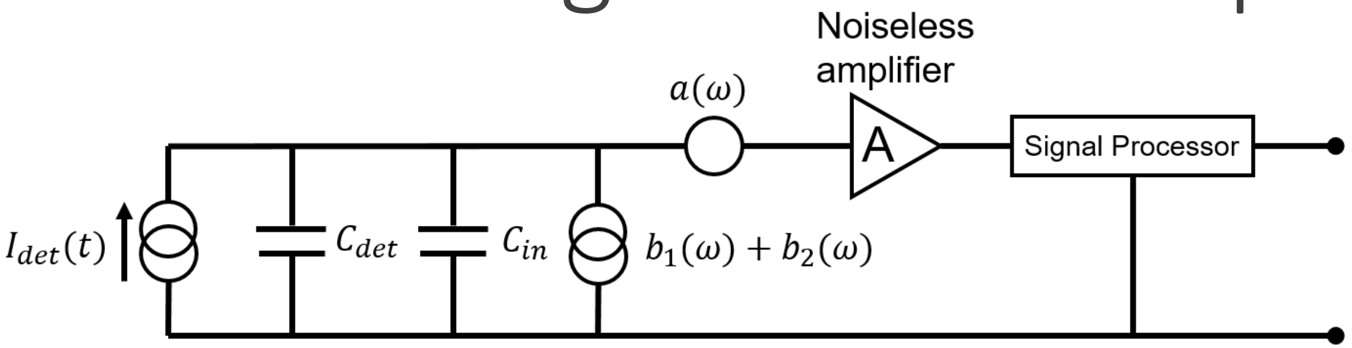


$$ENC^2 = A_1 \frac{a_W}{\tau_M}(C_{det} + C_{in})^2 + A_2 \frac{ln2}{\pi} c(C_{det} + C_{in})^2 + A_3(b_1 + b_2)\tau_M$$

$$\tau_M \sim 1\, ns$$

How do MOS-FET and BJT compare in terms of noise?

Equivalent Noise Charge: device comparison



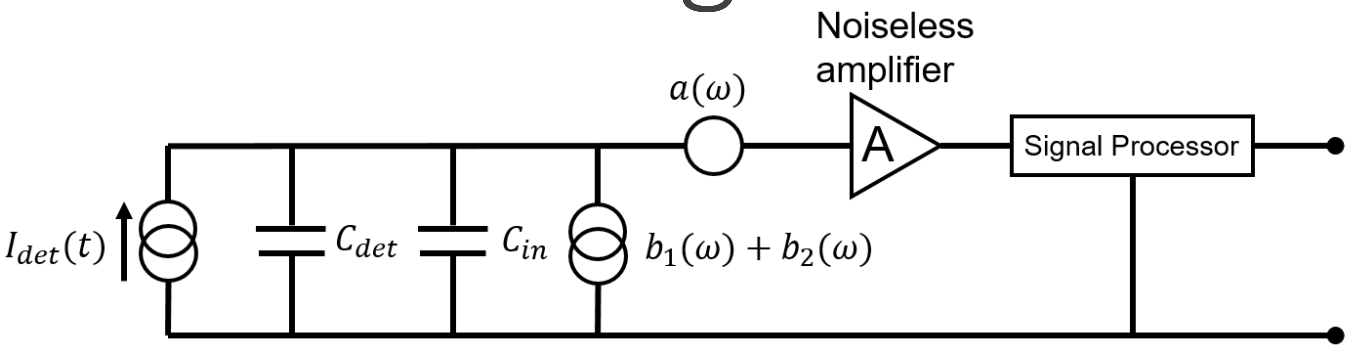
$$ENC^2 = A_1 \frac{a_W}{\tau_M}(C_{det} + C_{in})^2 + A_2 \frac{ln2}{\pi} c(C_{det} + C_{in})^2 + A_3(b_1 + b_2)\tau_M$$

CMOS based amplifier

$$2kT\frac{h}{g_m}$$

Large $^1/_f$ contribution

Equivalent Noise Charge: device level



$$ENC^2 = A_1 \frac{a_W}{\tau_M}(C_{det} + C_{in})^2 + A_2 \frac{ln2}{\pi} c(C_{det} + C_{in})^2 + A_3(b_1 + b_2)\tau_M$$

BJT based amplifier

$$ENC_{\text{series noise}} \propto \sqrt{k_1 \cdot \frac{C_{tot}^2}{\beta} + k_2 \cdot R_b C_{tot}^2}$$

Goal: maximize the current gain β at high frequencies while keeping a low base resistance R_b

Equivalent Noise Charge

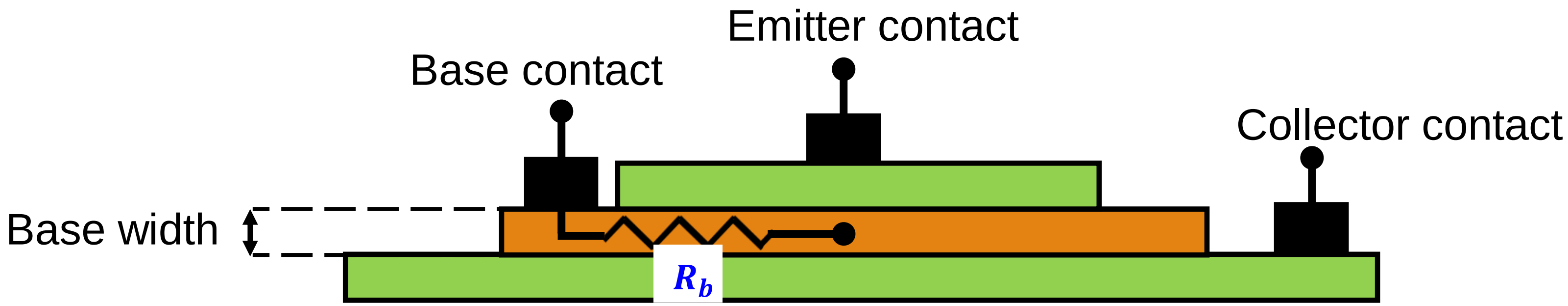
For a NPN BJT, the amplifier current gain β can be expressed as:

$$\beta = \frac{i_C}{i_B} = \frac{\tau_p}{\tau_t}$$

τ_p = hole recombination time in Base

τ_t = electron transit time (Emitter to Collector)

Large $\beta \Longrightarrow$ Minimize the electron transit time



SiGe BiCMOS: A commercial VLSI foundry process

Some foundries offering SiGe BiCMOS:

- IHP Microelectronics (→ Research Inst.)
- Tower Semiconductors
- Globafoundries
- TSMC
- STm
- AMS
- …

Implemented as an adder module to an existing CMOS technologies.

⇩

Typical increase for same tech. node in cost: ~10-15 %

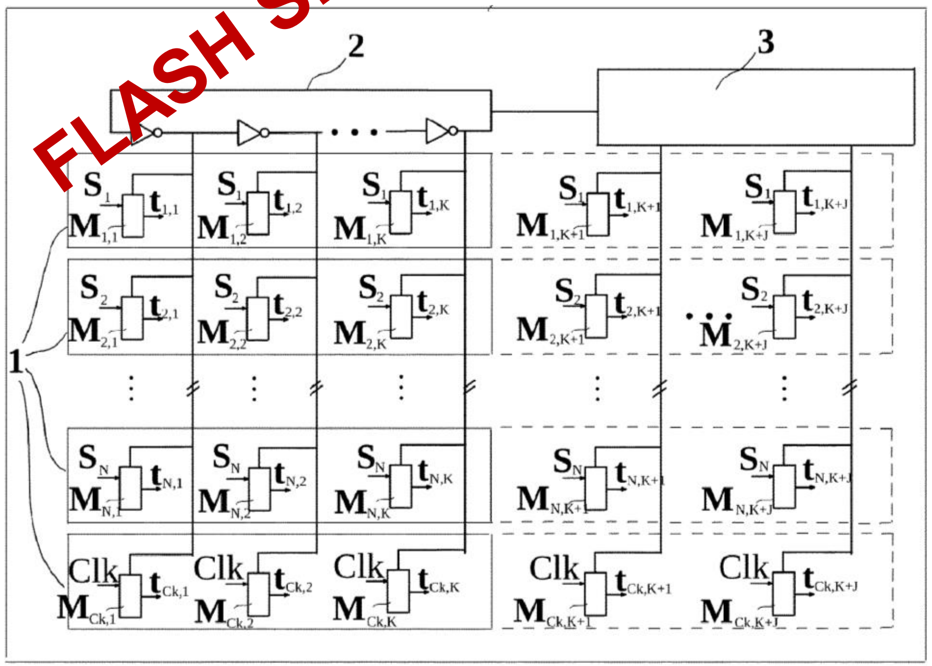
SiGe HBT scaling

Figure of merit	SiGe HBT		CMOS	
	Base	Scaling	Base	Scaling
f_T	Good	Improves	Good	Improves
f_{MAX}	Good	Improves	Good	Improves
NF_{MIN}	Good	Improves	Good	Improves
1/f noise	Good	Neutral	Neutral	Worsens
g_M/g_O	Good	Improves	Poor	Worsens
g_M	Good	Improves	Poor	Improves
mismatch	Good	Neutral	Poor	Worsens
linearity	Good	Neutral	Good	Worsens
voltage headroom	Neutral	Neutral	Poor	Worsens
breakdown voltage	Good	Neutral	Poor	Worsens

From: J.D. Cressler, IEEE transactions on nuclear science, vol. 60, n. 3 (2013)

A self calibrating, low-power TDC

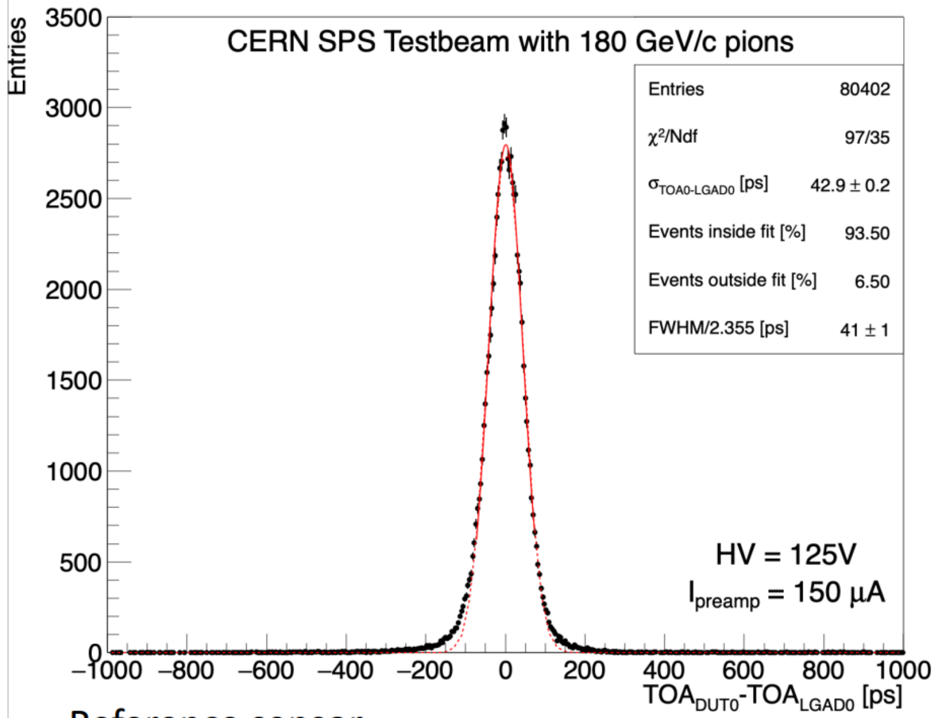
FLASH SLIDE



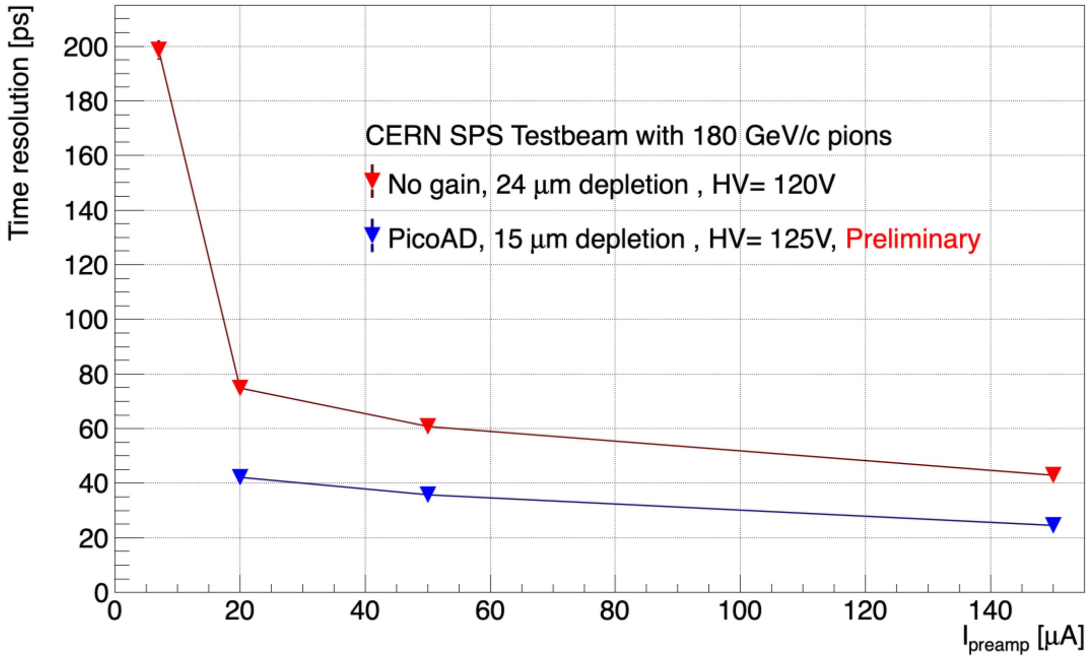
- 16 channels, each made by three sets of latches (1) connected to the same ring oscillator (2) to measure TOA and TOT of the signal.
- 1 calibration channel is used to measure the period of the ring oscillator on an event-by-event basis (UniGe patent).
- Linear Feedback Shift Registers (3) are used to extend the dynamic range of the measurements / also to store and trasnfer data.
- The large load on the Ring Oscillator may reduce its speed: a chain of buffers is connected to maintain a high oscillation frequency.
- The Ring Oscillator is always running, to increase its stability, while the buffers can be activated on demand, to reduce the power consumption.

https://worldwide.espacenet.com/patent/search?q=pn%3DEP3591477A1

PicoAD prototype: Time resolution



Reference sensor

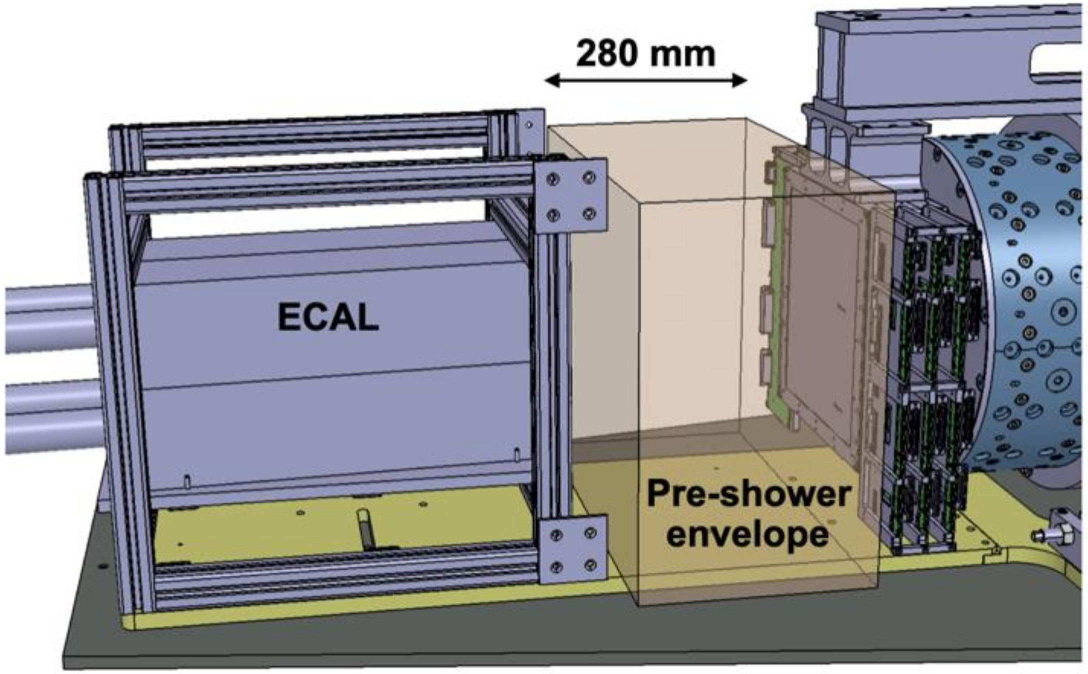


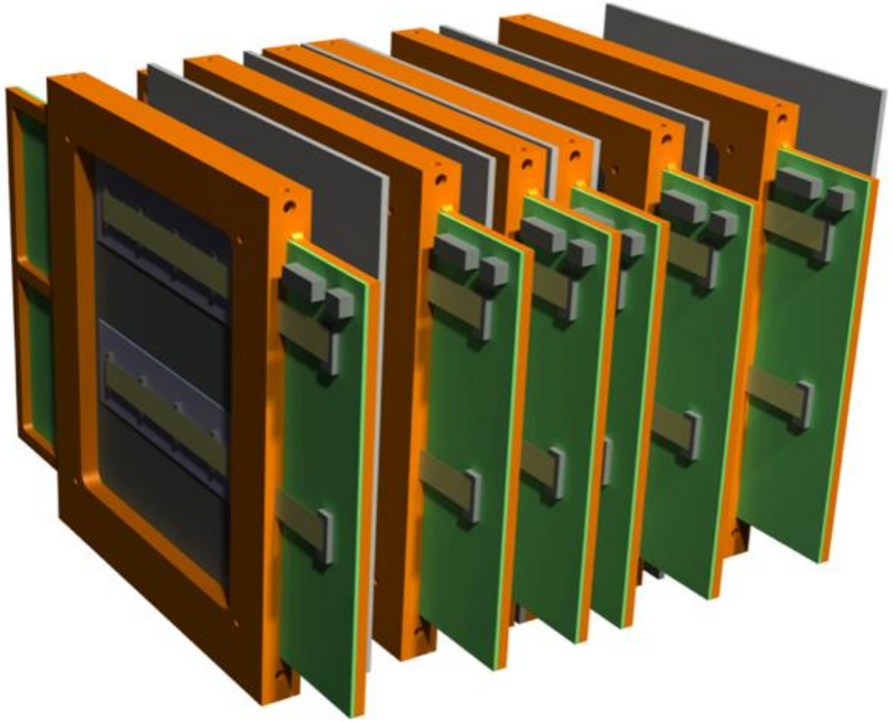
$\sigma_{LGAD} \approx 35.6ps$

$$\sigma_{PicoAD} \approx \sqrt{42.9ps^{\,2} - 35.6ps^{\,2}} \approx 24ps$$

More than 10ps improvement!

Pre-shower design



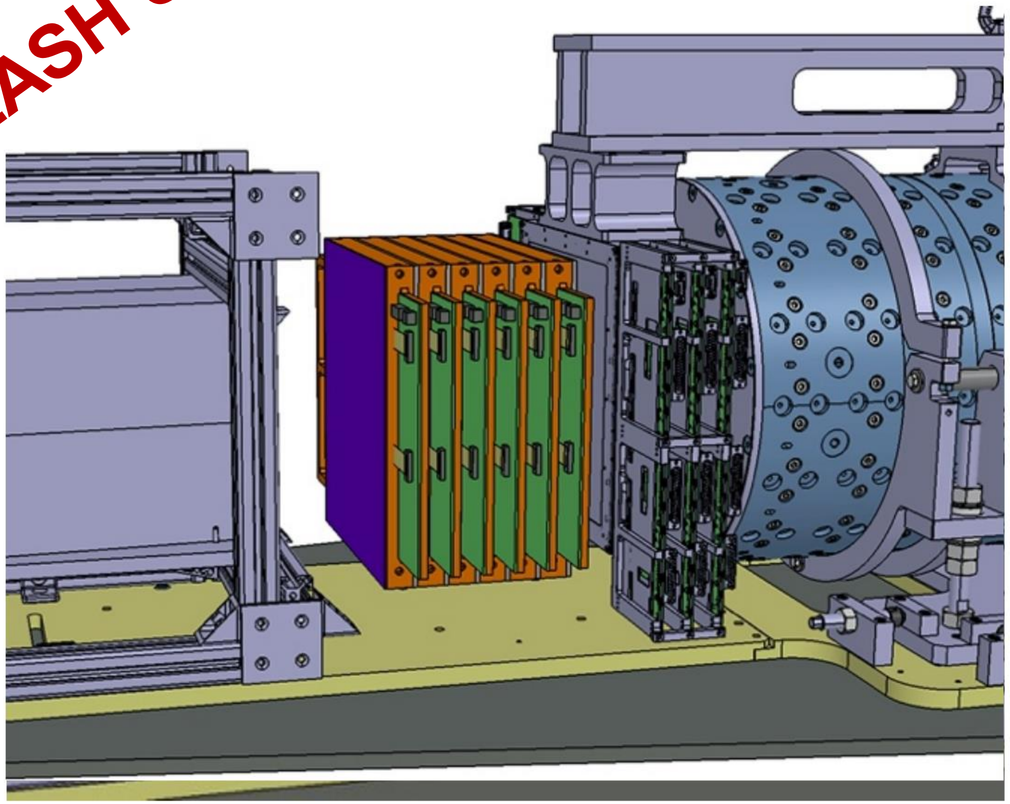


6 detector planes + 2 plastic scintillators:

Each plane: 1 X0 of tungsten + 1 plane of monolithic Si-pixel detectors

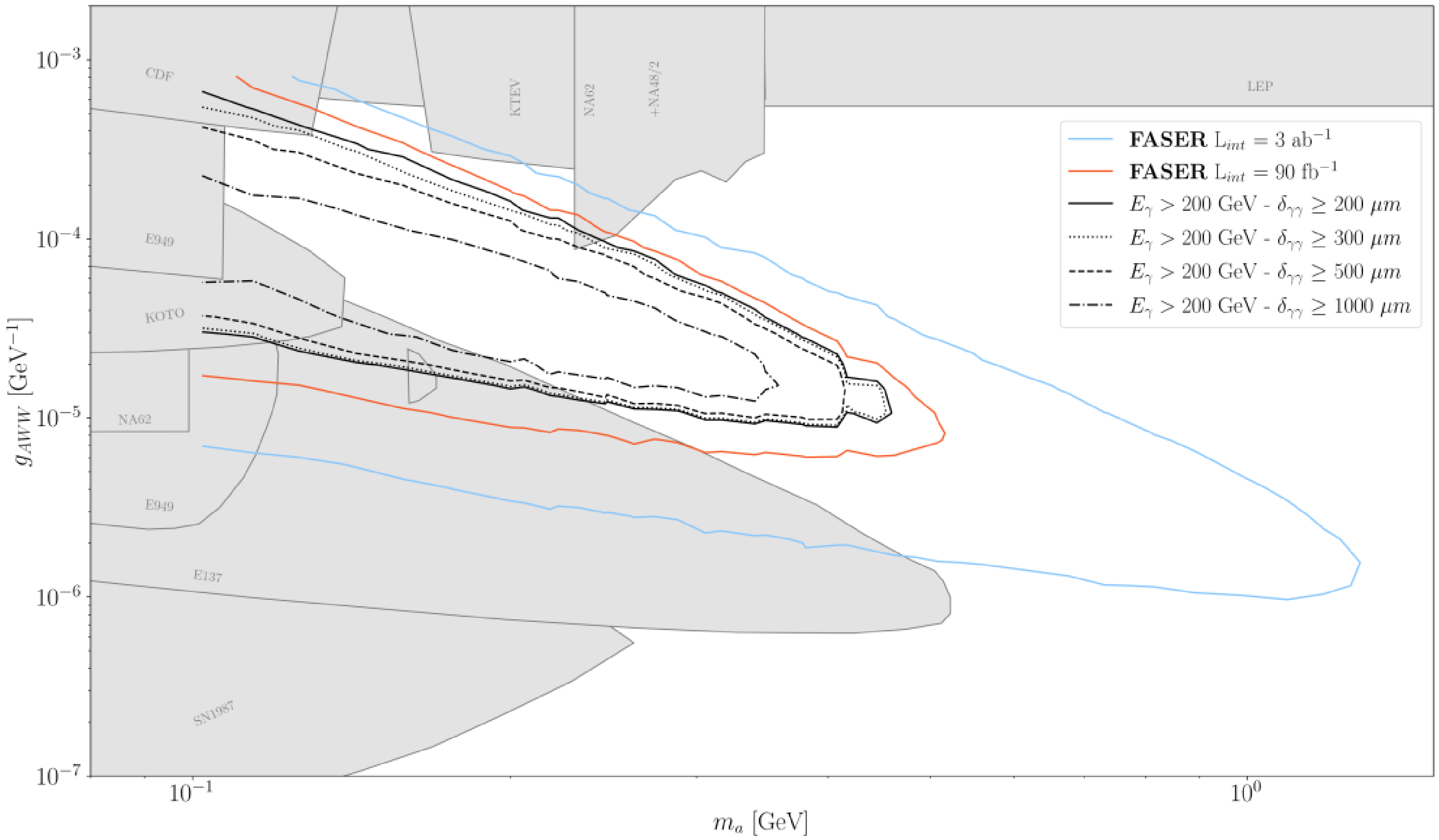
The FASER pre-shower

FLASH SLIDE



- Enable di-photon channel in FASER.
- Distinguish two ultra-collimated TeV-level EM showers.
- **Time resolution target: ~100 ps.**
- Very large pixel dynamic range: 0.5 fC – 64 fC.
- Large area prototype submission: July 2021.
- Full-reticle ASIC submission: October 2022.

Search for ALP: Expected performance



0 photon background assumption:

- High rejection probability of single photon events.
- Rare TeV-scale single photon events pointing to ATLAS IP.

Main background source:

- Neutrino background