The evolution of the ALICE inner tracking system

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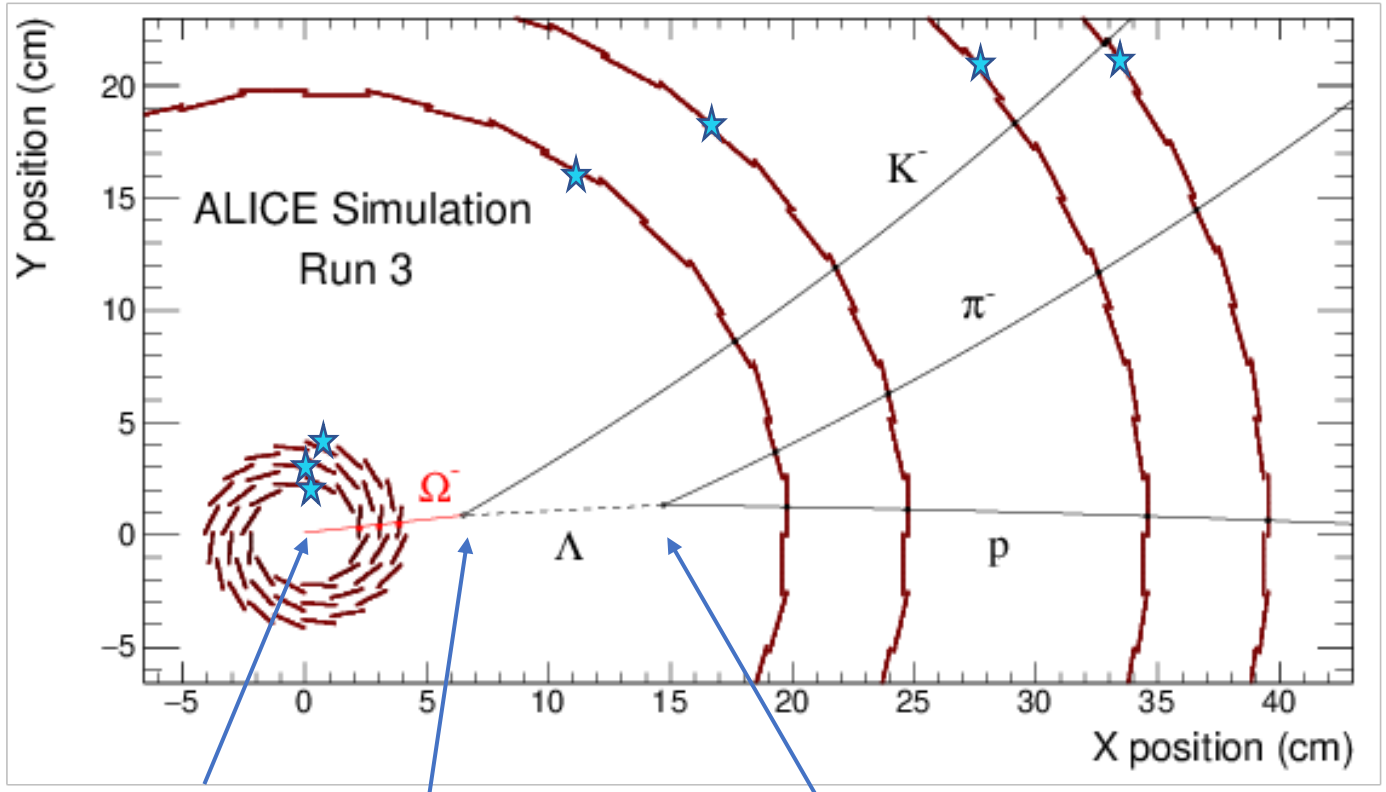
University of Geneva, 5 April 2023

Charged particle tracker: goals

- **Measure trajectory of charged particles**
  - Measure several points along the track and fit curves to the points (helix in a magnetic field)
- **Extrapolate tracks to the point of origin**
  - Determine positions of primary vertices and identify interesting collision vertex: **VERTEXING**
  - Find **secondary vertices** from decay of long-lived particles
- **Use the track curvature to determine the particle momentum: PID**



Primary vertex

Secondary vertex

Tertiary vertex

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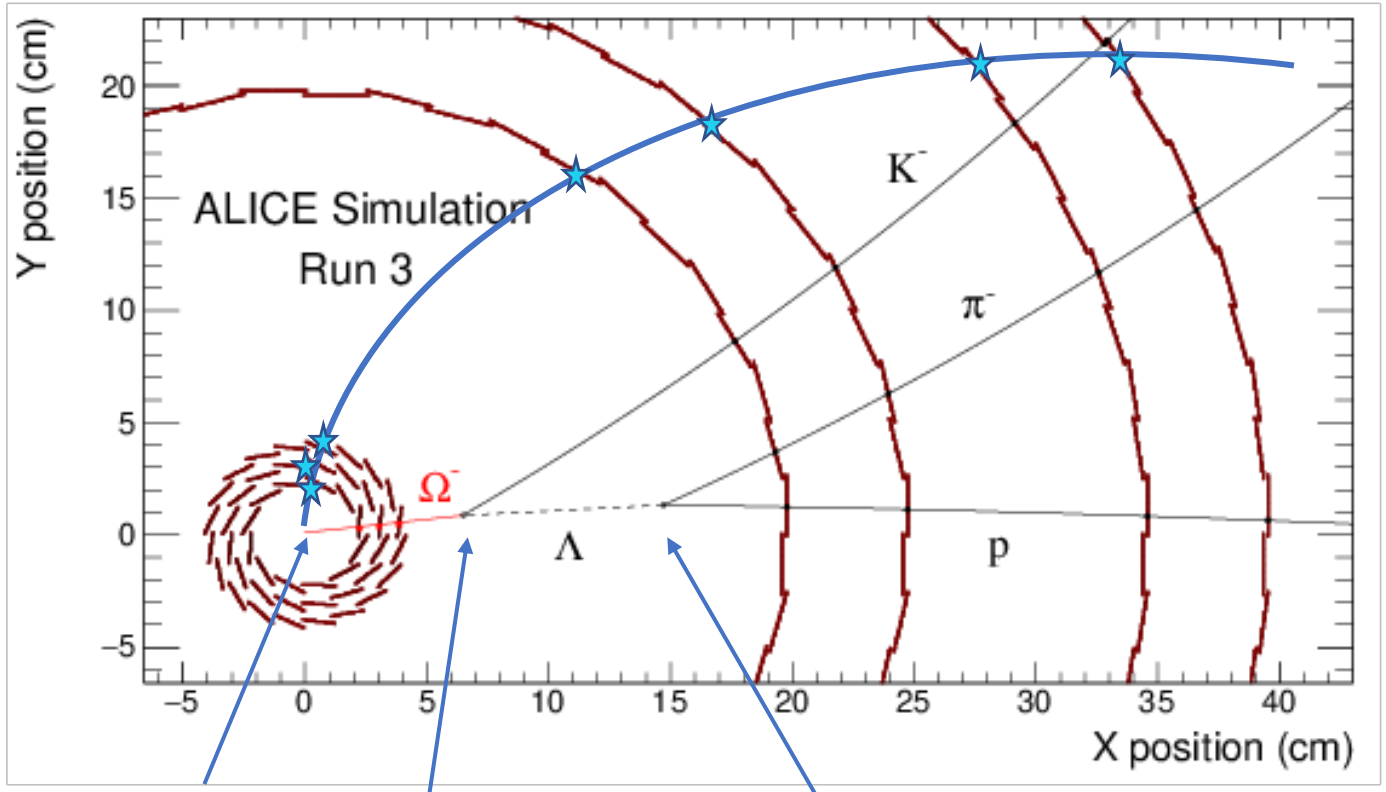
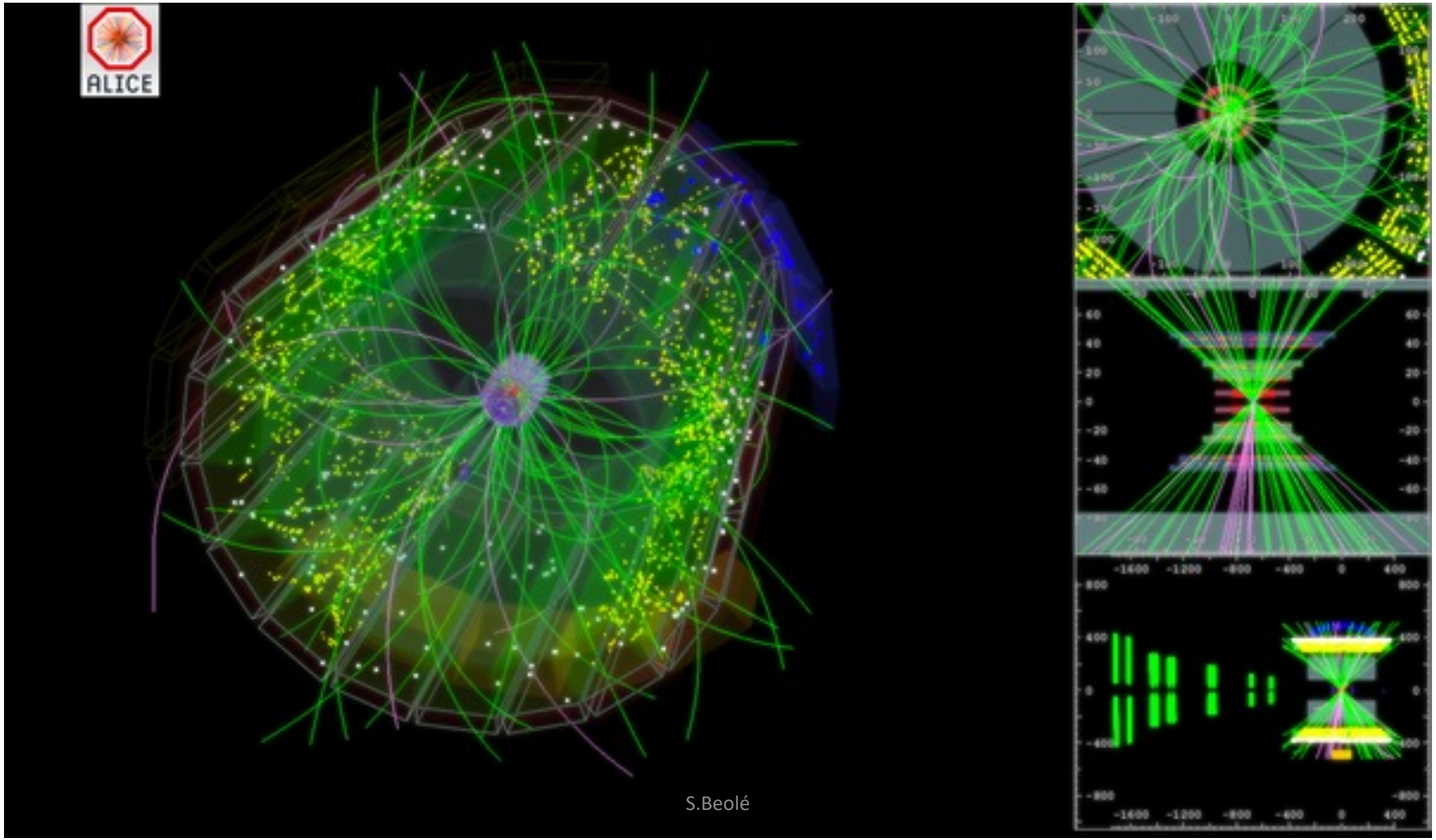


Primary vertex

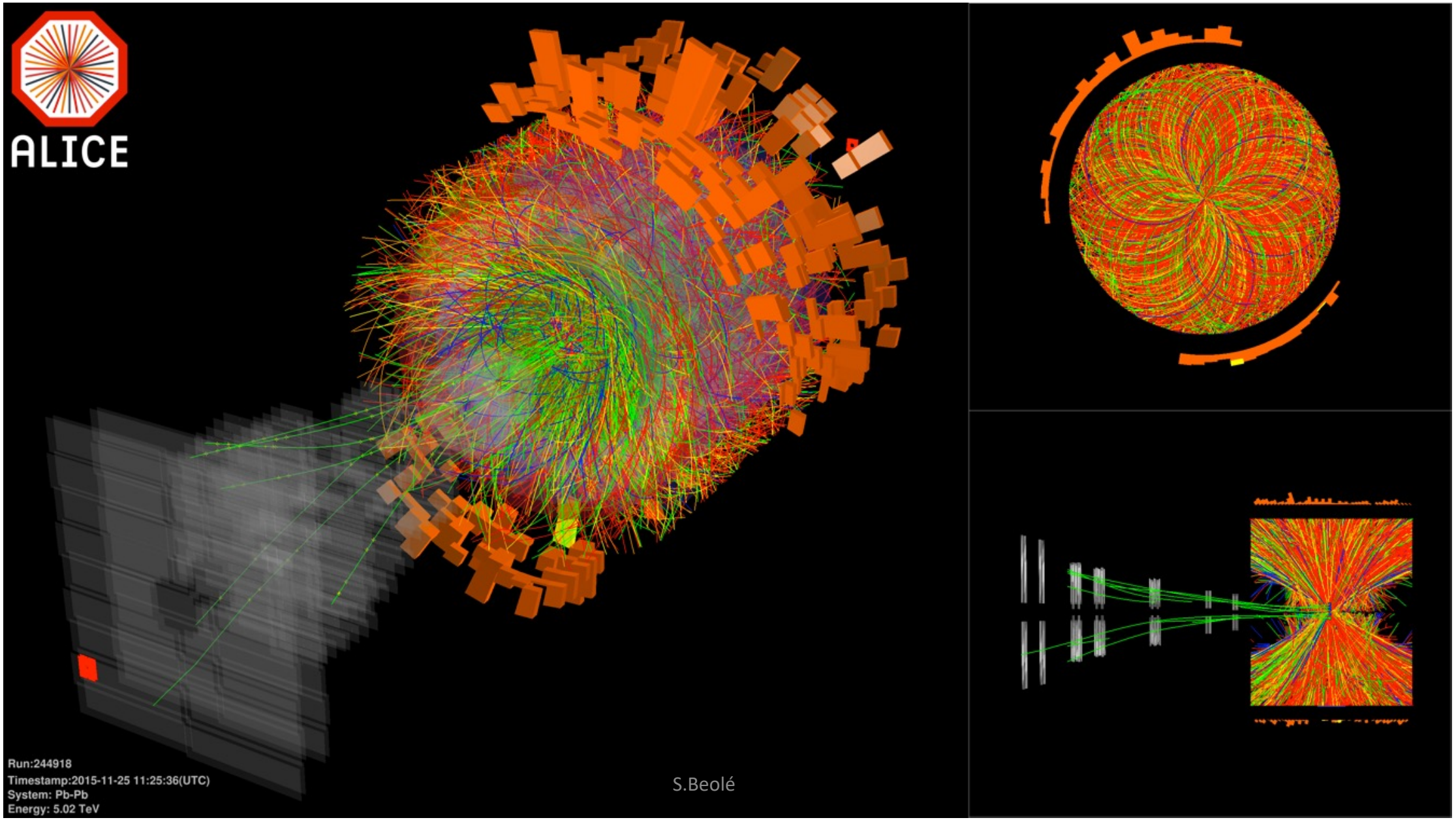
Secondary vertex

Tertiary vertex

proton-proton collisions at LHC



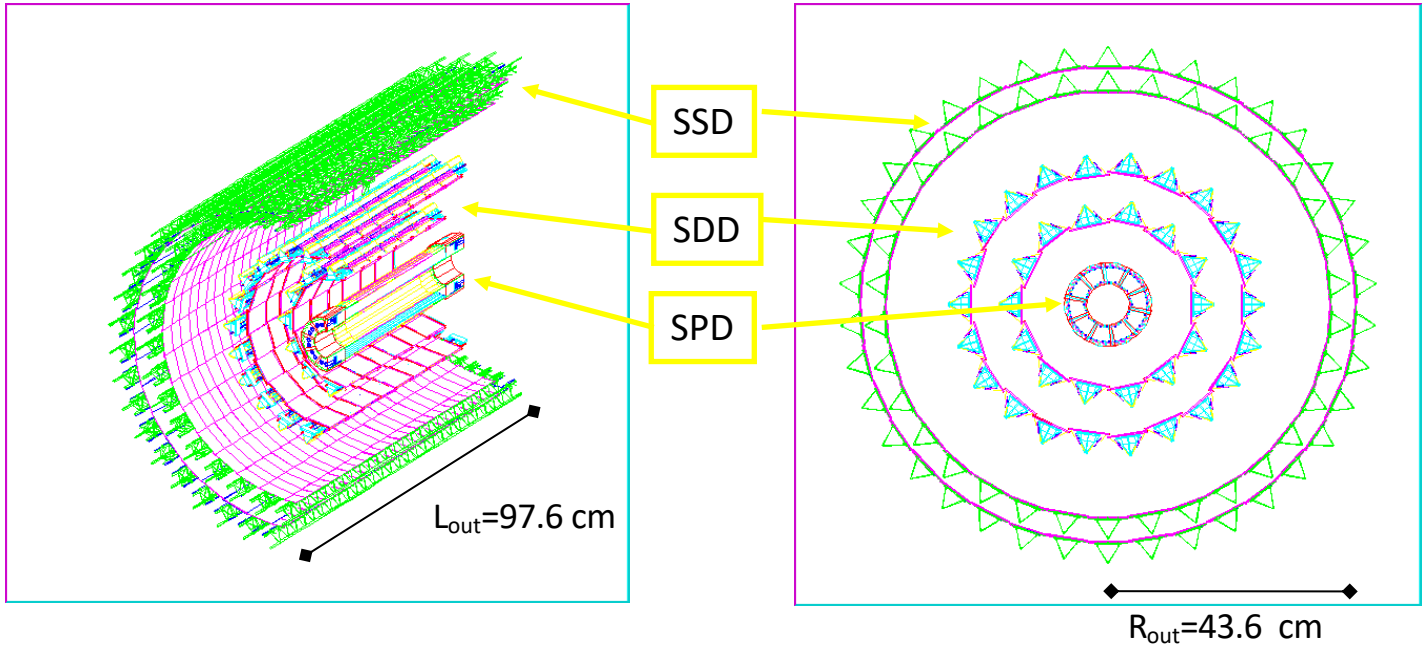
lead-lead collisions at LHC



Tracker requirements

- Excellent spatial resolution
  - Single point resolution
  - Double track resolution
- Efficiency (100%)
- As little material as possible
  - Multiple scattering
  - Photon conversion
- Time resolution (4D tracking)
- Radiation hardness

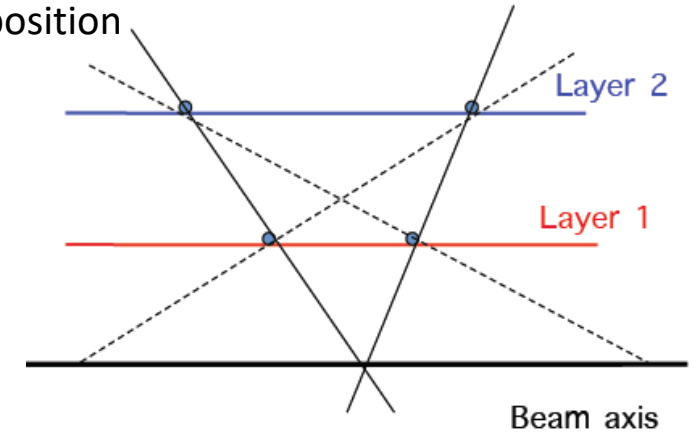
ALICE ITS1



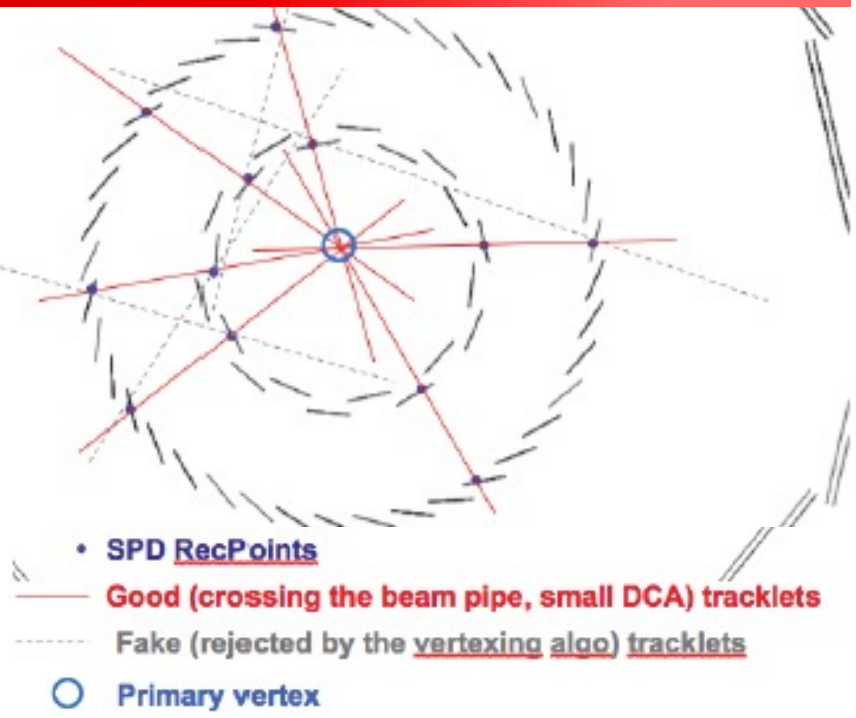
- 6 Layers, three technologies (keep occupancy ~constant ~2%)
  - **SPD: Silicon Pixels (0.2 m², 9.8 Mchannels)**
  - SDD: Silicon Drift (1.3 m², 133 kchannels)
  - SSD: Double-sided Strip Strip (4.9 m², 2.6 Mchannels)

Vertexing: primary vertex reconstruction

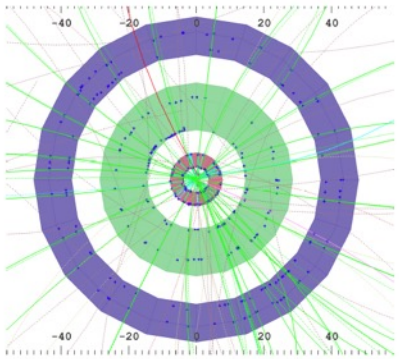
Side view: Z position

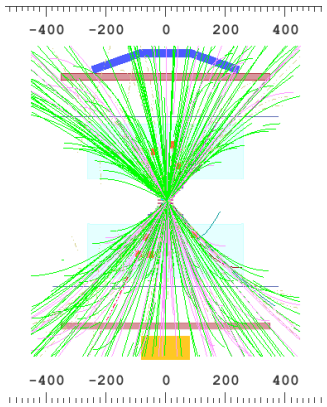


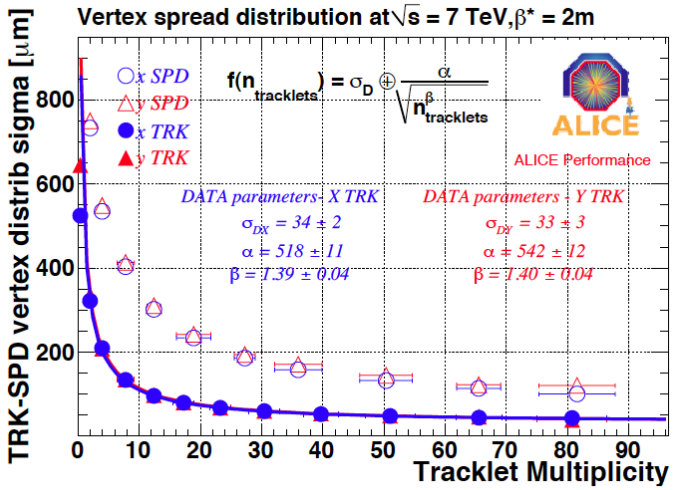
Front view: rϕ



- Pixel detector are used to provide vertex position (fast response – online determination)
  - Tracklets instead of tracks
- Vertex is used as seed for tracking
- Tracks are used to refine vertex position measurement after tracking

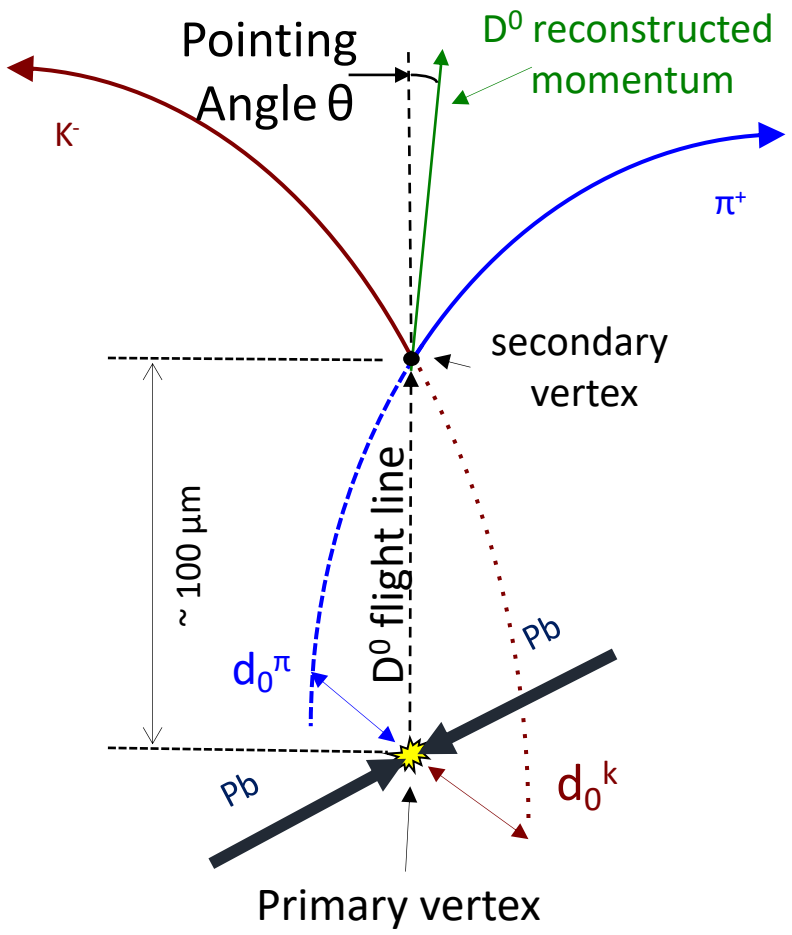




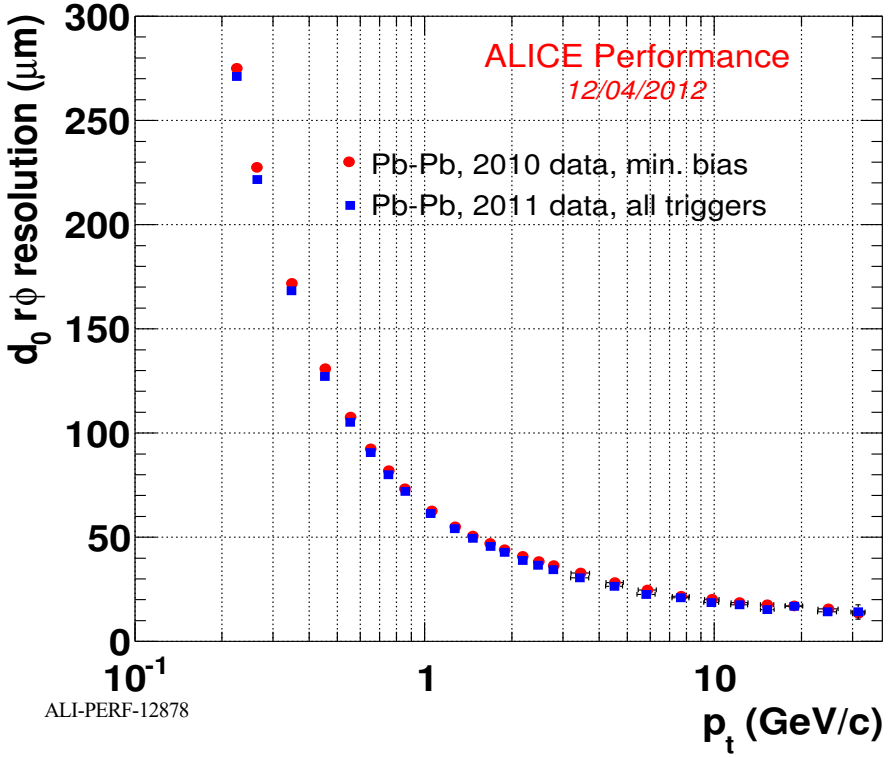


S.Beolé

Secondary Vertex reconstruction



Particle	Decay Channel	cτ (μm)
D^0	$K^- \pi^+$ (3.8%)	123
D^+	$K^- \pi^+ \pi^+$ (9.5%)	312
	$K^+ K^- \pi^+$ (5.2%)	150
	$p K^- \pi^+$ (5.0%)	60



- Example: ALICE ITS1

The ALICE experiment

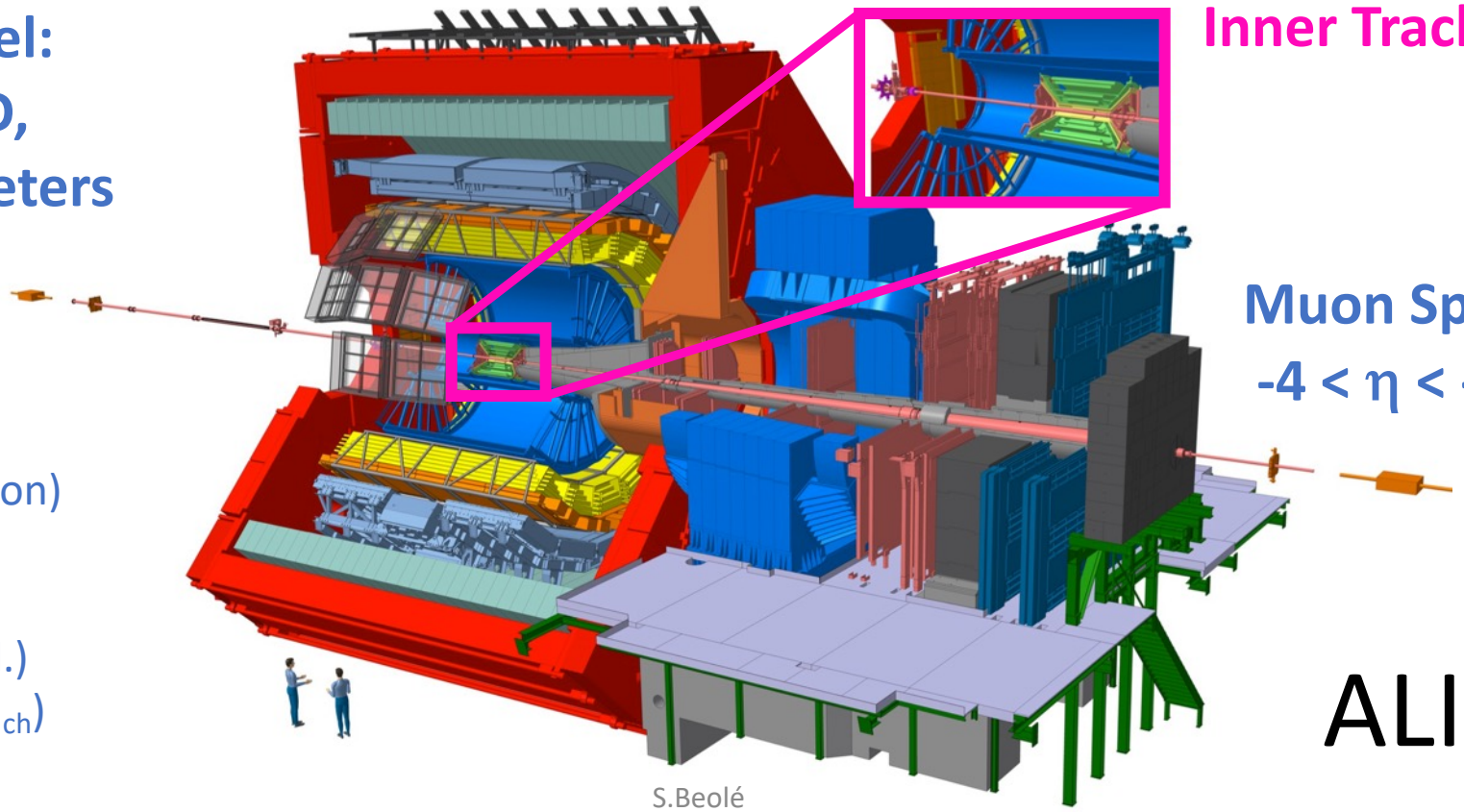
The ALICE experiment

- ALICE is the experiment at the LHC specifically designed for studying heavy ion collisions
- The main goal is exploring the deconfined phase of QCD matter → quark-gluon plasma

LHC Pb-Pb → large energy density (> 15 GeV/fm^3) & **large volume** (~ 5000 fm^3)

Central Barrel: Tracking, PID, EM-Calorimeters
$|\eta| < 0.9$

ACORDE (cosmics)
Forward detectors:
- AD (diffraction selection)
- V0 (trigger, centrality)
- T0 (timing, lumi)
- ZDC (centrality, ev. sel.)
- FMD (N_{ch}) PMD (N_γ, N_{ch})



Inner Tracking System

Muon Spectrometer
$-4 < \eta < -2.5$

ALICE 1

ALICE Upgrades in LS2

Motivation:

High-precision measurements of rare probes at **low transverse momentum**

- **Cannot be selected by hardware trigger**
- Need to record large minimum-bias data sample: **read out all Pb-Pb interactions** up to the **maximum collision rate of 50 kHz**

Goal:

- Pb-Pb integrated luminosity 13 nb^{-1} (plus pp, pA and O-O data)

  -> Gain factor 100 in statistics for min bias sample w.r.t. runs 1+2
- **Improve vertex reconstruction and tracking capabilities**

Strategy:

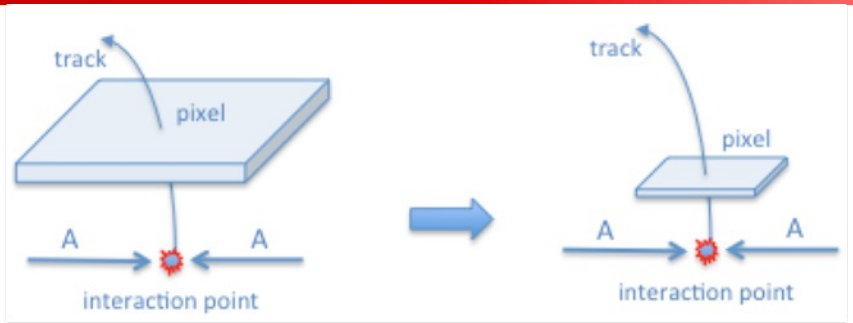
- **new ITS, MFT, FIT, TPC ROC**
- **update FEE of most detectors**
- **new integrated Online-Offline system (O^2)**

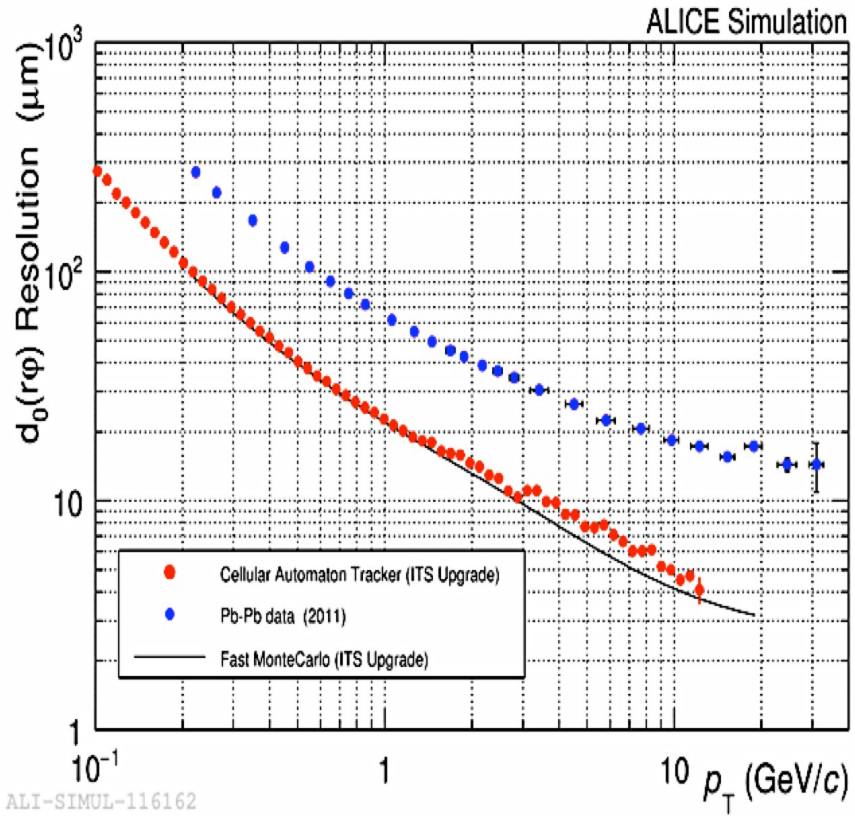
ALICE 2

New generation trackers: CMOS sensors

New ITS (ITS2) Design Objectives

- **Improve impact parameter resolution** by
  factor ~3 in rϕ and factor ~5 in z at p_T = 500 MeV/c
  - Get closer to Interaction Point: 39 mm -> 23 mm
  - Reduce material budget:
    1.14% X_0 -> 0.35% X_0 (inner layers)
  - Reduce pixel size:
    50 x 425 μm^2 -> ~30 x 30 μm^2
- **Improve tracking efficiency and p_T resolution at low p_T**
  - Increase number of track points: 6 -> 7 layers
- **Fast readout**
  - Readout of Pb-Pb collisions at 50 kHz (ITS1: 1 kHz) and p-p at 400 kHz





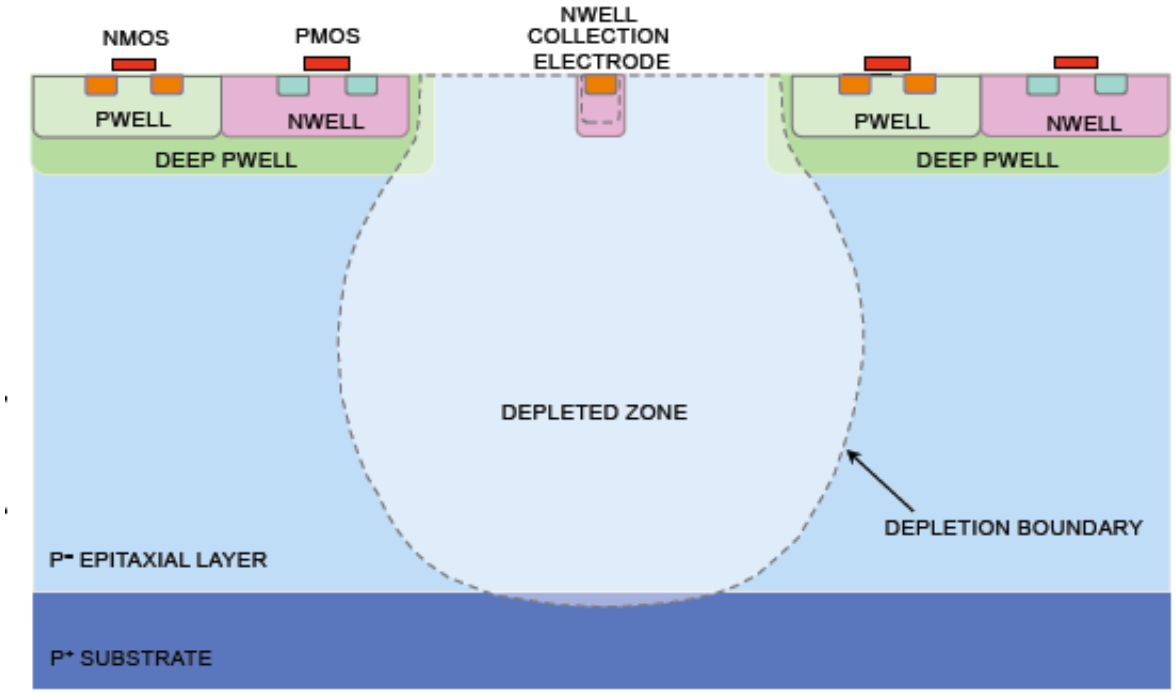
ITS TDR: J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002

MAPS: CMOS monolithic active pixel sensor

MAPS: sensor and electronics on the same substrate

Exploits commercial CMOS imaging sensor process to detect charge particles

A few modifications needed:
DEEP P-WELL to shield CMOS circuitry and avoid loss of efficiency



main advantages:

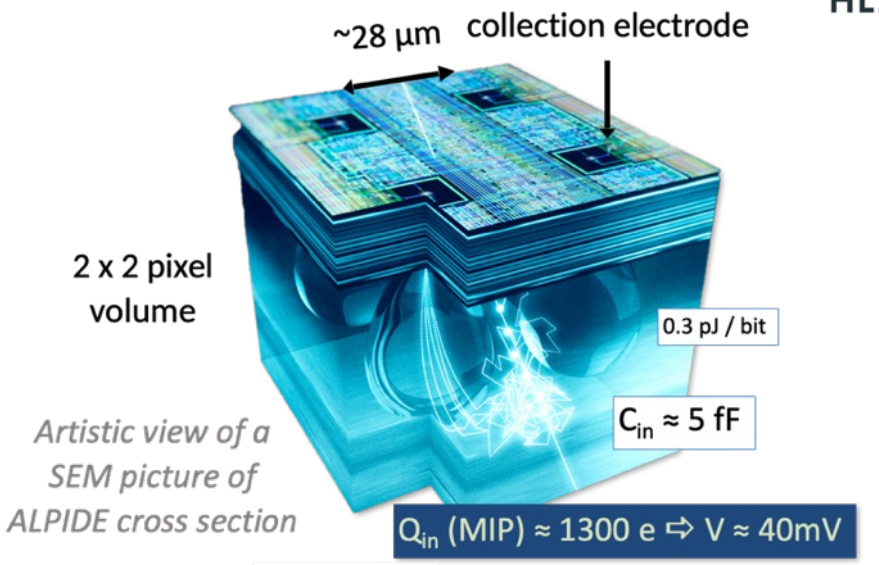
- thin sensor (all in 1 layer, thinned down to <50μm)
- easy integration
- low noise
- low power consumption

disadvantages:

- Signal charge is collected from the non-depleted layer, diffusion dominated and prone to trapping after irradiation
- Deep well and substrate limit extension of the depletion: to fix this -> pixel design/process modification.

ALPIDE Monolithic Pixel Sensor

CMOS Pixel Sensor – Tower Semiconductor 180nm CMOS Imaging Sensor (CIS) Process

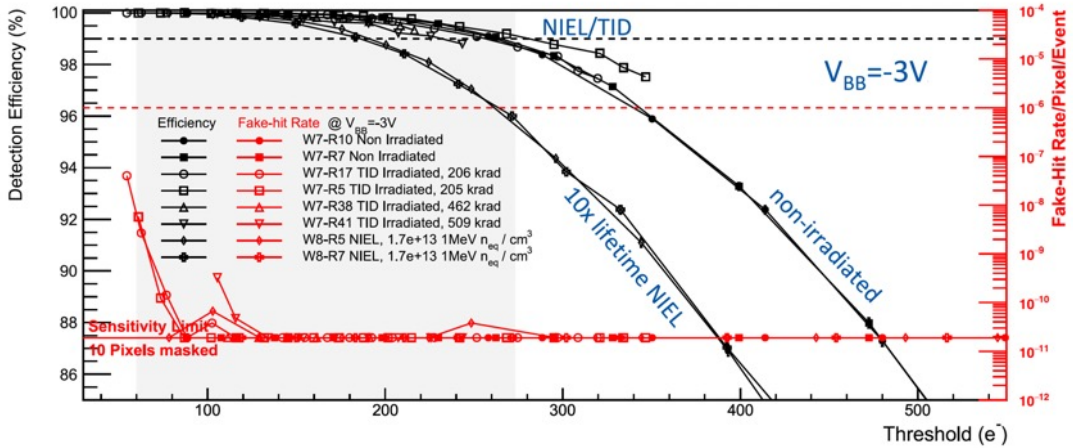


ALPIDE Key Features

- In-pixel: Amplification, Discrimination, multi event buffer
- In-matrix zero suppression: priority encoding
- Ultra-low power < 40mW/cm^2 (< 140mW full chip)
- Detection efficiency > 99%

- Spatial resolution ~5µm
- Low fake-hit rate: << 10^{-6}/pixel/event (10^{-8}/pixel/event measured during commissioning)
- Radiation tolerance: >270 krad (TID), > 1.7 10^{13} 1MeV/n_{eq} (NIEL)

Same chip used in ALICE2 for ITS and Muon Forward Tracker (MFT)



ALPIDE detection efficiency and fake hit rate

ALPIDE and other developments

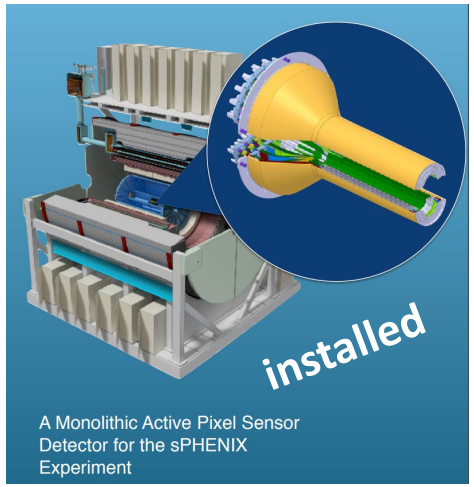
With permission. Article online

Adopted or considered for other experiments: **HADES, CBM, PANDA, NUSTAR, NA61, CSES2-Limadou, iMPACT, COMPASS++/AMBER, pCT, ePIC…**

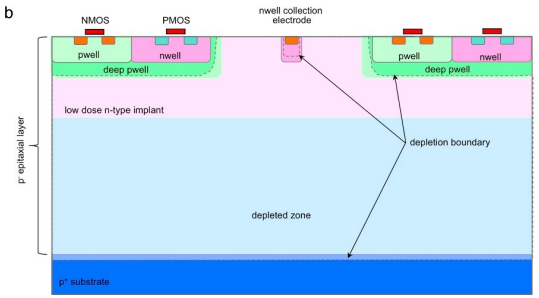
ALPIDE: Tower Semiconductor 180nm CMOS Imaging Sensor (CIS) Process

- R&D effort within the ALICE collaboration
  - excellent collaboration with foundry
  - more than 70k chips produced and tested
  - ALICE ITS pioneers large area trackers built of MAPS (EIC, ALICE 3, FCC?)

- in parallel studies to optimise process to reach full depletion and improve time response and radiation hardness up to 10^{15} 1MeV/n_{eq} :
  - **More details:** NIM **A871** (2017) https://doi.org/10.1016/j.nima.2017.07.046
  - **Now being further pursued: MALTA, CLICpix, FastPix, …**



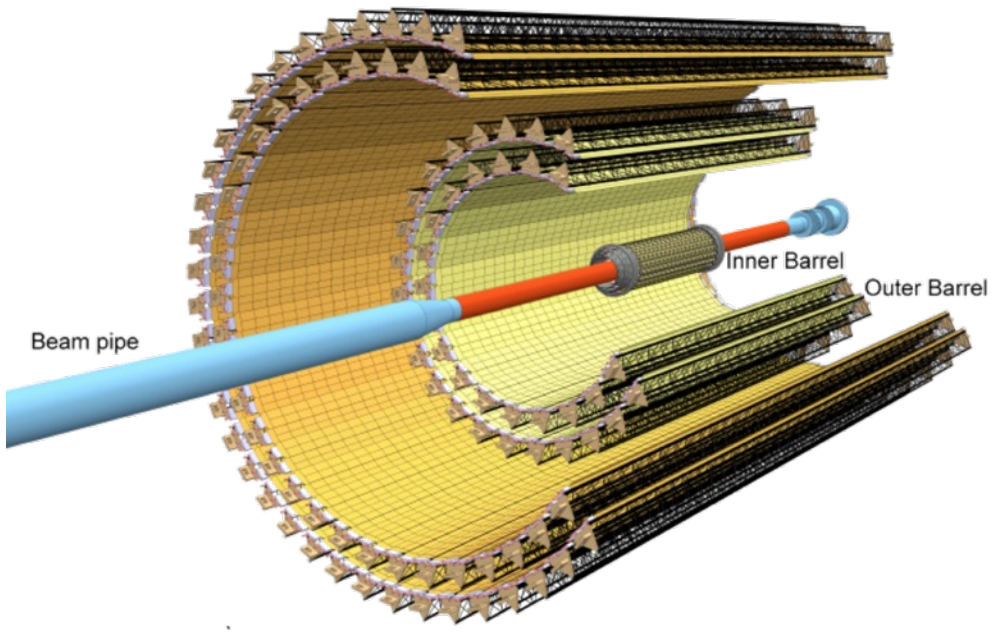
Detector replicas for new experiments **sPHENIX MVTX @RHIC**

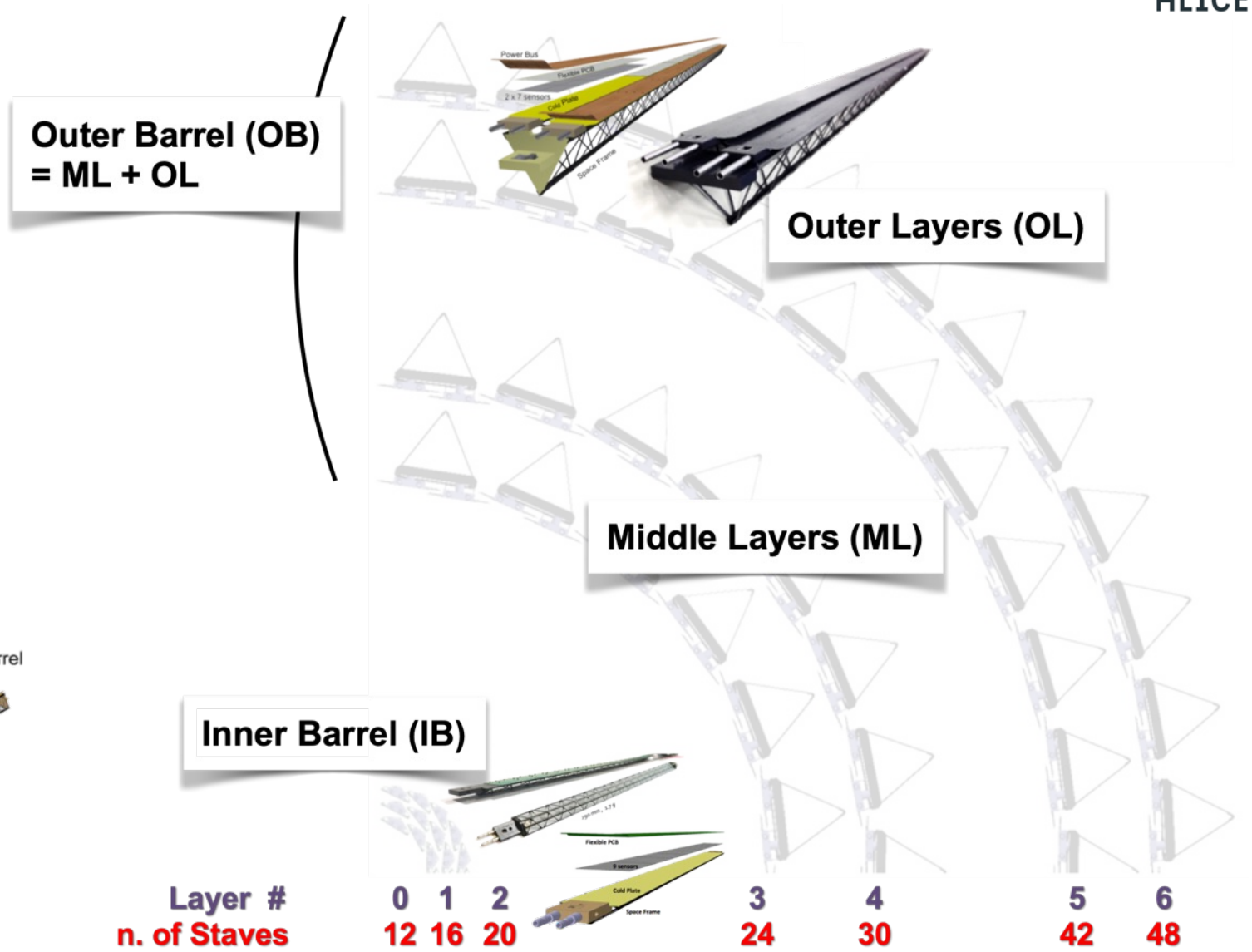


Modified process

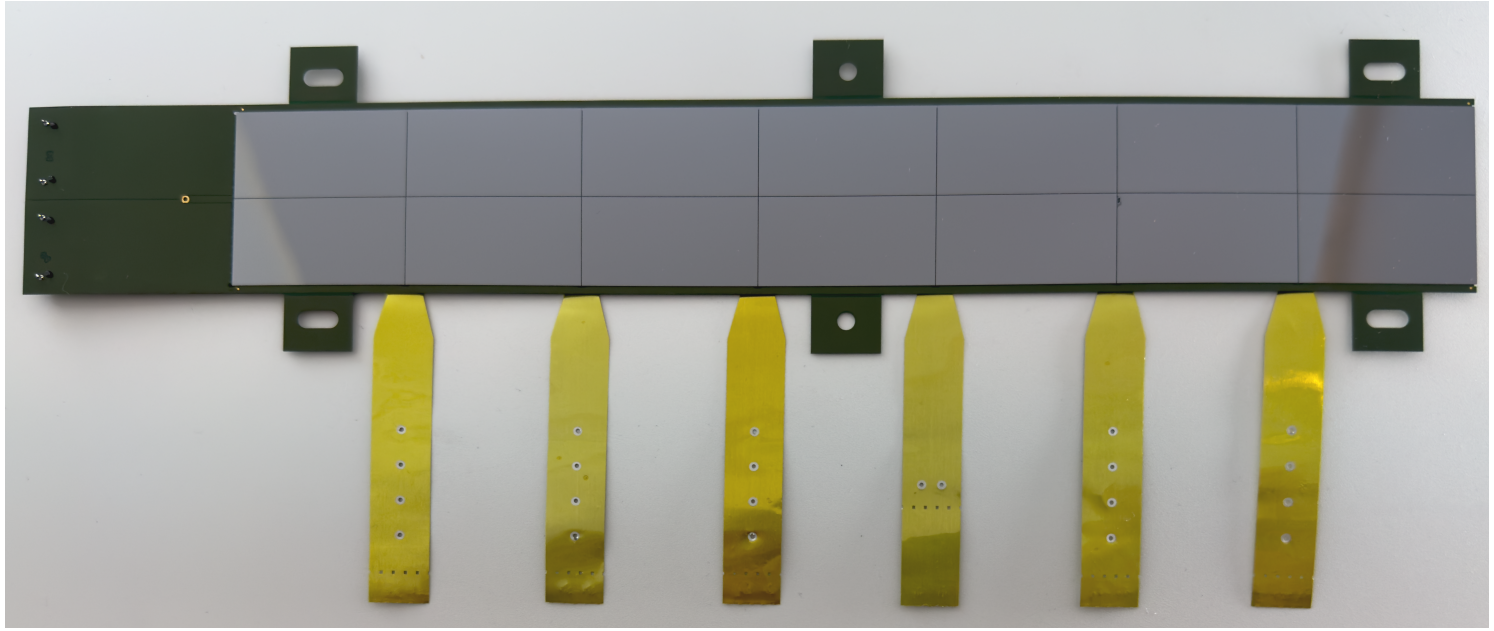
The largest MAPS pixel detector (so far)

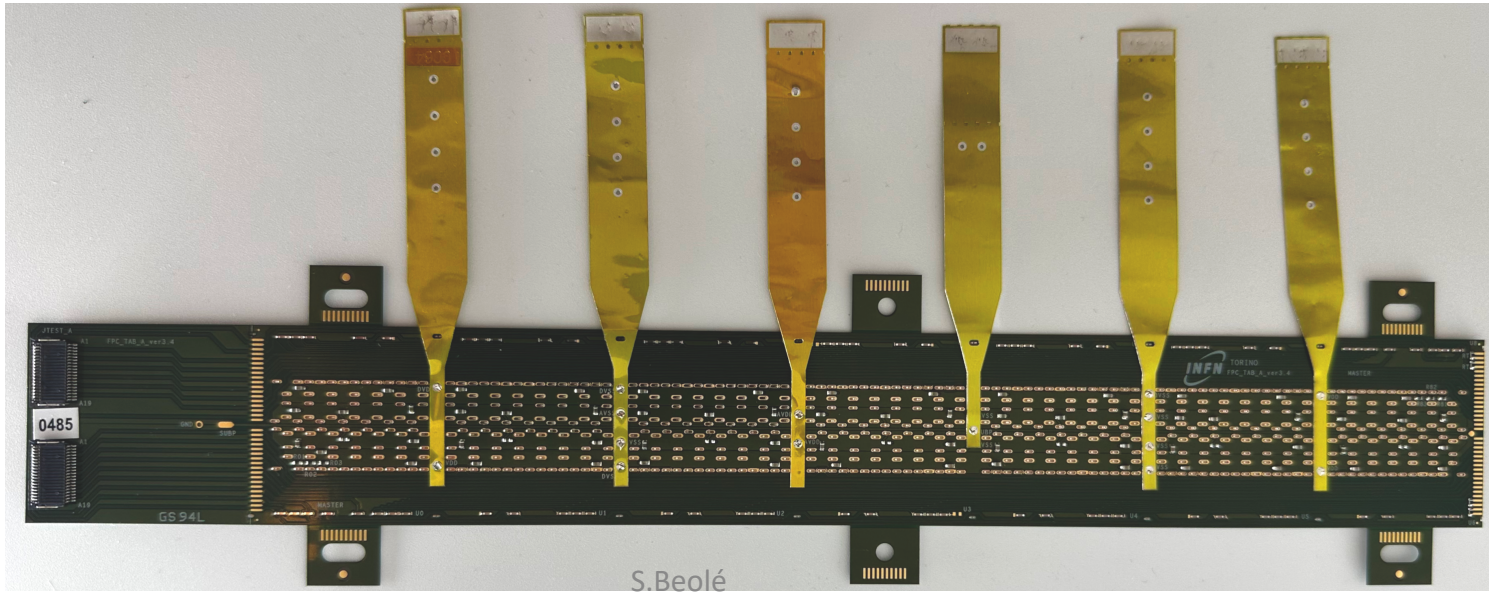
- 7 Layers (3 inner / 2 middle / 2 outer) from R = 22 mm to R = 400 mm
- 192 Staves (48 IL / 54 ML / 90 OL)
- Ultra-lightweight support structure and cooling
- 10 m^2 active silicon area, 12.5 x 10^9 pixels



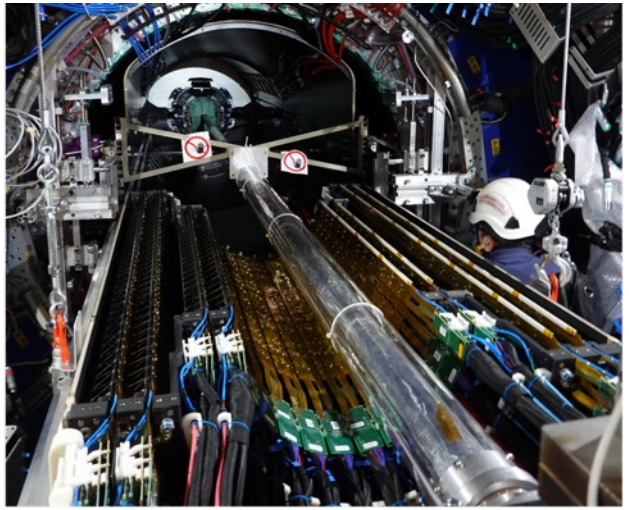


Tiling up

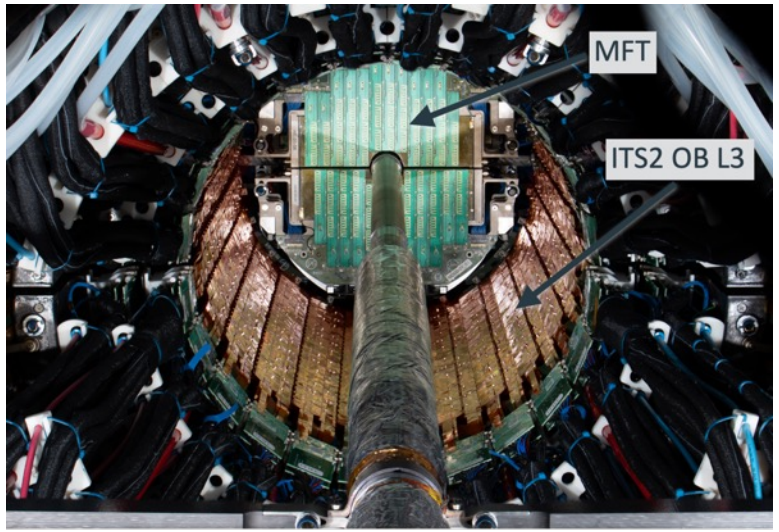




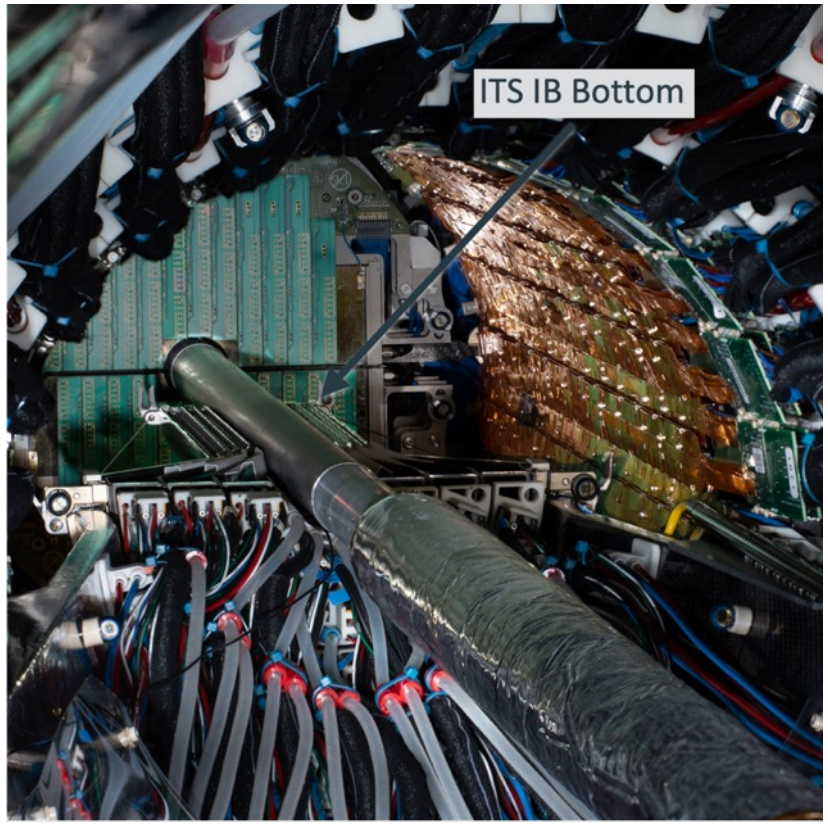
ITS installation



Outer Barrel Bottom being inserted on the rails inside the TPC



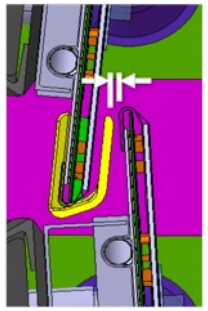
ITS Outer Barrel surrounding the beam pipe, MFT in the back



ITS Inner Barrel Bottom and Outer Barrel

- Installation challenges
  - Precise positioning around the beam pipe (nominal clearance ~ 2 mm)
  - Manipulating from 4 m distance
  - Difficult to see actual position by eye
  - precise mating of top and bottom barrel halves (clearance between adjacent staves ~ 1.2 mm)
- Dry-installation tests on the surface to test and exercise procedures
- Use of 3D scans, surveys and cameras

1.2 mm nominal clearance



OB stave edge clearance when fully mated

Calibration

The Challenge:

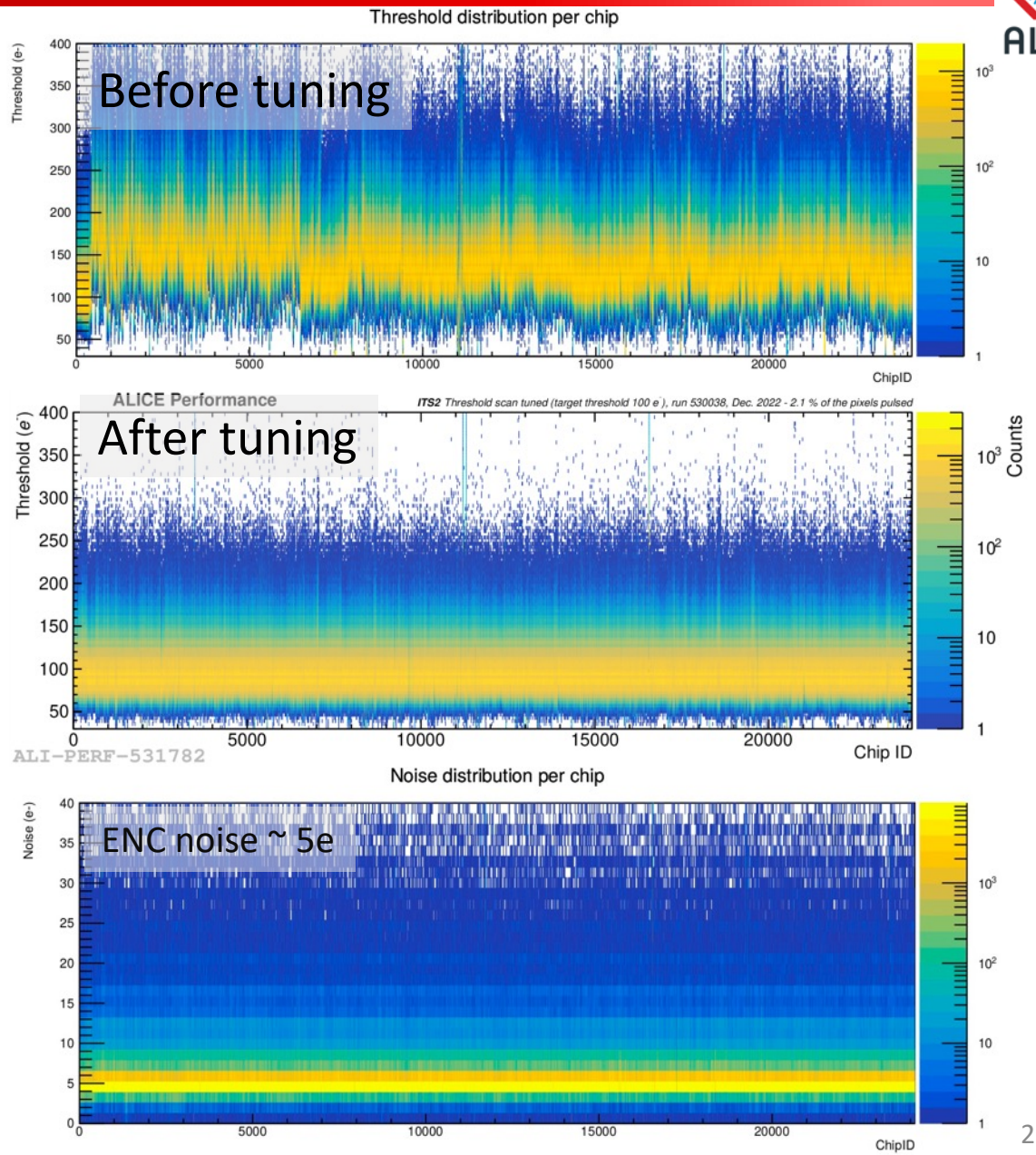
- Online calibration of 12.5 billion channels
- Threshold scan of full detector: > 50 TB of event data
- Several scans to be run sequentially
  - Threshold tuning (adjust thresholds to target)
  - Threshold scan (measure actual thresholds)

Procedure:

- DCS performs actual scans: configure and trigger test injections
- Scan runs in parallel but independently on all staves
- Distributed analysis on event processing nodes
- full procedure takes **less than 30 minutes**

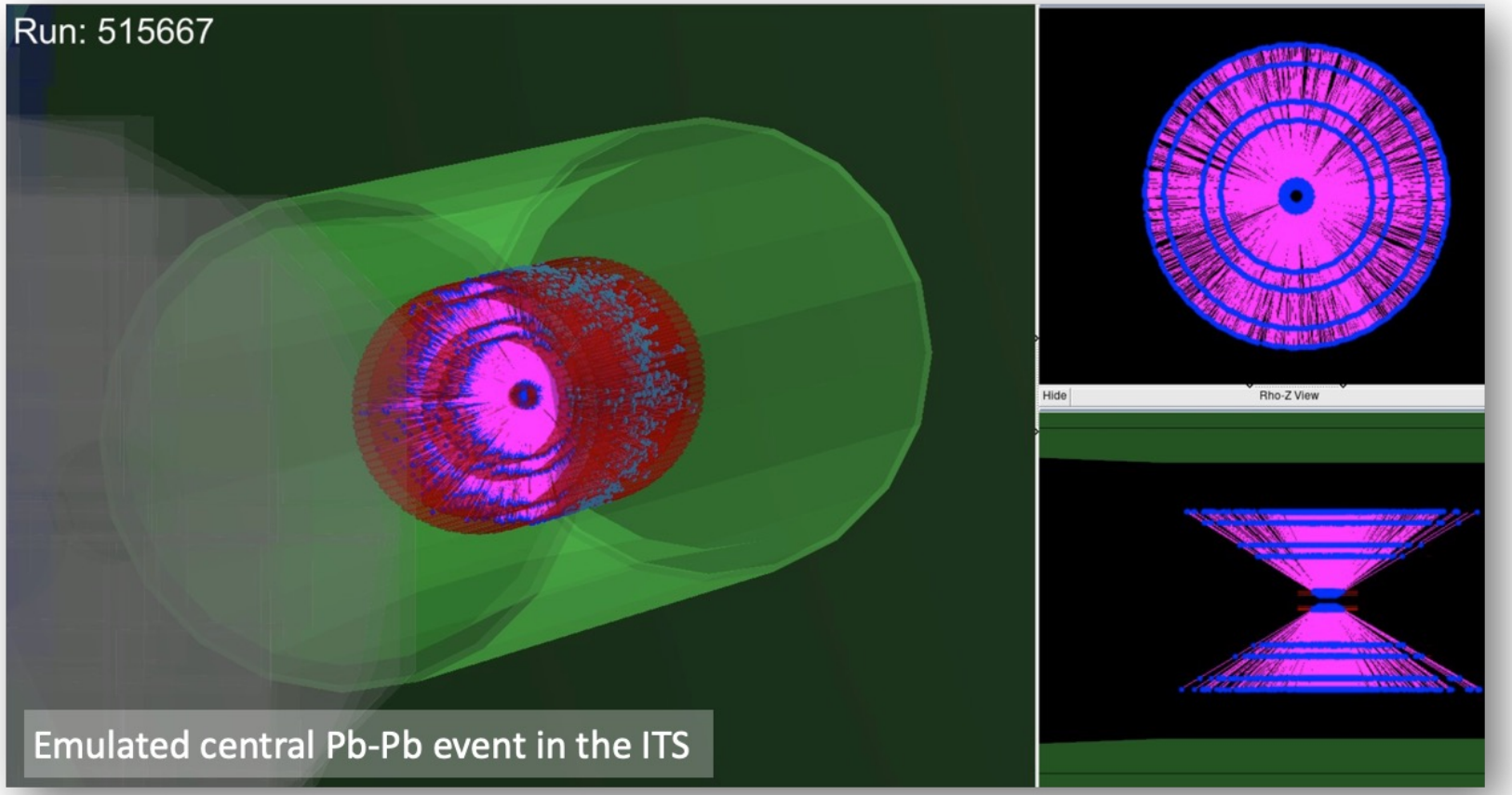
Results:

- Scan with online analysis successfully run on full detector
- before tuning: settings used in surface commissioning, detector already fully efficient
- After tuning: Thresholds very stable on all the chips: RMS of threshold distribution compatible with what we had during production
- ENC noise ~ 5e$^-$



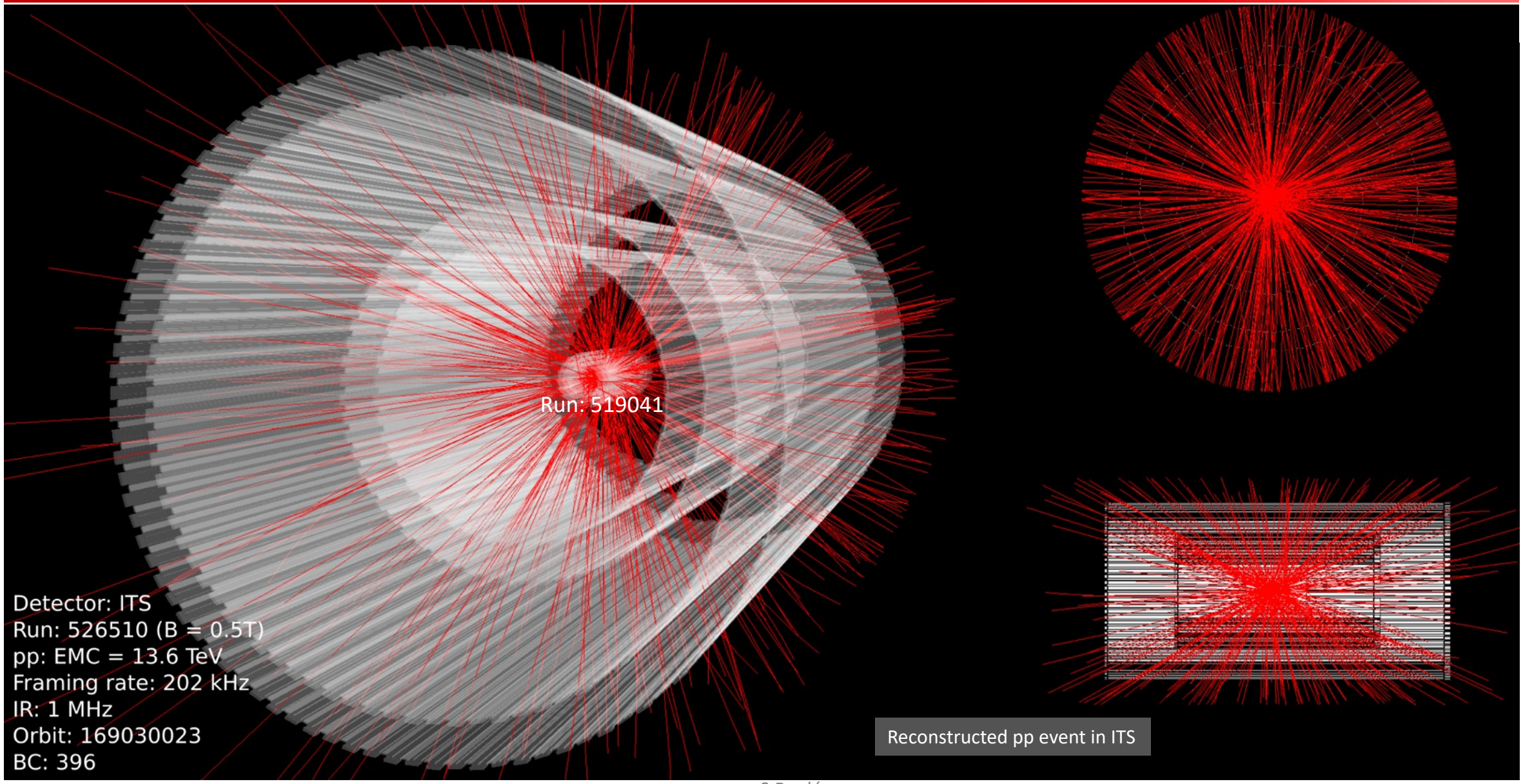
Data Taking Preparation

- Last part of commissioning phase devoted to prepare and test settings optimized for pp with 200 kHz framing rate (instead of 45 kHz for Pb-Pb) to achieve better time resolution reducing pile-up
  - successfully tested tested in pp Pilot Beam (2022)
- **Extensive test runs with emulated Pb-Pb and pp events (injected into the detector front-end) to test detector, processing chain under realistic load**

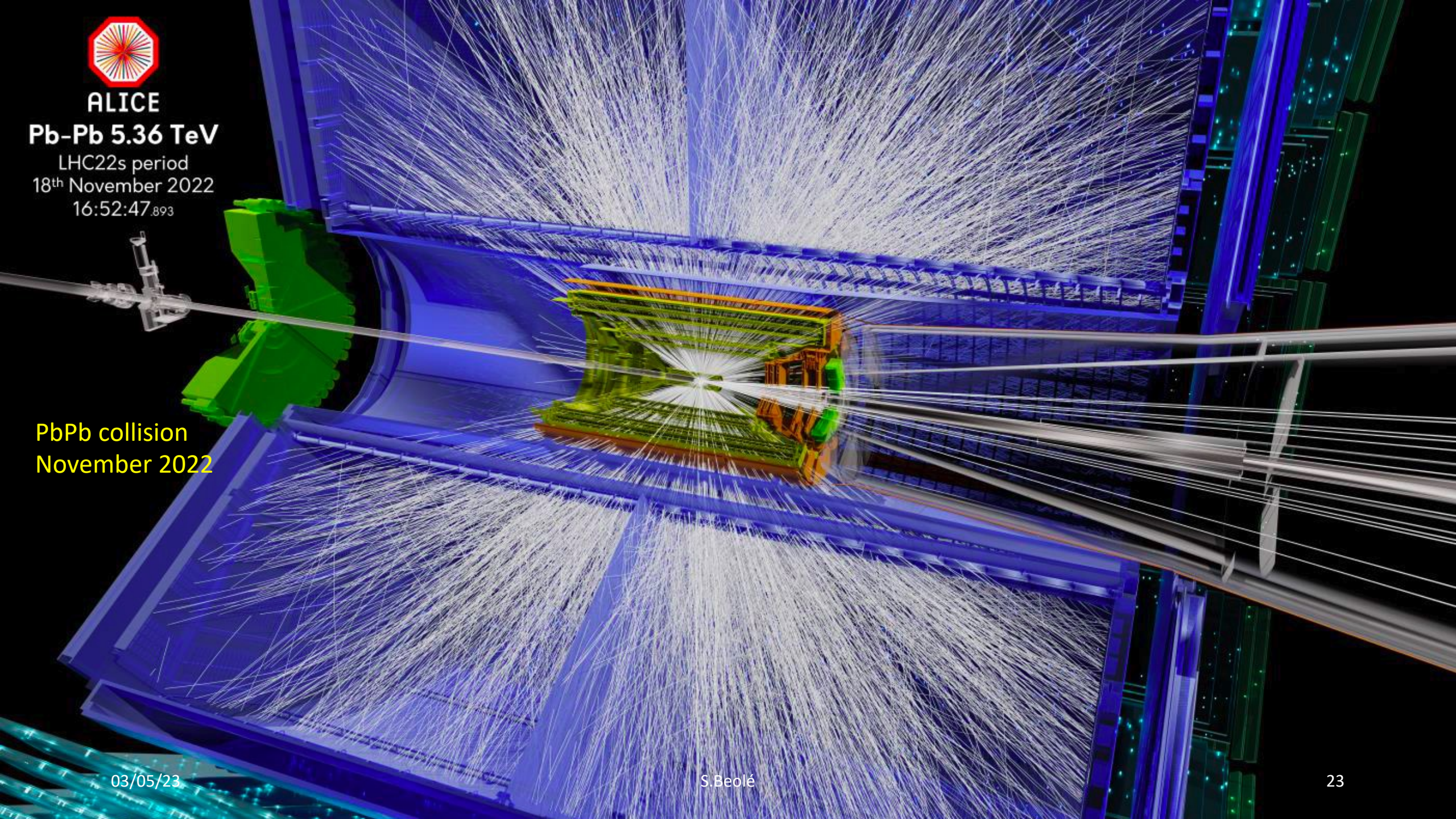


Emulated central Pb-Pb event in the ITS

RUN 3 readiness



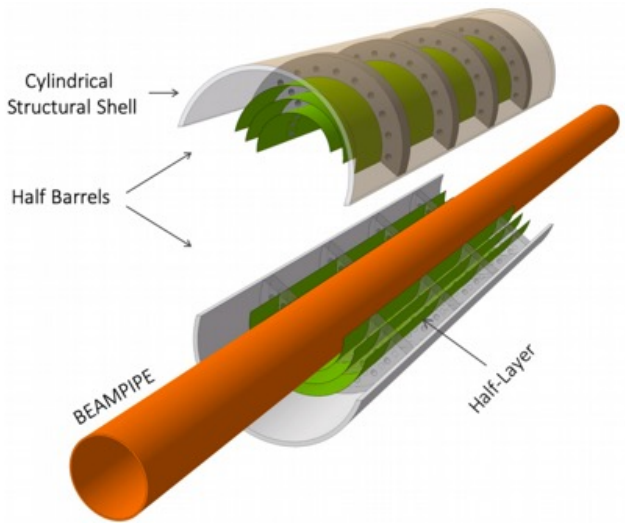
Reconstructed pp event in ITS

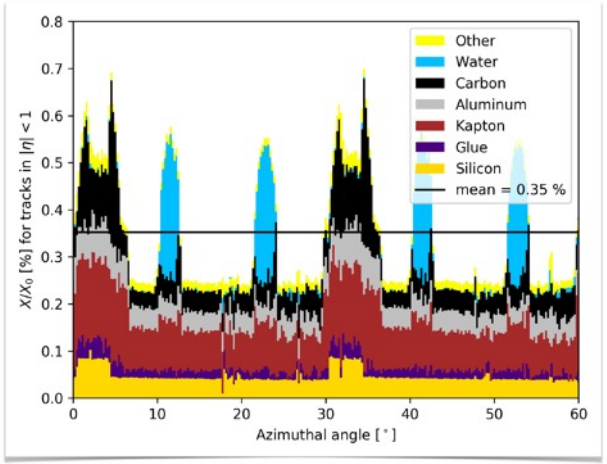


PbPb collision
November 2022

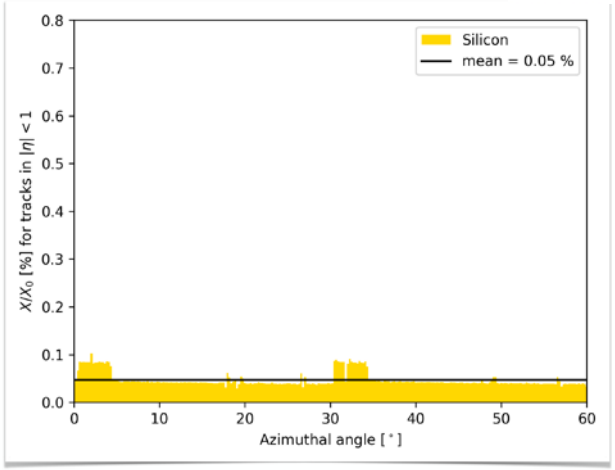
Can we improve further?

ALICE 2.1: ITS3 the “all silicon” detector





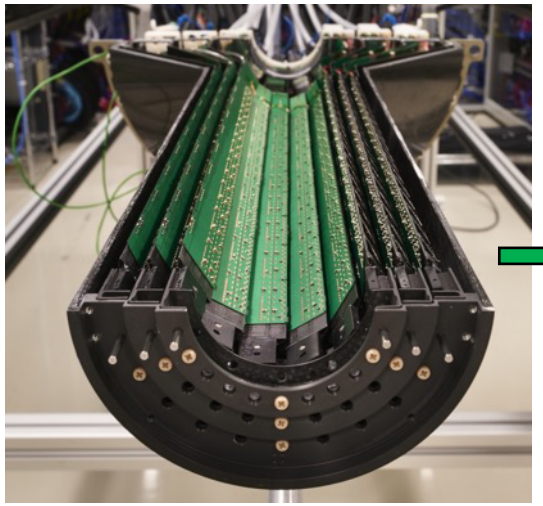
ITS2 Layer 0: X/X0=0.35%



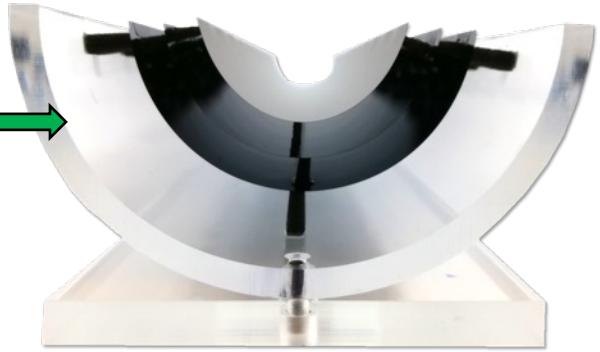
ITS3 only silicon: X/X0=0.05%

- GOAL for ALICE ITS3:
  - improve determination of primary and secondary vertices at high rate
  - go closer to interaction point
  - reduce material budget X/X_0 0.35%→0.05%
- “SILICON ONLY” TRACKER?
  - exploit stitching → large area sensors
  - thin and bend → sigle sensor half layers
- TECHNOLOGY CHOICE:
  - 65 nm TPSCo (Tower & Partners Semiconductor): 300mm wafers and stitching available
  - 65 nm → lower power consumption
  - 7 metal layers

ITS2 Inner Barrel



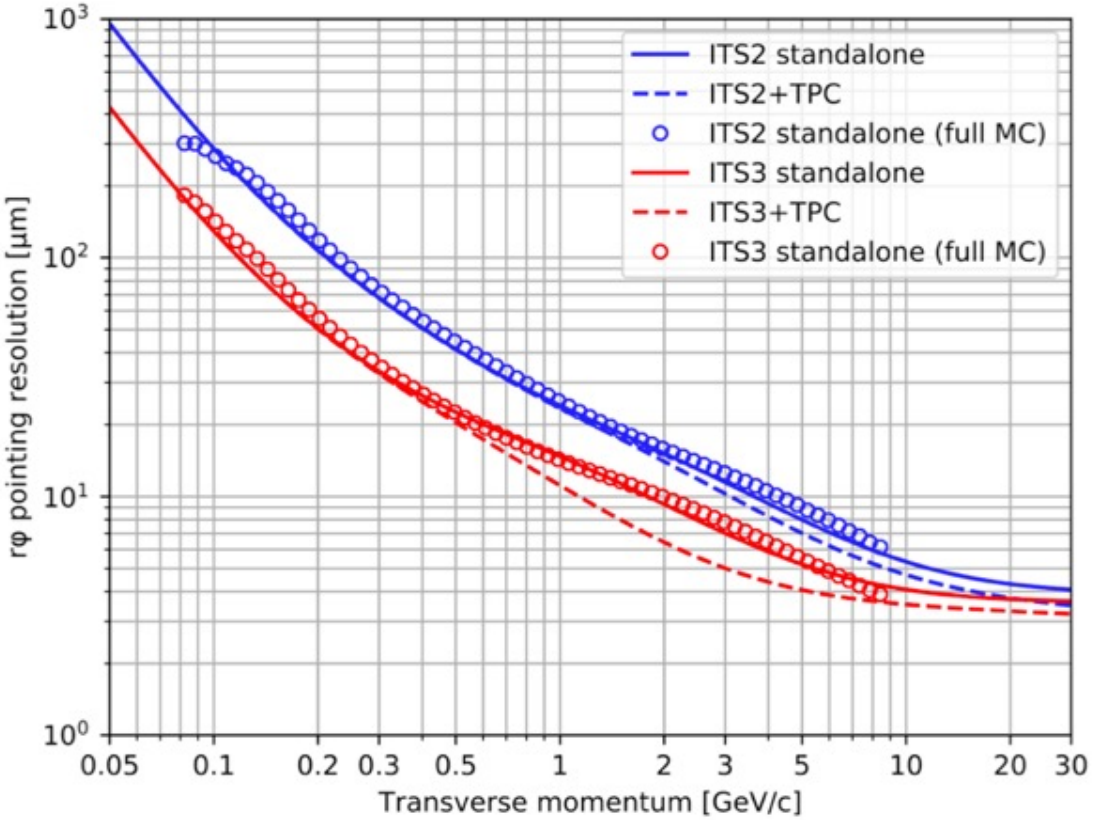
ITS3 mechanical mockup



Letter of Intent for an ALICE ITS Upgrade in LS3 https://cds.cern.ch/record/2703140

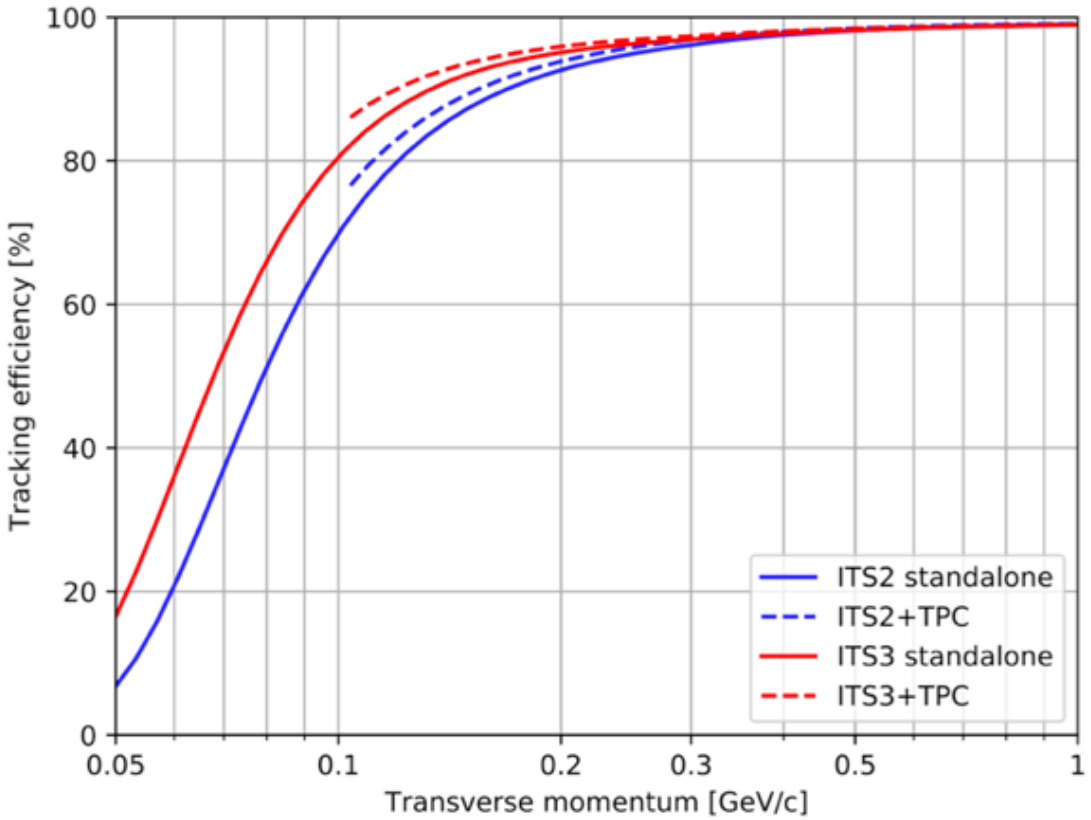
ITS3 expected performance

pointing resolution



Improvement of a factor 2 over all momenta

tracking efficiency

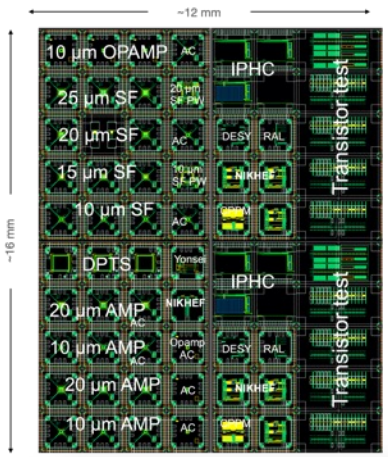


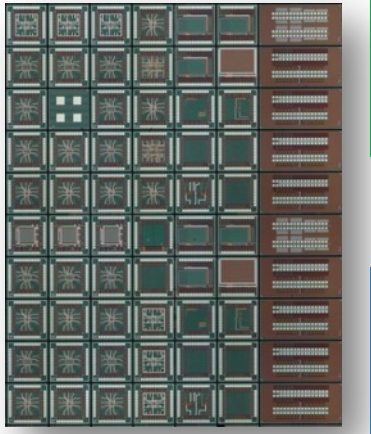
Large Improvement for low transverse momenta

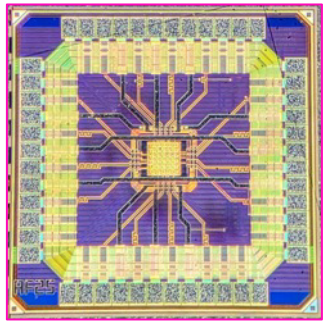
Validation of 65nm technology

Ongoing R&D: technology validation

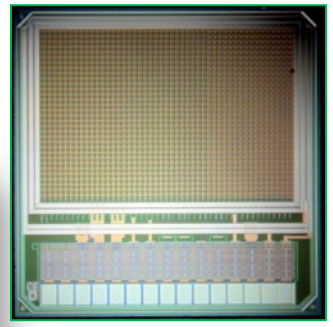
- First test submission (MLR1) for 65nm in December 2020
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- Each reticle (12×16 mm^2):
  - 10 transistor test structures (3×1.5 mm^2)
  - 60 chips (1.5×1.5 mm^2)
    - Analogue blocks
    - Digital blocks
    - **Pixel prototype chips: APTS, CE65, DPTS**
- Testing since September 2021:
  - huge effort shared among many institutes
  - laboratory tests with ^{55}Fe source
  - beam tests @ PS, SPS, Desy, MAMI



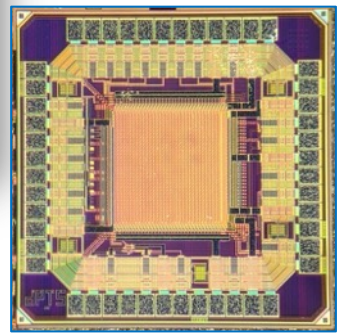




APTS:
- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  1. Traditional source follower (APTS-SF)
  2. Very fast OpAmp (APTS-OA)
- 4 pitches: 10, 15, 20, 25 µm



CE65:
- 2 matrix sizes, 15 or 25 µm pitch
- Rolling shutter readout (50 µs integration time)
- 3 in-pixel architectures:
  1. AC-coupled amplifier
  2. DC-coupled amplifier
  3. Source follower



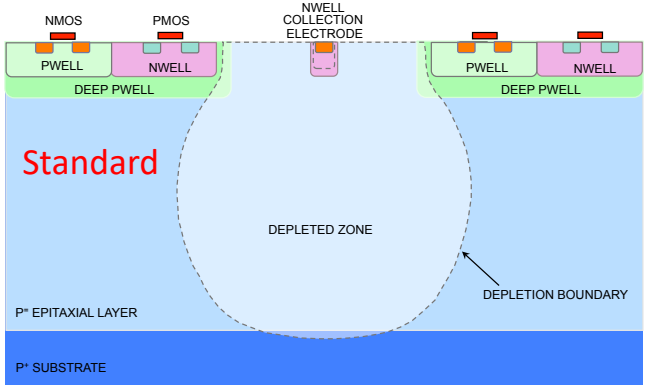
DPTS:
- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 µm^2

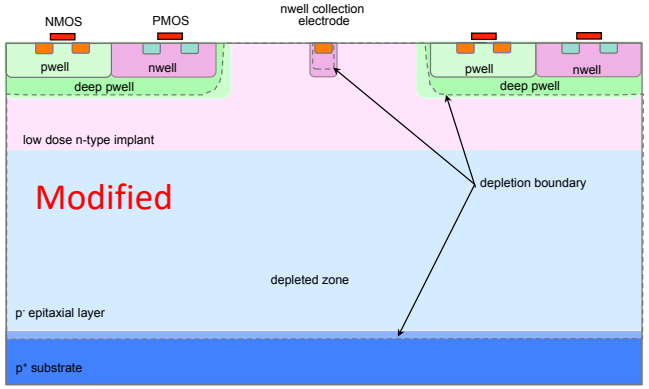
AREA: 1.5×1.5 mm^2

Optimization of the sensor

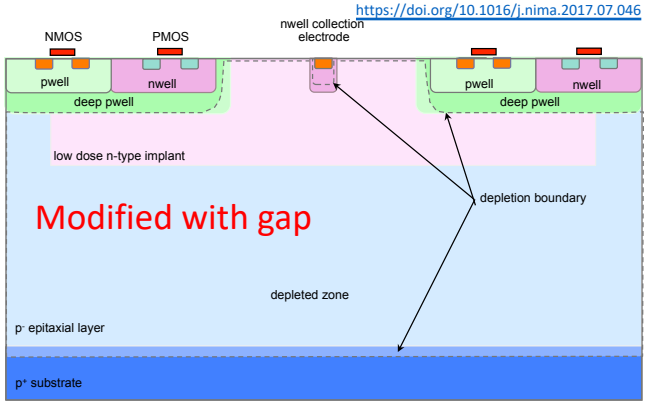
- GOAL: create planar junction using deep **low dose n-type implant** and **deplete the epitaxial layer**: same approach as 180nm
- Additional deep p-type implant or **gap in the low dose n-type implant improves lateral field near the pixel** boundary and accelerates the signal charge to the collection electrode.

- Process optimization (4 splits):
  - Add and adjust the low-dose deep n-well implant in the pixel to obtain easier depletion
  - Adjust the deep p-well implant
    - improve the isolation between the circuit and the sensor,
    - prevent punch through between deep n-type implant and circuitry
    - prevent local potential wells retaining the signal charge





https://doi.org/10.1016/j.nima.2017.07.046



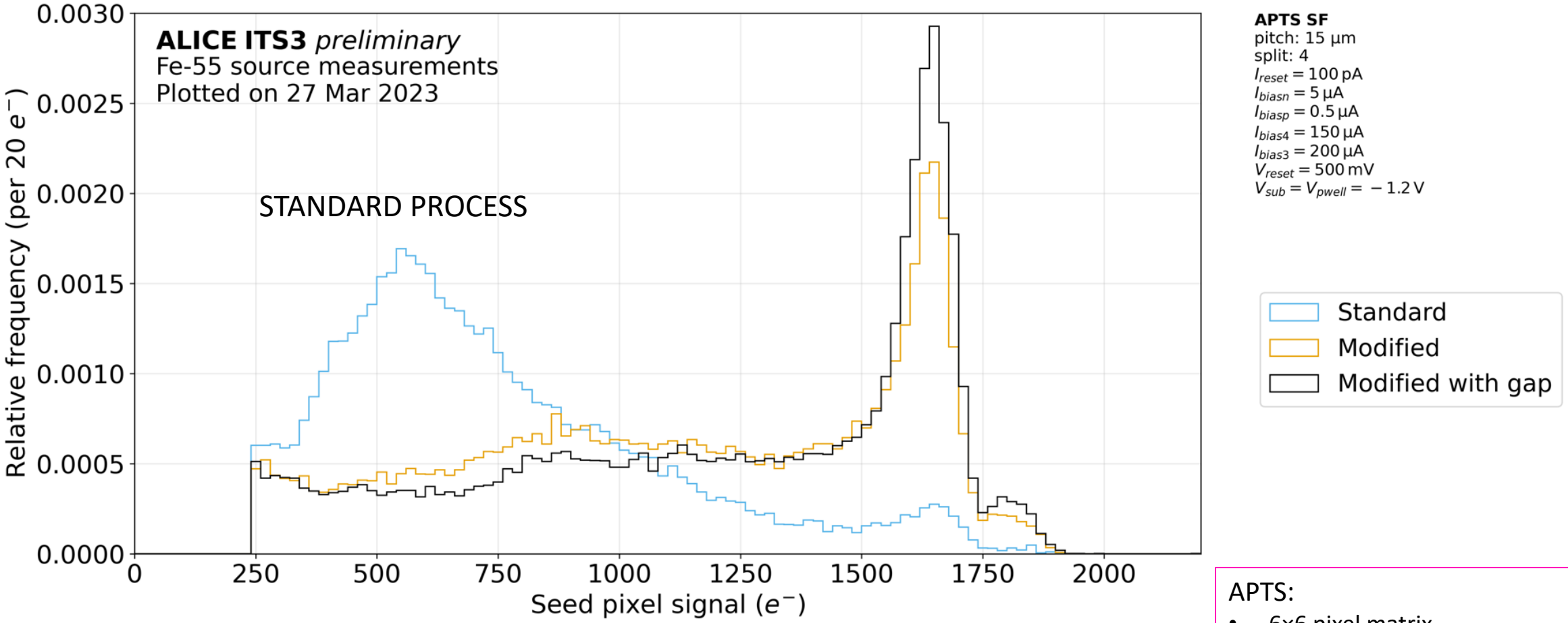
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

3 main pixel designs implemented in all 4 process splits

https://doi.org/10.22323/1.420.0083

Preliminary results for APTS: charge collection

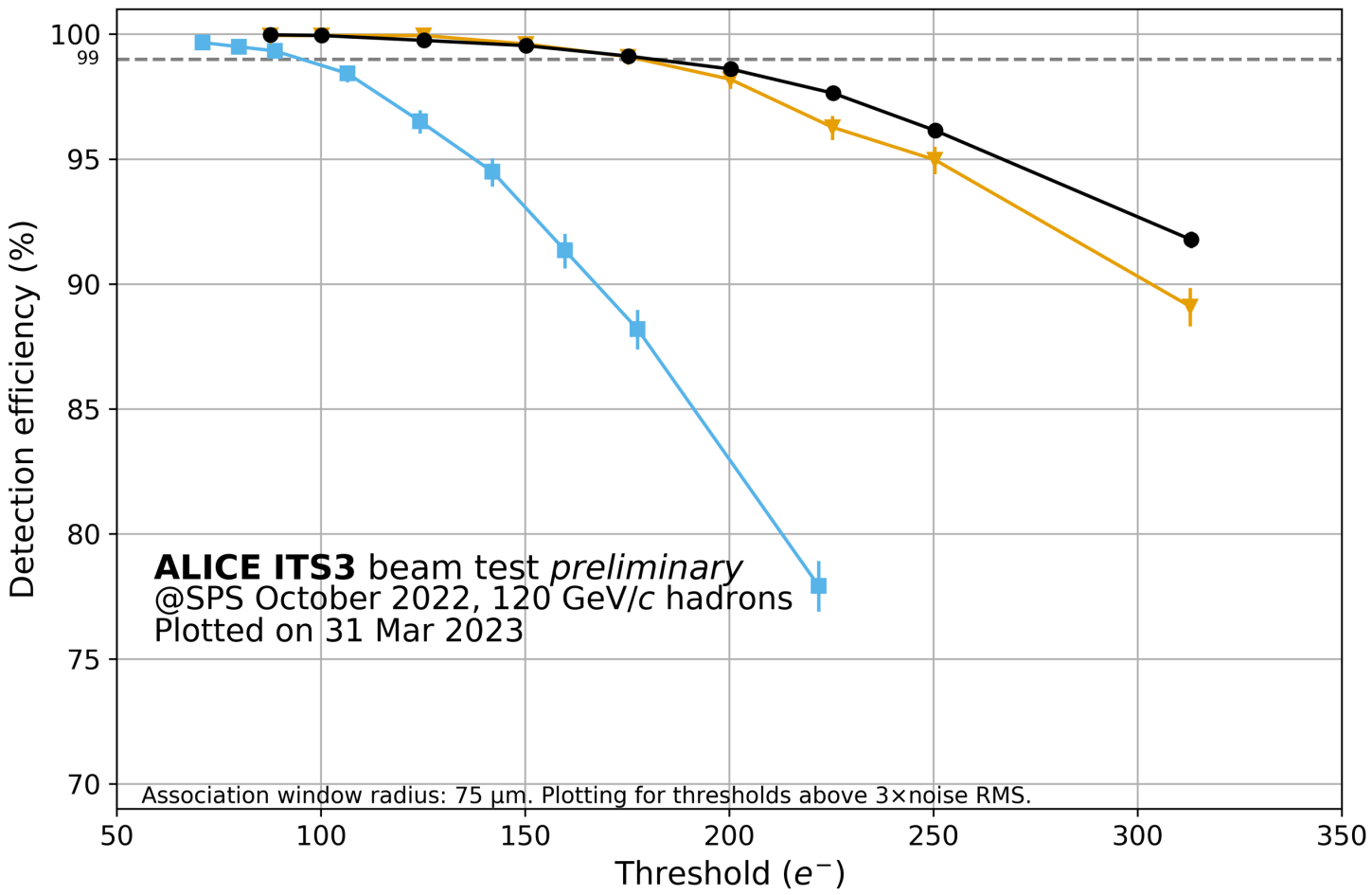
MODIFIED PROCESS: fully depleted epi layer



APTS:

- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  1. Traditional source follower (APTS-SF)

Preliminary results for APTS: detection efficiency

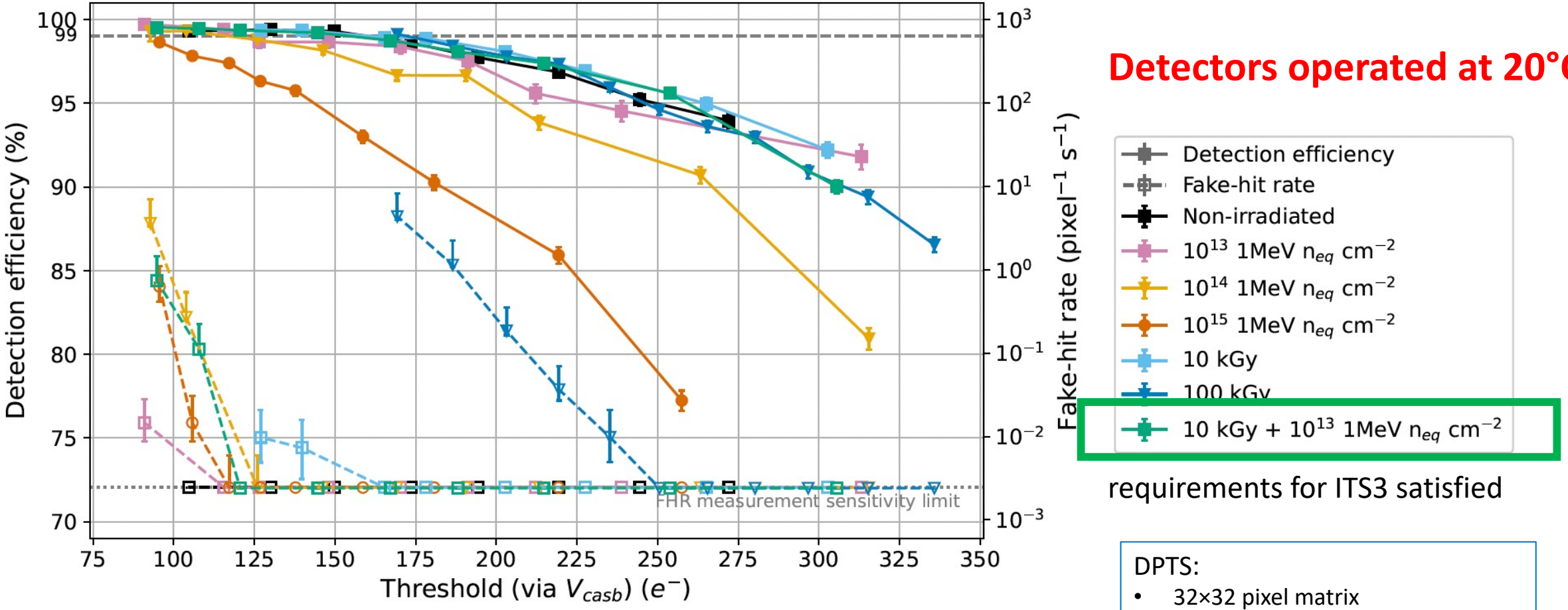


APTS SF
Non-irradiated
pitch: 15 µm
split: 4
$I_{reset} = 100$ pA
$I_{biasn} = 5$ µA
$I_{biasp} = 0.5$ µA
$I_{bias4} = 150$ µA
$I_{bias3} = 200$ µA
$V_{reset} = 500$ mV
$V_{pwell} = V_{sub}$=-1.2 V
T = 20 °C

Standard
Modified
Modified with gap

APTS:
- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  1. Traditional source follower (APTS-SF)

DPTS: radiation hardness



Detectors operated at 20°C

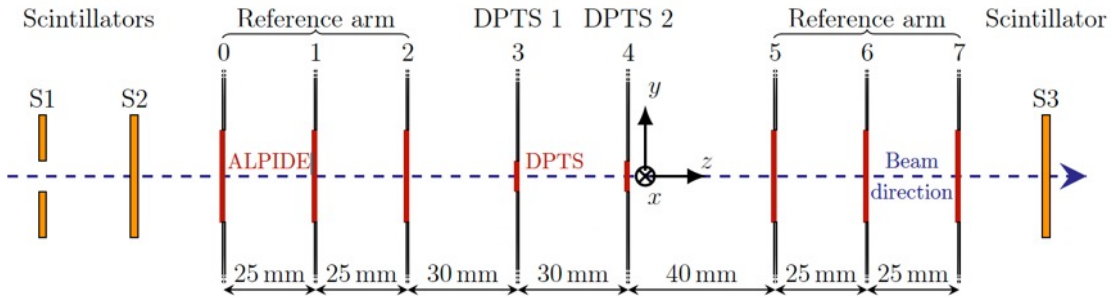
requirements for ITS3 satisfied

DPTS:
- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 µm²

Detection efficiency and FHR for different irradiation levels

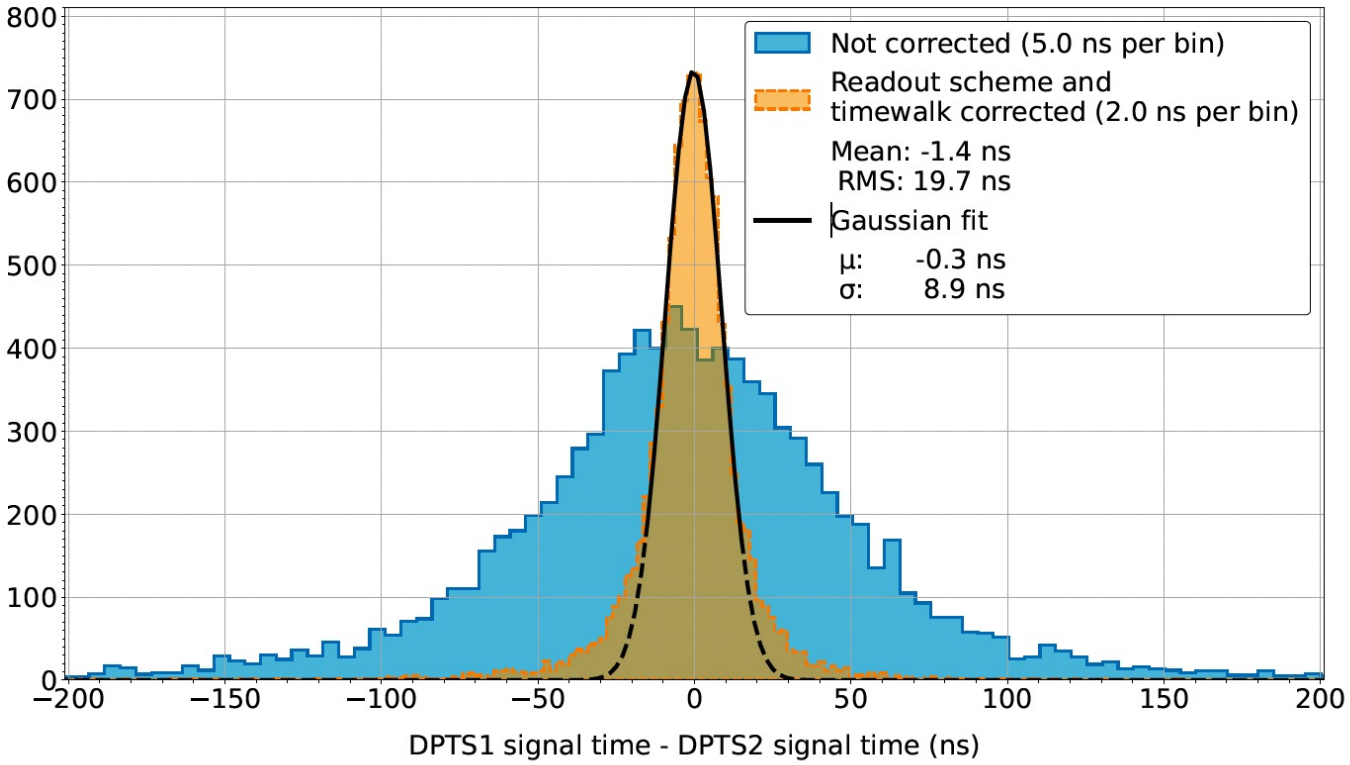
Gianluca Aglieri Rinella et al. arXiv:2212.08621v2

DPTS Timing resolution



Sketch of the beam test telescope

- Two DPTS are sandwiched between reference planes made of ALPIDE chips.
- Two scintillators (S2 and S3), operated in coincidence, and one featuring a 1mm hole (S1), operated in anti-coincidence, are used for triggering.
- The trigger can also be provided by one of the two DPTS
- Beam: 5.4 GeV/c electrons



- Time residuals distributions of two DPTSs with no corrections (blue) and with readout scheme and time walk corrections applied (orange)
- FE parameters not optimised for timing performance(I_{bias}=10nA)

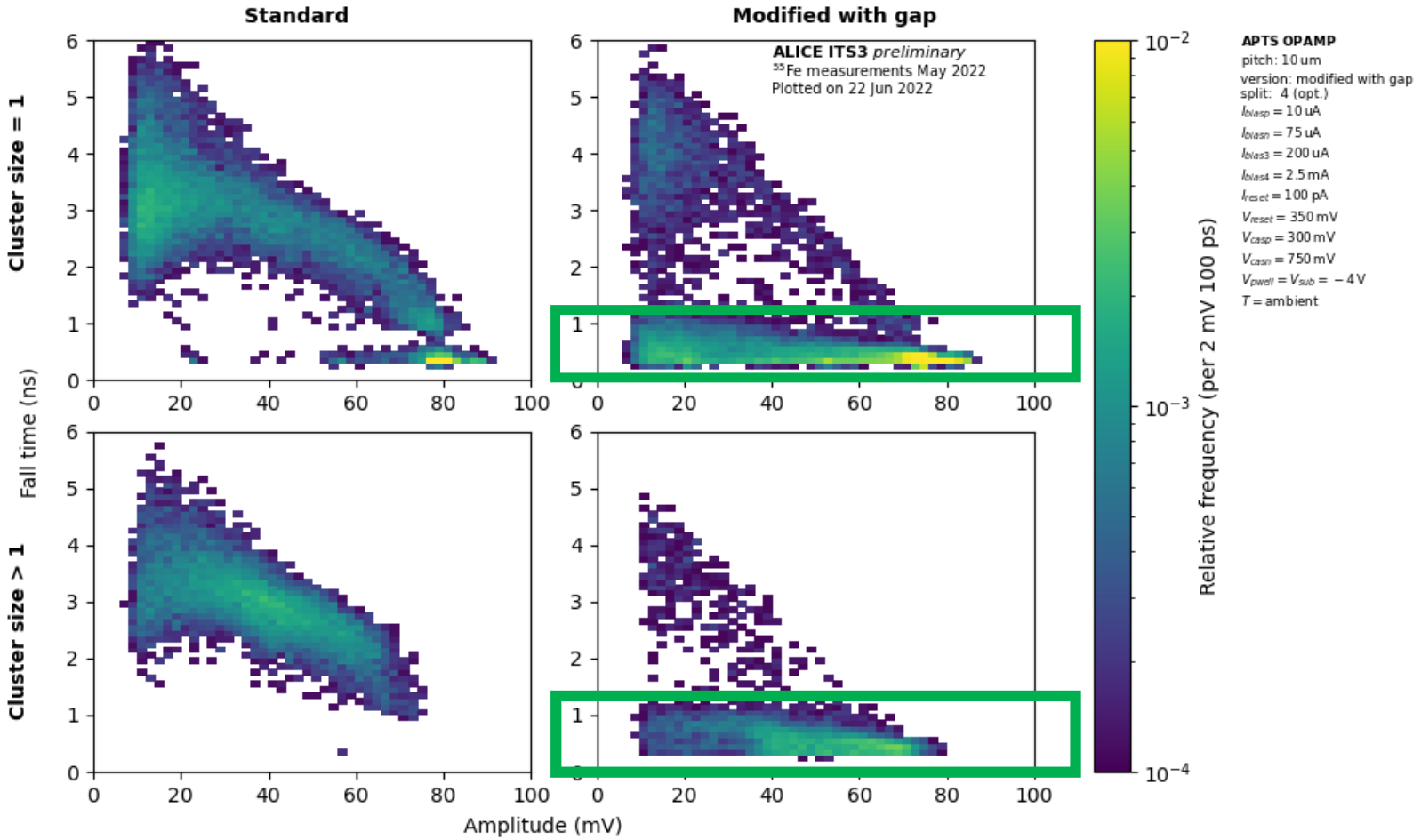
Gianluca Aglieri Rinella et al. arXiv:2212.08621v2

Preliminary results for APTS OpAmp: timing response

- Analog output test structure with OpAmp to start test the timing performance of the technology

- First results from June 2022 beam test available:
  - timing performance
  - efficiency

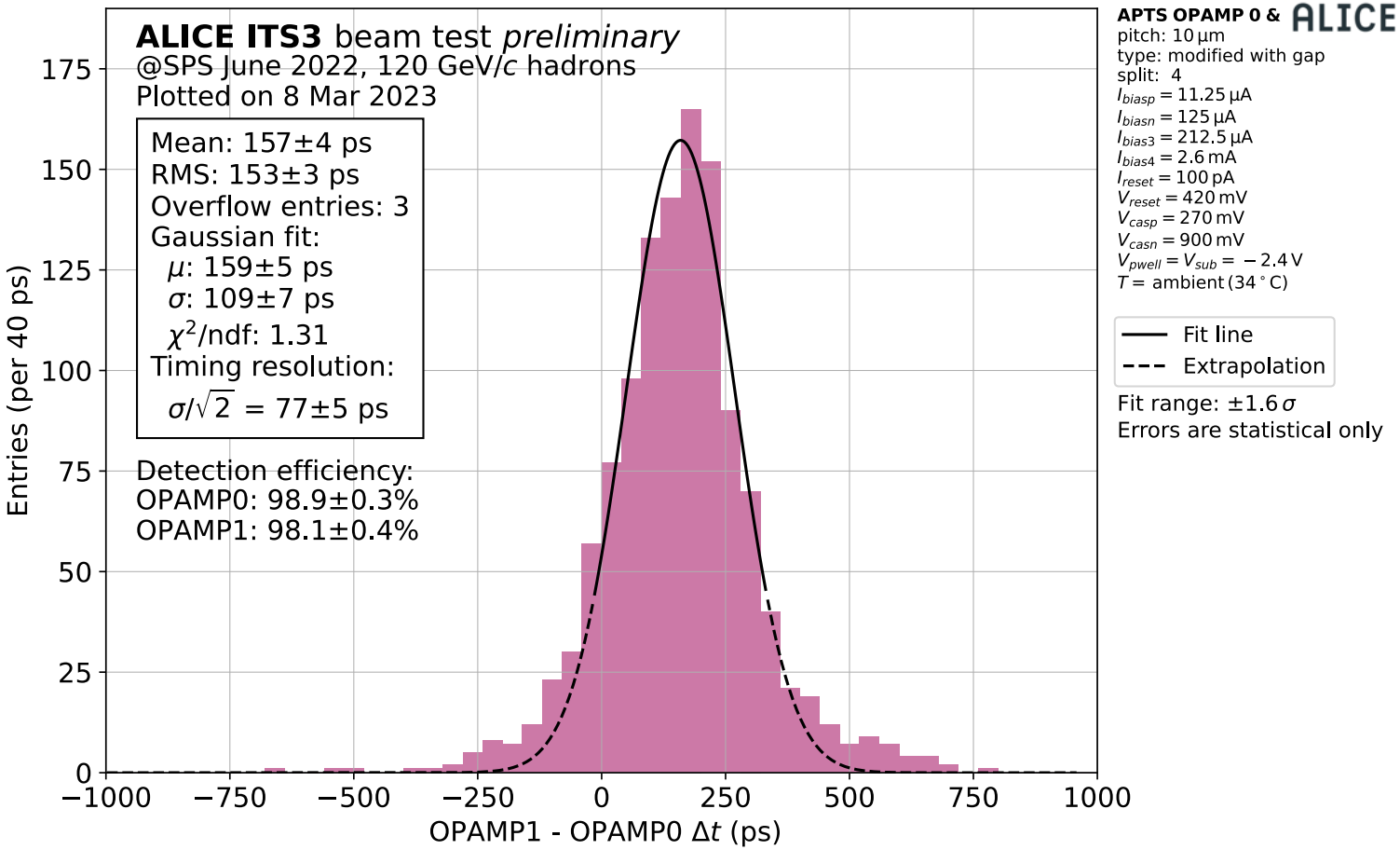
Modified process shows faster charge collection as expected



Preliminary results for APTS OpAmp: timing resolution

- Analog output test structure with OpAmp to start test the timing performance of the technology

- First results from June 2022 beam test available:
  - timing performance
  - efficiency



- **CFD Time stamp** $t = t_{10\%\mathrm{CFD}}$
- **Time difference** $\Delta t = t_{\mathrm{OPAMP1}} - t_{\mathrm{OPAMP0}}$ distribution is fitted with **Gaussian** function
  - Fitted with $\pm 1.5\sigma$ range (solid line)
- **Efficiency** on both OPAMP plane with **5.5 mV (150e)** threshold: **~99%**
- **Time resolution:** 77 ± 5 ps without time walk/jitter correction

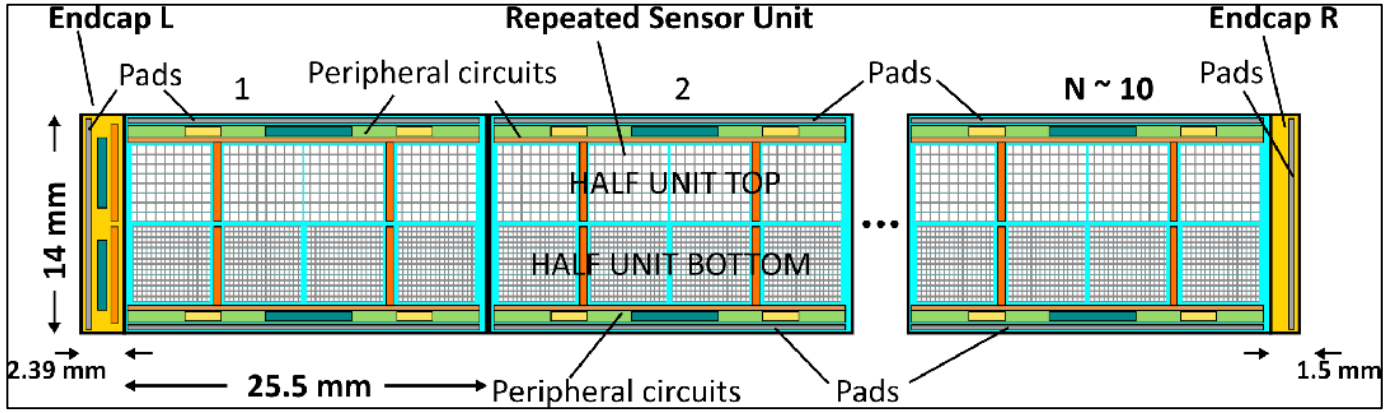
ER1: evaluation of stitching

Large area sensors exploit stitching: repeating identical but functionally independent units

- MOSS
  260×14 mm^2 6.72 Mpixels
- MOST
  260×2.5 mm^2 900 kPixels
- + multiple small chips for further technology exploration

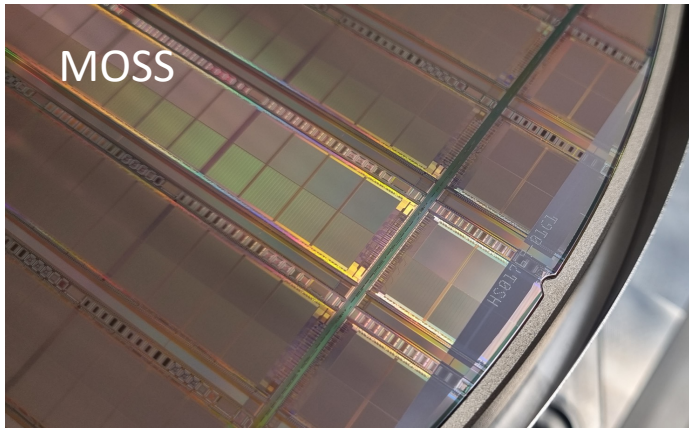
Status:

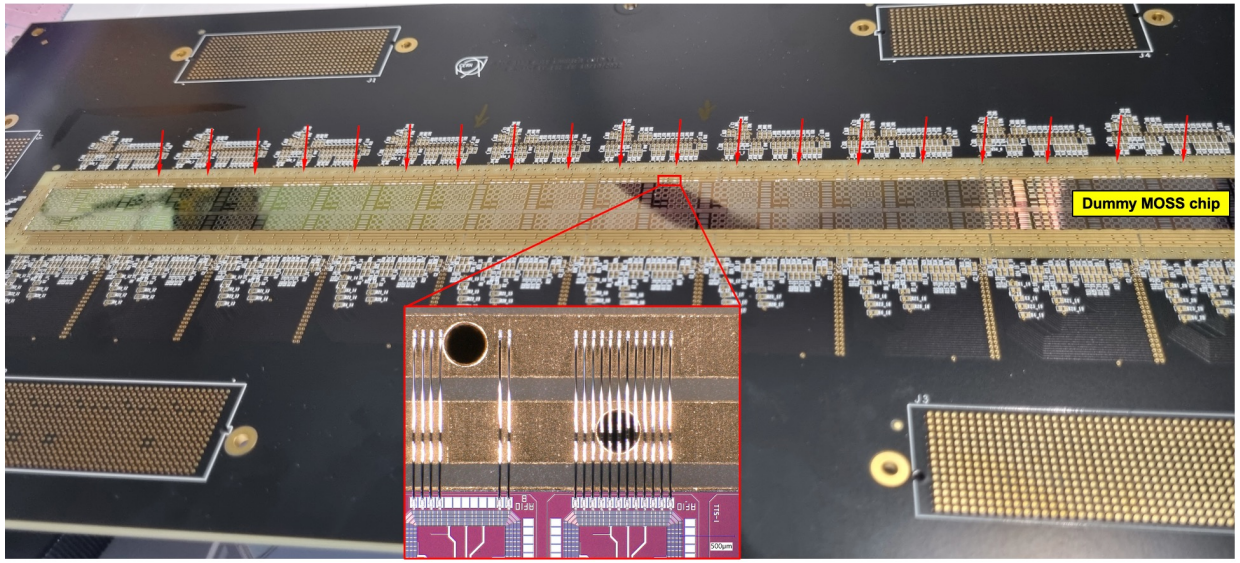
- Preparation for the first stitched sensors characterization: **Stitching yield measurement** to assess in-chip power distribution and data transfer over long distances
- First wafers delivered
- Next: thinning and dicing



MOSS layout

ER1 wafer



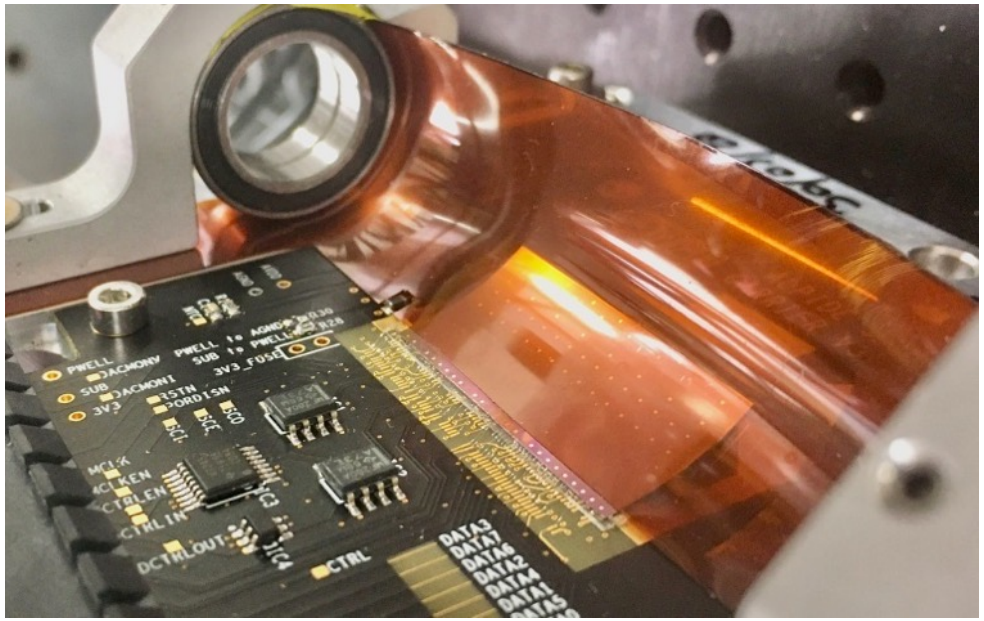


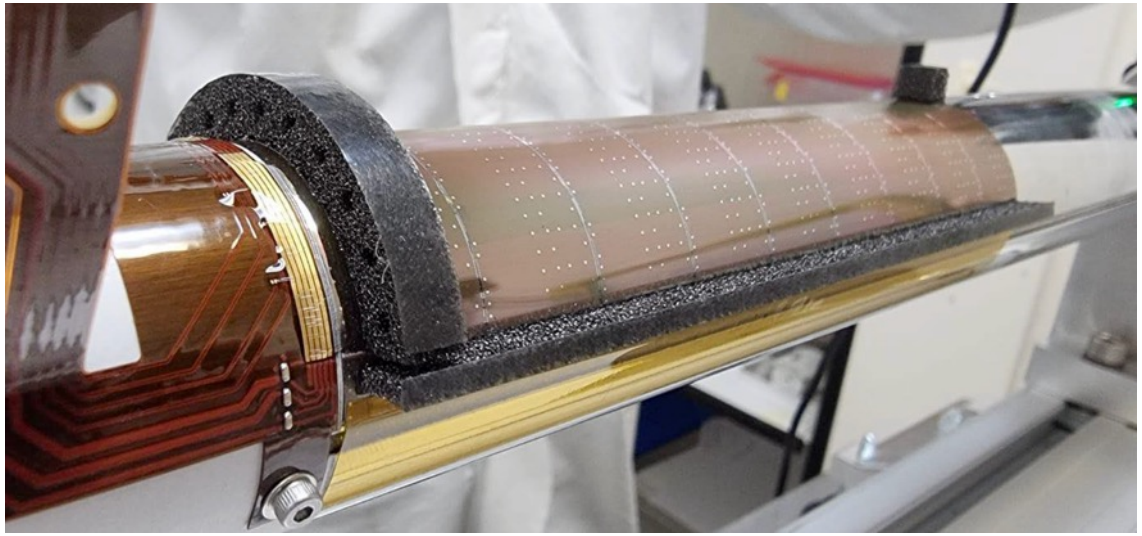
MOSS carrier card, bonding tests

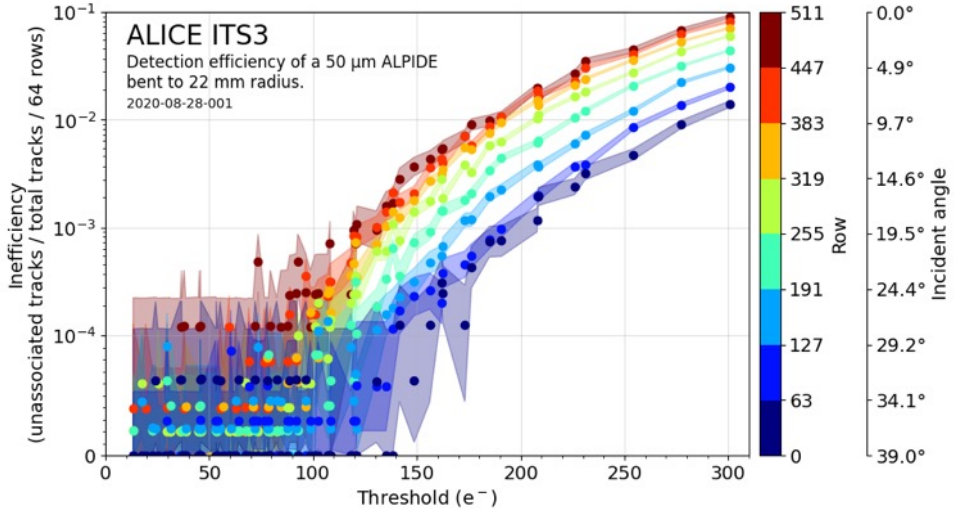
ONGOING R&D

Thinning and Bending of CMOS sensors: 180nm

- Bending of 180nm small size MAPS
  - 50 µm thick ITS2 chip (ALPIDE) bent to 22 mm showed excellent efficiency in the beam test in 2020
  - no significant variation in the performance
- Development of tools to bend large area silicon sensors: SuperALPIDE (9x2 ALPIDE die)



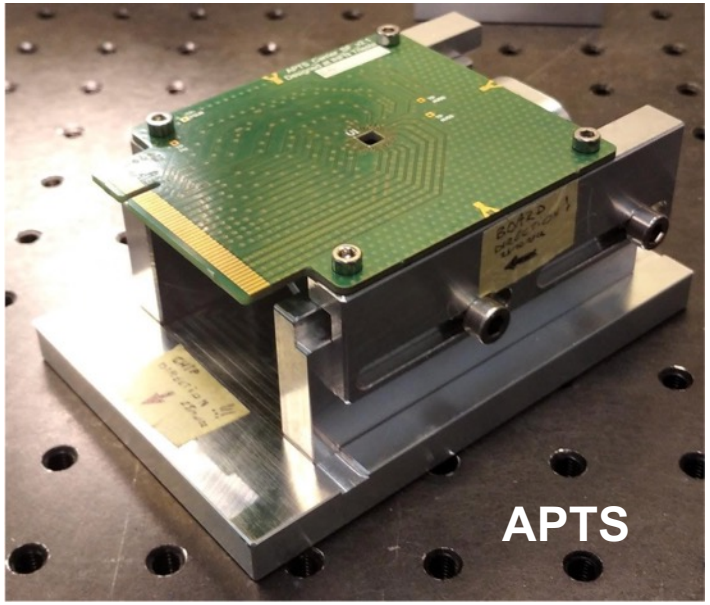


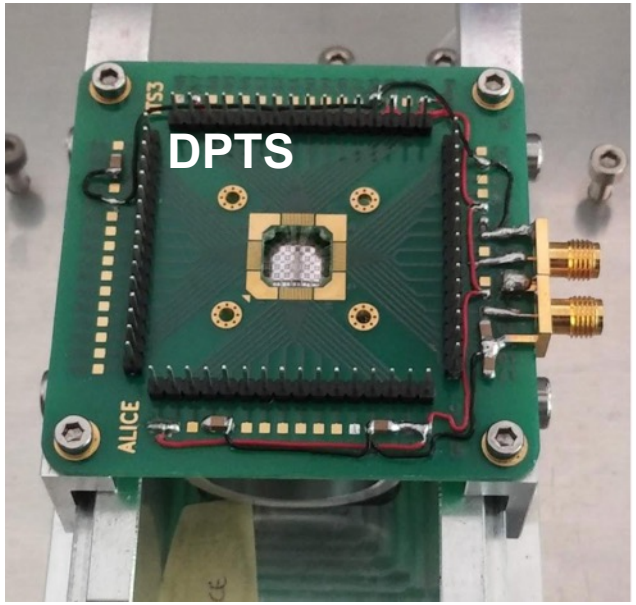


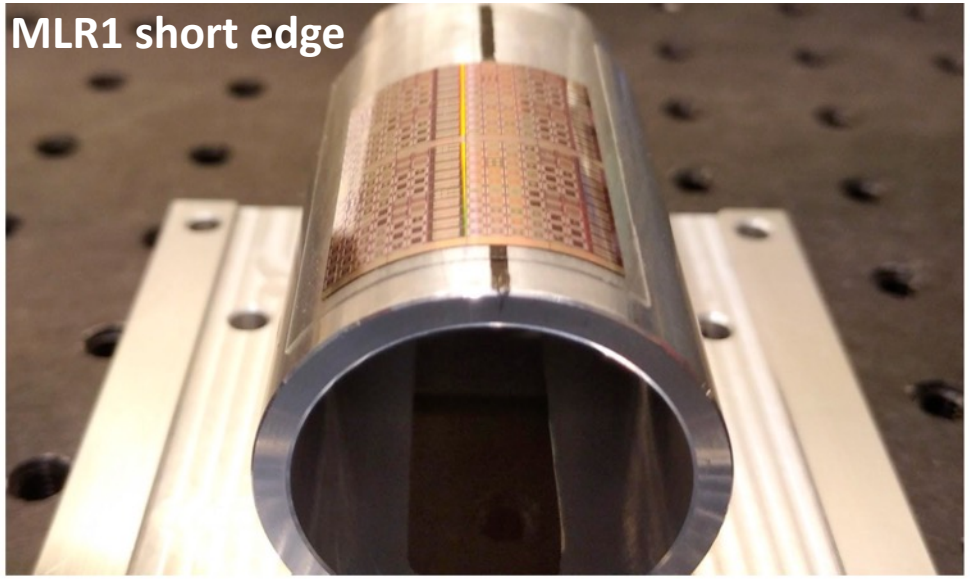
https://doi.org/10.1016/j.nima.2021.166280

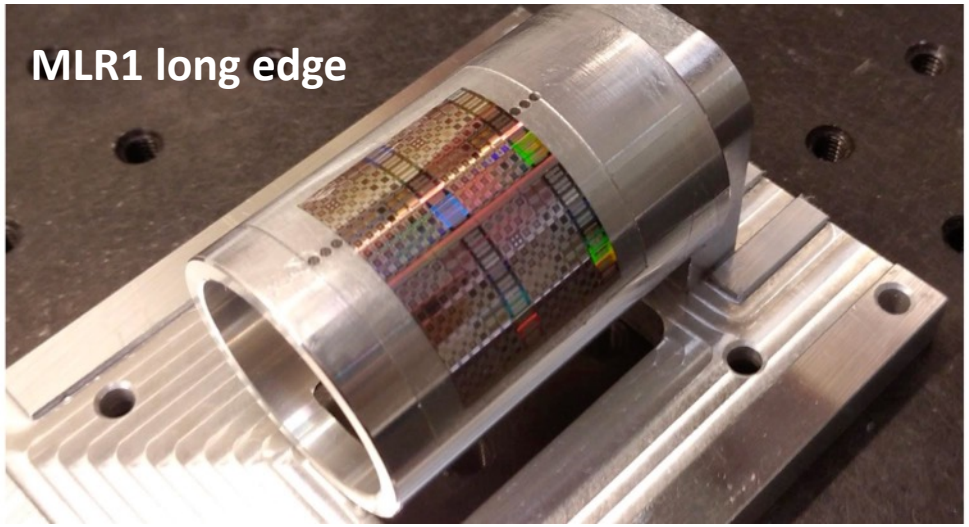
Thinning and Bending of CMOS sensors: 65 nm

- MLR1 chips bending: both APTS and DPTS
- special boards developed to bond on the bent structure
- tests ongoing





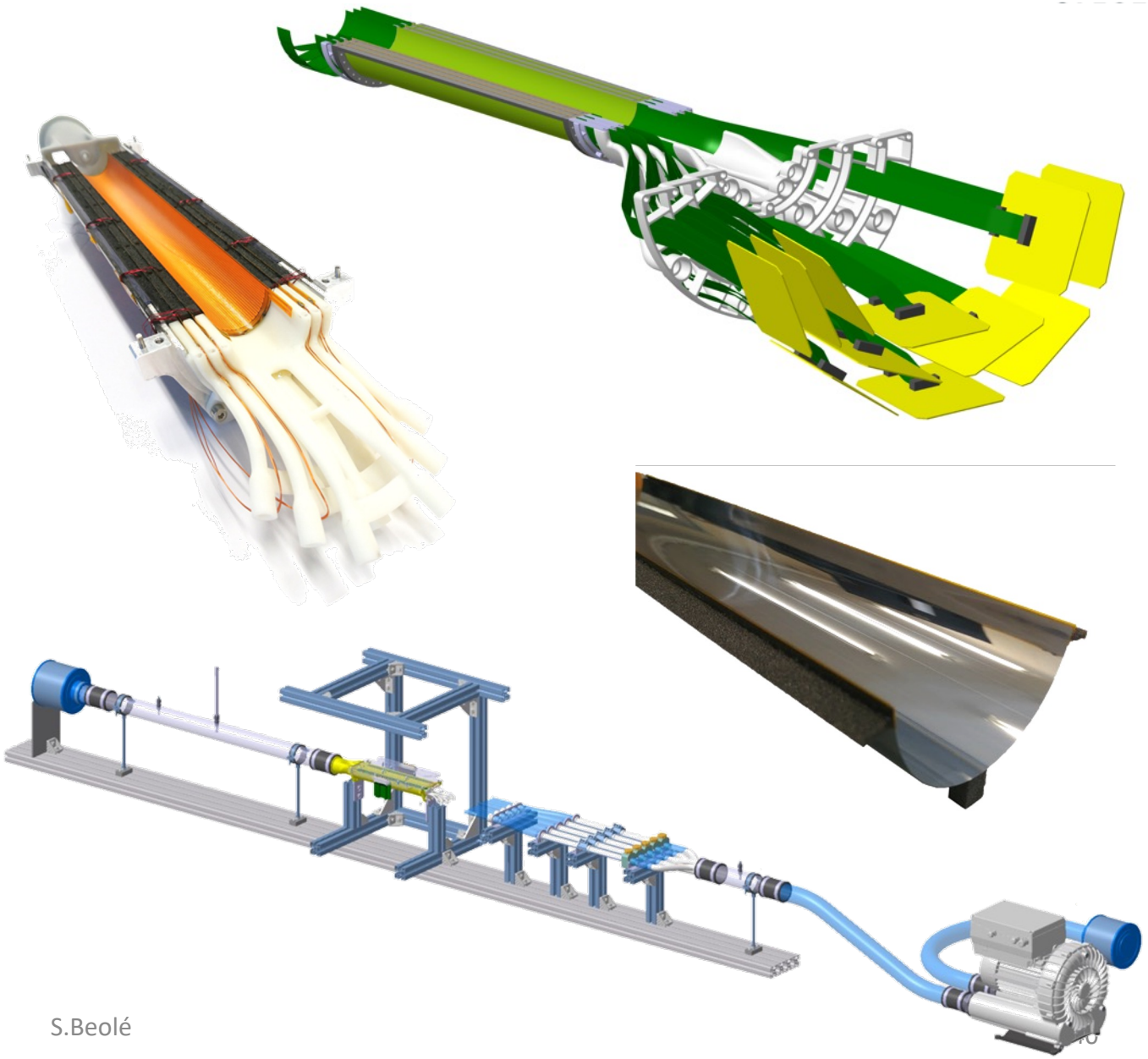




Mechanical support and cooling

Mechanics:

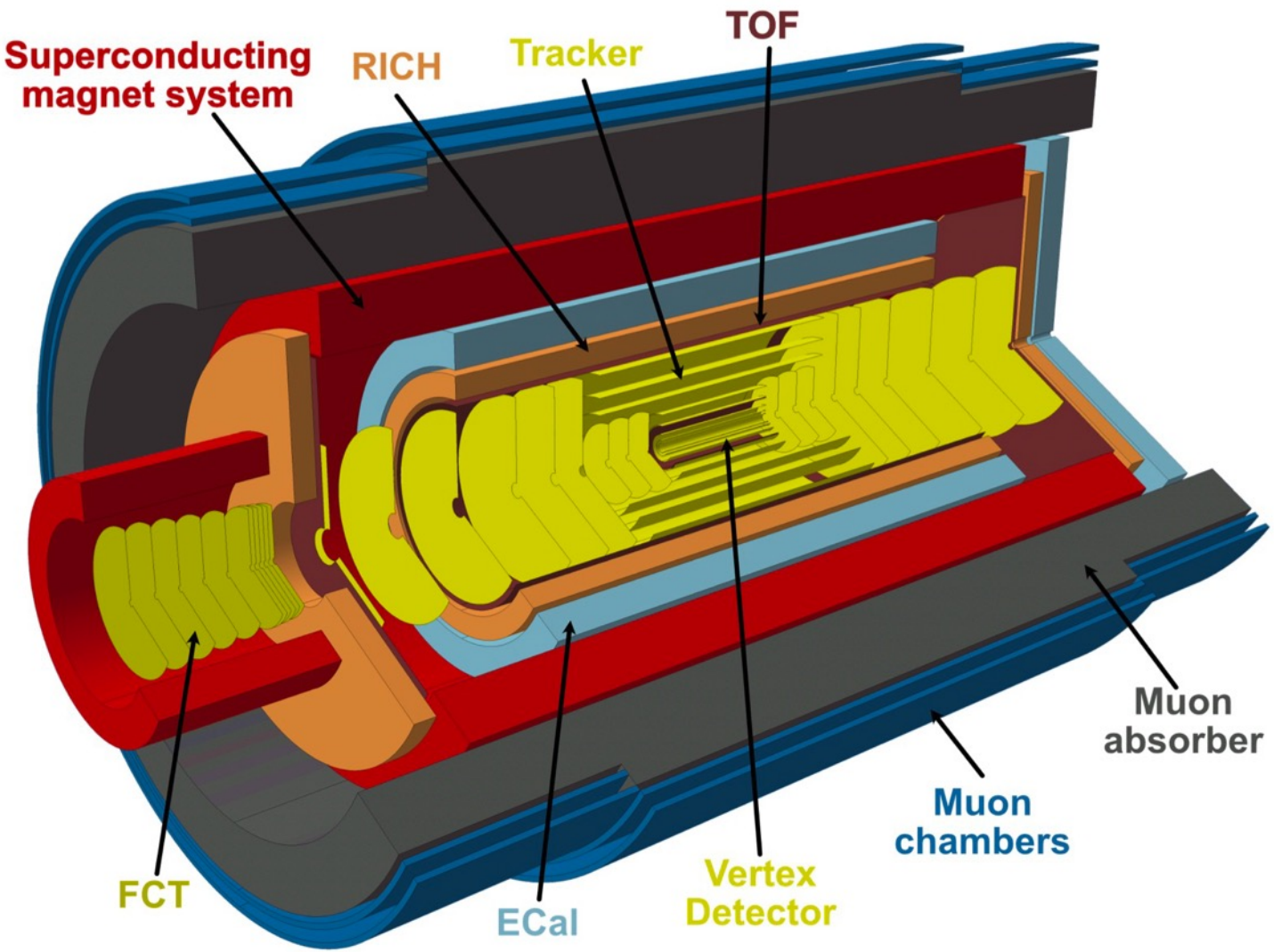
- Layout study including
  - A/C-side FPC integration
- Engineering models of ITS3 are being produced
  - Equipped with dummy silicon
- Breadboard for cooling studies:
  - dummy silicon + flex circuit heaters
- Used to study:
  - support structures
  - bending
  - integration
  - cooling
- Very successful integration of EM1 and EM2



A silicon only experiment?

Large future silicon based experimental set-ups

LHC timeline after RUN 4:



ALICE3

Ambition to design a new experiment to continue with a rich heavy-ion programme at the HL-LHC" mentioned in the Update of the European strategy for particle physics

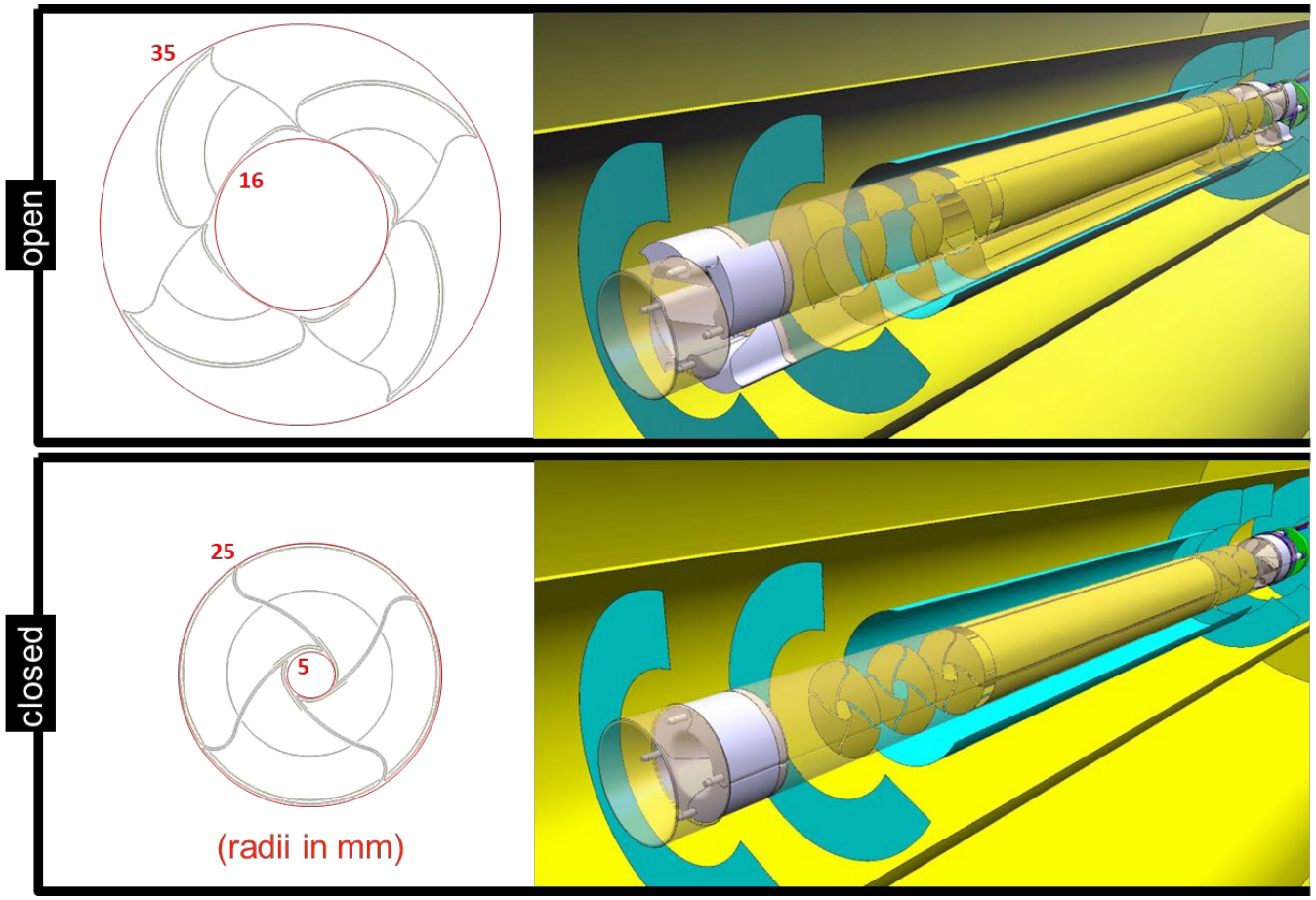
arXiv:2211.02491

LoI positively reviewed by LHCC last year

Vertex Detector: Iris inside the beam pipe

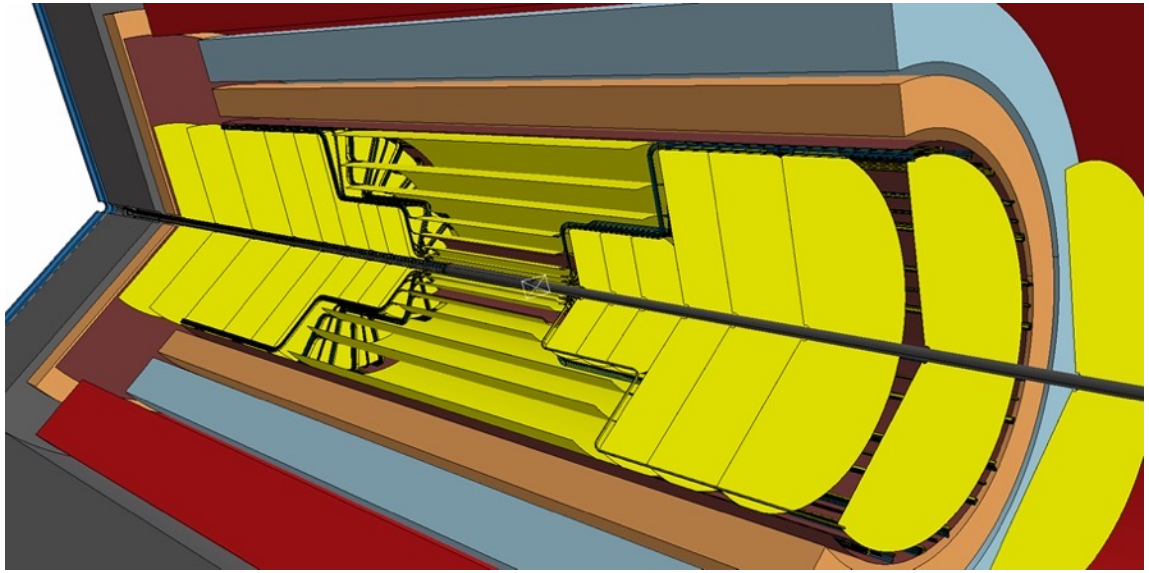
- **Curved sensors**
- **5 mm** from IP
  - Crucial to gain highest possible vertex resolution
  - Extremely challenging requirements on sensor
- **Retractable mechanics** inside the beam pipe
- **Vacuum-compatible** services and interconnections

R&D challenges on
mechanics, cooling, radiation tolerance



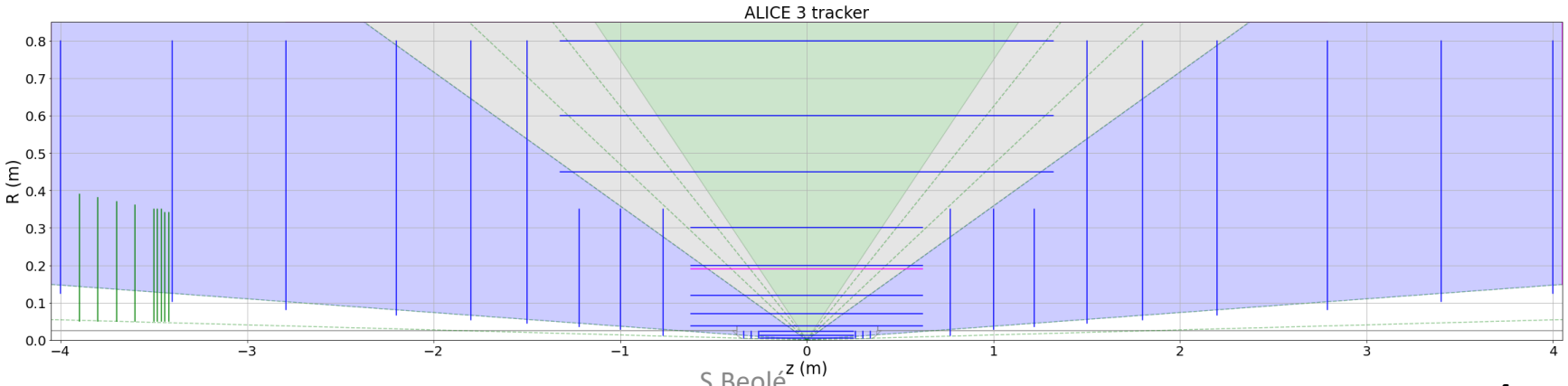
Outer tracker

- **Relative p_T resolution** $\propto \frac{\sqrt{x/X_0}}{B \cdot L}$ ⟹ ~1 % up to η = 4
  - critically depends on integrated magnetic field and overall material budget
- **Layout: ~11 tracking layers (barrel + disks) to be optimised**
  - **MAPS modules** on water-cooled carbon-fibre cold plate
  - σ_{pos} ~10 µm → 50 µm pixel pitch
  - timing resolution ~100 ns (→ reduce mismatch probability)
  - material ~1 % X_0 / layer → overall X/X_0 =10%
- **R&D challenges** on
  - powering scheme (→ material)
  - industrialisation



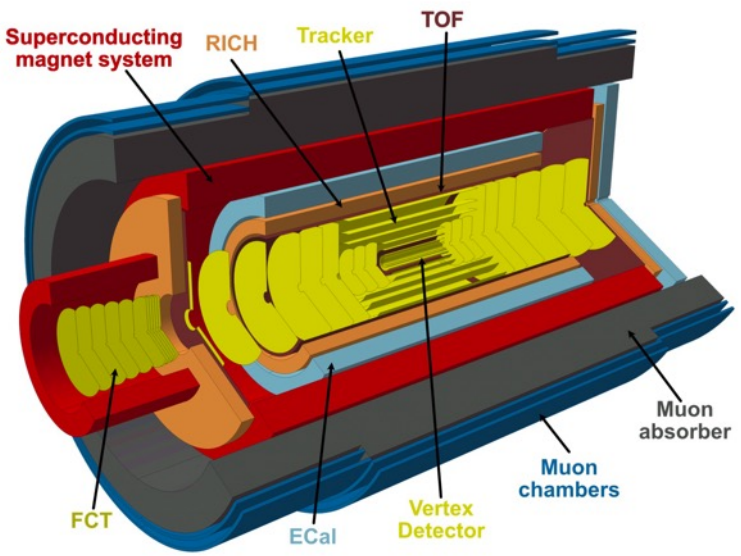
Total silicon surface ~60 m^2

80cm



4m

ALICE 3 time of flight with silicon sensors?



Separation power $\propto L/\sigma_{TOF}$

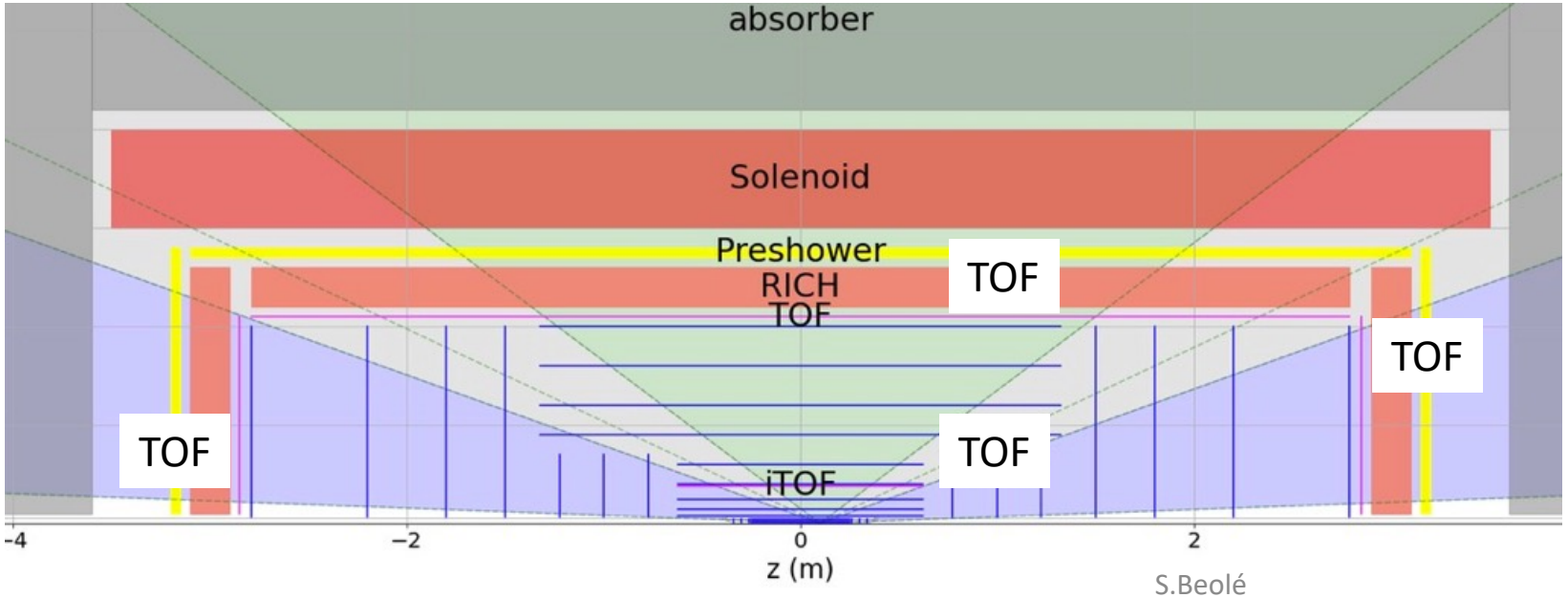
- distance and time resolution crucial
- larger radius results in lower p_T bound

2 barrel + 1 forward TOF layers

Silicon timing sensors ($\sigma_{TOF} \approx 20$ ps)

Material budget: 1-3% X/X_0

Power consumption: <50mW/cm^2



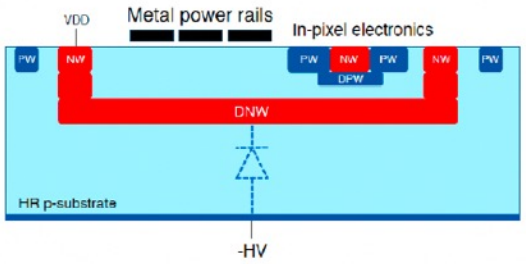
TOF 45 m^2 in total

- outer TOF at R ≈ 85 cm
- inner TOF at R ≈ 19 cm
- forward TOF at z ≈ 405 cm

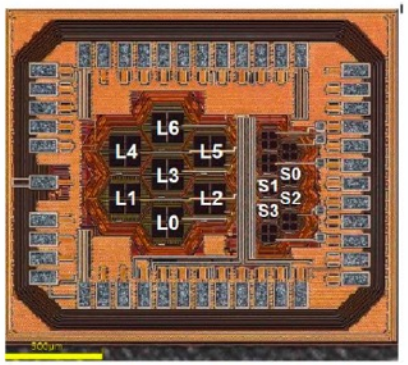
S.Beolé

TIMING WITH MONOLITHIC SENSORS: OPPORTUNITIES AND CHALLENGES

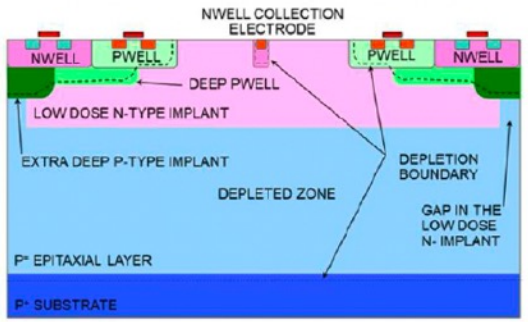
- Advantages:
  - Potentially 100% efficiency
  - Excellent radiation hardness demonstrated for several processes
  - Cost-effectiveness–on chip digitization, time-tagging and data pre-processing



Y. Degerli et al., 2020 JINST 15 P06011



G. Iacobucci et al., 2019 JINST 14 P11008



T. Kugathasan et al., Nucl. Inst. Meth. A Vol. 979, Nov. 2020

Several monolithic projects targeting enhanced timing resolution

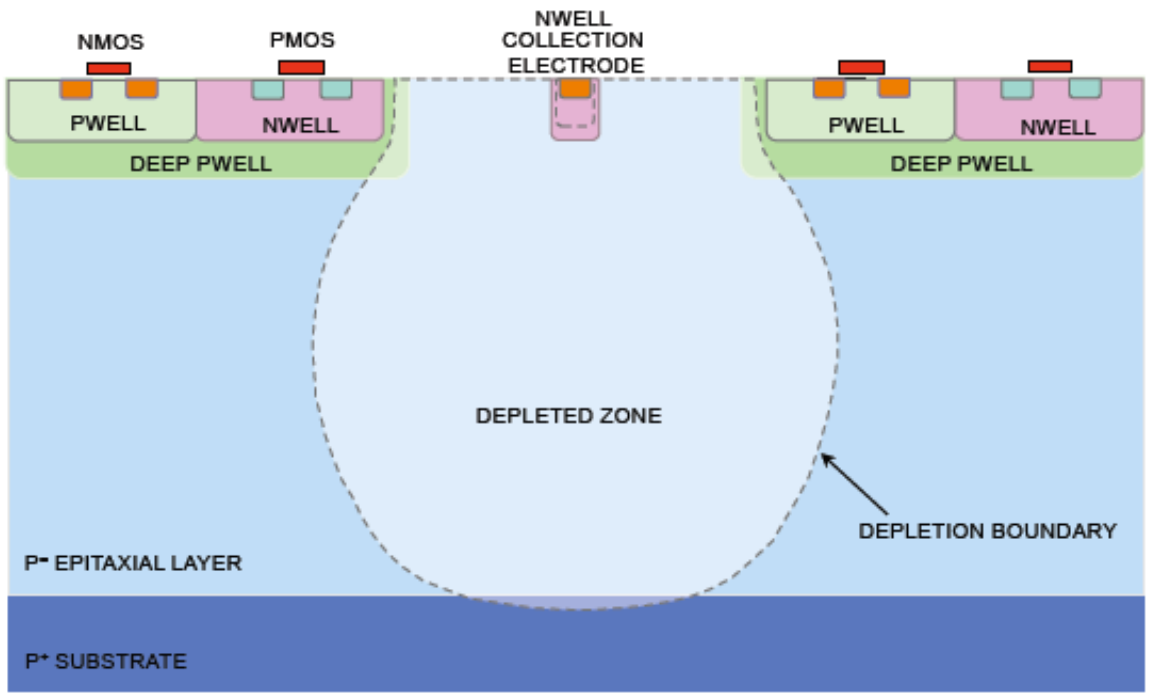
- Challenges
  - Fast collection (100s of ps) and low capacitance at the same time
  - Low power consumption
  - **20 ps resolution obtained experimentally recently by Monolith project** (https://arxiv.org/abs/2301.12244), not yet in reach for the other developments...

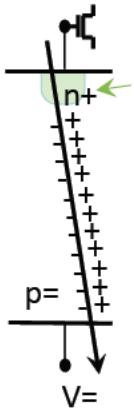
Summary

- CMOS sensors in 180nm technology successfully used for trackers
  - **used in ALICE (ITS2, MFT), sPhenix, CSES2/Limadou (Space)** and considered for other experiments (modified process)
  - limited by slow charge collection
  - process modification needed -> many developments ongoing
- Future developments rely on wafer scale sensors (ITS3, ALICE3)
  - **65nm TPSCo technology validated!!**
  - extremely successful characterization campaign ongoing (with contribution by many groups interesed in the technology)
  - ER1 wafers for stitching elavuation delivered
  - ER2 submission in preparation
- Extensive R&D ongoing:
  - bending of wafer scale sensors
  - characterization of 65nm bent structures
  - mechanical support and cooling studies

ADDITIONAL SLIDES

ALPIDE: sensitive epitaxial layer not depleted





$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

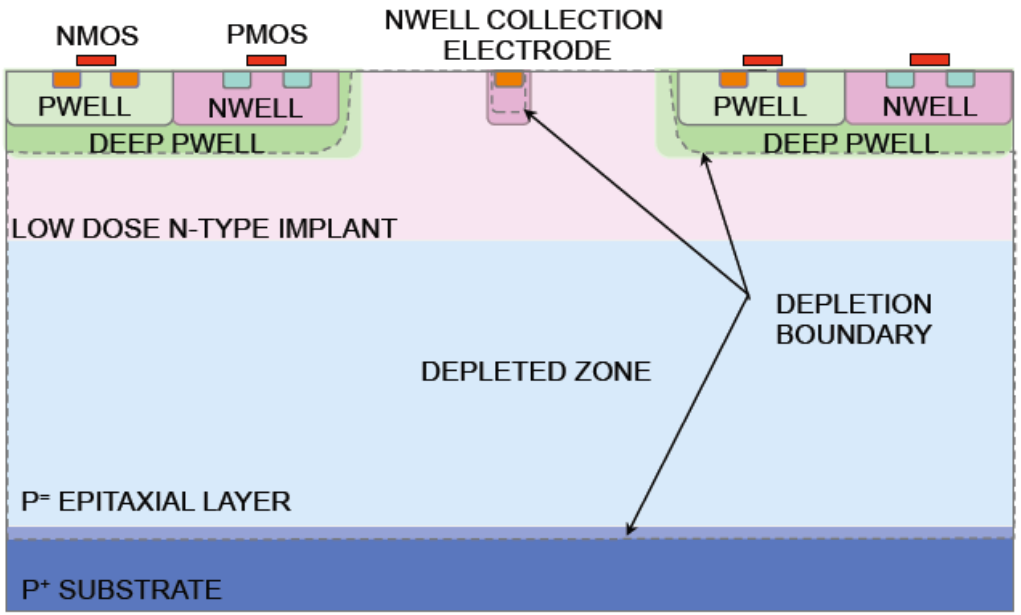
Add connection & circuit

Planar junction
Depletion width $= \sqrt{\frac{2\mathcal{E}|V|}{qN_A}}$

Spherical junction
Outer depletion radius $= \sqrt[3]{\frac{2\mathcal{E}|V|}{qN_A}\frac{3R_1}{2}}$

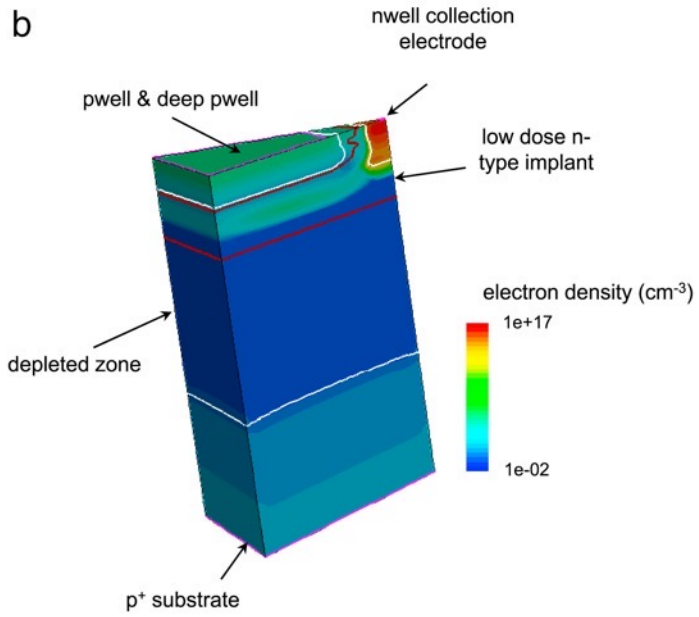
- Tower Semiconductor 180nm CMOS imaging sensor process
- **Signal charge is collected from the non-depleted layer,** diffusion dominated and prone to trapping after irradiation
- Planar vs spherical junction
  - Planar junction: depletion thickness proportional to **square root of reverse bias**.
  - Spherical junction : depletion thickness proportional only to **cubic root of reverse bias**, inner radius R1 to be kept small for low capacitance
- Deep well and substrate limit extension of the depletion: to fix this -> pixel design/process modification.

Sensor optimization (1): DEPLETED MAPS



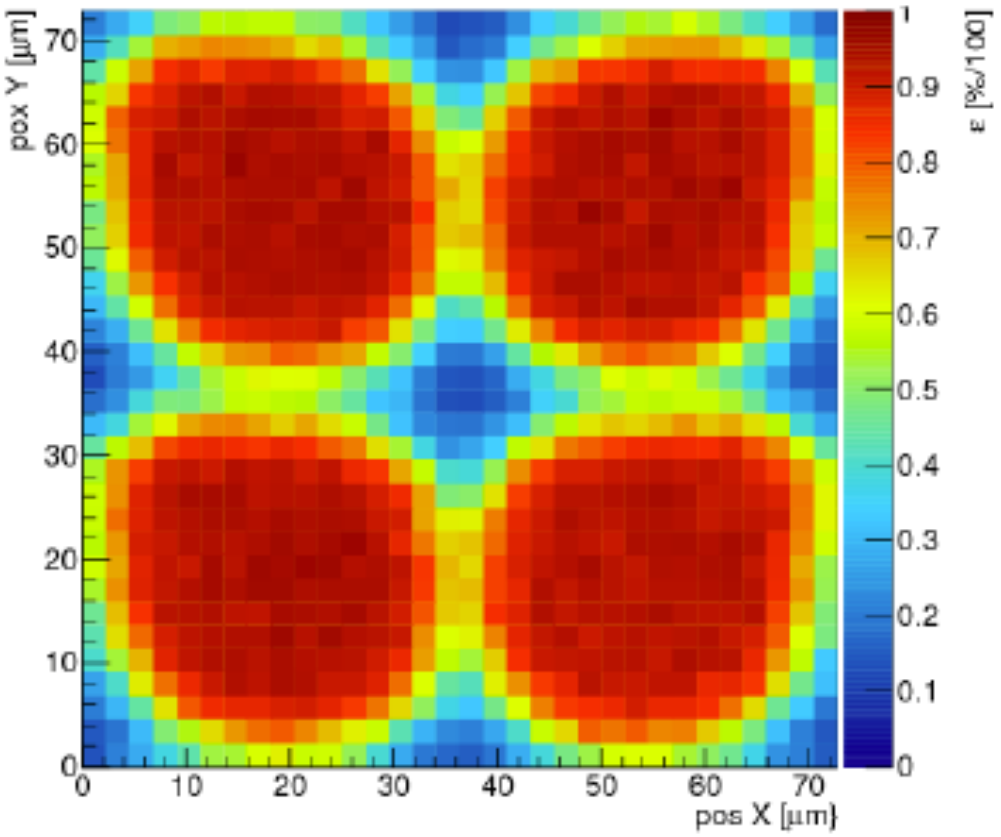
https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

- GOAL: create planar junction using deep **low dose n-type implant** and deplete the epitaxial layer
- initial interest from ATLAS followed by many others: MALTA/TJ MONOPIX development (Bonn, CPPM, IRFU and CERN)



Tower Semiconductor 180nm

Sensor optimization (1): results



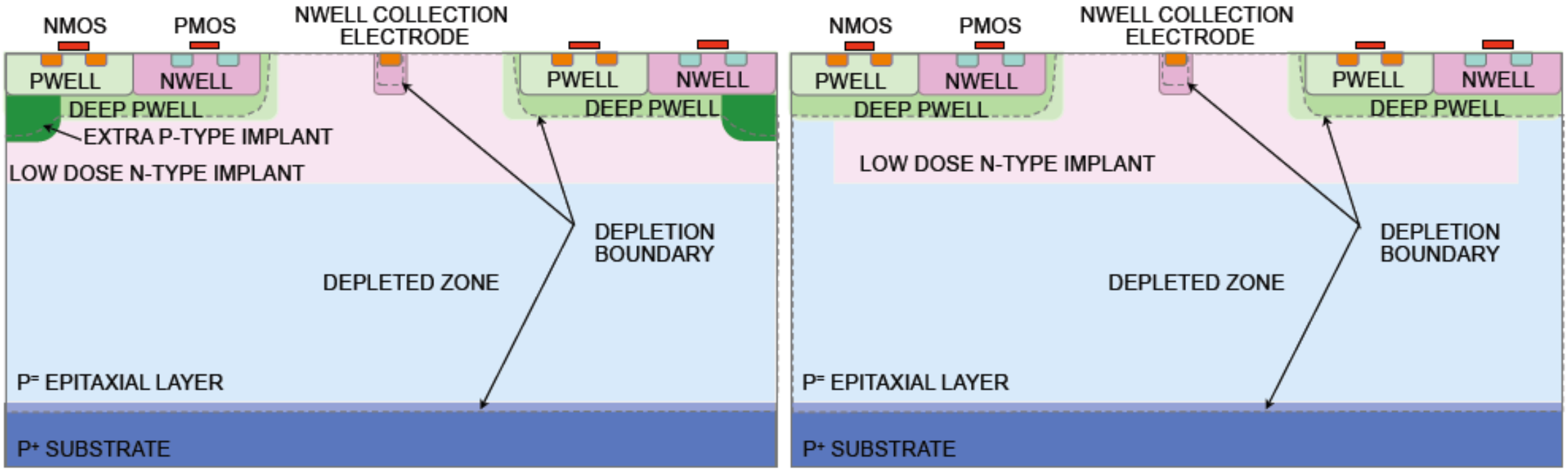
However:

- efficiency loss at ~ 10^{15} 1 MeV n_{eq}/cm^2 on the pixel edges and corners due to a too weak lateral field
- Lateral electric field not sufficient to push the deposited charge towards the small central electrode.
- Efficiency decreases in pixel corners
- Effect amplified by radiation damage

https://doi.org/10.1016/j.nima.2019.162404

Tower Semiconductor 180nm

Sensor optimization (2): improvement of the lateral field



3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

- Additional deep p-type implant or gap in the low dose n-type implant improves lateral field near the pixel boundary and accelerates the signal charge to the collection electrode.

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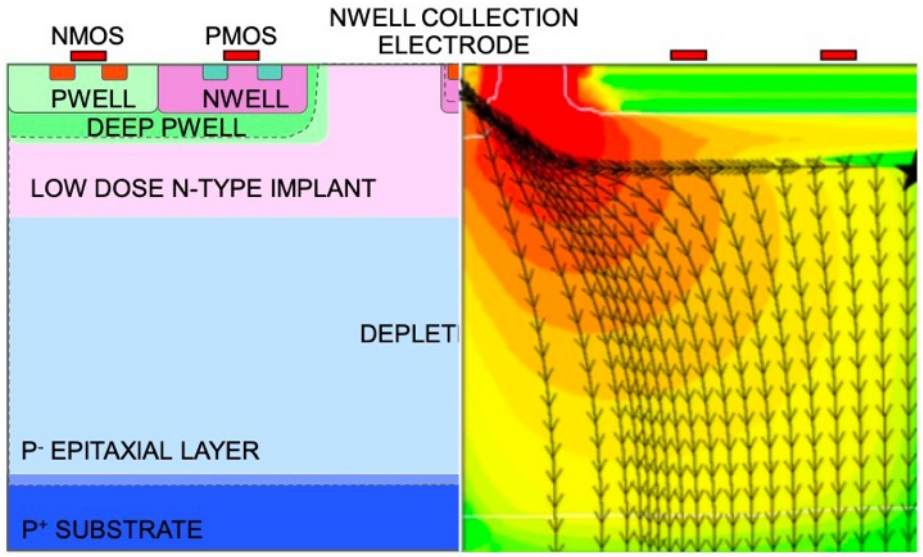
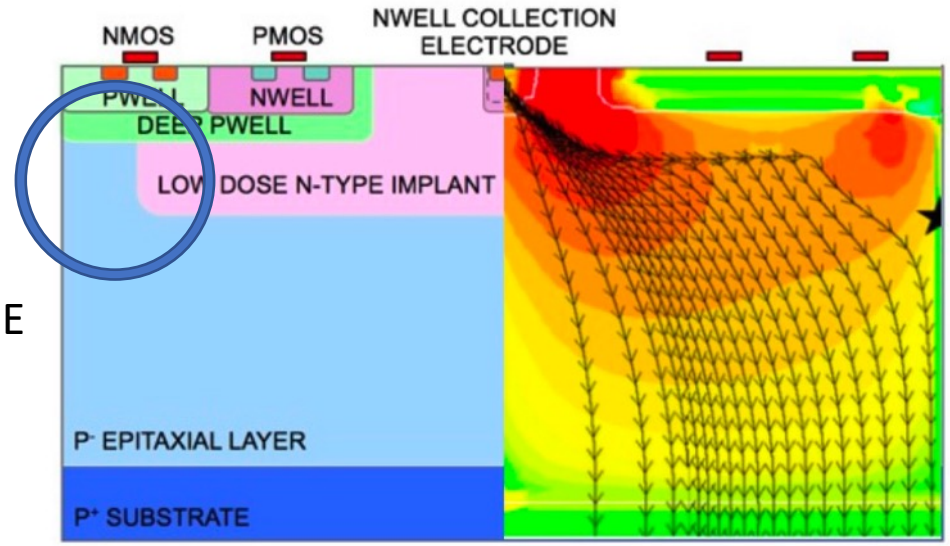
Sensor optimization (2): improvement of the lateral field



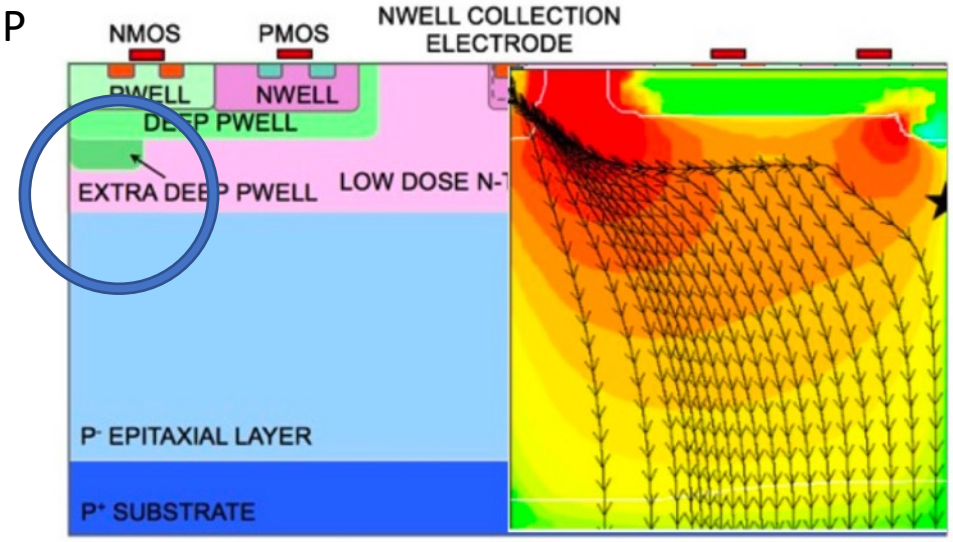
Standard modified process

GAP IN THE N LAYER



Gap in the n- layer (NGAP)

EXTRA DEEP P-WELL



Extra deep p-well (EDPW)

Process modifications to improve charge collection in the pixel edges

3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

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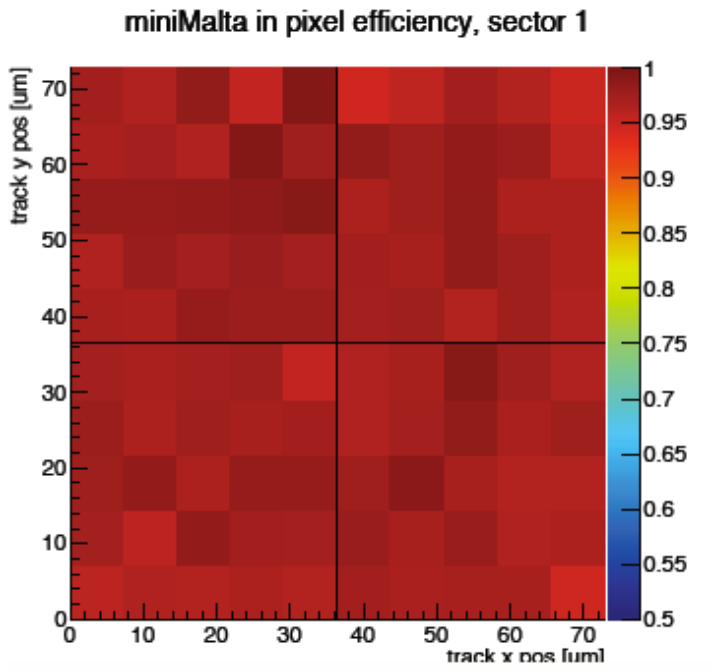
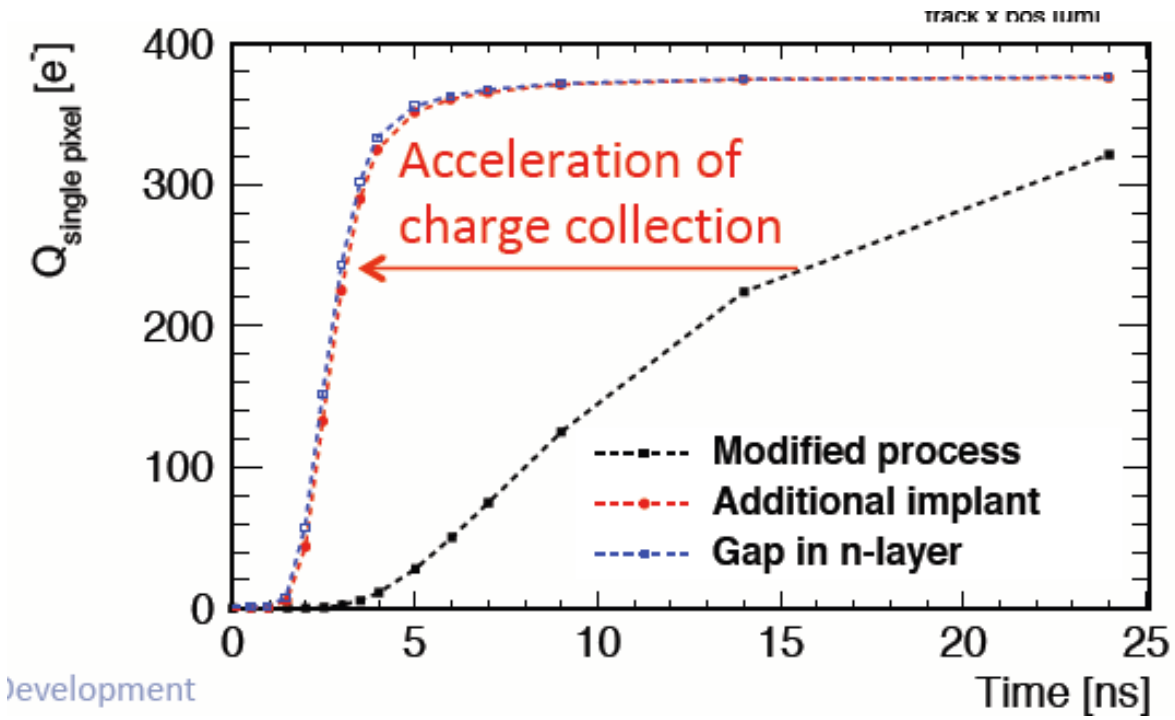
Sensor optimization (2): results





- Full detection efficiency at 10^{15} n_{eq}/cm^2
- better sensor timing

H. Pernegger et al., Hiroshima 2019,
M. Dyndal et al 2020 JINST 15 P0200

3D TCAD simulation M. Munker et al. PIXEL2018
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

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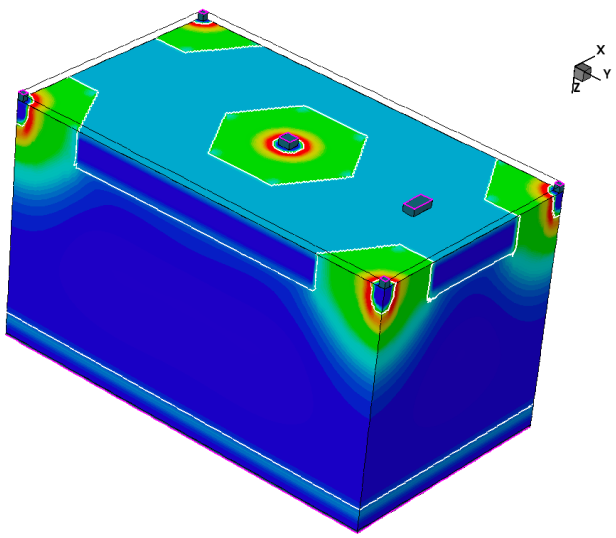
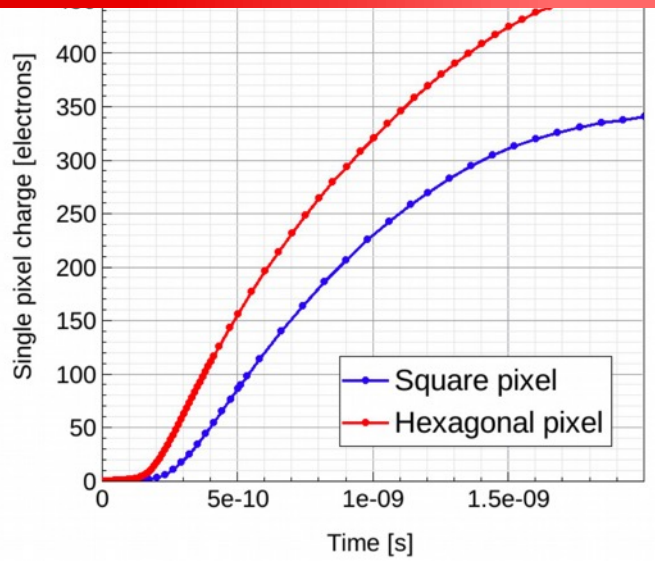
FASTPIX

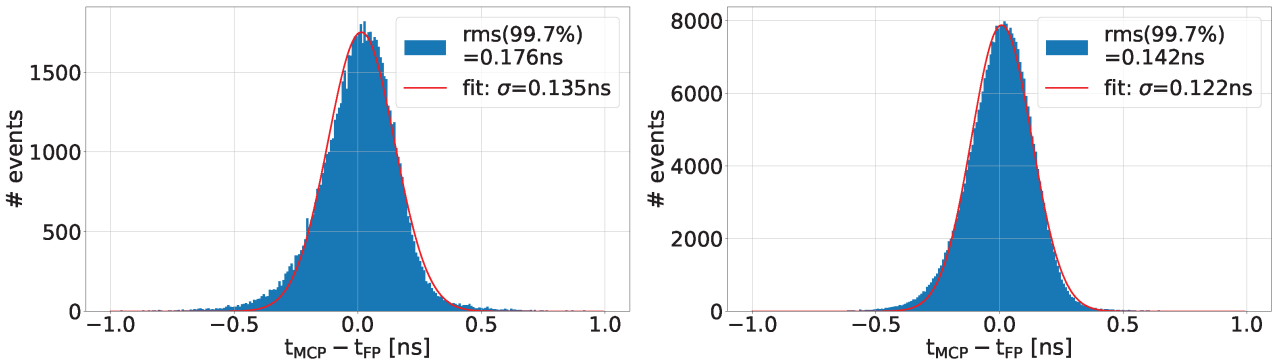
Simulated hexagonal unit cell – electrostatic potential:

- Hexagonal design reduces the number of neighbors and charge sharing → **higher efficiency**
- Hexagonal design minimizes the edge regions while maintaining area for circuitry → **faster charge collection**
- Optimisations important not only for timing, but also for efficiency and radiation tolerance

Preliminary test-beam results showed MIP time resolution of approximately 120-130 ps







Seed-pixel time residuals after timewalk correction for the inner region of the 10 μm (**a**) and 20 μm (**b**) pitch matrix.

J. Braach et al. Instruments 6 (2022) 13

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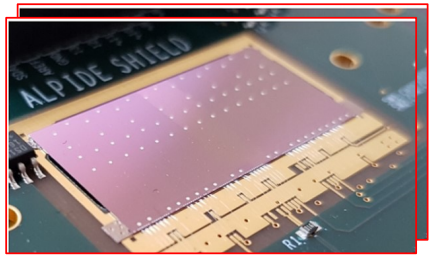
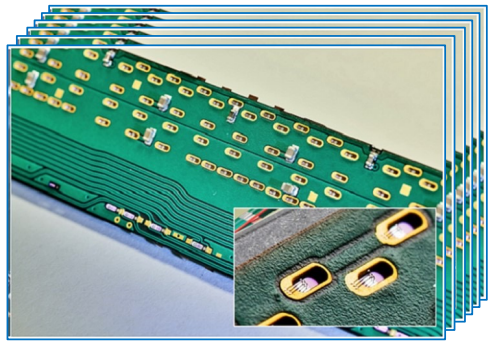
A long and complex journey….



chip test

FPC test



HIC assembly

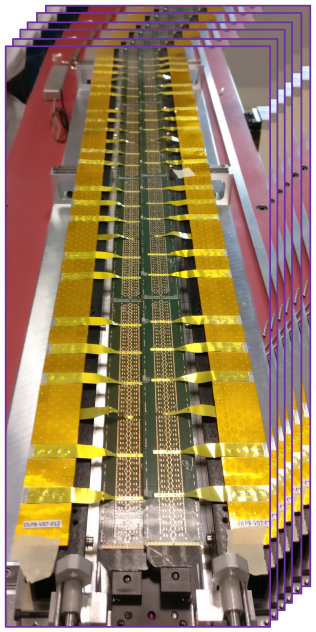
HIC characterization

CP and SF characterization

for OB: PB characterization

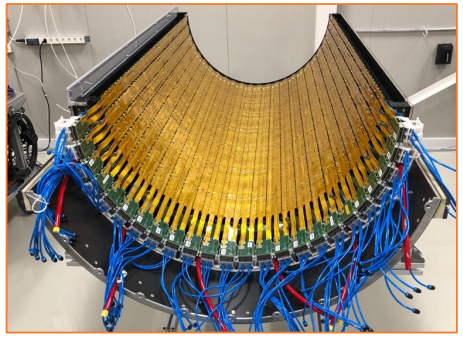
Stave assembly

Stave characterization



Installation

commissioning

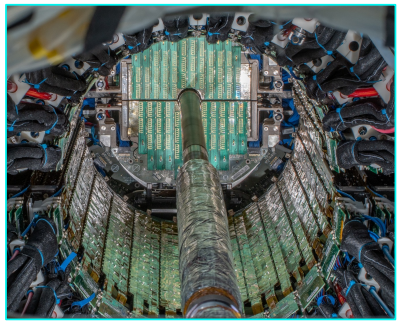


Half layer assembly

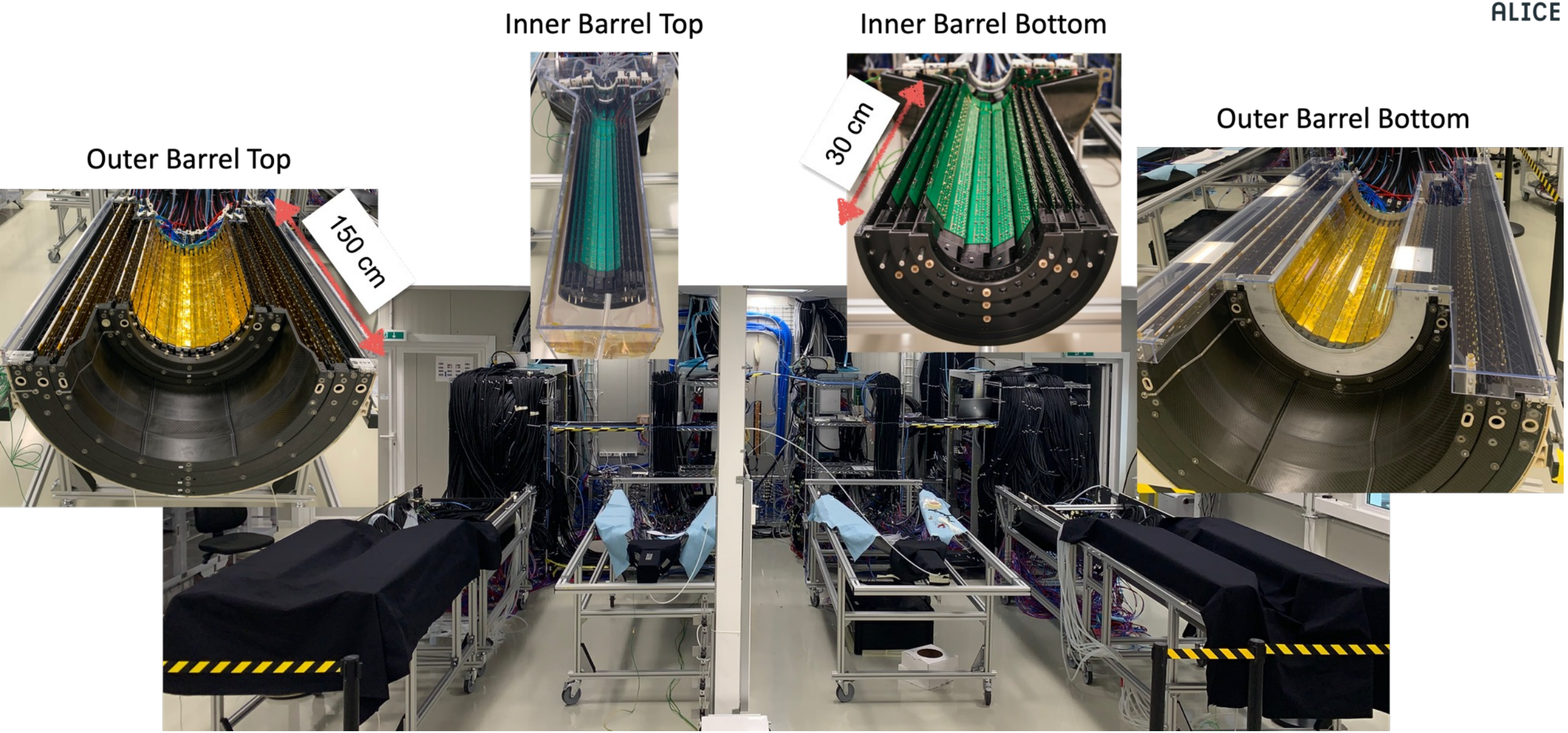
Half layer characterization

Half barrel assembly

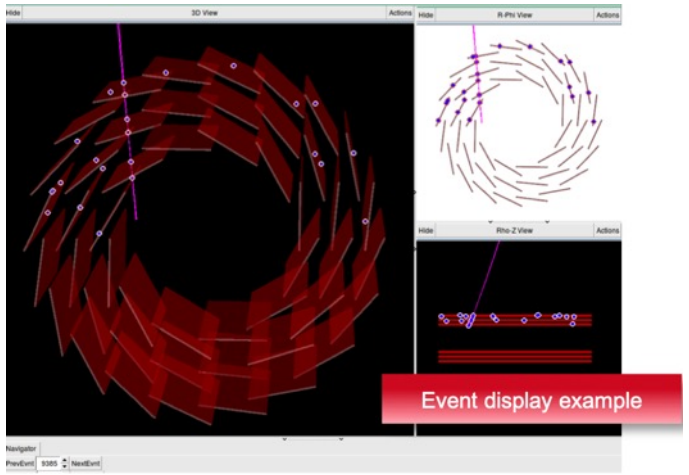
Half barrel characterization

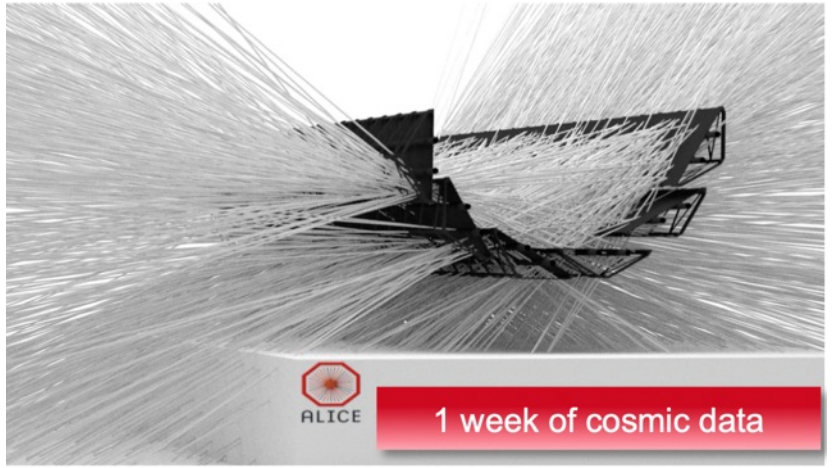


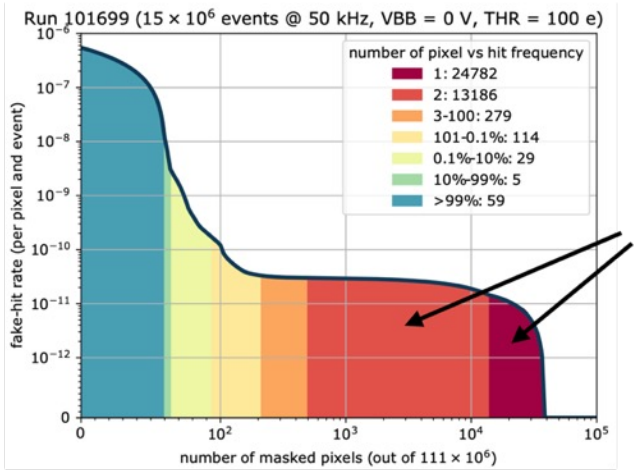
On-Surface Commissioning



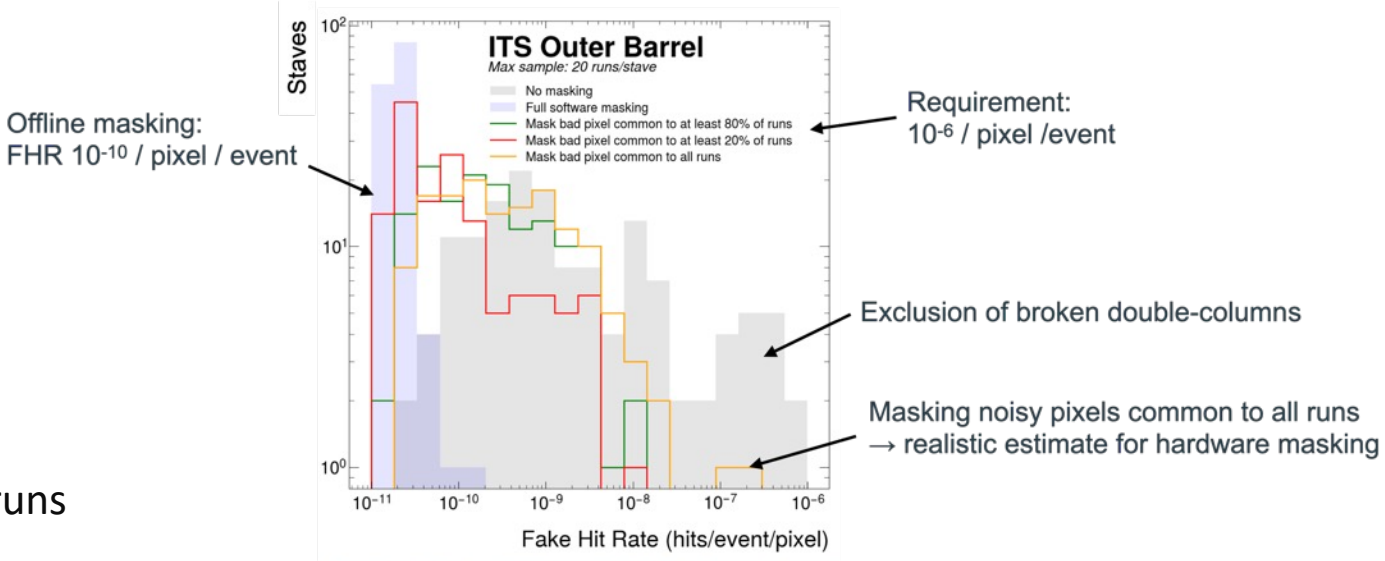
On-Surface Commissioning results







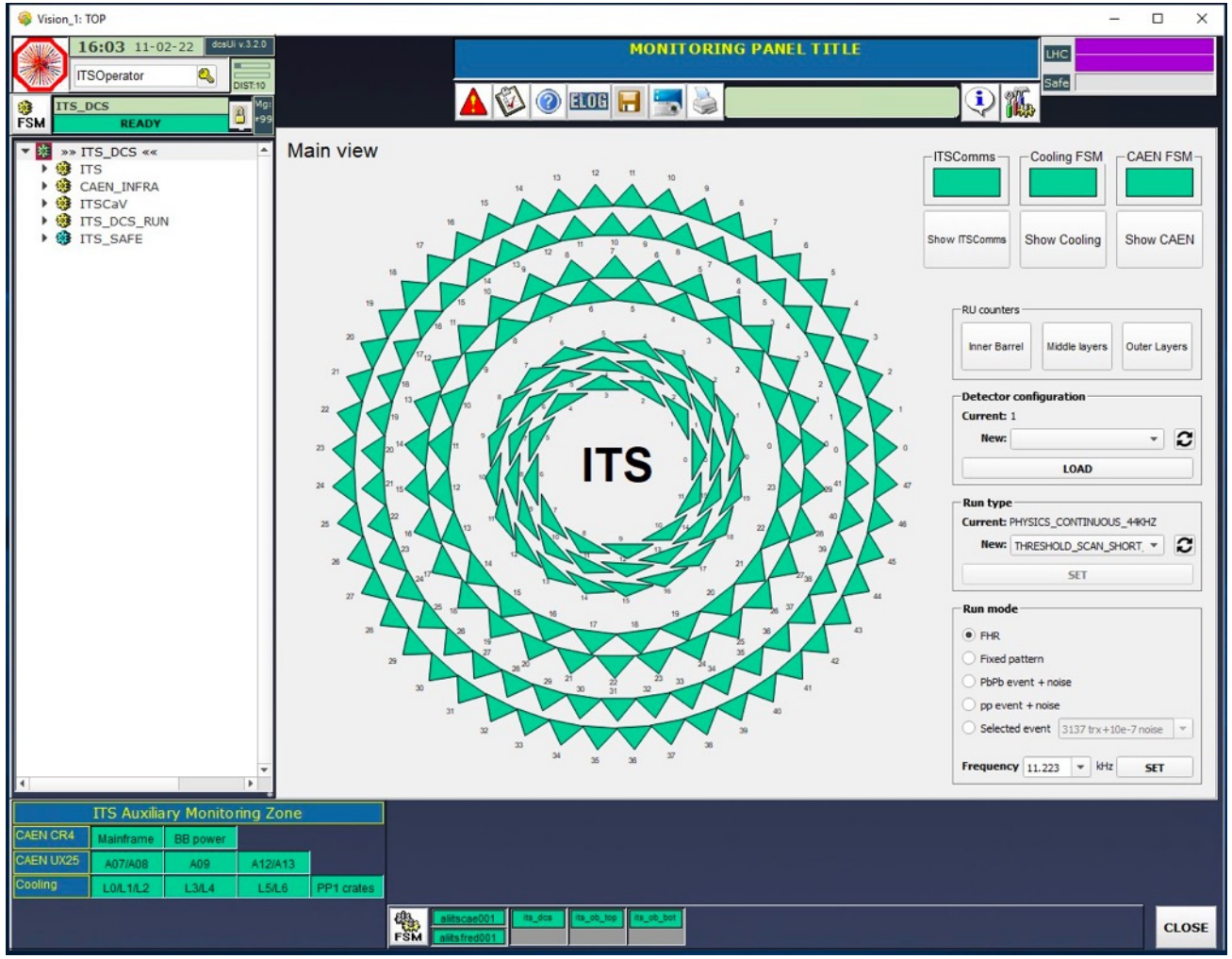
- Cosmics tracks reconstructed
- IB: fake-hit rate of 10^{-10} / pixel / event
  - Achieved by masking fraction of 10^{-8} pixels
- OB: fake-hit rate of 10^{-8} / pixel / event
  - Achieved by masking noisy pixels common to all runs



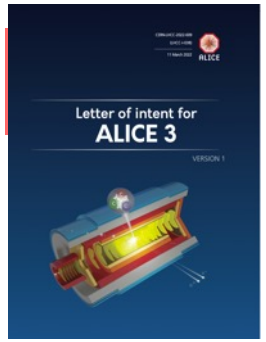
Excellent Fake-Hit Rate (FHR) in the entire OB

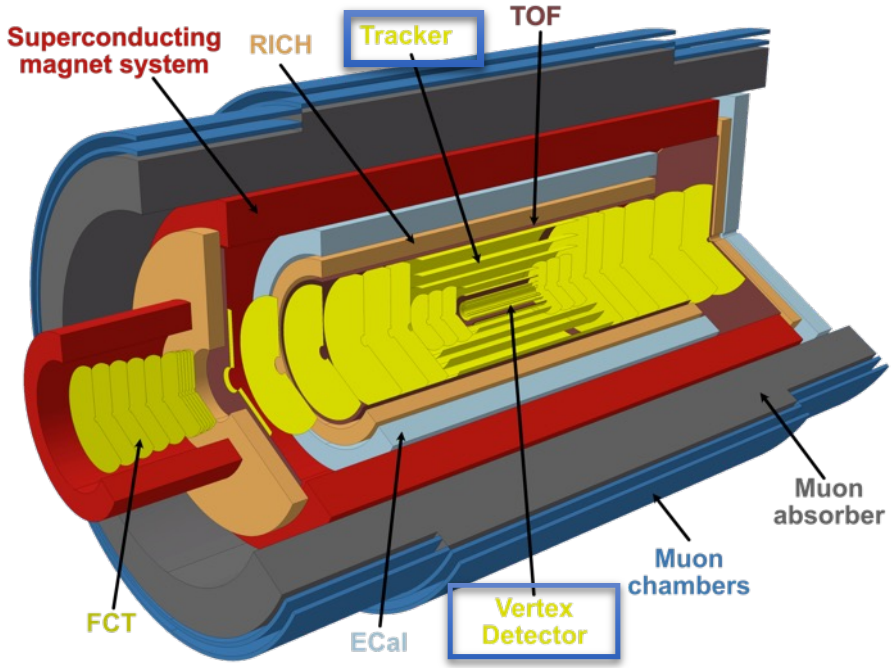
Detector Control System

- DCS ready to control detector in all phases of operation:
  - Controls and configures pixel chips and entire infrastructure
  - Error recovery during a run to continue running with minimal data loss
  - Detector functionality implemented in C++ library (pixel chips, readout cards, regulator boards)
  - GUI, FSM and alarms in Siemens WinCC OA
  - fully integrated into ALICE DCS
- Routinely used during commissioning and Pilot Beams

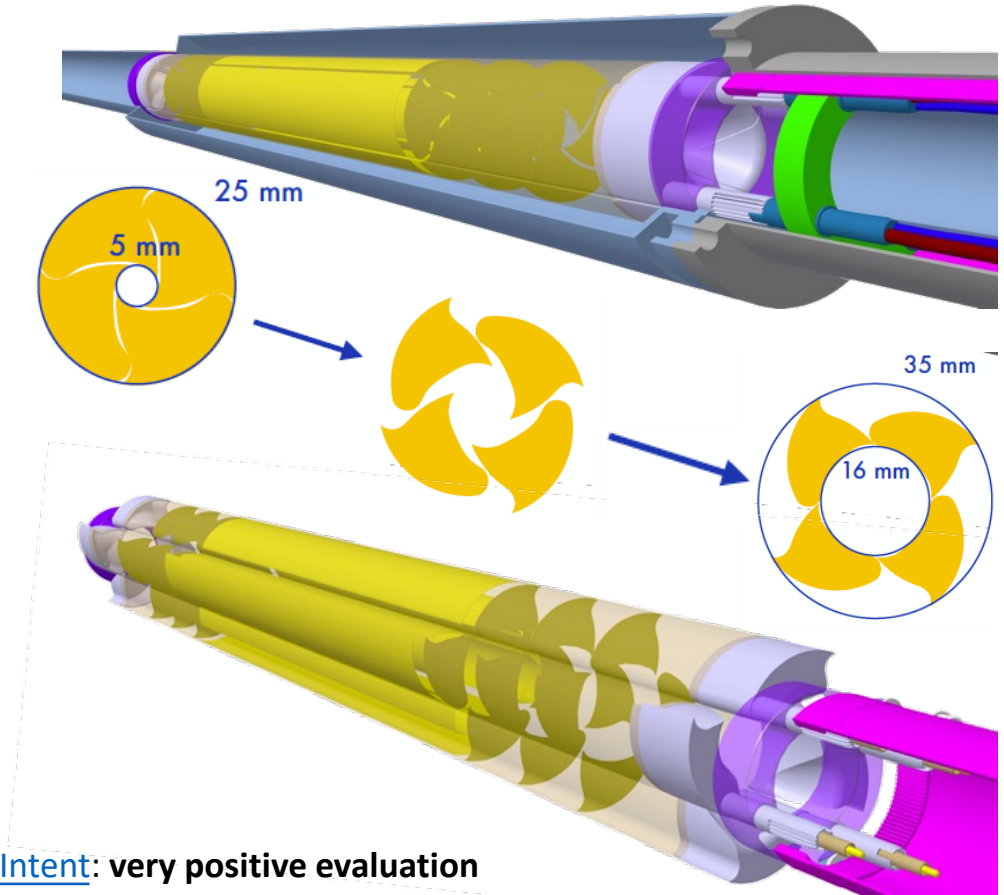


ALICE 3: tracker + vertex detector





- **Conceptual study of iris tracker**
  - wafer-sized, bent MAPS (leveraging on ITS3 activities)
  - rotary petals (thin Be walls) for secondary vacuum
  - match beampipe parameters (impedance, aperture, …)
  - feed-throughs for power, cooling, data
- **R&D programme** on mechanics, cooling, radiation tolerance



GOALS:

- **Tracking and PID over large acceptance**
- **Excellent vertexing**
- **Continuous readout**

REQUIREMENTS

- **Tracker:** low power, large surface **60 m²** (challenges: yield, fill factor)
  - Monolithic CMOS sensors with timing (4D tracking)
- **Vertex detector:** very close to IP (challenges: high rate, high radiation load)
  - Retractable detector (iris tracker) $R_{in} \approx 5$ mm
  - Wafer-scale monolithic CMOS sensors

[CERN-LHCC-2022-009] LHCC review of Letter of Intent: **very positive evaluation**