ATLAS Detector Upgrade

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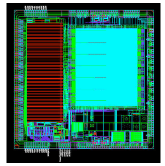
Outline



- Introduction
  - why upgrading ?
  - LHC plans for luminosity increase
- Upgrade plans for ATLAS
  - Muon Spectrometer
    - new Small Wheel
  - Calorimetry
    - LAr forward calorimeter
  - Trigger
    - Track Trigger
  - Inner tracker
    - Insertable B-Layer (IBL)
    - A new silicon tracker
- Summary

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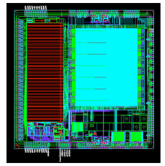
DISCLAIMER

- Sub-systems other than Inner Detector...

- Off-detector components
  - RODs, opto-links, DCS, services...

- All the rest I forgot about...

Why upgrading ?



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  - charged particle multiplicities, W, Z, ttbar cross-sections, etc.
  - starting to extend Tevatron reach for new physics

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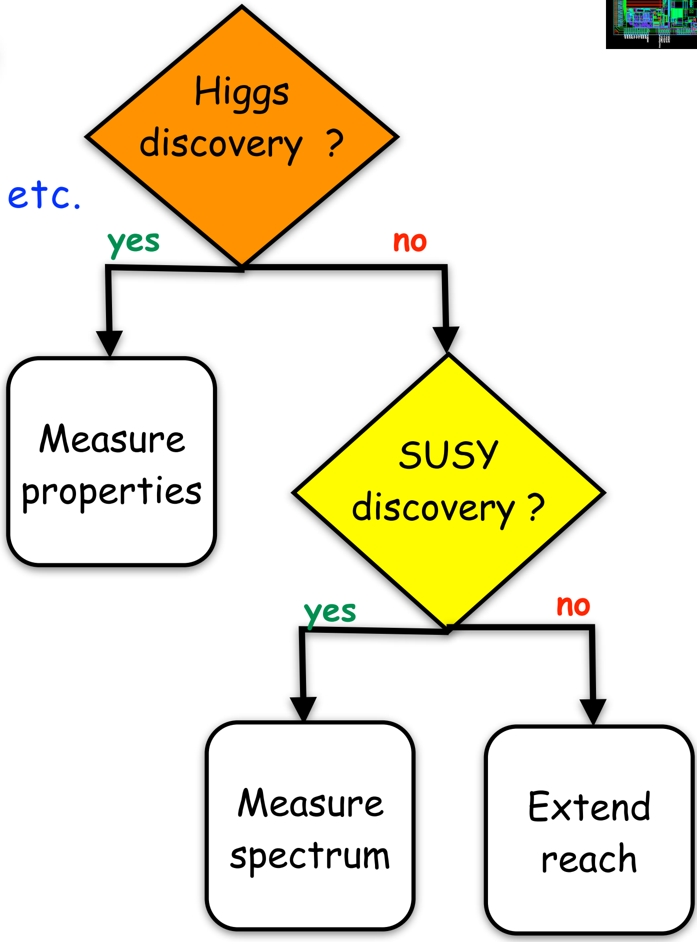
  - origin of EW symmetry breaking
  - Higgs, Supersymmetry, whatever...



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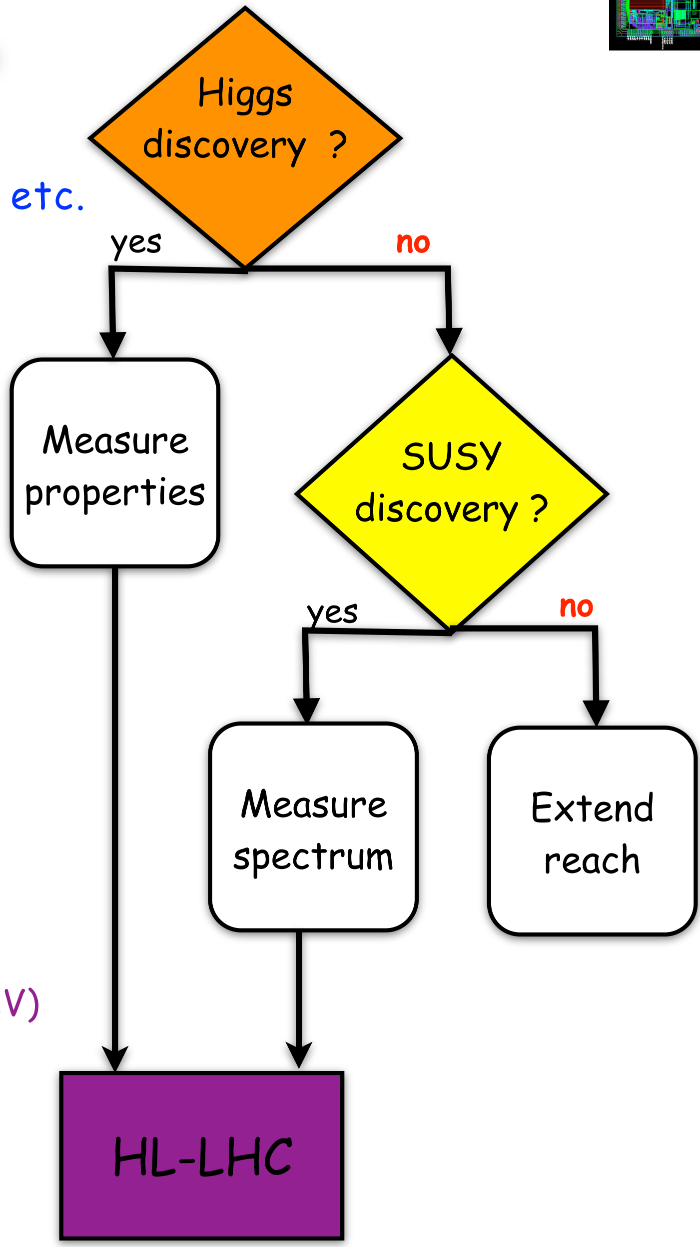
- Reasons for un upgrade ➡ physics-driven
  - improve measurements of new phenomena seen at the LHC
    - Higgs couplings to bosons and fermions and self-couplings
    - properties of SUSY particles
  - detect/search low rate phenomena inaccessible at the LHC
    - $H\rightarrow\mu^+\mu^-$ (BR~O(10^{-4}), $H\rightarrow Z\gamma$ (BR~O(10^{-3}) in M_H~100-160 GeV)
  - extend sensitivity to new high-mass scales
    - extra gauge bosons (Z',W')
- Are we starting to early ? **NO !!**
  - long times required for both accelerator and detectors R&D
    - R&D, production, assembly



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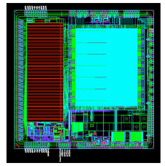

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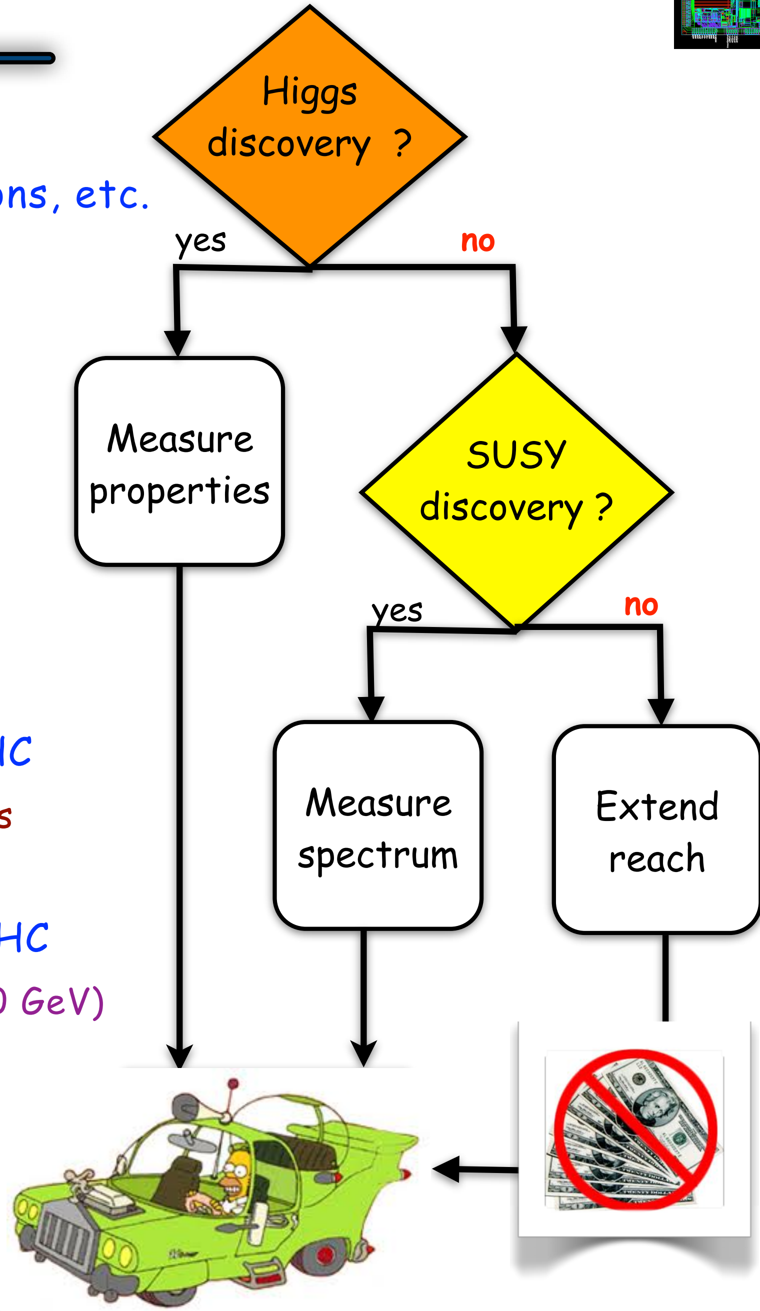
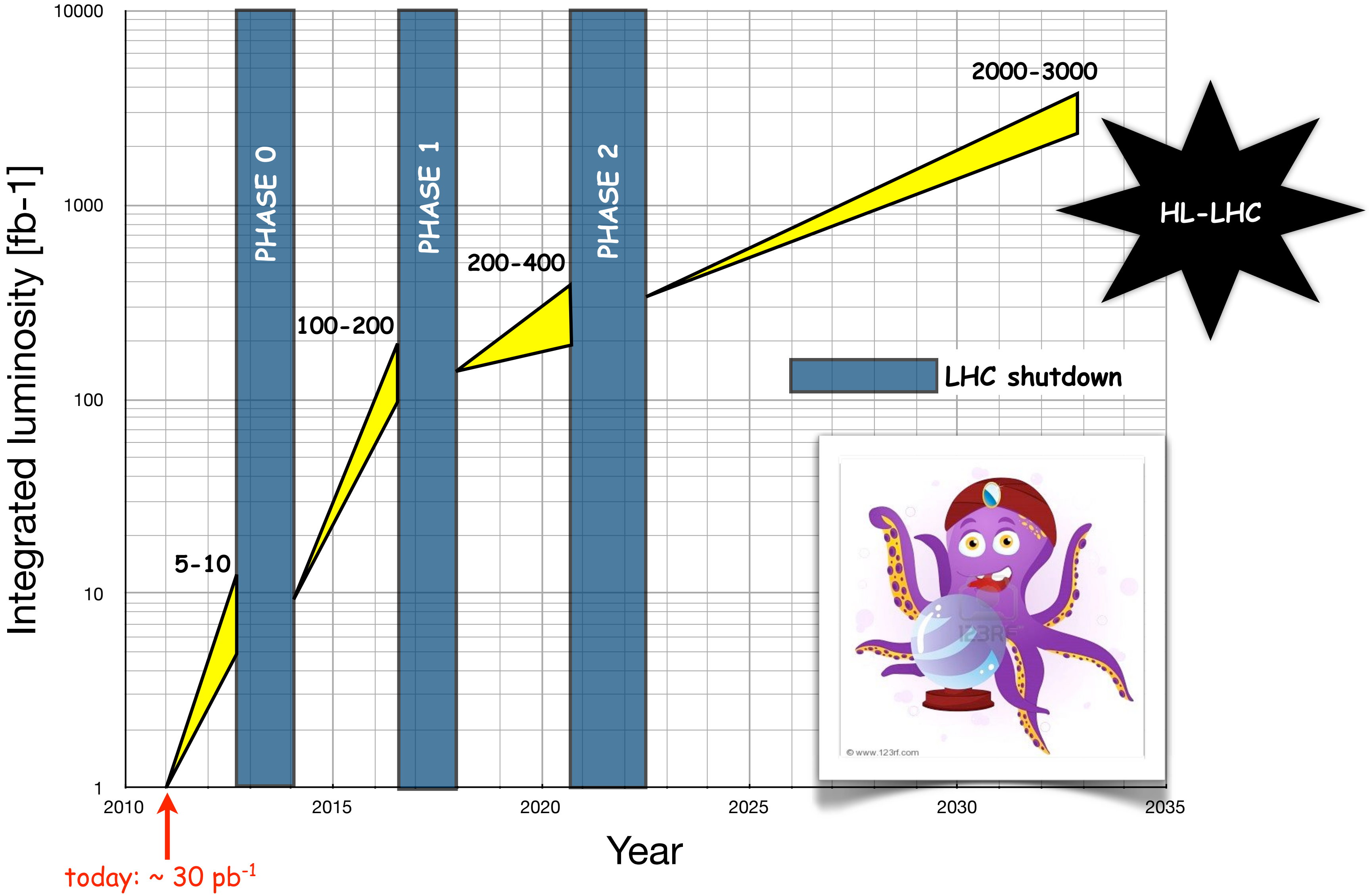
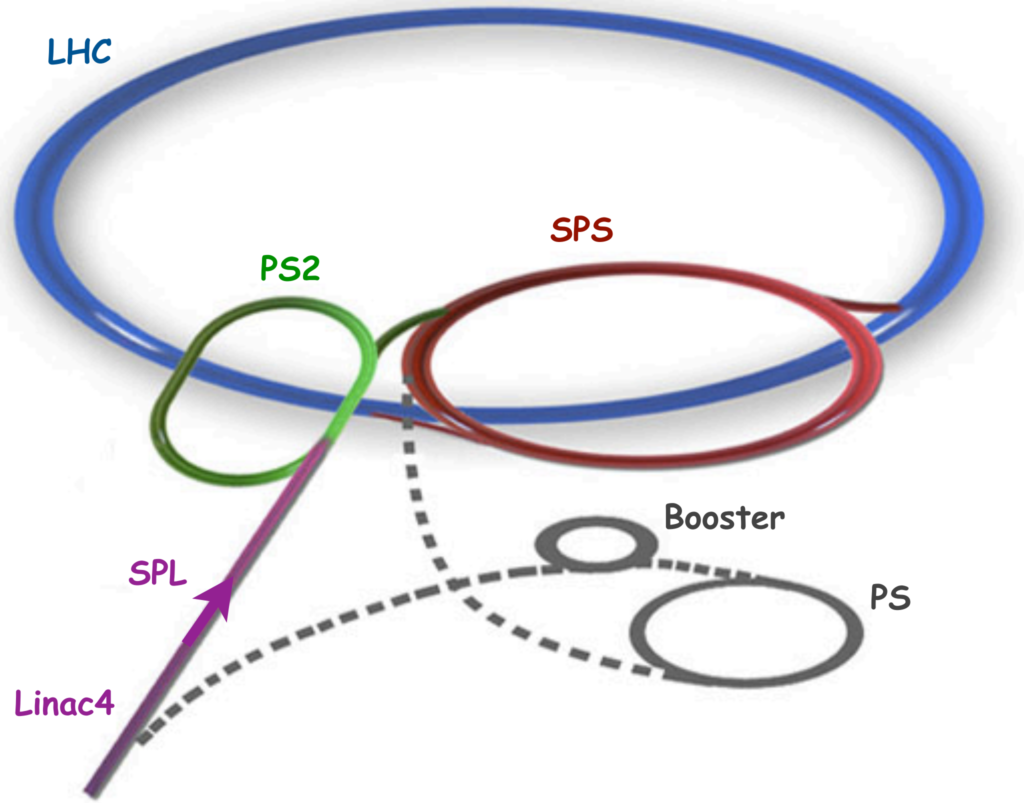


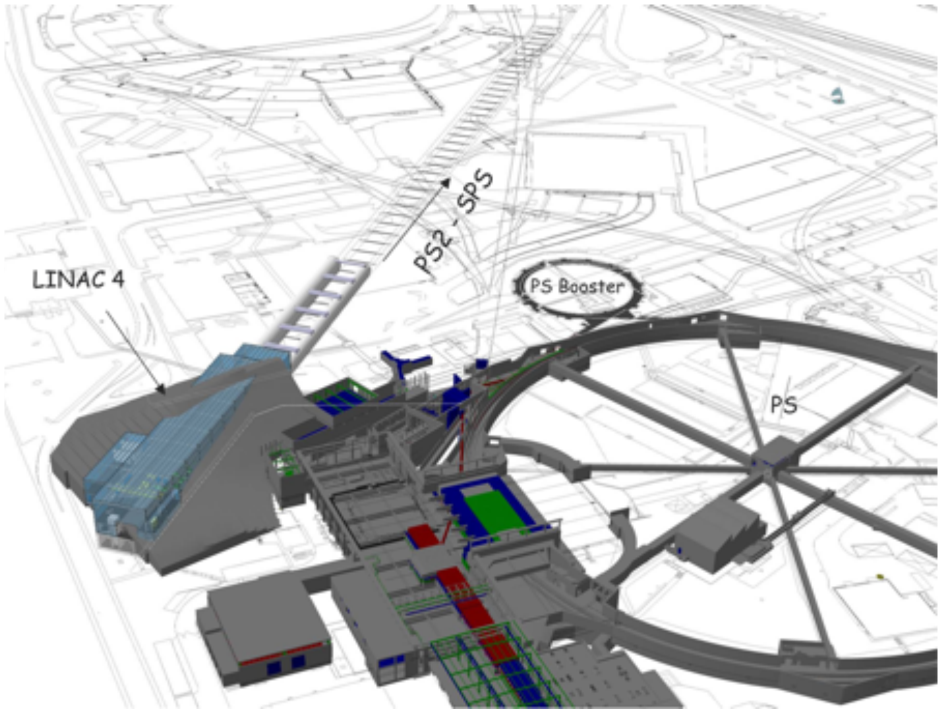
Luminosity evolution



- Most probably LHC will go for 50 ns collisions as it is <u>**less challenging option**</u>
- still ~200 pile-up events / crossing

CERN accelerator chain upgrade





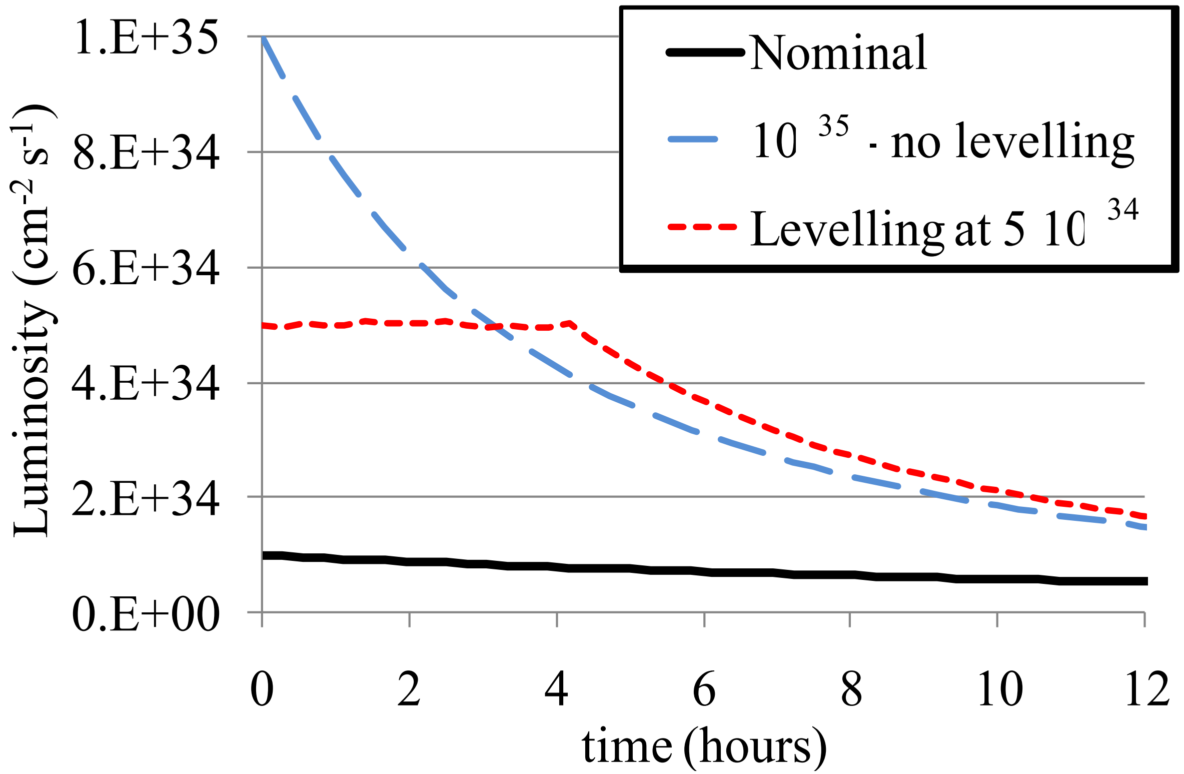
Linac2	50 MeV
Booster	1.4 GeV
PS	26 GeV
SPS	450 GeV

→

Linac4	160 MeV
SPL	4 GeV
PS2	50 GeV
SPS+	1 TeV

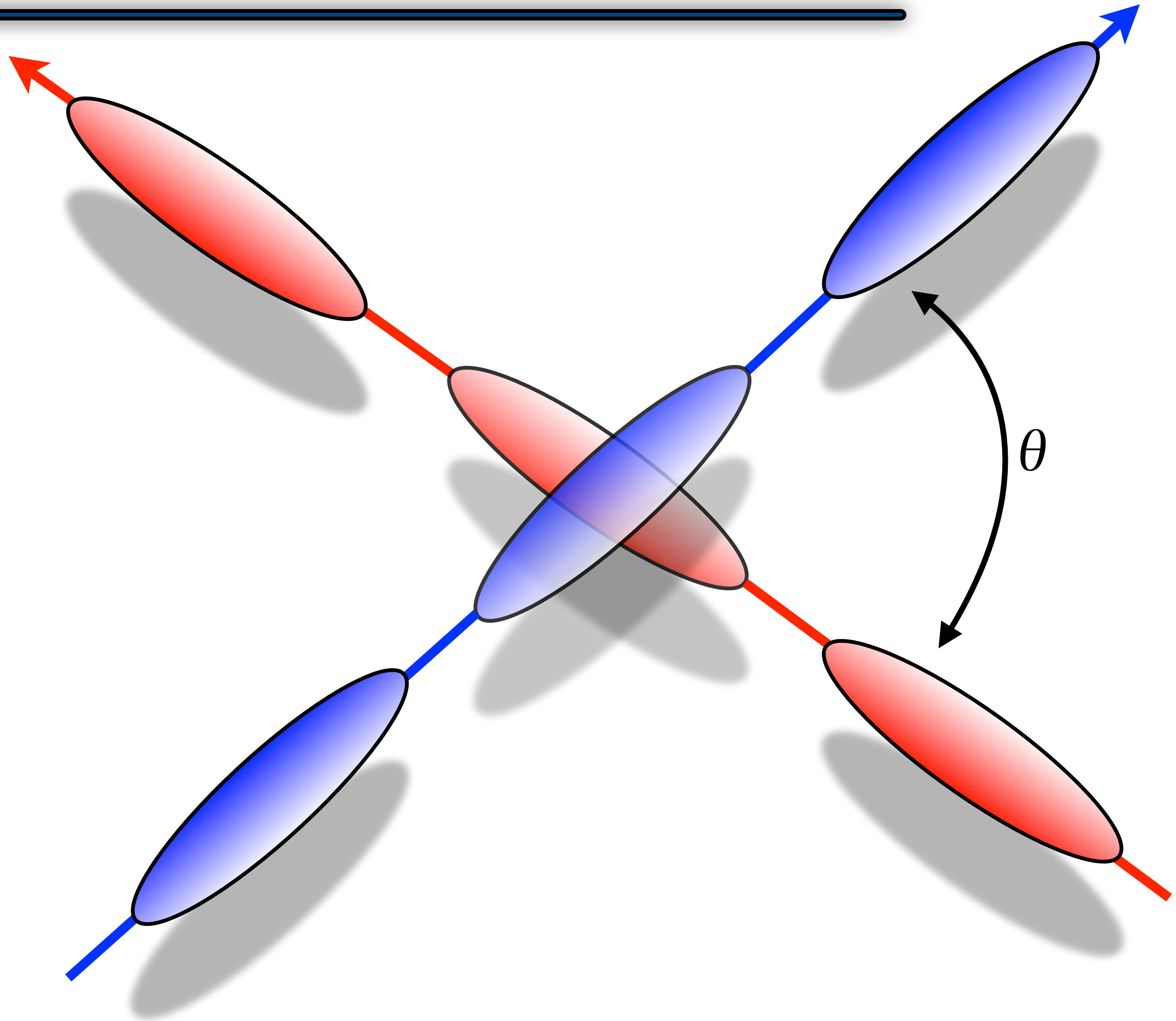
- **New injectors:** increased reliability and superior beam parameters
    - higher intensity beams, minimized turnaround times, increased flexibility

Luminosity levelling

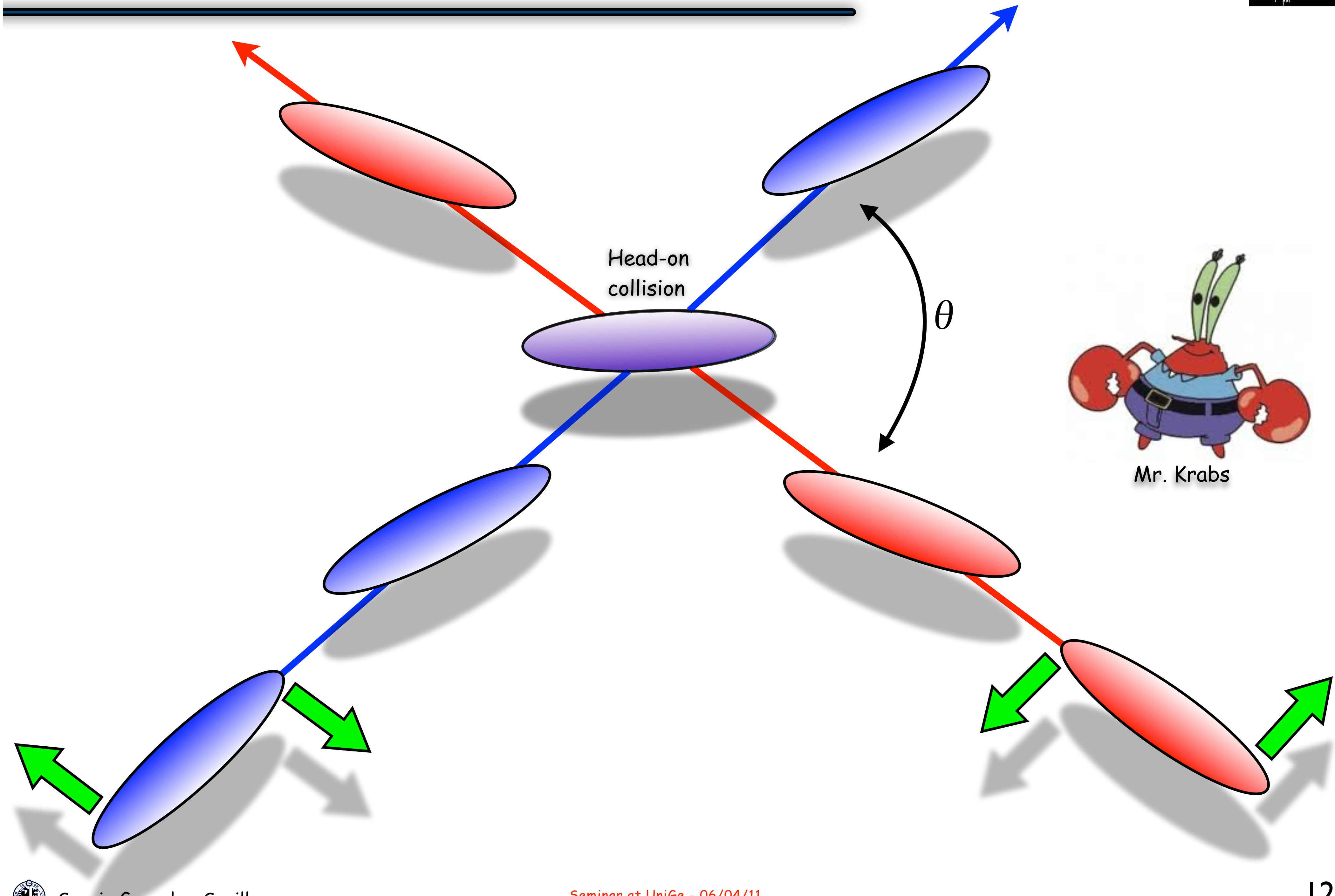


- ~3000 fb^{-1} total IL / 10-12 years ➡ ~250-300 fb^{-1} / year ➡ **~1 fb^{-1} / fill**
- Luminosity decay in storage rings dominated by parasitic effects
  - lifetime recovered with operational experience
  - HL-LHC: unavoidable luminosity decay due to proton burning in the luminous collisions
- **Luminosity levelling**
  - optimize data taking and minimize the required "over-design" of detectors and machine comp.
  - sustained 5×10^{34} $cm^{-2}s^{-1}$ while leveling for 3-5 hours + decay of few hours

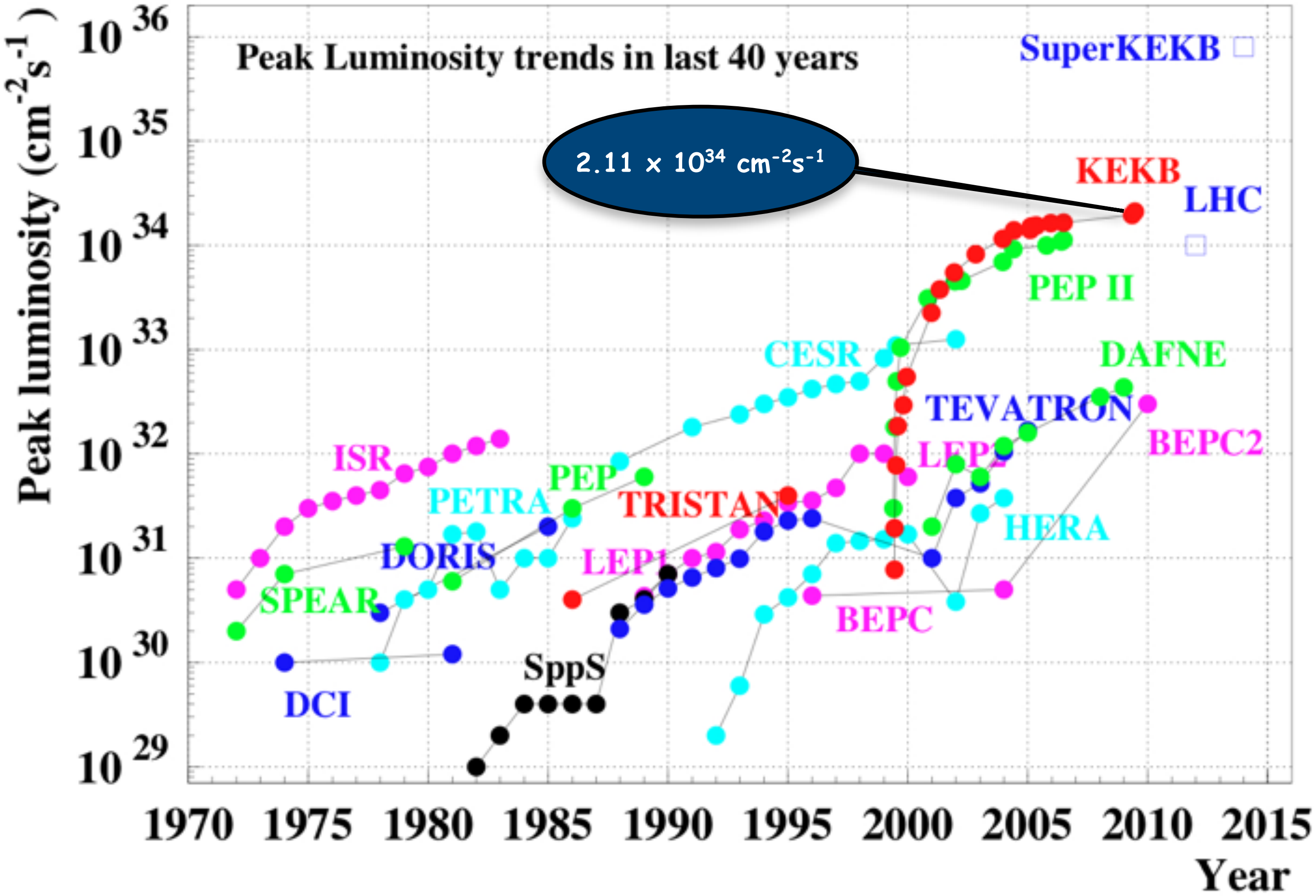
Colliding beams

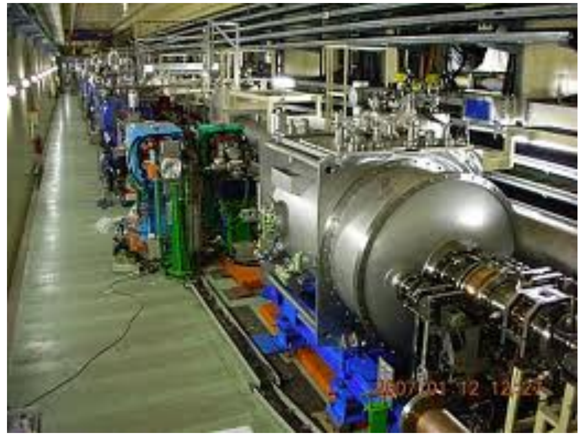


Crab crossing

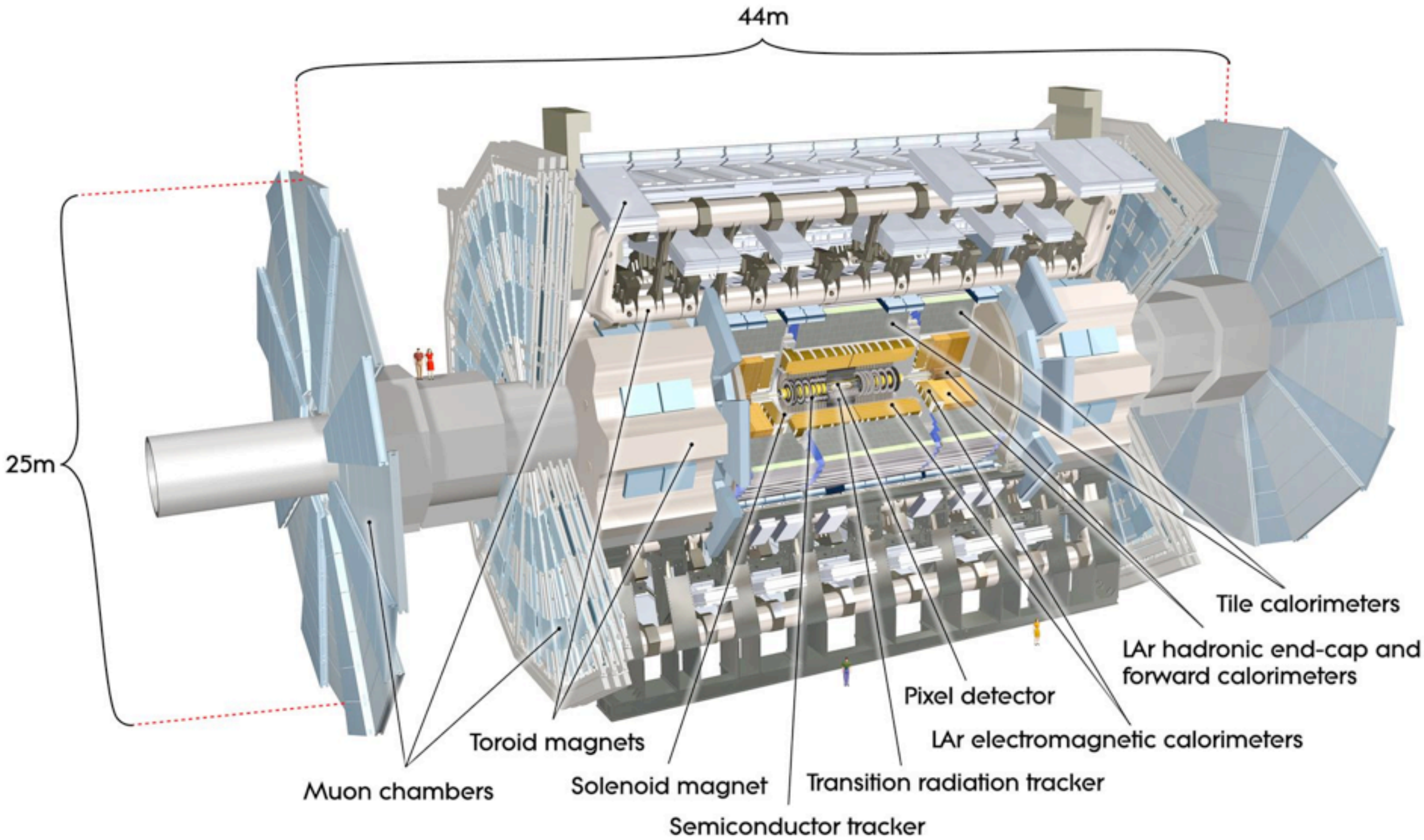


KEKB: world's luminosity record !!!





The ATLAS experiment

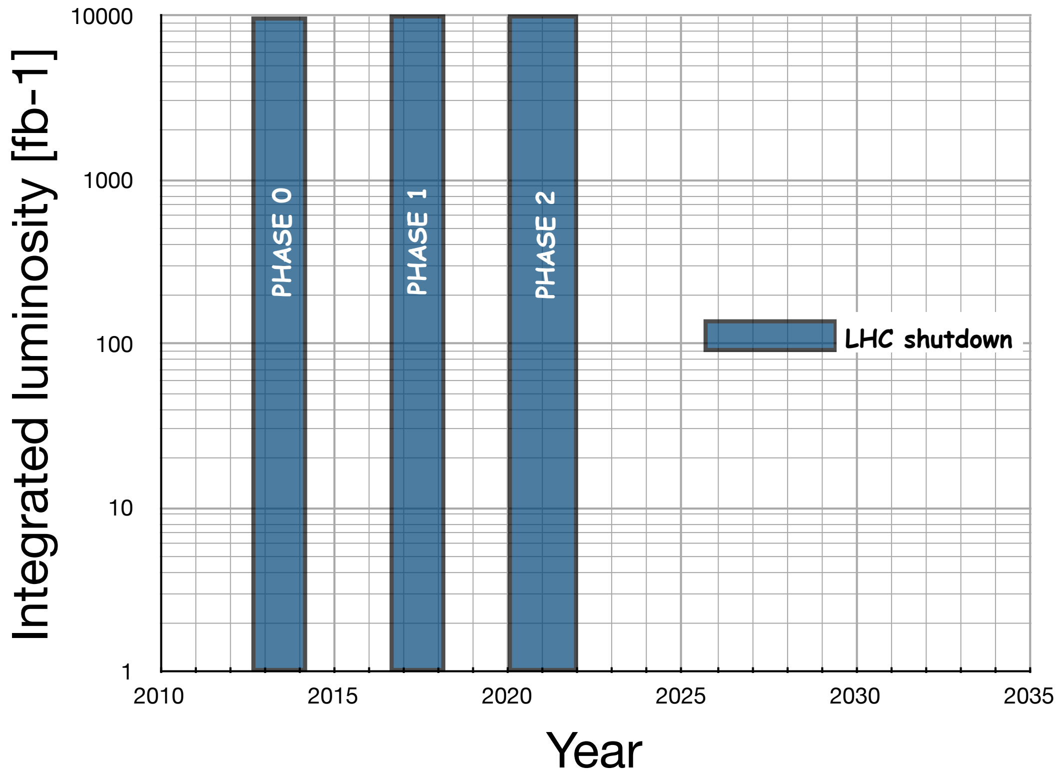


ATLAS upgrade schedule

- Phase 0 - 2013
  - instrument more muon trigger electronics
  - update pixel services and IBL

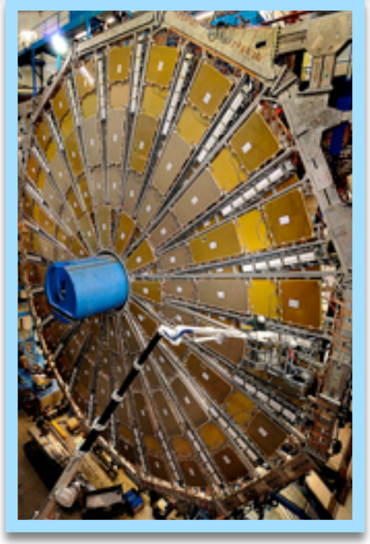
- Phase 1 - 2017
  - upgrade forward muon wheel
  - Topological trigger

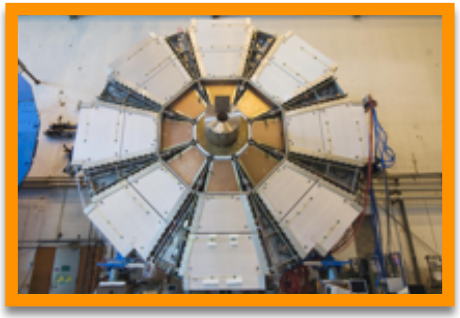
- Phase 2 - 2020
  - replace Inner Detector
  - L1 track trigger

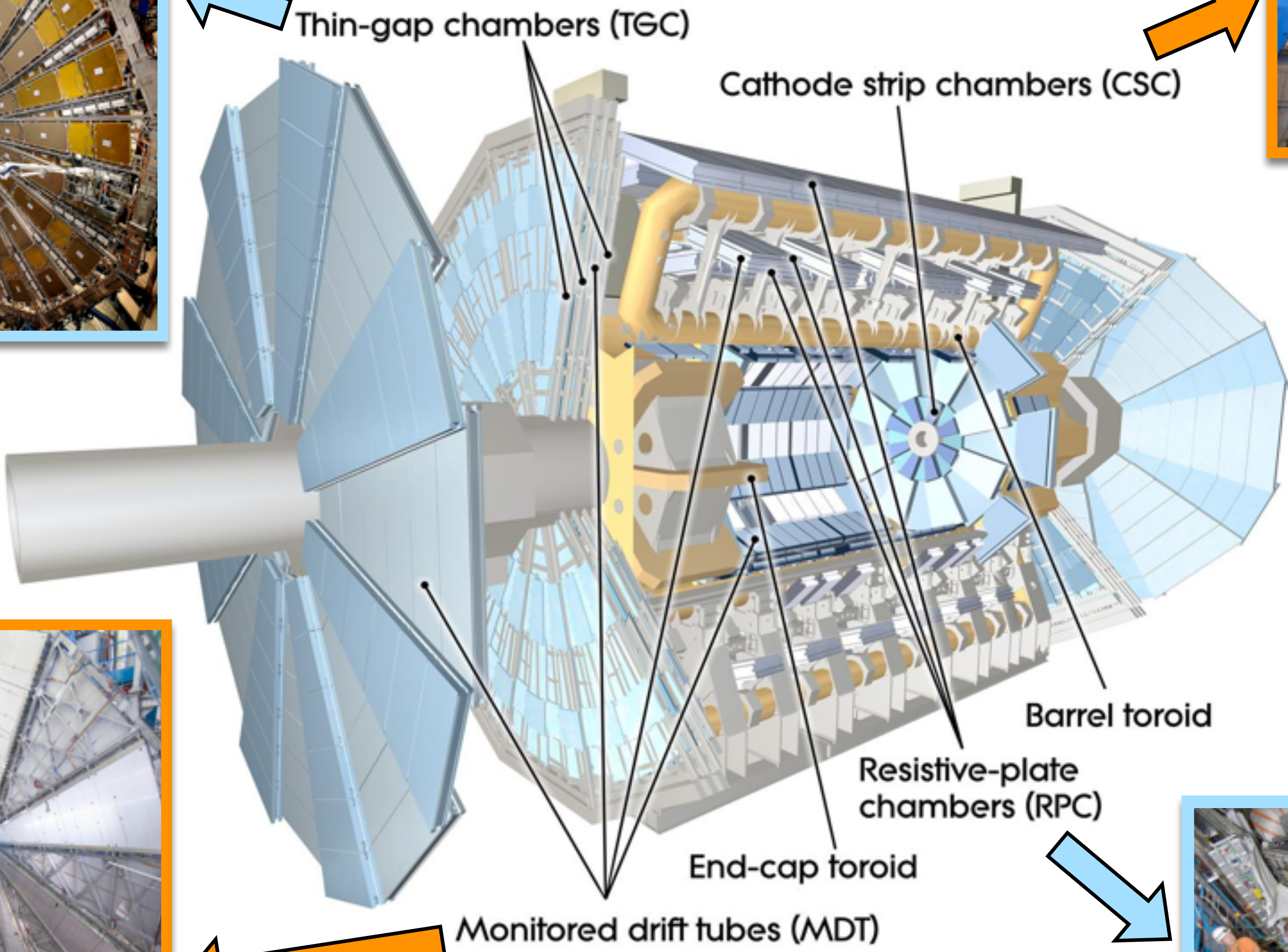


Muon Spectrometer

The ATLAS Muon Spectrometer



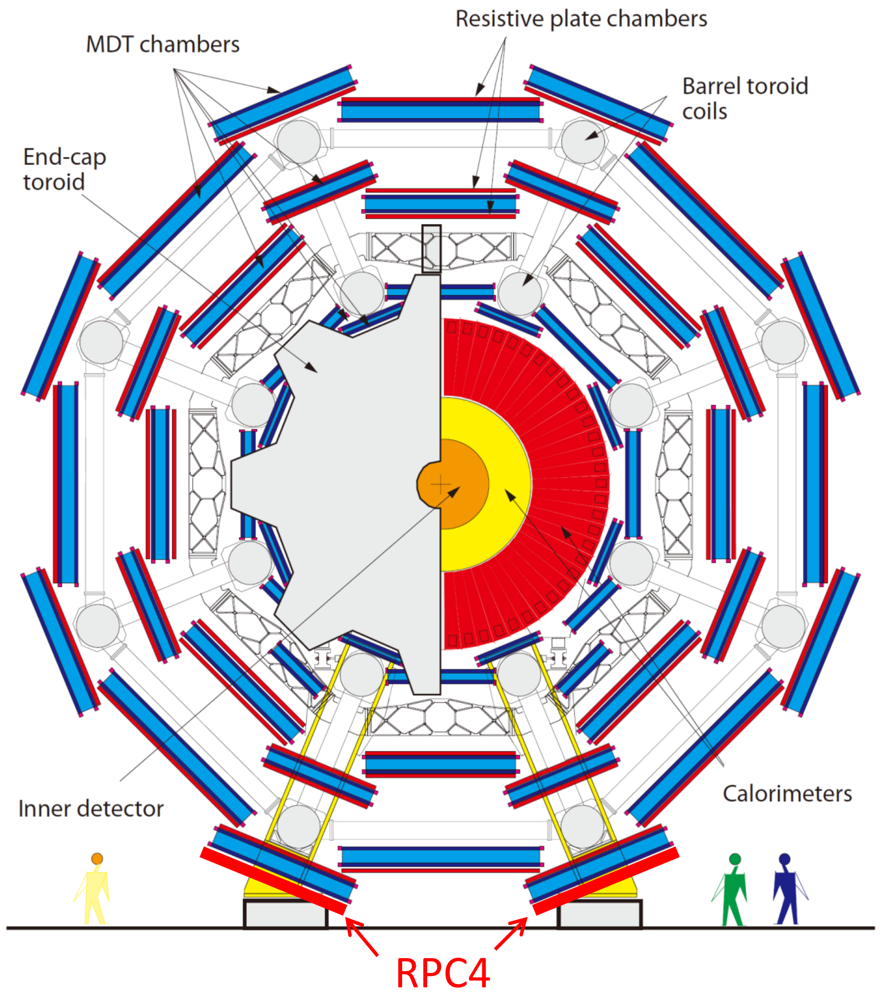




TRIGGER
- RPC
- TGC

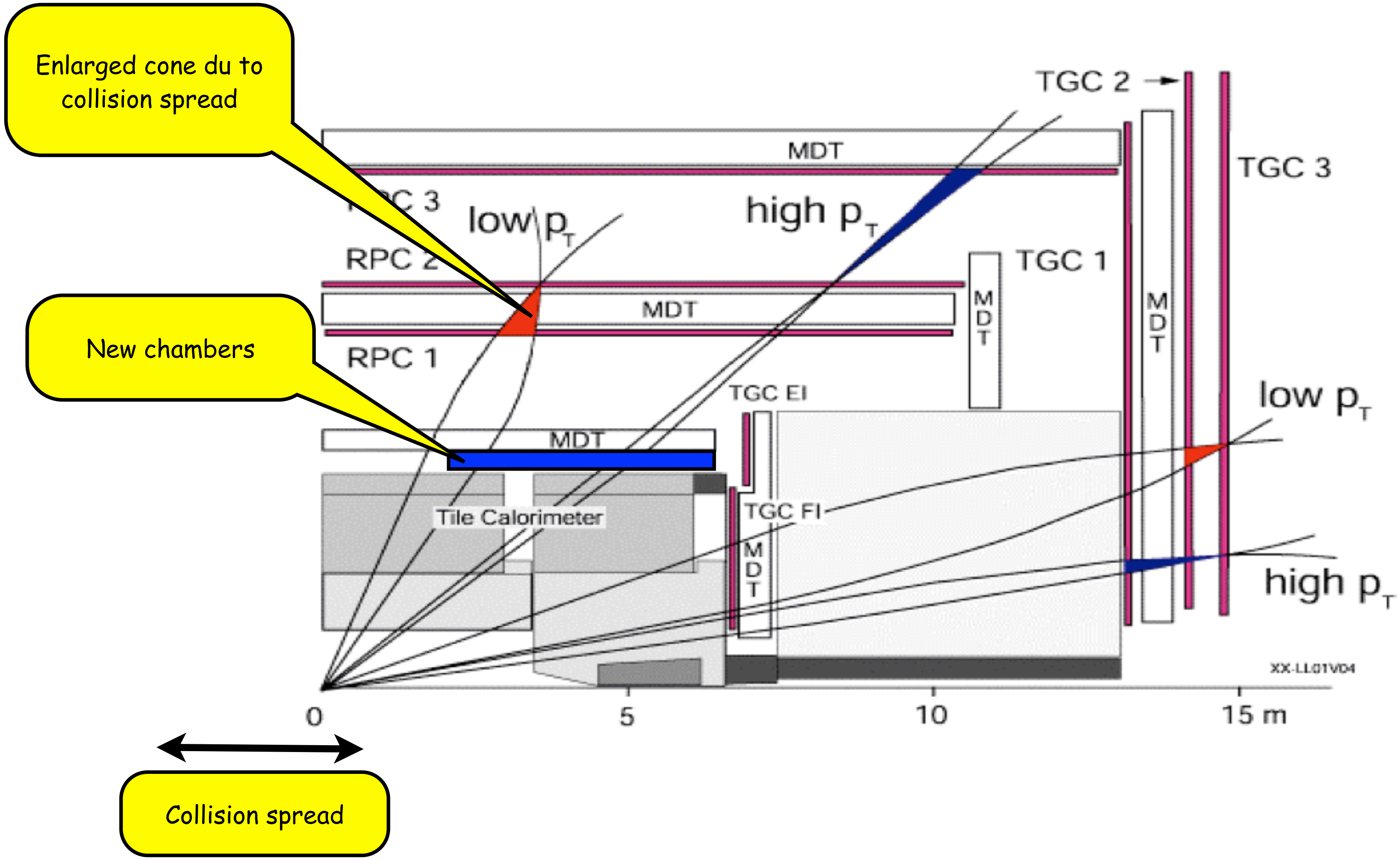
TRACKING
- MDT
- CSC

Muon trigger upgrade (barrel)



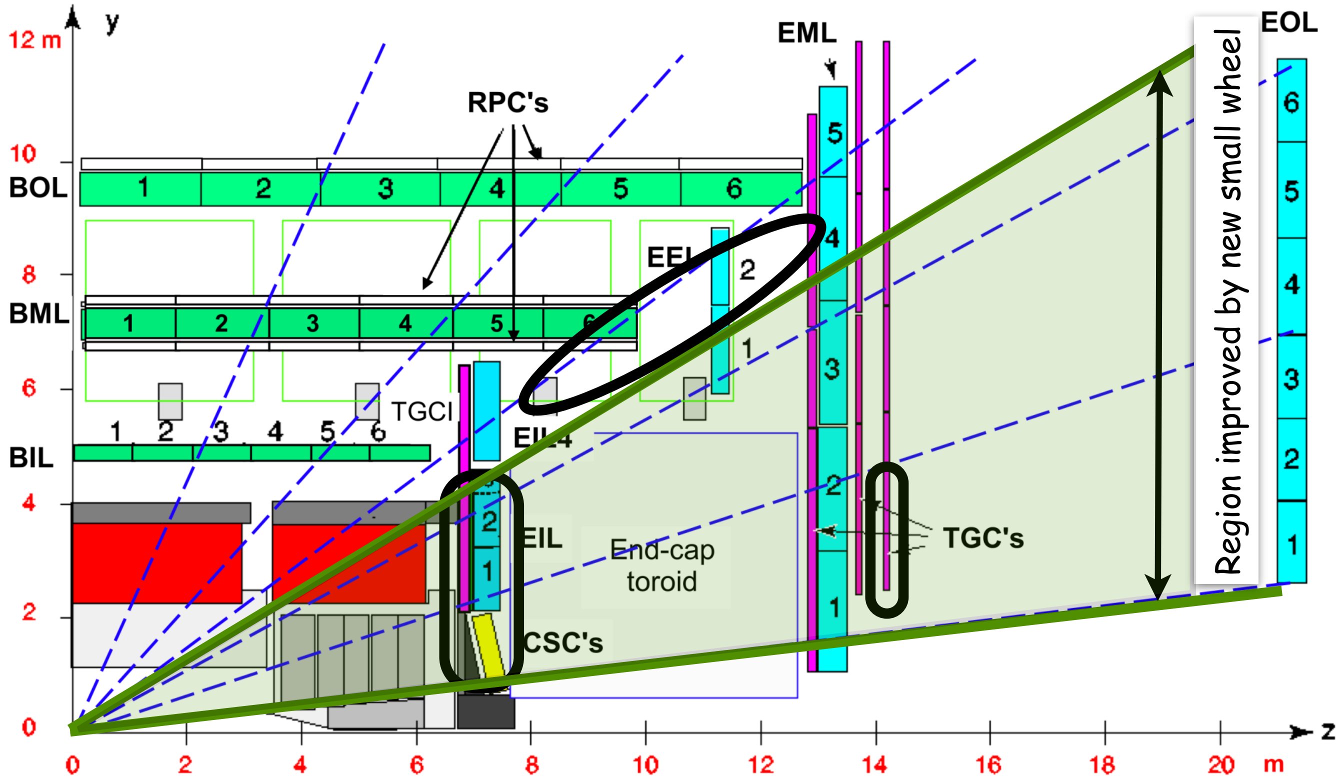
- LVL1 muon trigger efficiency in the feet sectors is lower than in standard sectors
- Installation of fourth layer of RPC chambers
- Upgrade of electronics on-going ➡ optical links, muon trigger logic upgrade...

Muon trigger upgrade (barrel)



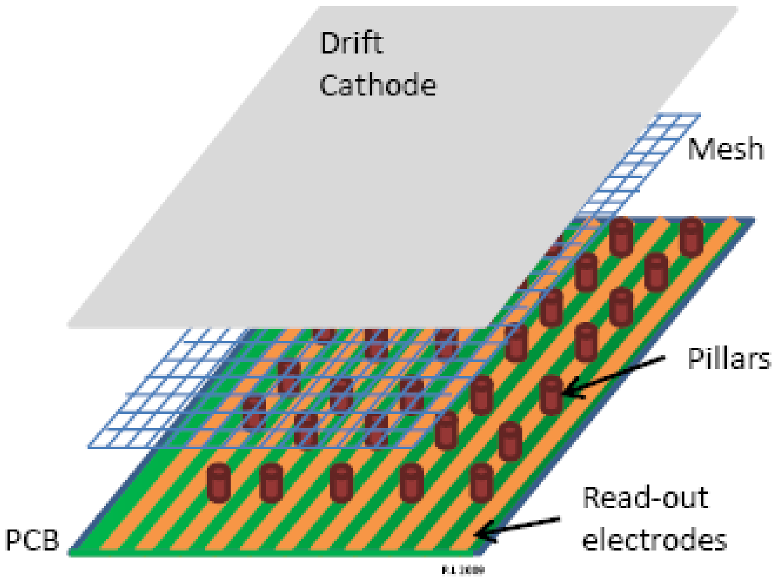
- RPC used for fast triggers
- Adding additional trigger chamber (RPC) to cancel the momentum error by collision spread on low p_T tracks

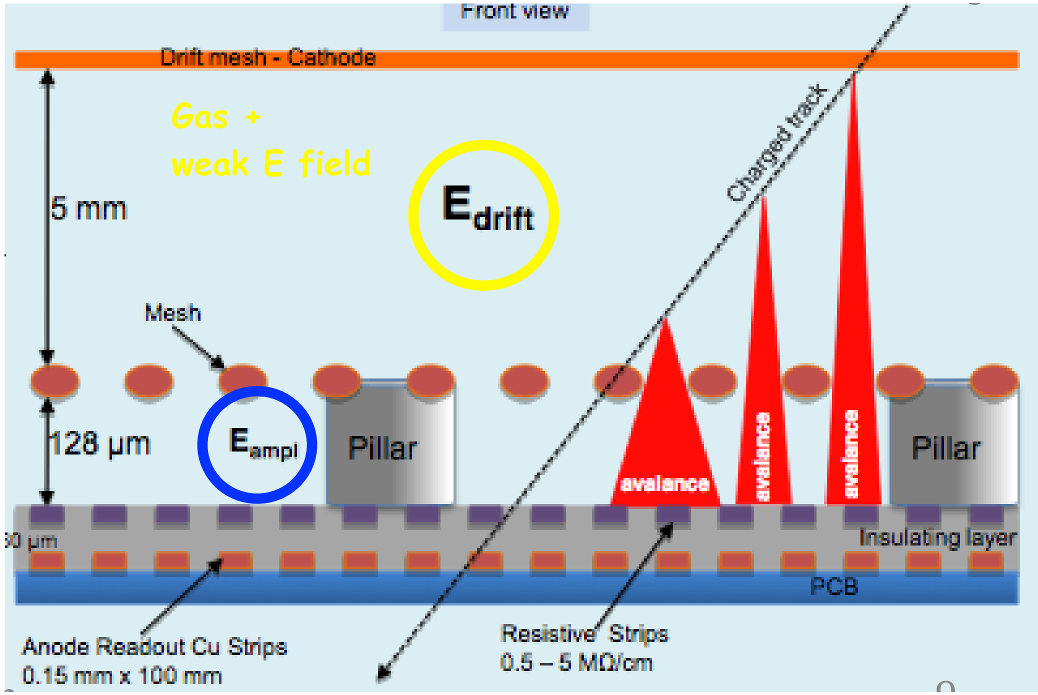
Muon trigger upgrade (end-cap)



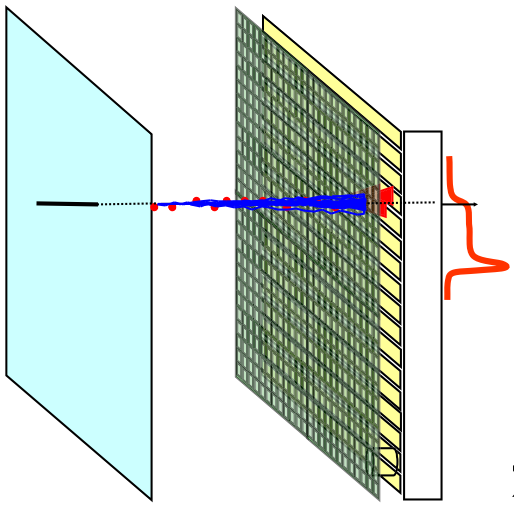
- Replace small wheel in end-cap regions ➡ control L1 rate without raising (much) thresholds
  - light and monolithic; several technologies under evaluation to provide L1 trigger
    - Homogenous wheel (i.e. one type of stations) if possible
    - Integrated stations if separate trigger and precision chambers used
- Possibly additional chambers in overlap region
- Very forward chambers for higher resolution and rate capabilities

MicroMegas



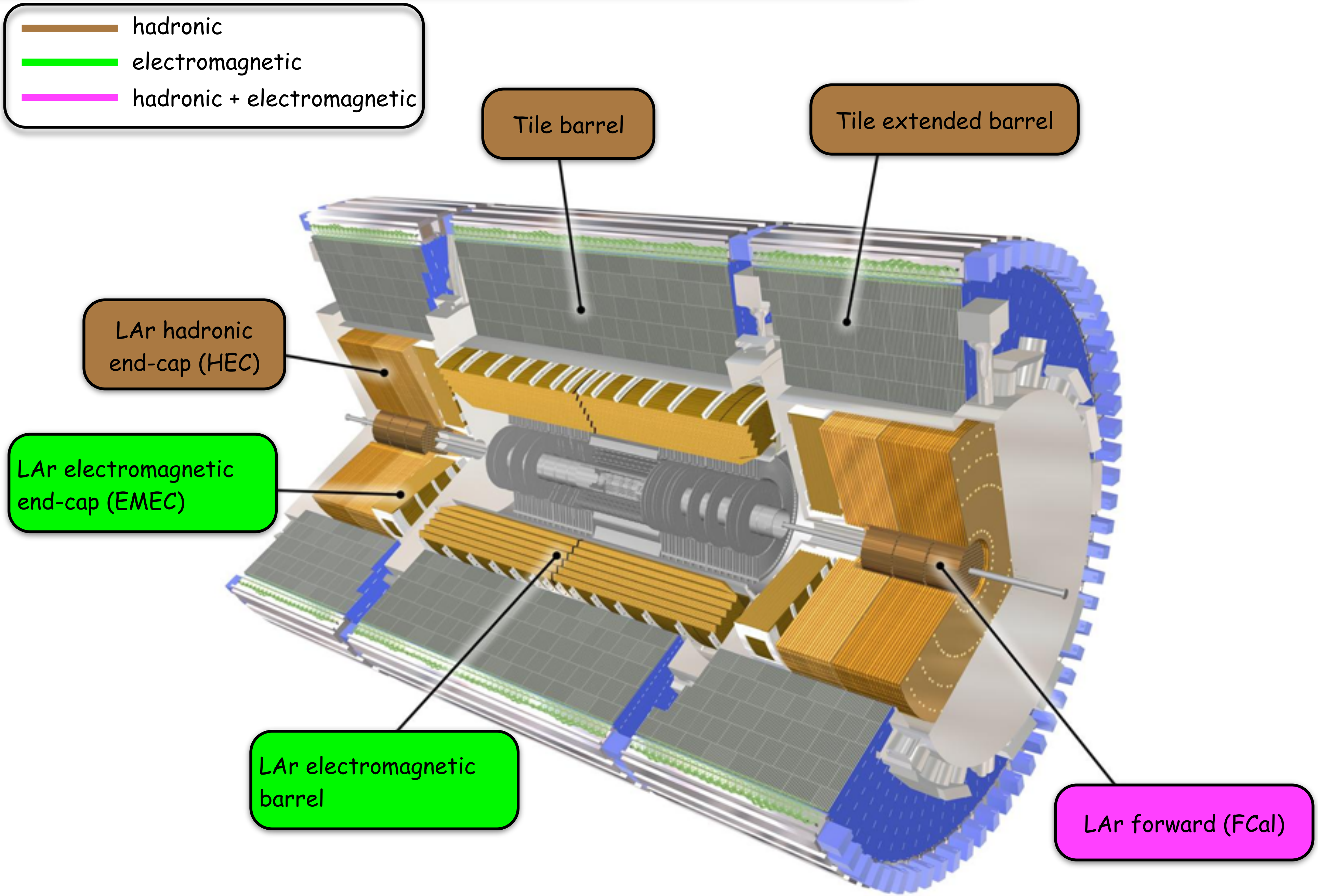


- Technology candidate for chambers with highest rates
- MicroMegas (**MicroMesh Gaseous Structure**): **combination of triggering and tracking functions**
- Matches expected performance
  - spatial resolution < 100 μm
  - time resolution ~ 5 ns
  - efficiency > 98%
  - rate capability > 5 kHz / cm^2
- Potential for large area detector (2 m^2) with industrial process



Calorimetry

ATLAS Calorimetry system



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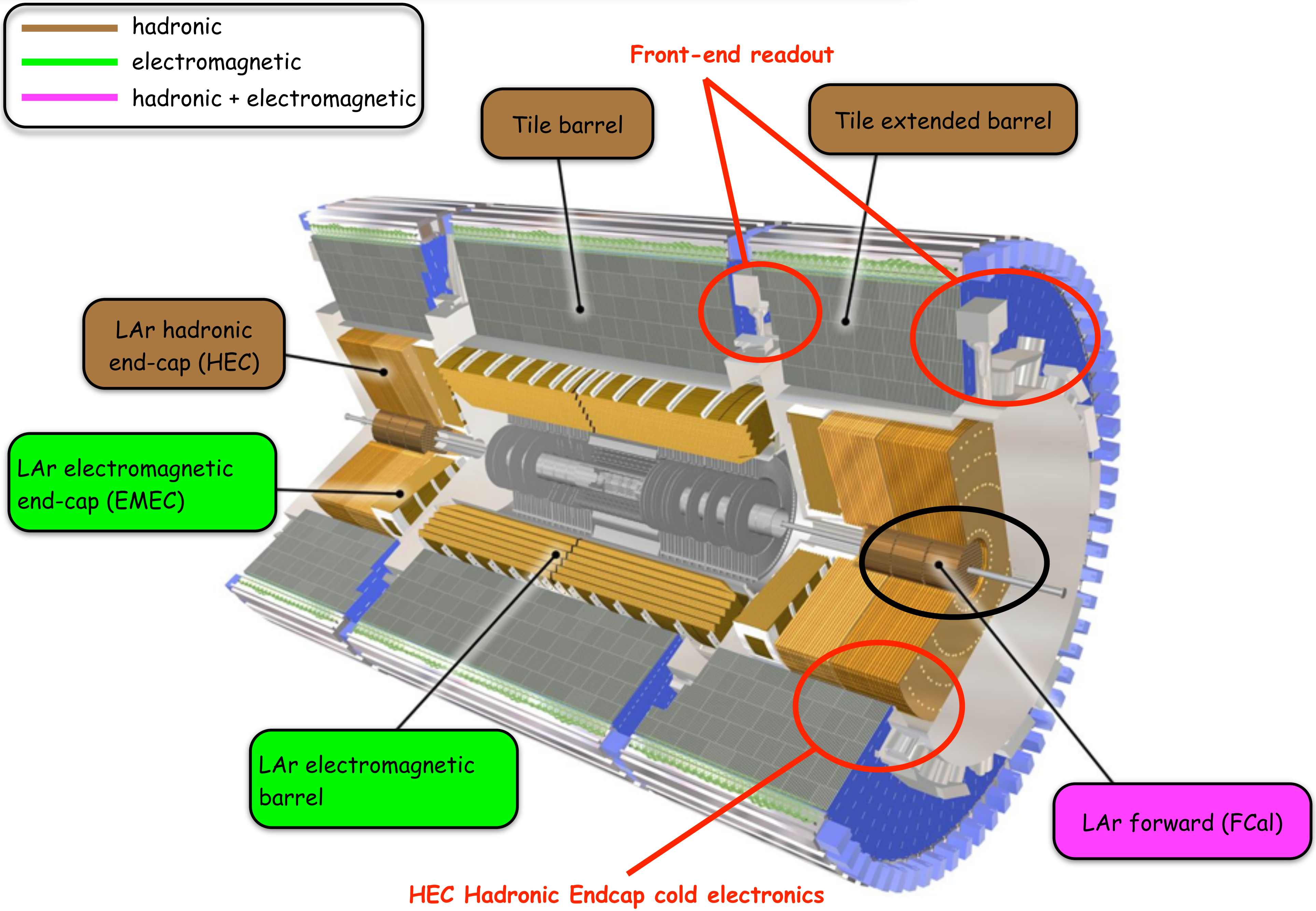
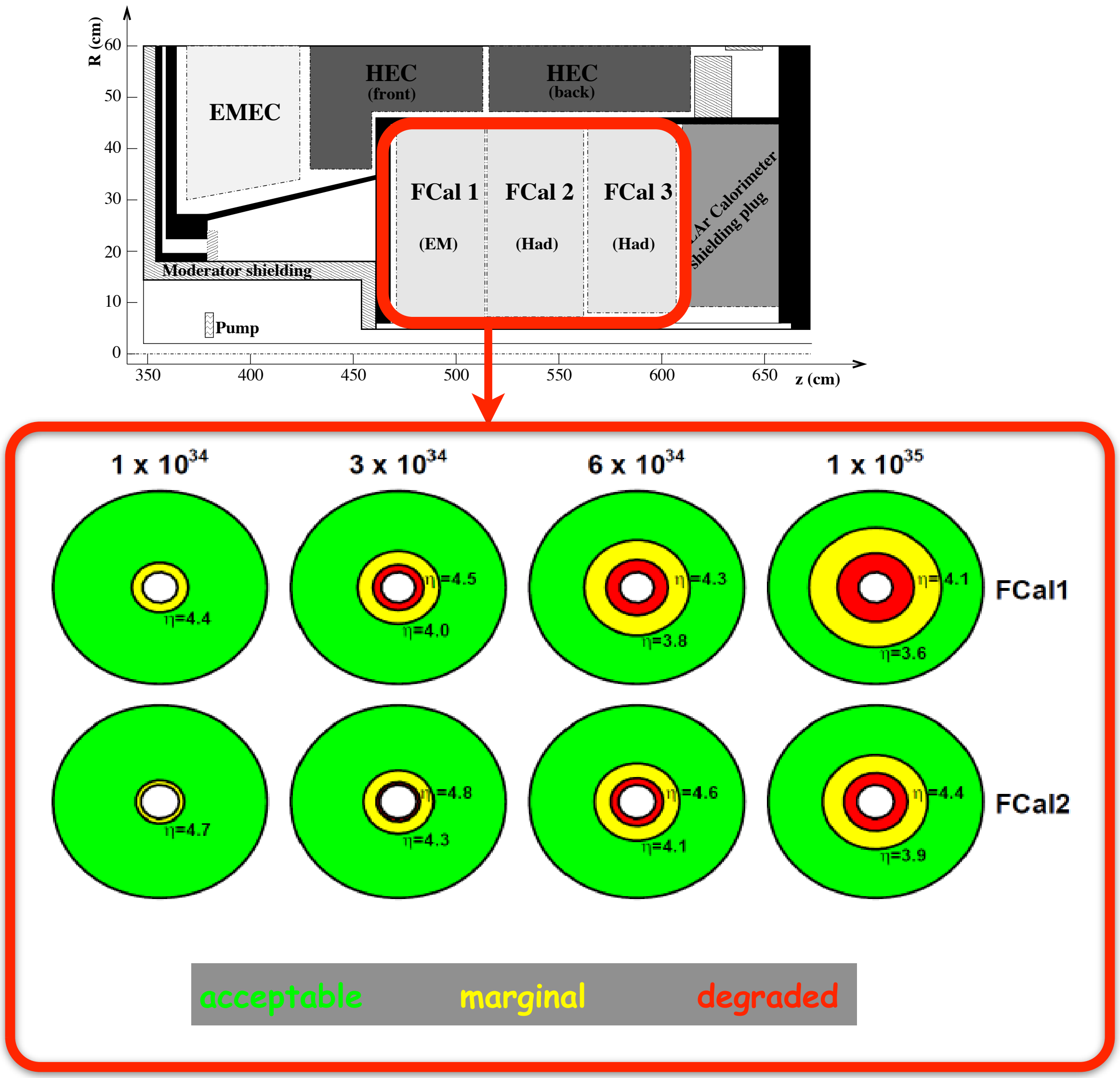
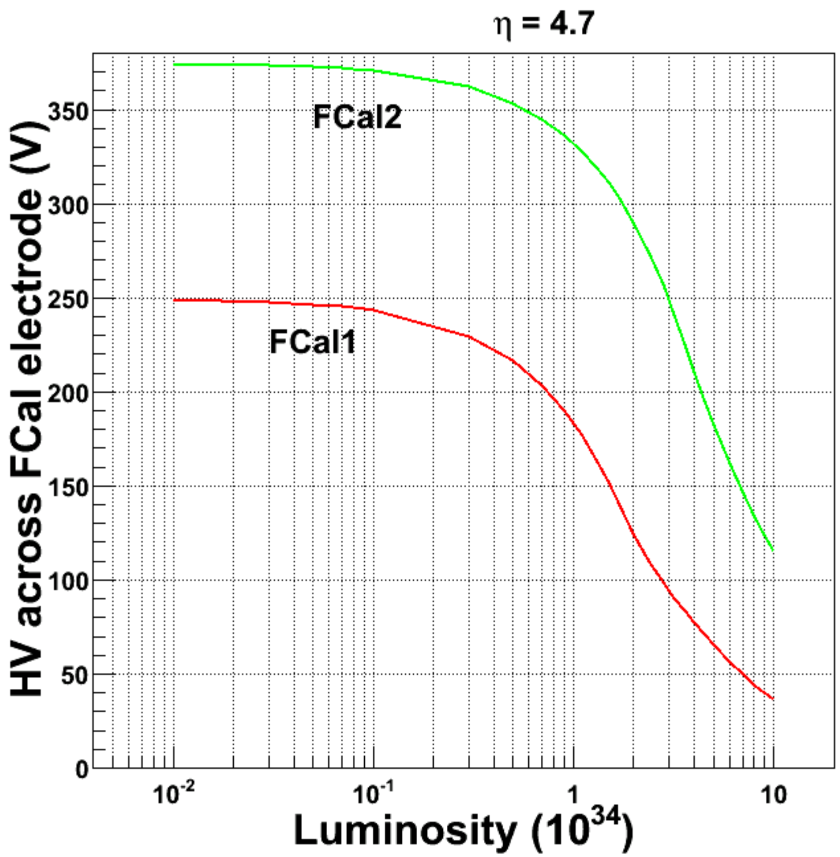


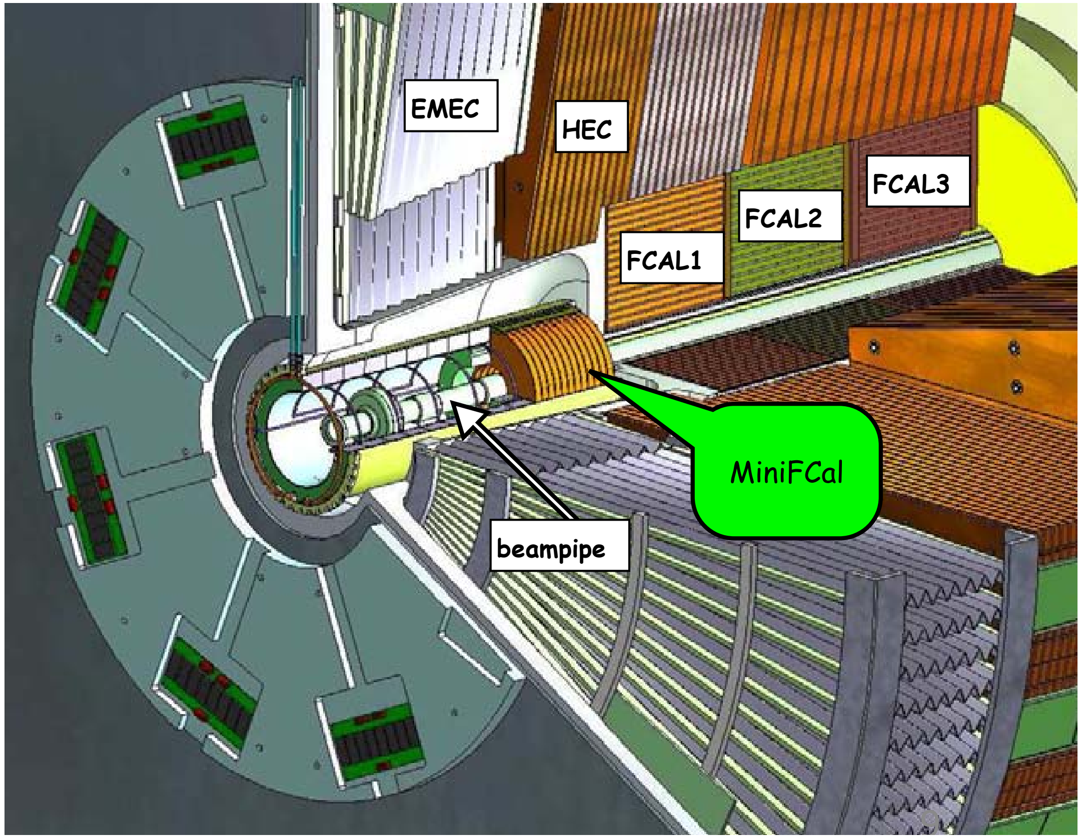
LAr forward calorimeter: issues

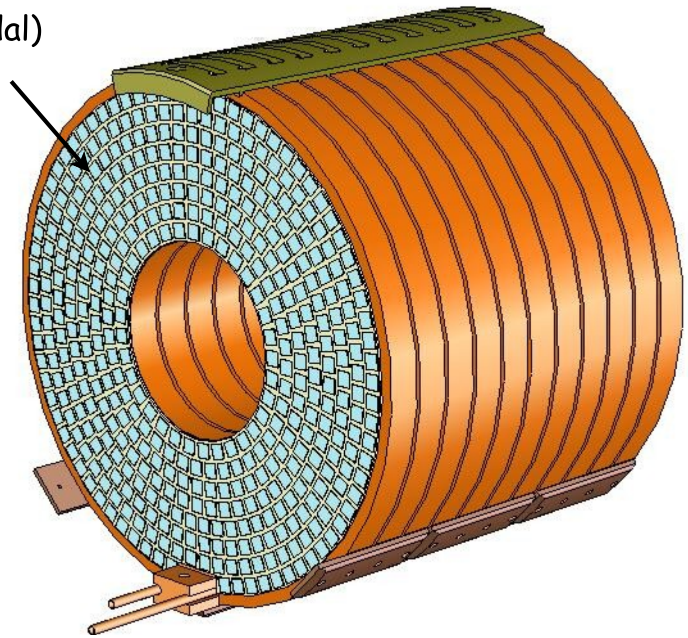
- The LAr FCAL coverage : $3.1 < |\eta| < 4.9$ ➡ **very high particle fluxes**
  - dE/dx beam heating of LAr ➡ **boiling ???**
  - Ar^+ ion build-up and (fluctuating) voltage drop across HV resistors will deteriorate performance





Warm forward calorimeter





- Design a new re-optimized FCal1 with smaller gaps ➡ long installation (~1 year)
- <u>**New warm mini-FCAL**</u> ➡ favoured solution
  - installation without opening cryostat; integration of existing LAr services can be "accomodated"
  - provides calorimetry and <u>**shields current FCal**</u> (though more diffuse and spread-out showers)
  - 12 Cu absorber plates + 11 detector plates
  - Major current uncertainties:
    - radiation hard detector technology

Trigger

Current ATLAS trigger system

LEVEL 1 (L1) ➡ <75 kHz

- hardware based
  - 2.5 μs max latency
  - fast custom-built electronics
  - inputs mainly from Calorimeter and Muon Spectrometer
  - defines Regions Of Interest (RoI)
  - inputs combined in Central Trigger Processor

LEVEL 2 (L2) ➡ ~3 kHz

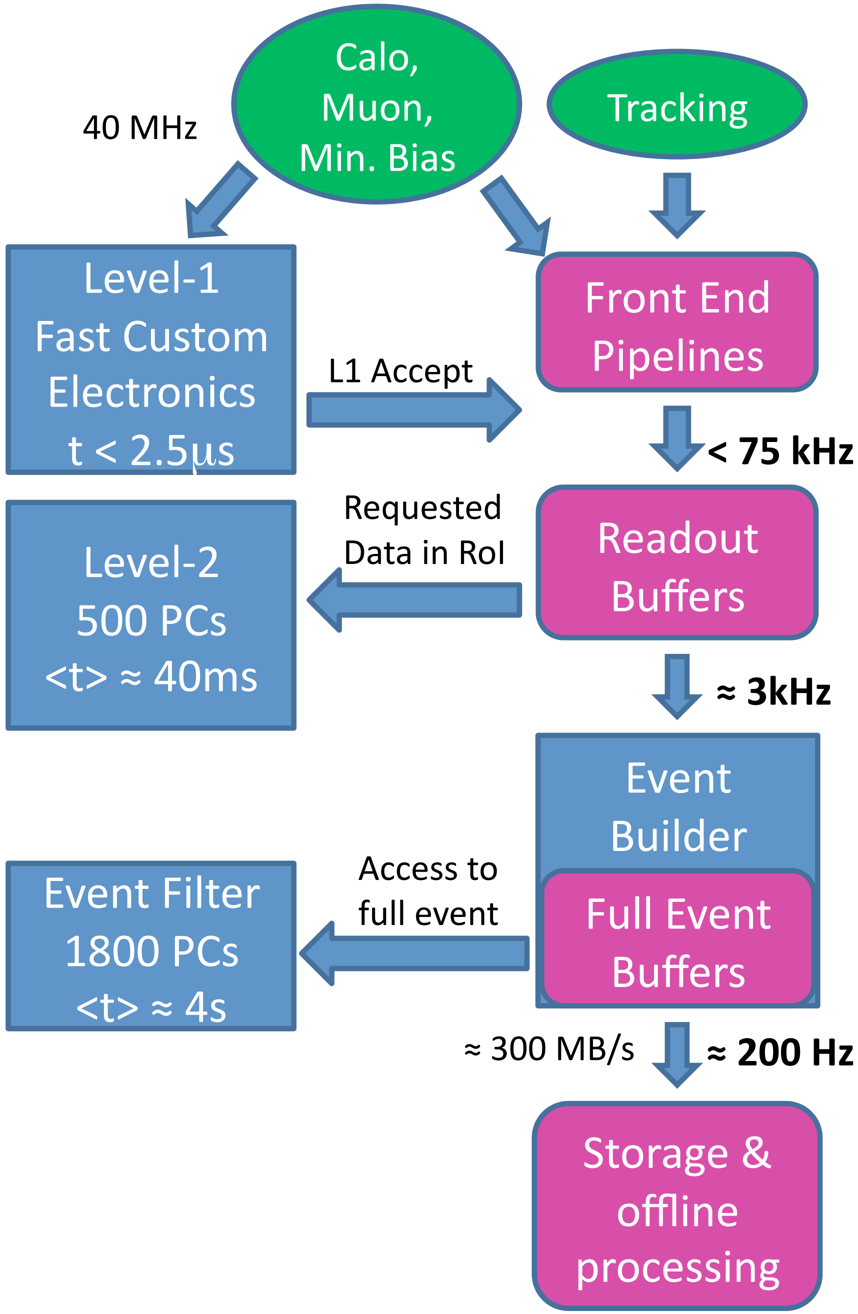
- PC farms, software based
  - 40 ms mean processing time
  - fast custom algorithms
  - Inner Detector / Calo track matching
  - access to full granularity data within an RoI

HLT

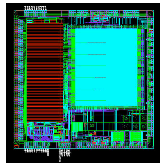
EVENT FILTER (EF) ➡ ~200 Hz

- PC farms, software based
  - 4 s mean processing time
  - adapted offline reconstructions algorithms for physics signatures
  - refines LVL2 selection
  - access to full event information, complete calibration and alignment data

Overall recording rate ~200 Hz



L1Calo



- Current ATLAS trigger
  - no track information at L1
  - L1 rate < 75 kHz
- For HL-LHC the goal is to maintain the present trigger rate
  - (phase-2) new L0 trigger 500 kHz but longer latency
    - pipeline of L0 to extend L1 further

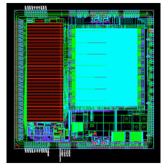
- L1Calo
  - Phase-1: limited to current analog trigger granularity and resolution
    - EM/hadron little room for improvement
  - Phase-2: full digital calorimeter readout
    - better EM/hadron ID with access to full granularity
      - longitudinal shower profile

- Topological processing
  - reduce rates while saving physics efficiency
    - current triggers are multiplicity based
    - raise thresholds impacts physics
  - keep present granularity: jet, em/τ cluster algorithms

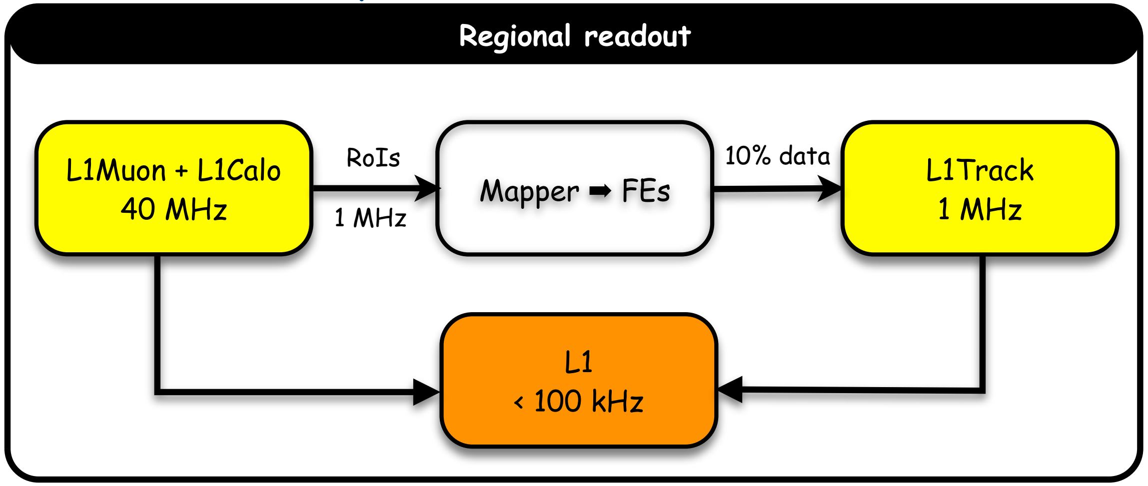
Motivations for a track trigger

- From current L2, **track matching** to Calo or Muon objects **is key for L2 rate reduction**
  - a track trigger ➡ needed extra flexibility and redundancy (i.e. robustness) to L1
    - z_0 matching for multiple trigger signatures
    - track-based isolation perhaps vital for $e/\mu/\tau$ triggers at ~10^{35}
- Track-trigger considerations:
  - not necessary to use layers close to the beamline
  - mainly looking for high p_T (> ~10 GeV/c) tracks
    - pattern recognition easier/faster
    - modest track parameter resolutions are sufficient
  - increase in tracker material should be small
- Readout portions of tracker at L0
- Input into L1 trigger

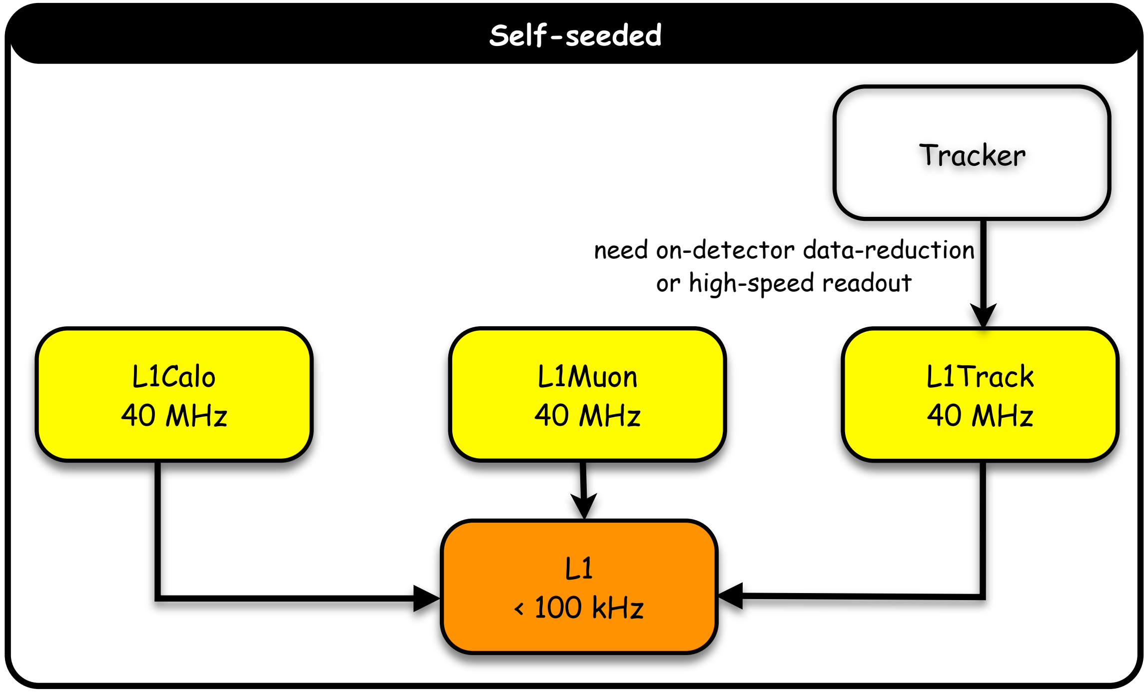
Track trigger: approaches



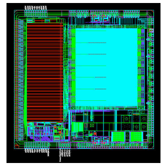
- **Regional readout:** seeded by L1Calo or L1Muon information



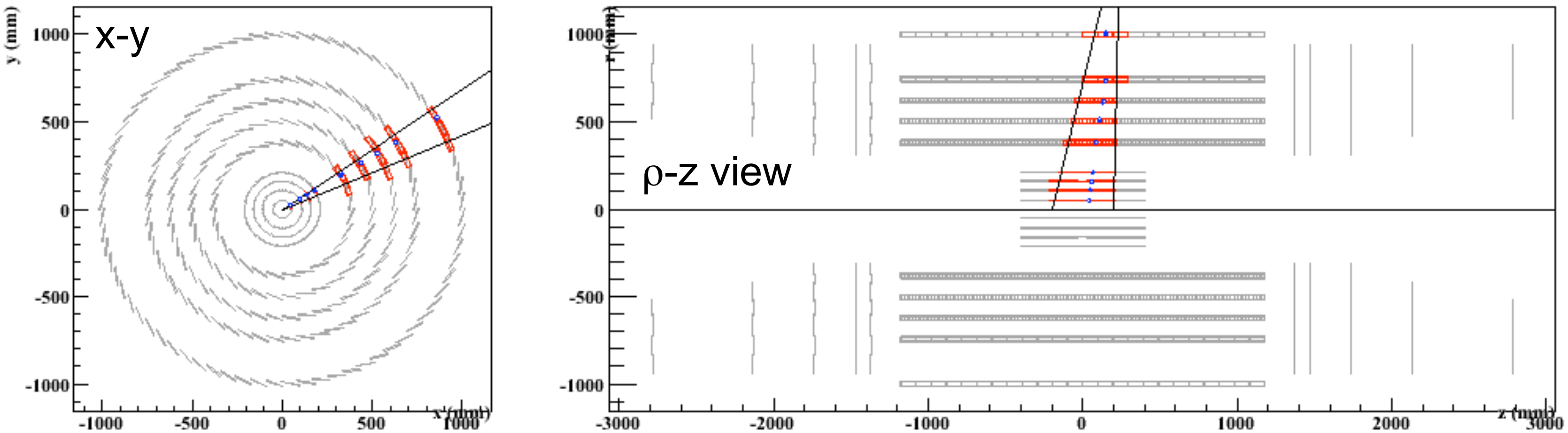
- **Self-seeded:** dedicated tracker layers select hits from high p_T tracks

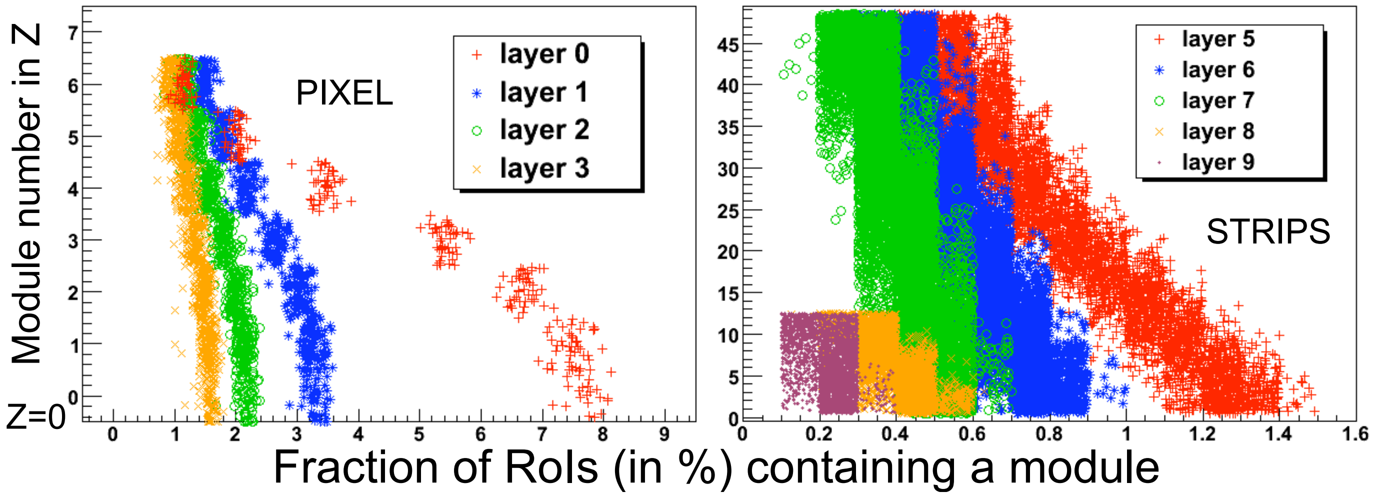


Track trigger: regional readout



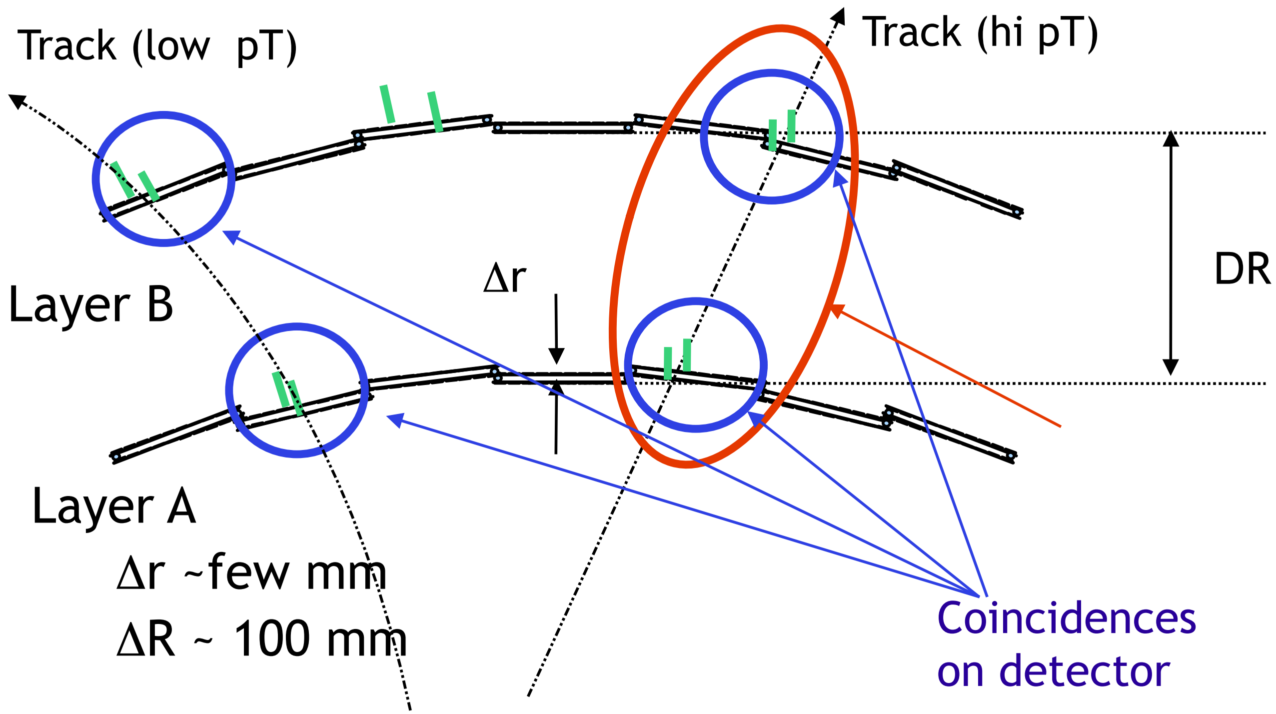
- L1Calo/L1Muon: from 40 MHz to ~1 MHz
- Identification of few RoIs & send readout request to tracker modules inside RoIs
  - a typical lepton RoI contains ~1% of the tracker modules
    - wider in z near beamline to account for spread in the interaction region
    - central module in layers near the beamline are more frequently inside an RoI





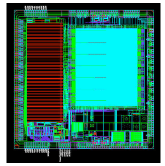
Track trigger: self-seeded

- Tracking contributes to L1 decision without seeding from Calo/Muons
- A number of strip layers are equipped with trigger functionality to give an efficient trigger with built-in redundancy
- Bandwith is the main issue (**raw data ~ 200 Gb/module/BC**)
  - co-incidence between module sides
  - low-mass, low-power and faster readout links
  - fast off-detector track-finding

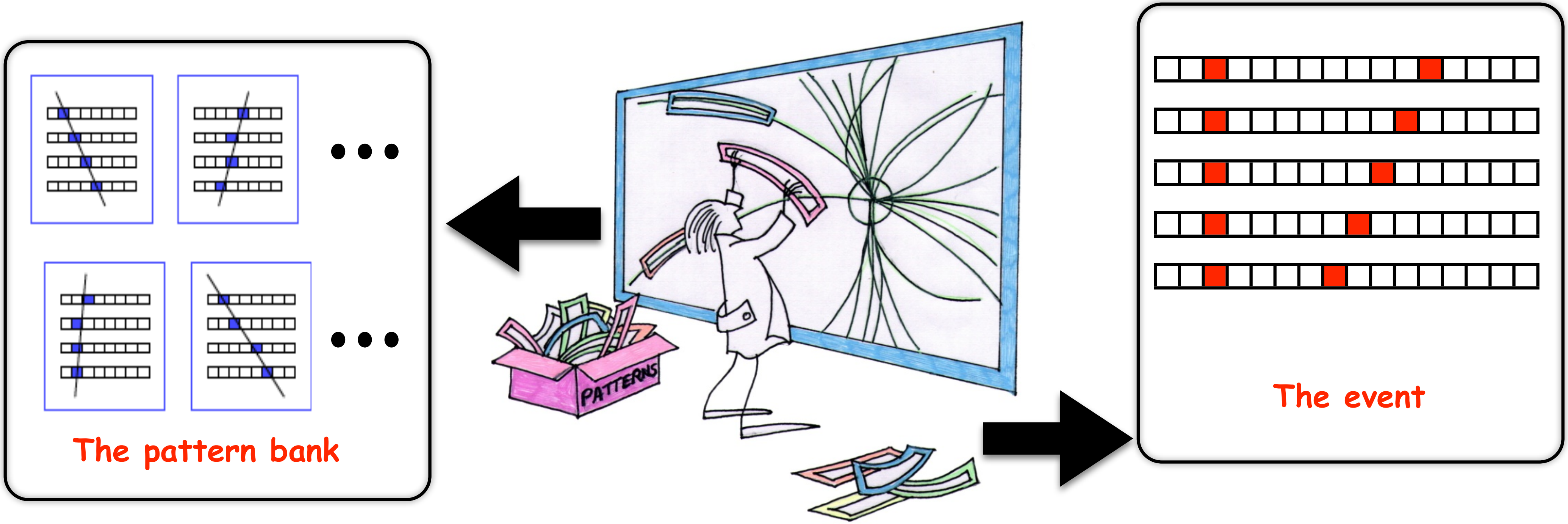


Barrel cross-section

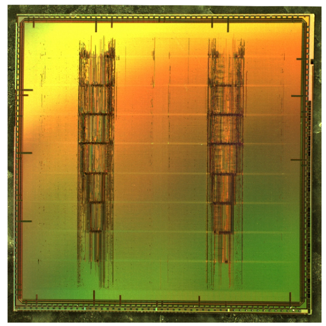
Hardware track finder



- Fast tracker (FTK)
  - dedicated hardware for on-line pattern recognition
  - high quality track reconstruction at high event rates (L1 output)

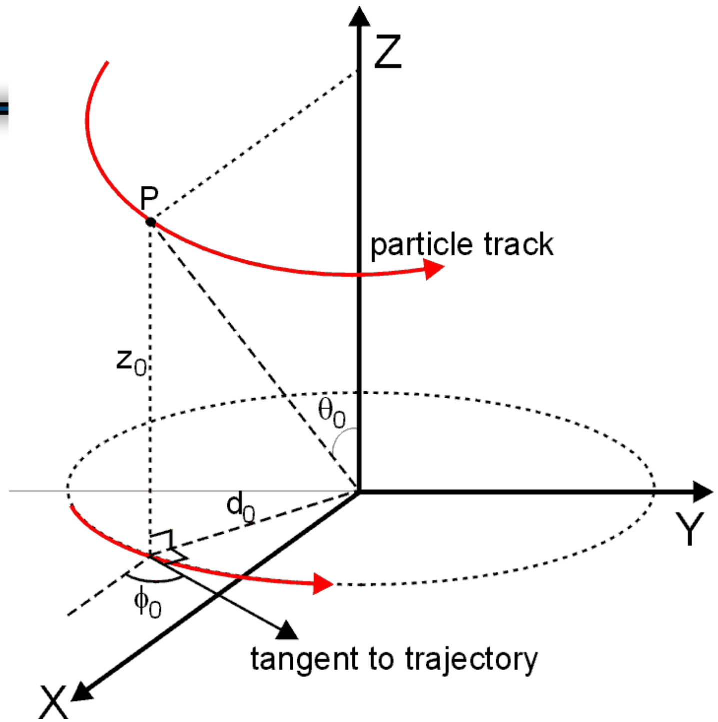


- Pattern recognition
  - find track candidates with enough silicon hits
  - 10^9 stored patterns (roads)
  - based on the Associative Memory chip (content-addressable memory or CAM)
    - initially developed for the CDF Silicon Vertex Trigger (SVT)

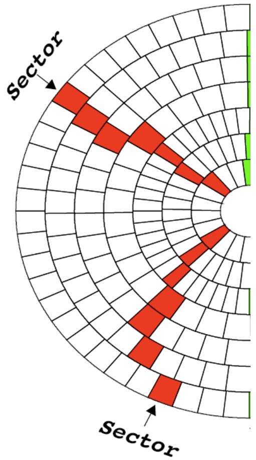


Track fitting

- Track parameters at the perigee
  - perigee = point of closest approach to the Z-axis
  - d_0: transverse impact parameter
  - z_0: longitudinal impact parameter
  - ϕ_0: azimuthal angle
  - θ_0: polar angle
  - q/p: charge over momentum



- Track fitting:
  - within all hit combinations in a road, find the physical track and compute its parameters
  - charge particle in a uniform B-field ➡ helix
  - over a narrow region, equations are linear in local hit coordinates ➡ excellent resolutions



helix paramaters and χ^2 components

hit coordinates in silicon layers

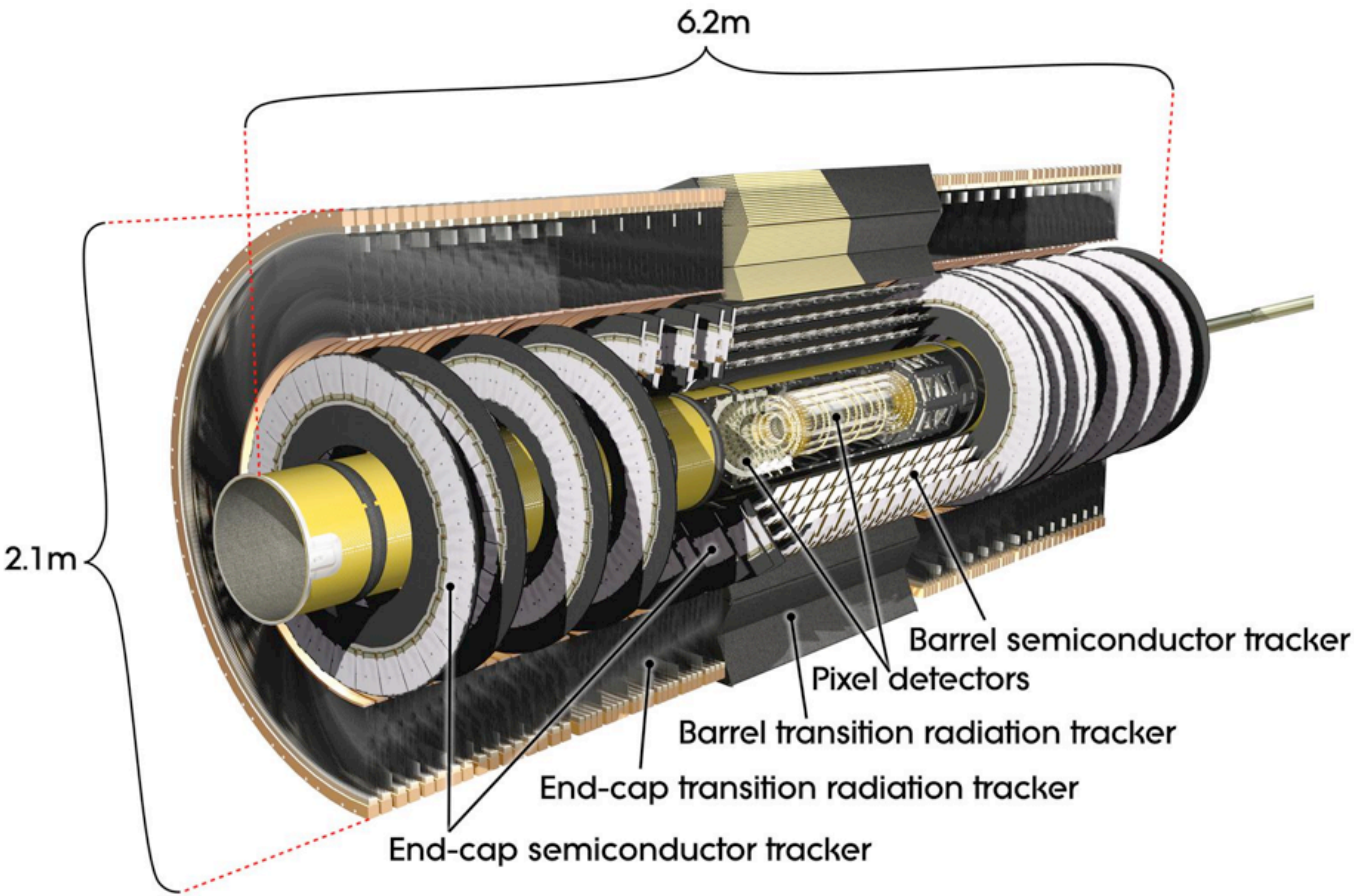
$$p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$$

pre-stored constants (full sim or real data)

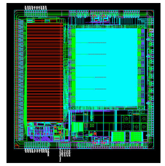
Implementation in FPGAs ➡ VERY FAST !!!

Inner Tracker

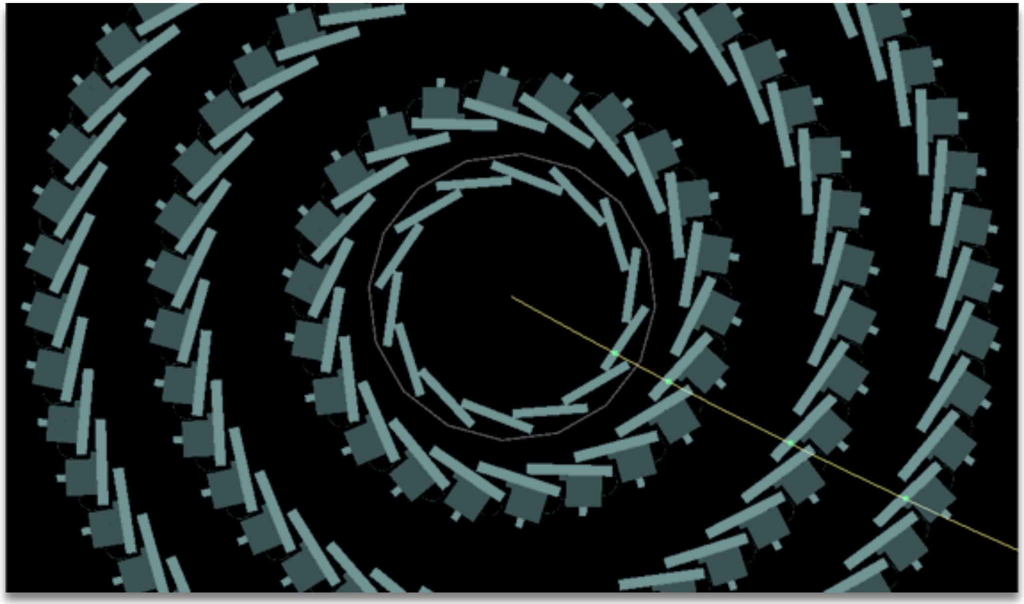
The Inner Detector (ATLAS internal tracker)

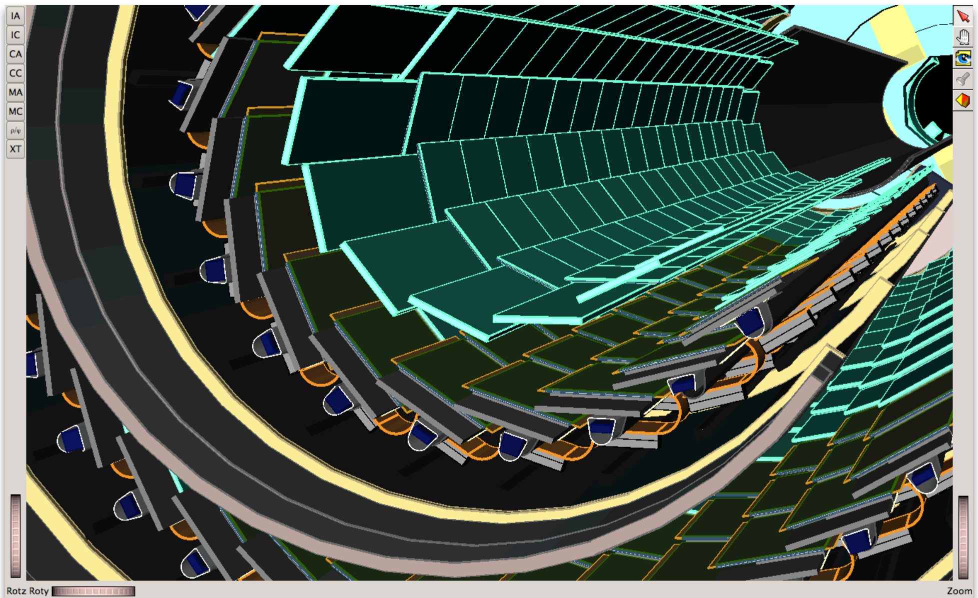


New Insertable B-Layer (IBL)



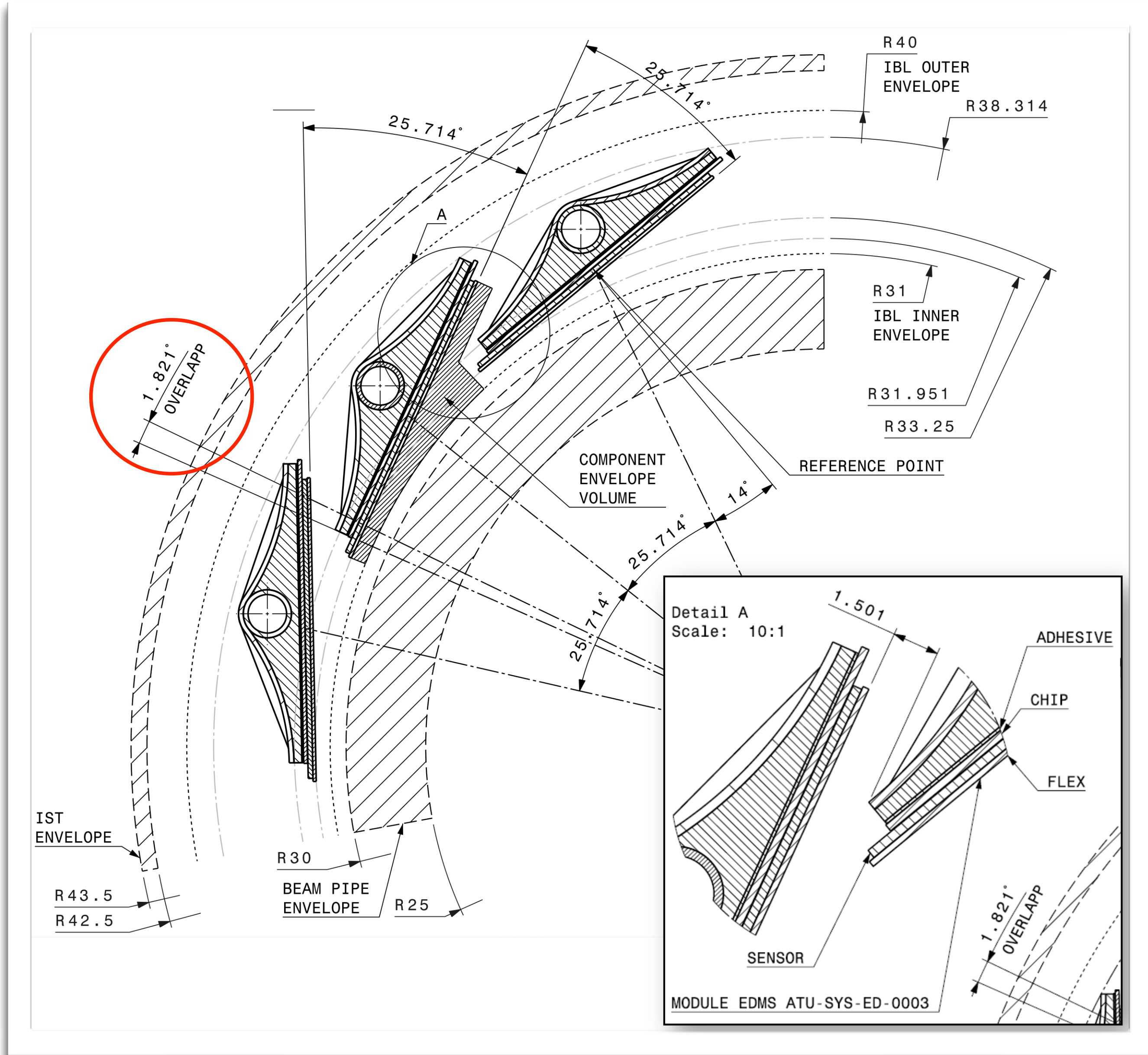
- Fourth pixel layer ➡ to be installed in the current Pixel detector
  - originally planned for the 2016 shutdown...
- Installation in 2013 motivated by improving physics performance in ATLAS...
  - luminosity
    - luminosities higher than 10^{34} $cm^{-2}s^{-1}$ ➡ pileup and readout inefficiencies
  - tracking robustness
    - compensates for inefficiencies and damage
  - tracking precision
    - additional layer closer to interaction point will improve the quality of track impact parameters
- ...but also as a technology step towards HL-LHC !!



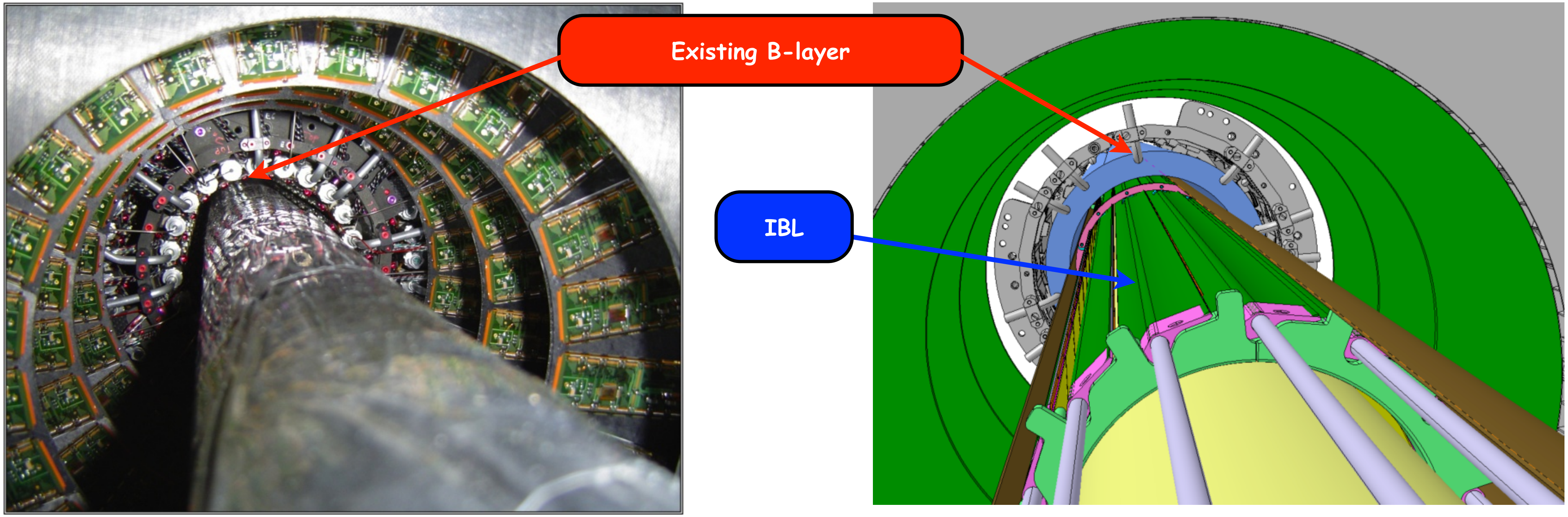


IBL overview

Number of staves	14
Stave length	706 mm
Stave tilt angle	14°
Modules per stave	16
Pixel size (Φ,z)	50 x 250 μm^2
Module active size	40.8 x 20.4 mm^2
IBL nominal radius	33.25 mm
IBL inner enveloppe	31.0 mm
IBL outer enveloppe	38.2 mm

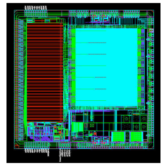


Tight clearence !!



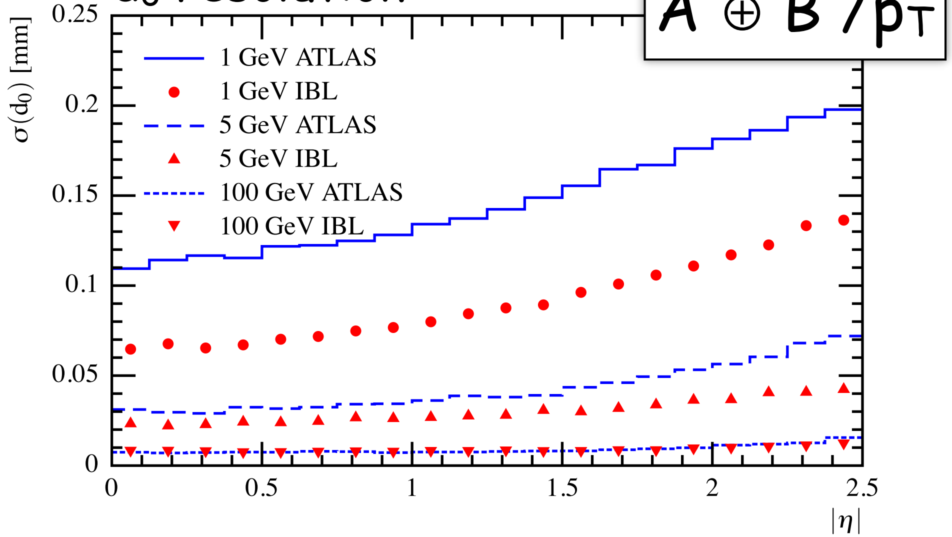
- Current radial clearance: 8.5 mm
- Reduction of the beam-pipe by 4 mm brings it to 12.5 mm
  - new Be beampipe (0.7% X0)
    - inner radius 29 → 25 mm
    - expensive but significant reduction of the MS background
- The IBL must fit in a very tight space !!!

IBL performance

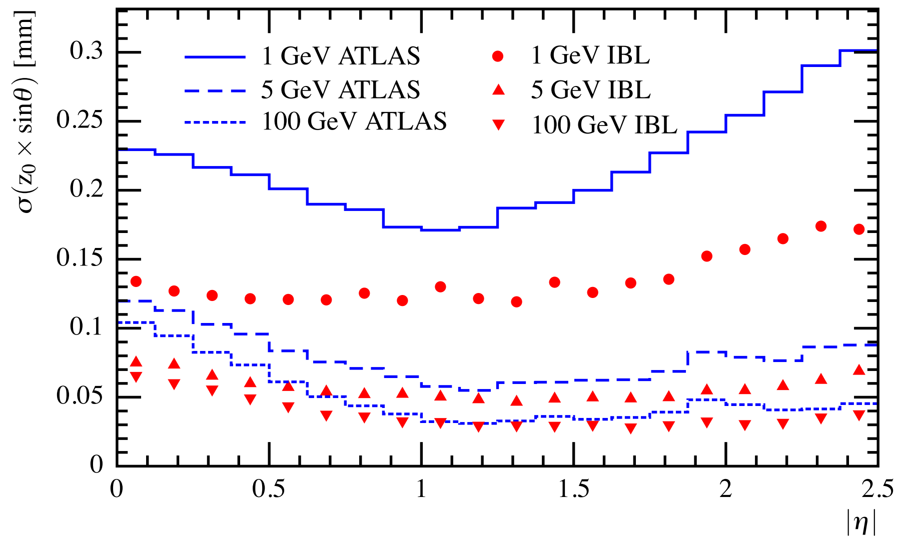


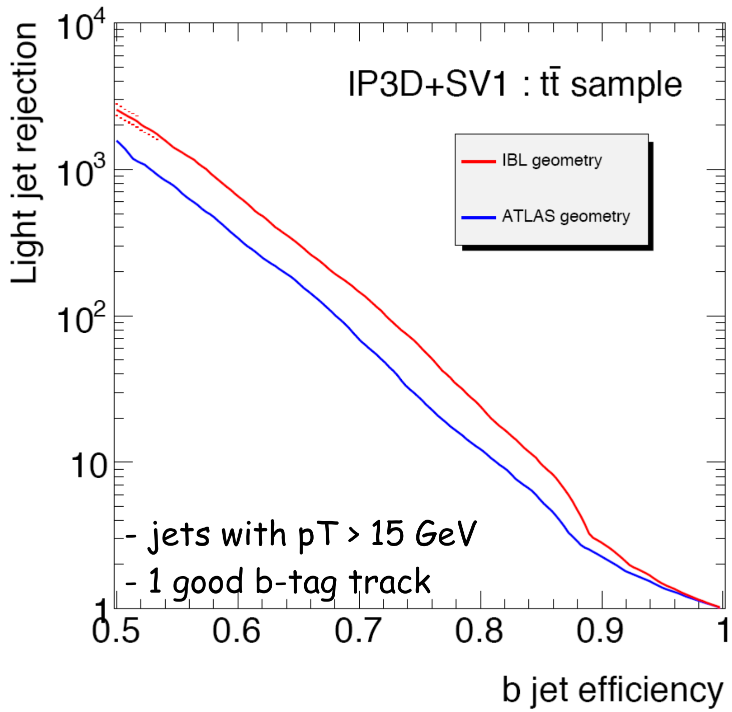
d_0 resolution

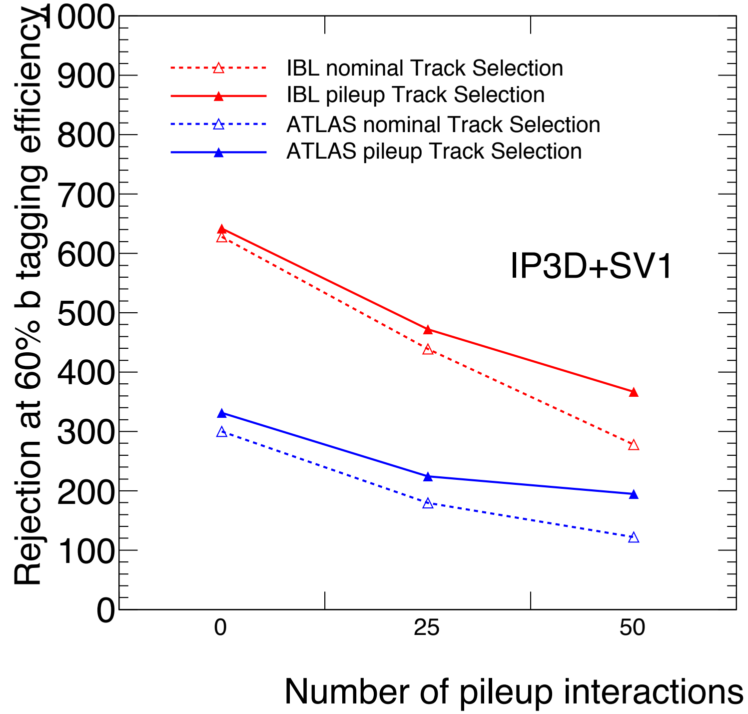
$A \oplus B / p_T$



z_0 resolution

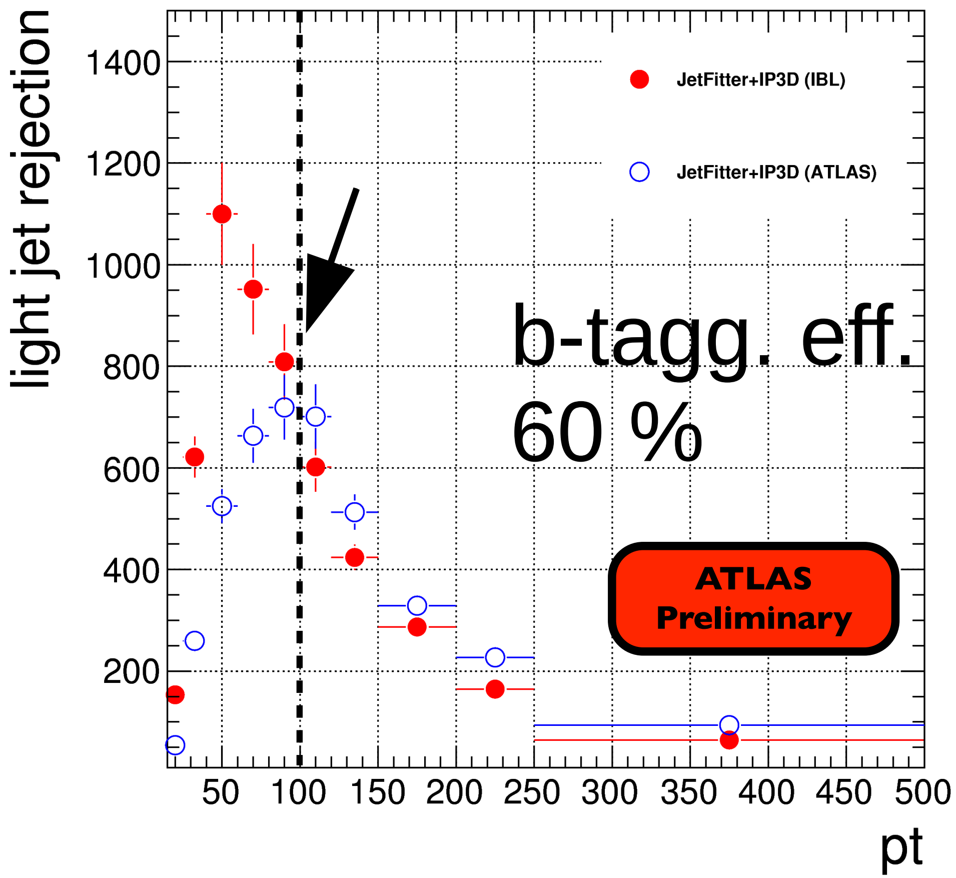


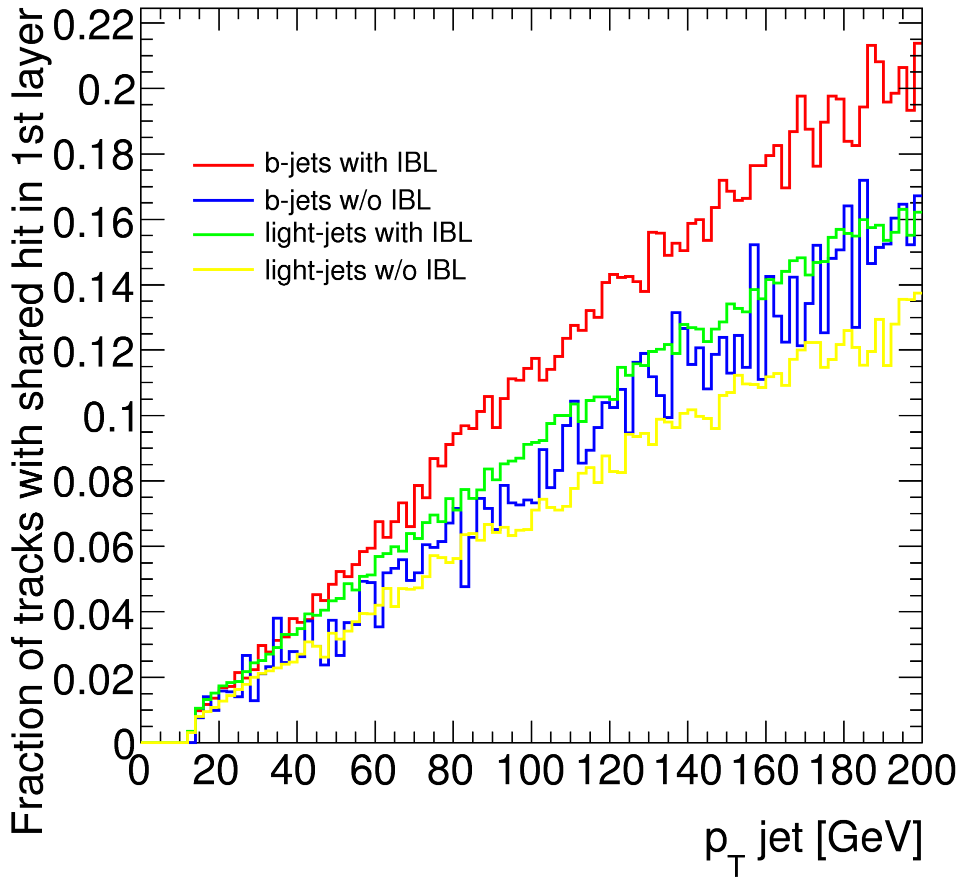




But tracking in a dense jet environment is tough...

WH, H → bb

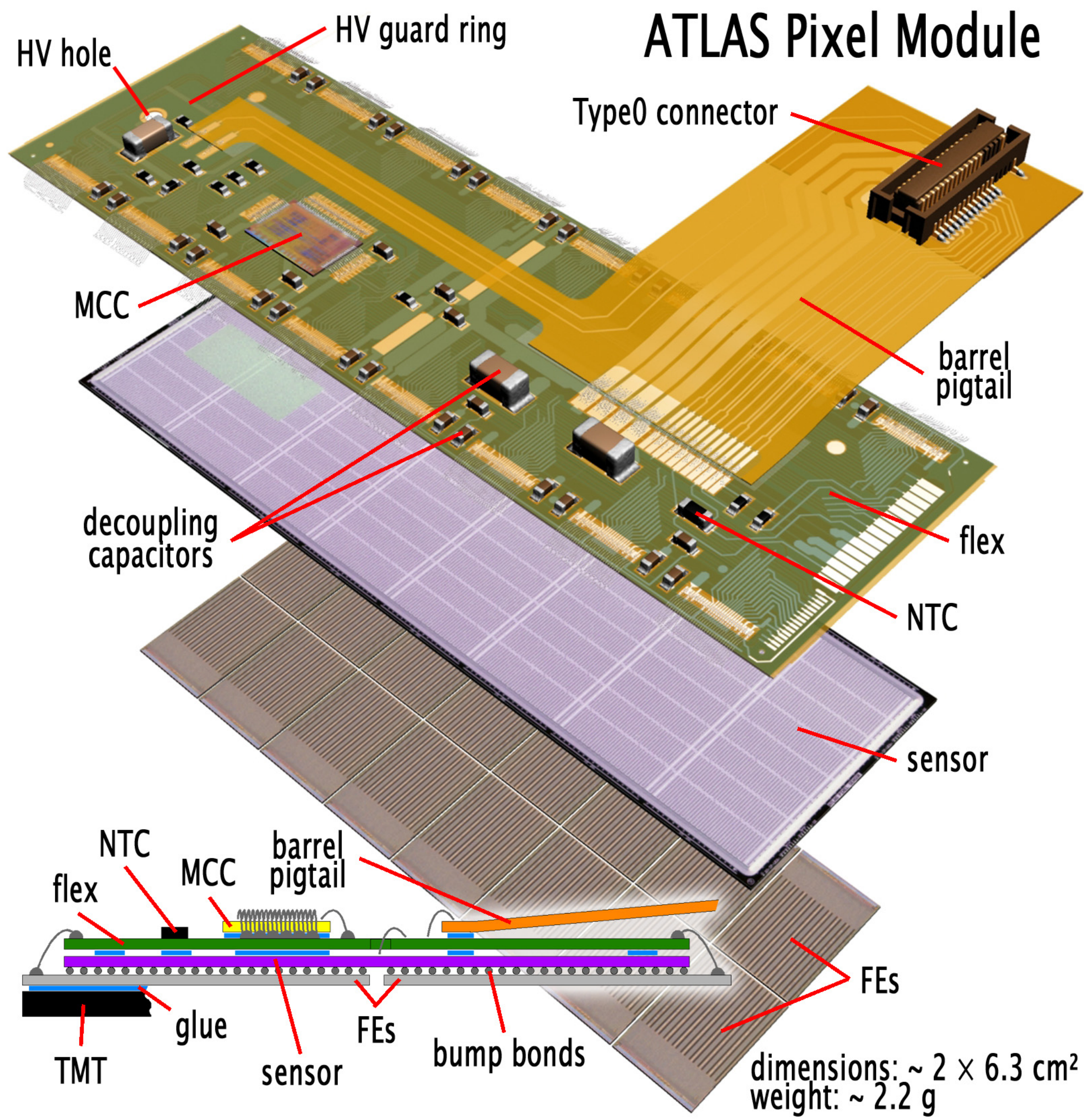


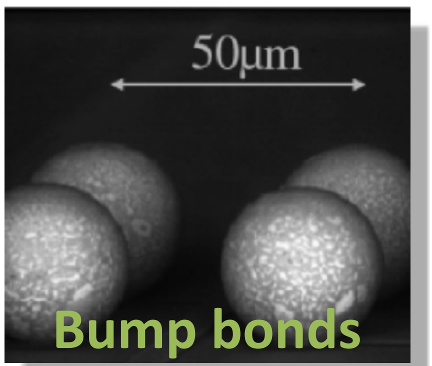


- Improve treatment of merged clusters !!
- New pixel clusterization algorithms being implemented in the ATLAS sofware:
  - "aggressive": neural networks
  - "robust": finding a minima of energy between two maxima

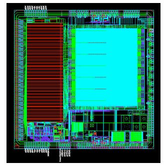
The ATLAS Pixel module

- Silicon sensor
  - planar n-in-n, 250 μm thick
  - designed for 1x1015 1MeV fluence and 50 MRad
- Front-end chips
  - 16 FE-I3, bump-bonded
- 46080 readout channels
  - 50 x 400 μm
  - 50 x 600 μm for edge pixel columns in neighbour ASICs
- Barrel and end-cap modules identical

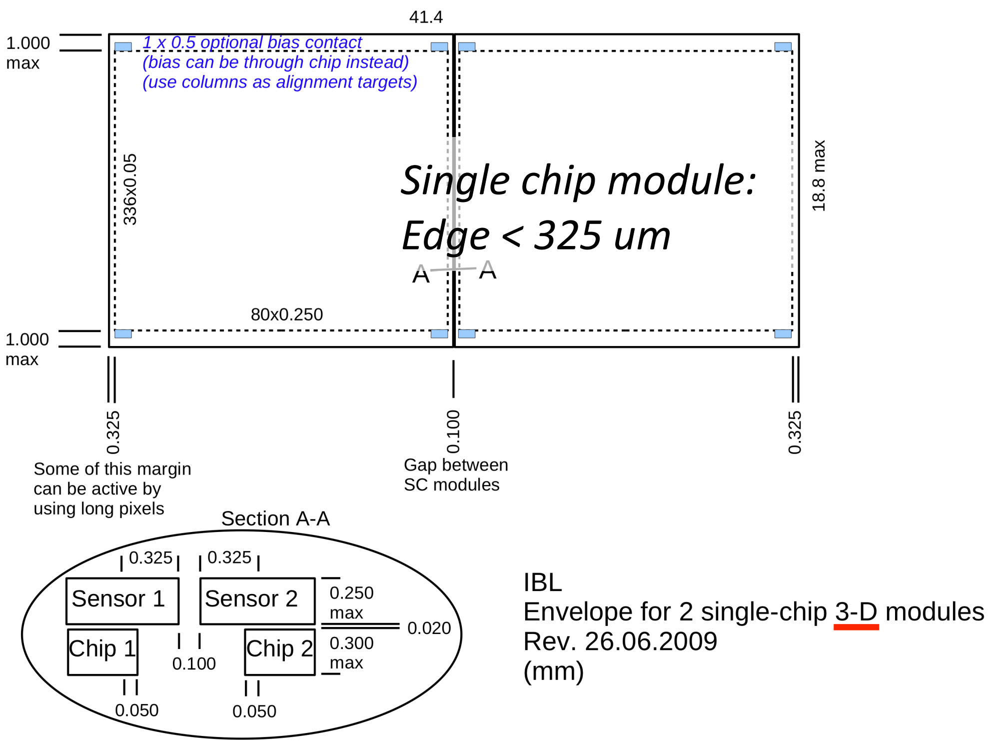


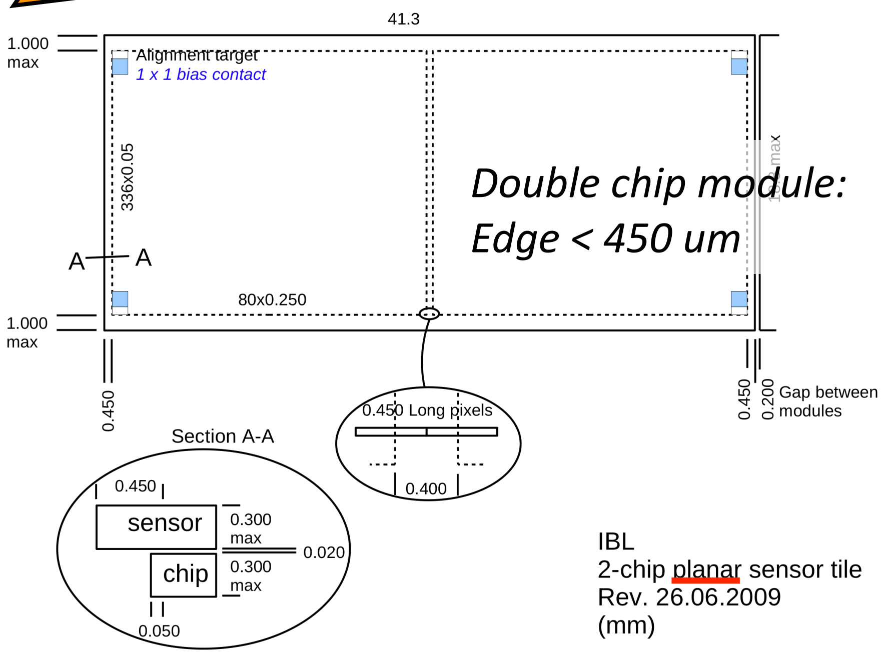


The IBL module

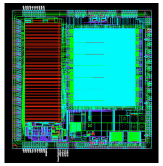


- New readout chip: FE-I4
- Single or double chip module
- Sensor technology independent
  - planar ➡ double-chip module
  - 3D ➡ single chip module
  - diamond





The IBL module

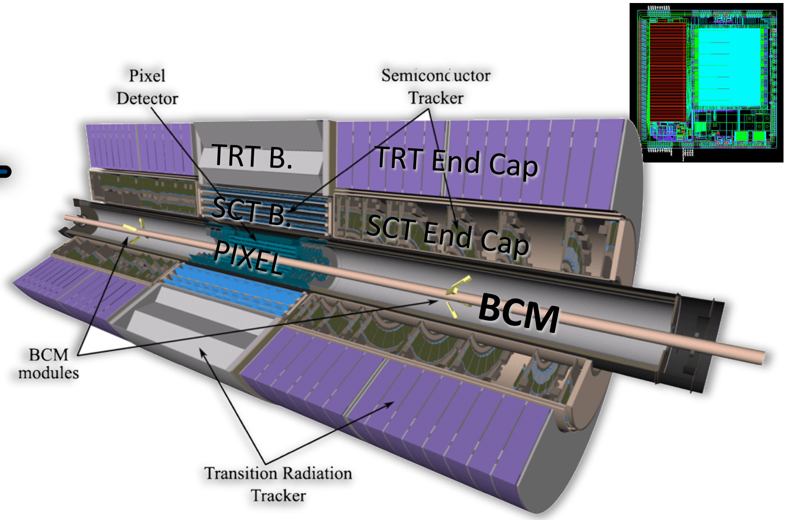


- New readout chip: FE-I4
- Single or double chip module
- Sensor technology independent
  - planar
  - 3D
  - diamond ➡ **abandonned for IBL...**

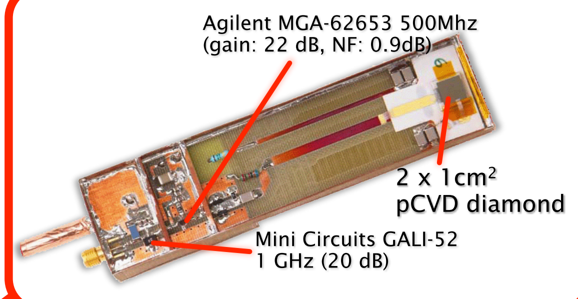
- original production time of 2 years (mid 2013)
- no resources to cope with increasing number of sensors

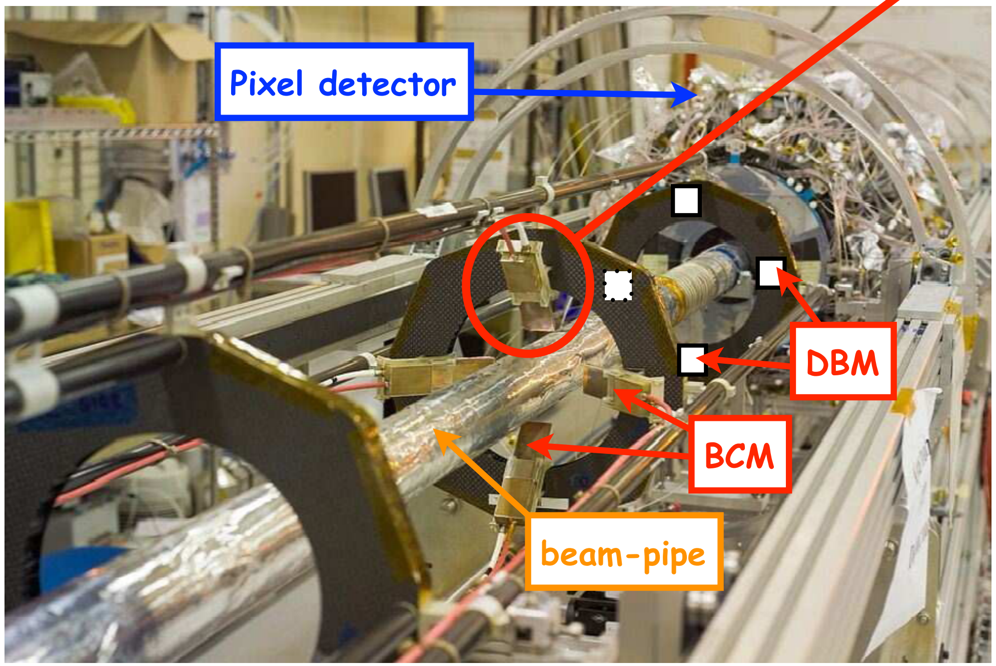
The IBL module

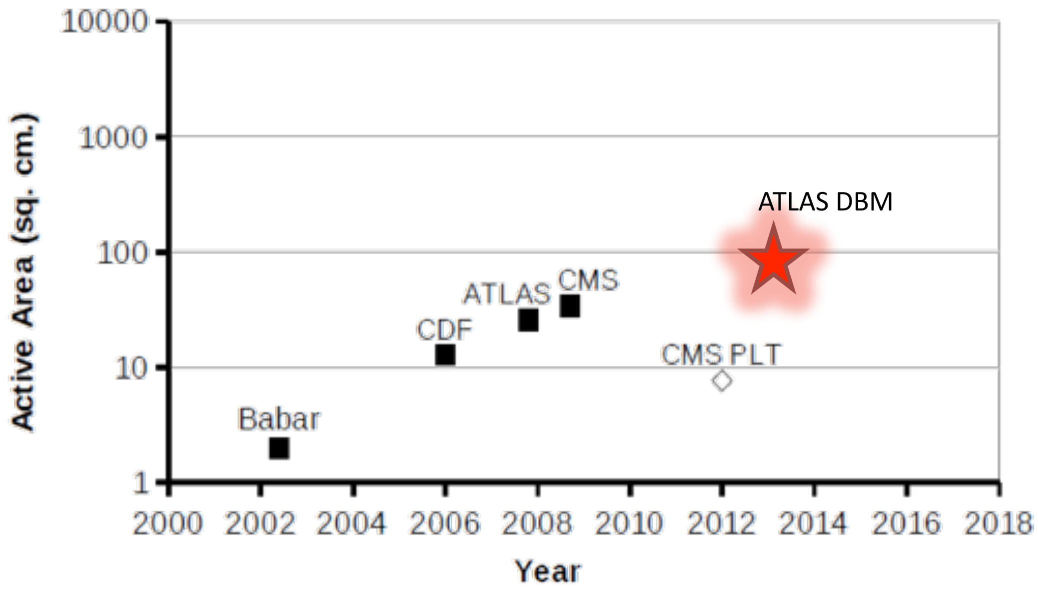
- New readout chip: FE-I4
- Single or double chip module
- Sensor technology independent
  - planar
  - 3D
  - diamond ➡ **but still useful for DBM !!!**



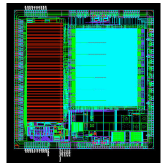
- DBM = Diamond Beam Monitor
- bunch-by-bunch luminosity monitor
  - larger acceptance than BCM
- bunch-by-bunch beam spot monitor





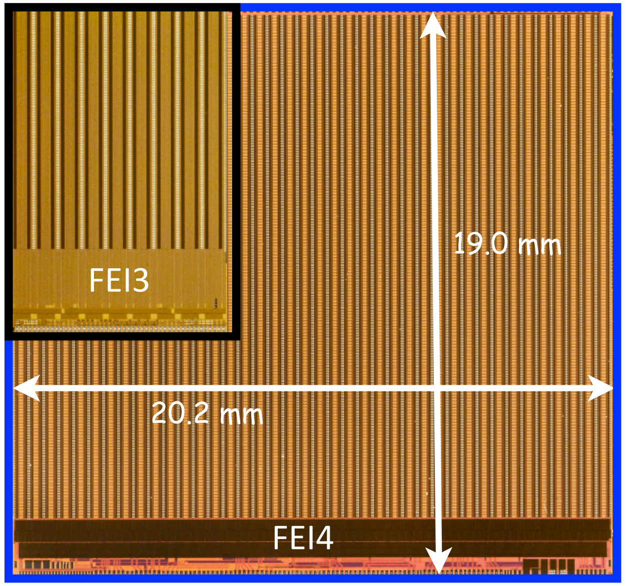


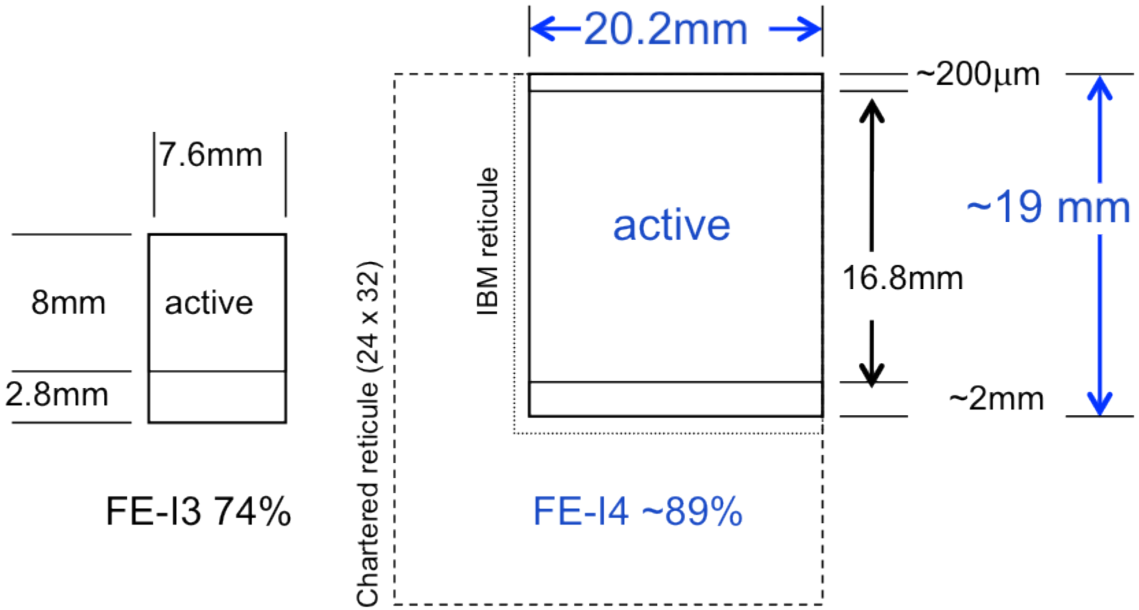
FE-I4



- New readout chip for IBL and outer layers of future upgraded Pixel detector
- Smaller pixel size (50x250 μm^2) and higher rate capabilities (160 MB/s)
- Improved cost effectiveness
  - large chip (20x19 mm^2) with large active area (90%)
- Low power
- Increased radiation tolerance (130 nm)

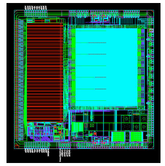
FE-I3: chip used in current Pixel modules





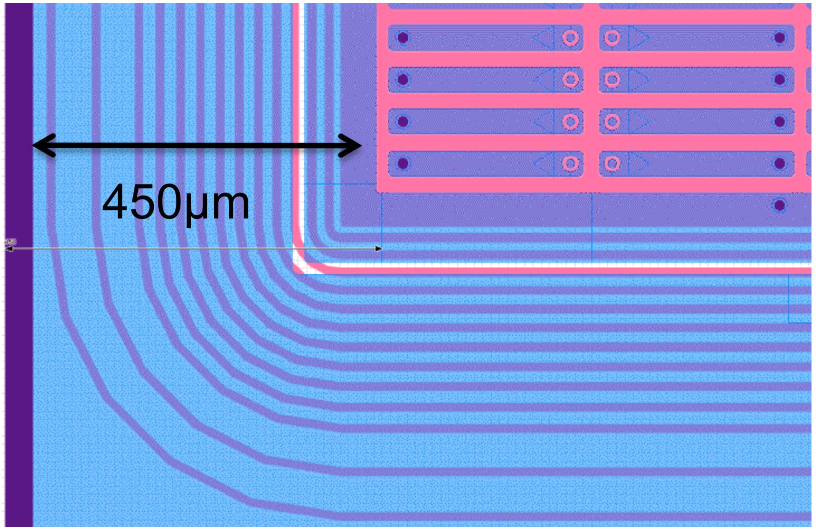
FE-I4: chip used in IBL Pixel modules

Planar silicon sensors

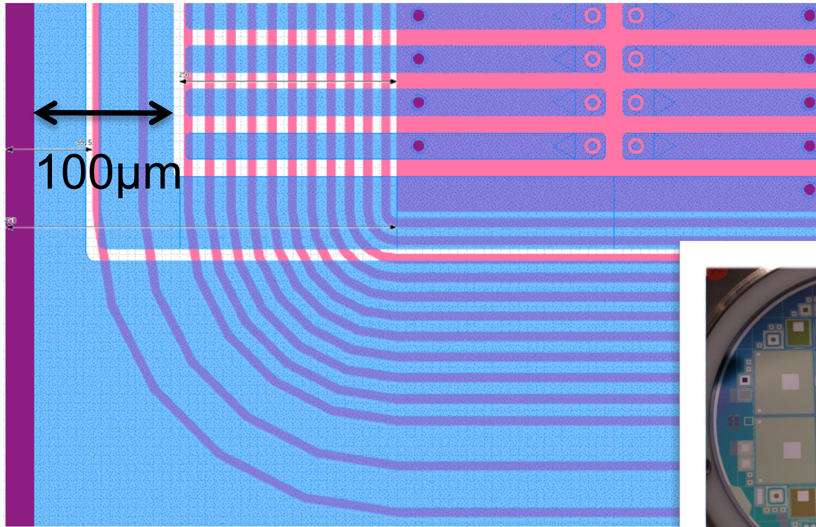


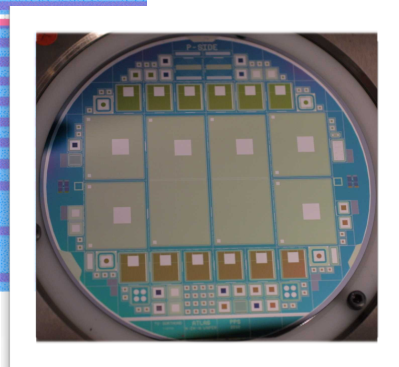
- Two **n-in-n** sensors with different guard ring structures:

"conservative": 450 μm guard-ring

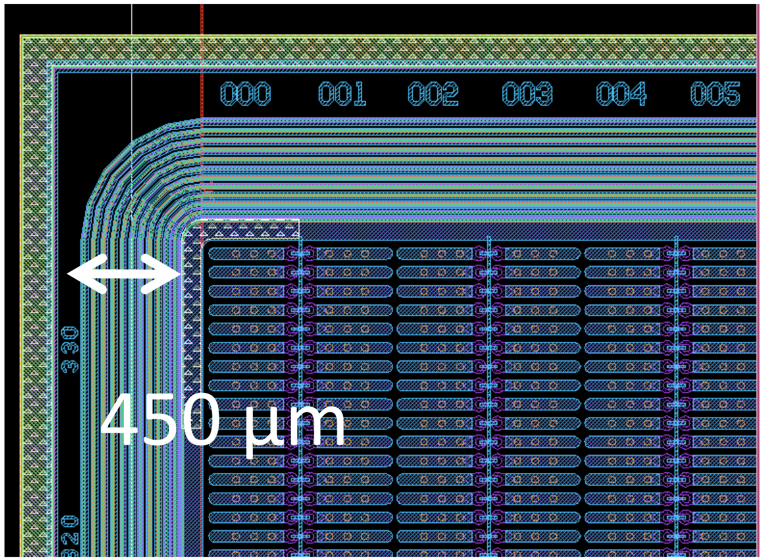


"aggressive": silm edge, 100 μm inactive area

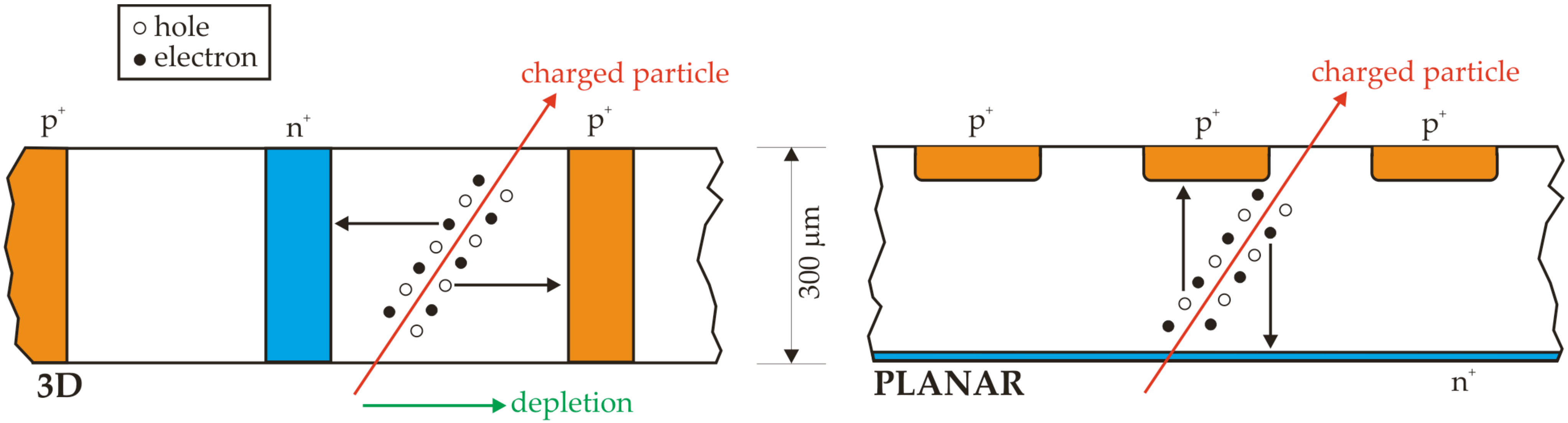




- Thin **n-in-p** sensors:



3D sensors: basics



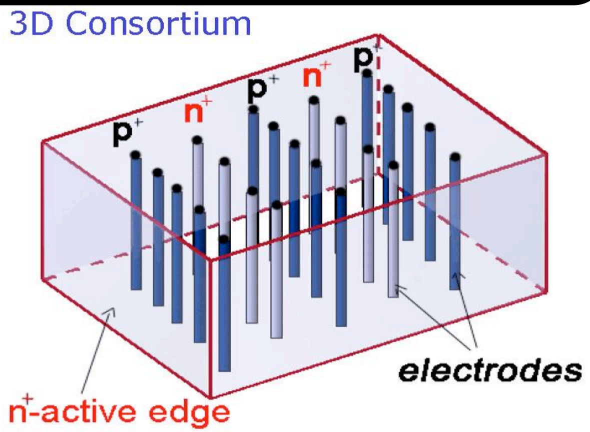
3D

- Advantages
  - lower full depletion voltage
  - short collection distance
  - smaller trapping probability
    - higher signal yield after irradiation
  - active edge
- Complications
  - partially inactive columns
    - efficiency loss at normal incidence
  - higher capacitance (but higher signal)
  - production cost

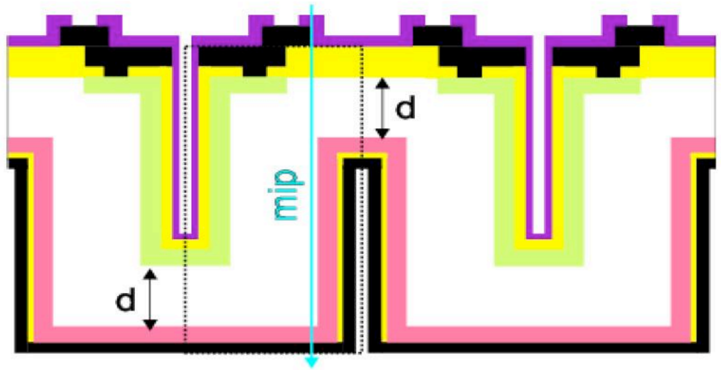
3D sensors

- Two designs with equivalent electrical performance
  - full 3D active design ➡ prefered option
  - double column design
  - 10-14 μm hole diameter

Full 3D active edge



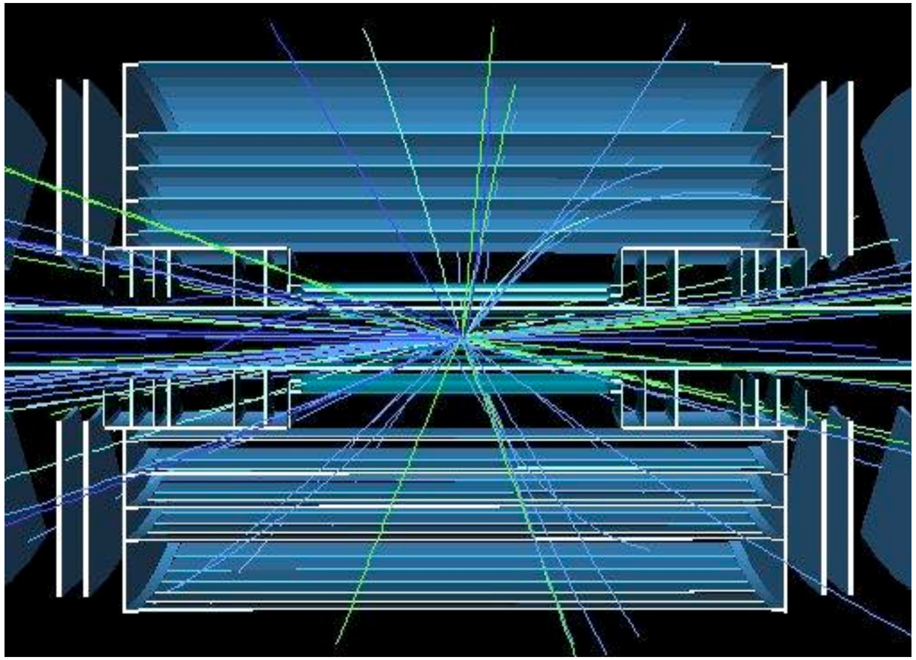
Double column design



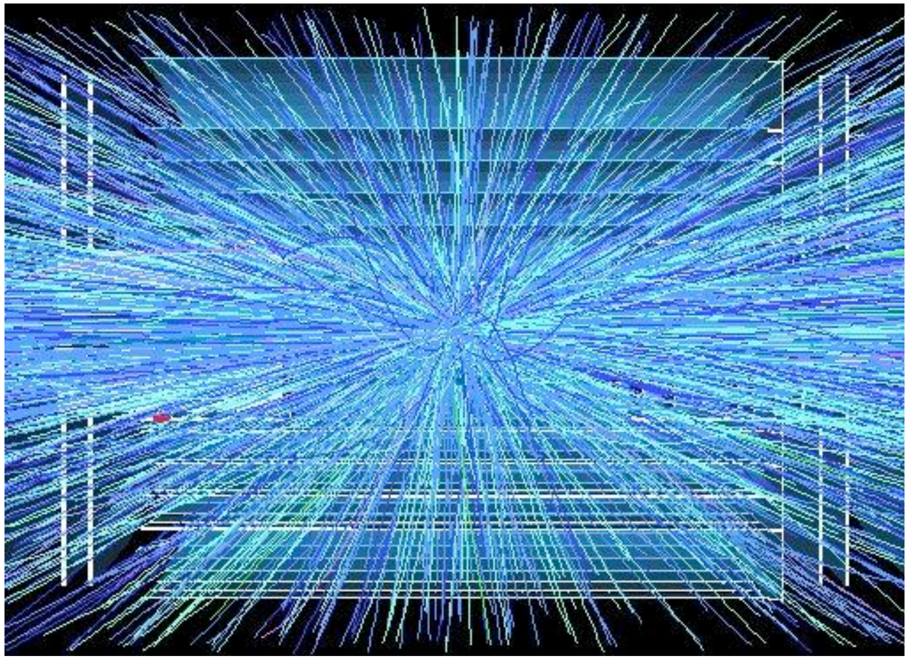
PHASE-2: a new ATLAS tracker

- Increase in pile-up events from ~23 to ~200
  - Radiation damage
  - >10^5 particles $|\eta|<3.2$ ➡ occupancy in the TRT ~100%

5 collisions (0.2×10^{34} cm^{-2} s^{-1})

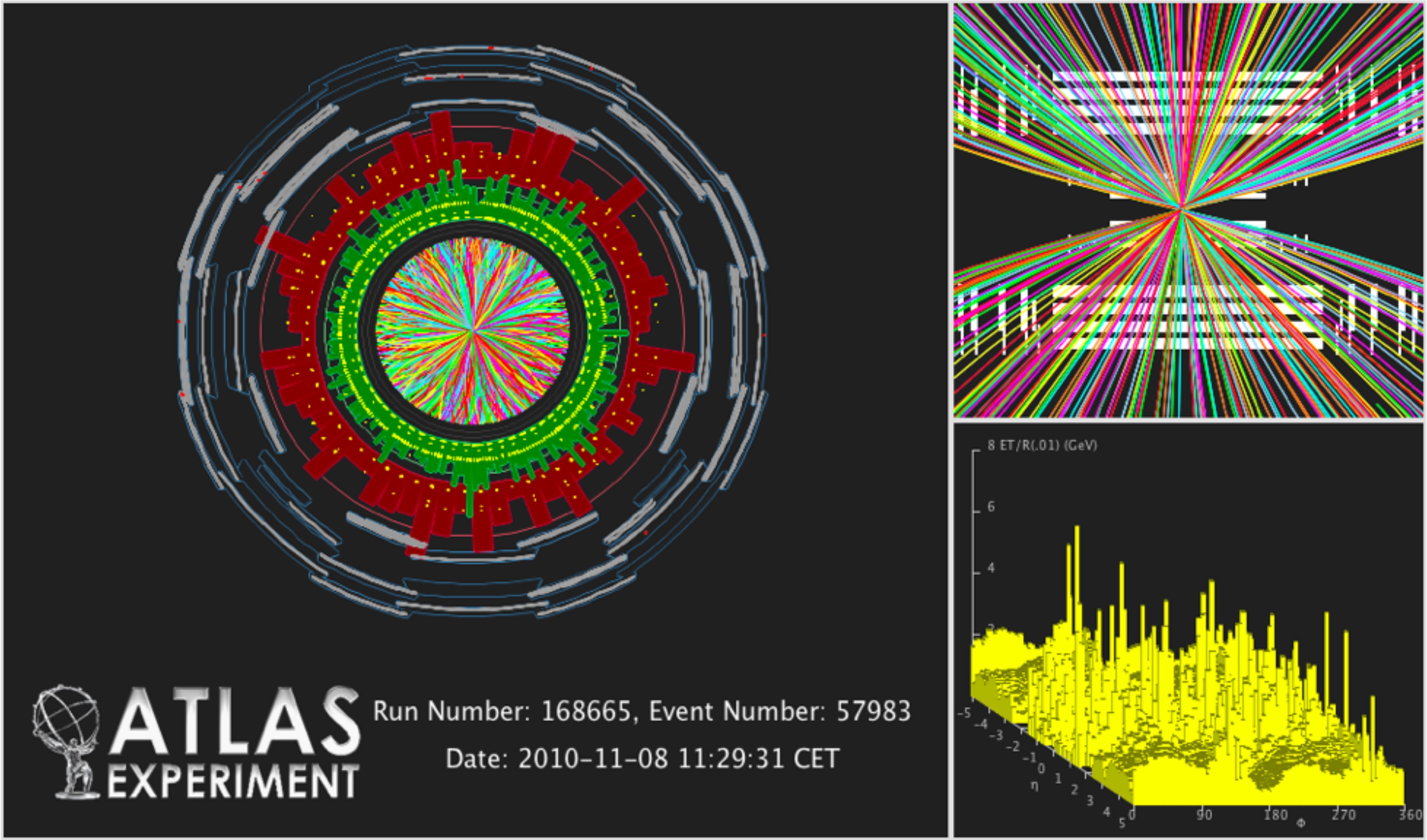


400 collisions (10^{35} cm^{-2} s^{-1})

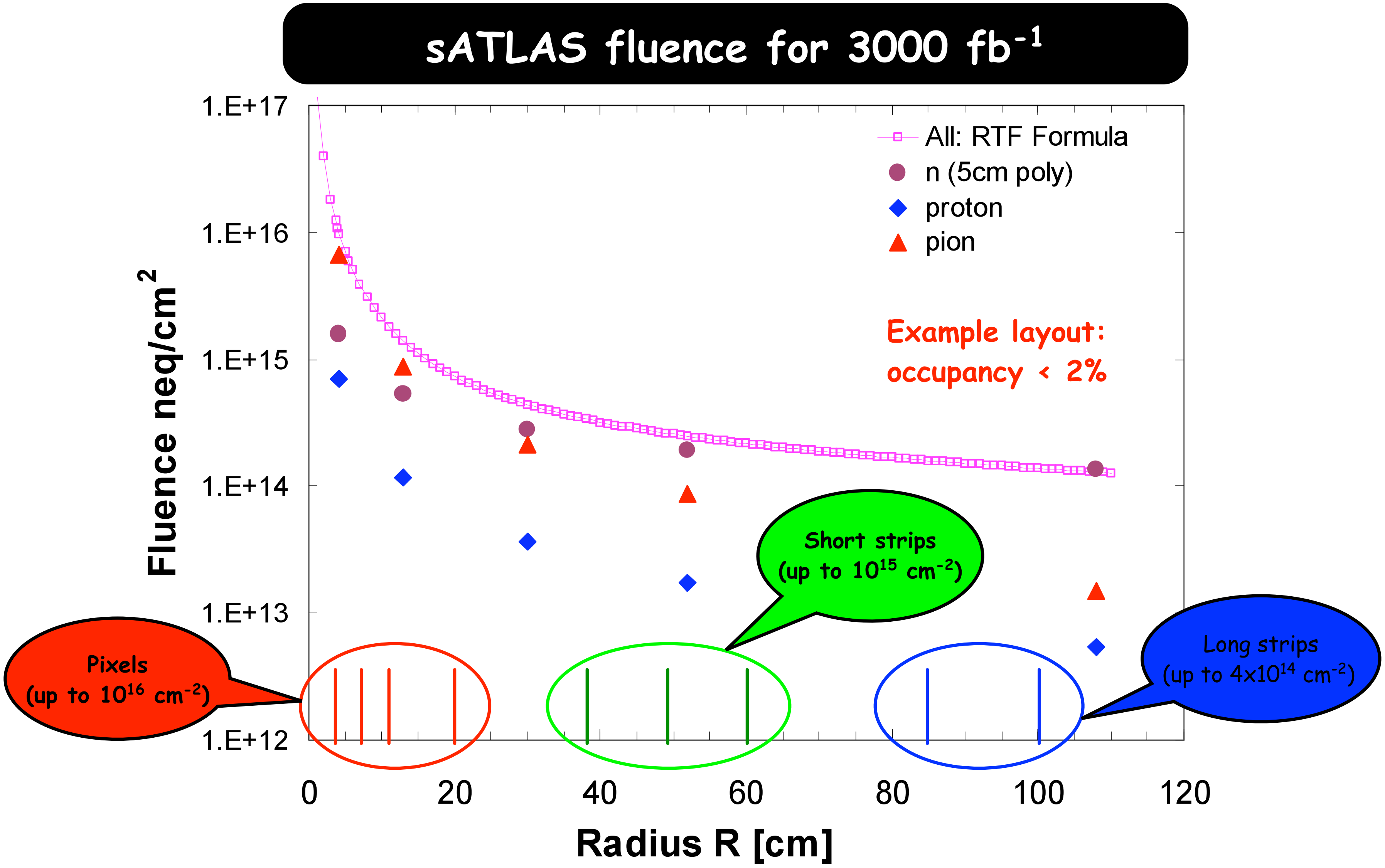


- **Build a completely new ATLAS Inner Detector !!**
- Pattern reco, good tracking eff+low fake rate, minimise occu
  - better detector granularity
- silicon-based tracker: **pixels** and **strips** (short and long)

Heavy-ion collision event



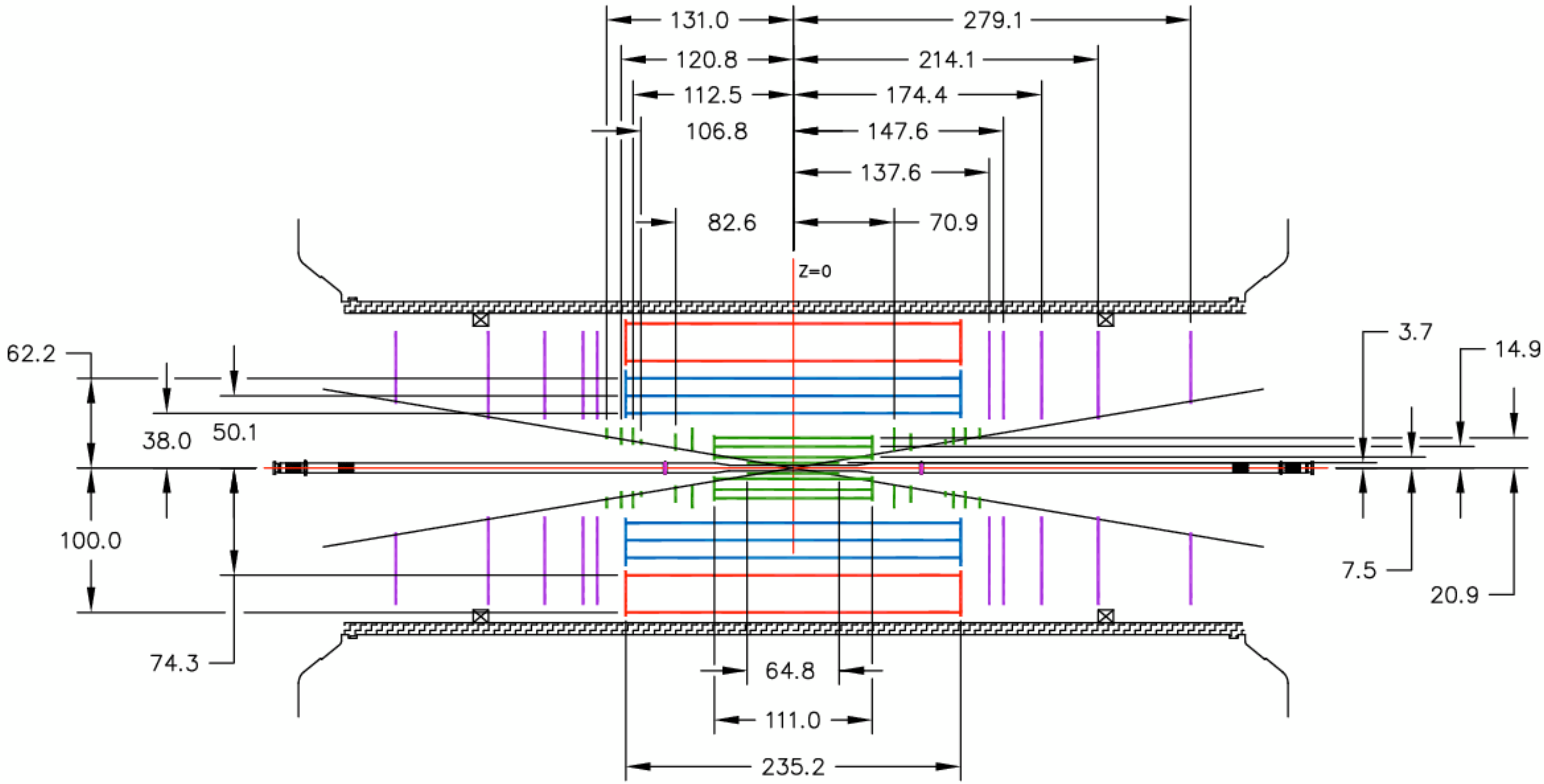
Fluences



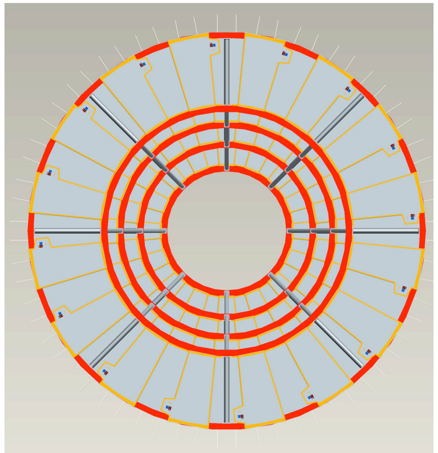
<u>ATLAS Radiation Taskforce Report</u>

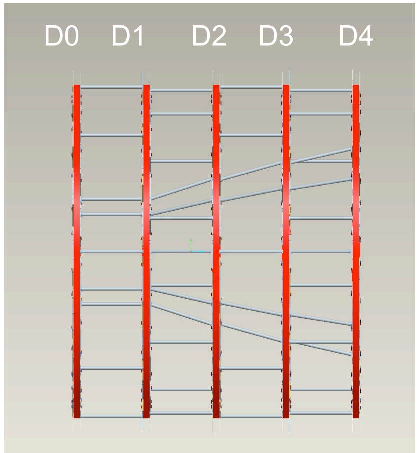
$\Phi=1.3\times10^{17}/r^2+4.8\times10^{15}/r+9.9\times10^{13}-3.6\times10^{11}r$ $[n_{eq}/cm^2]$

A strawman layout for the future tracker



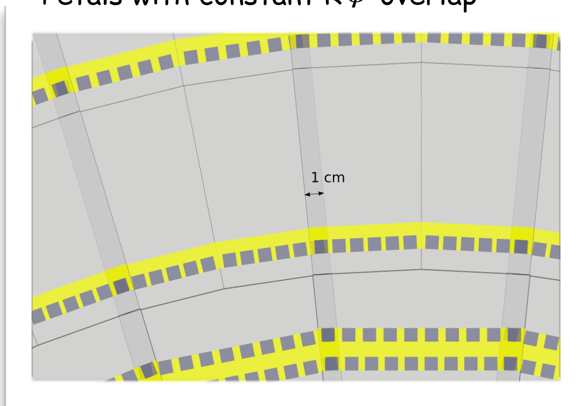
Strip end-cap petals

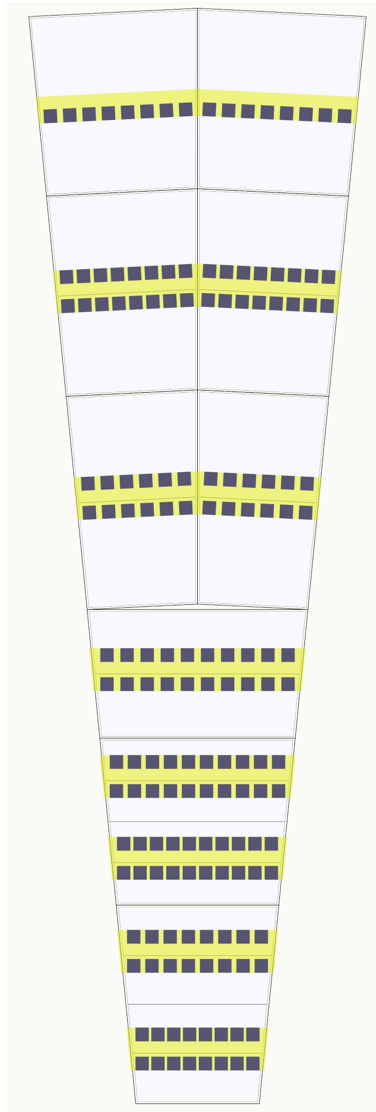


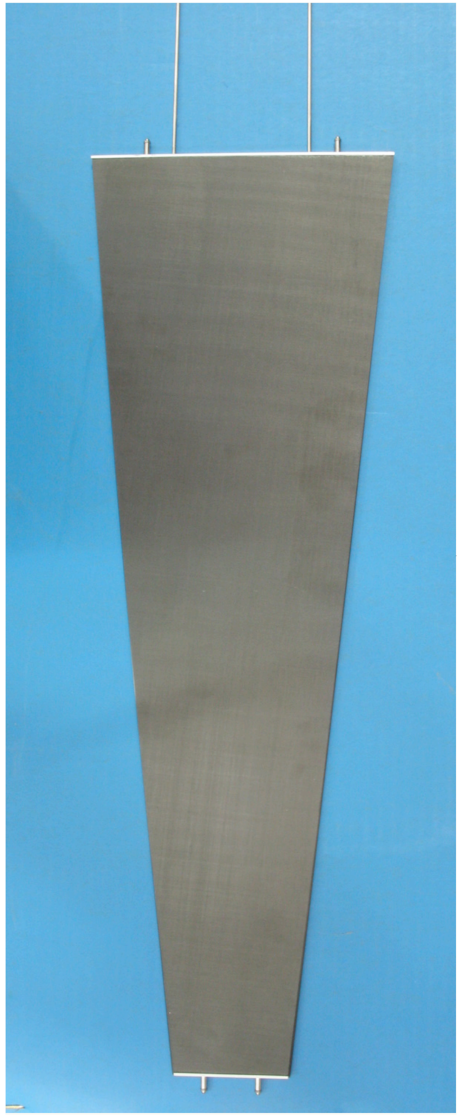


- Sensors mounted on petals and disks made of petals
  - Coverage from R=340 mm to R=950 mm
  - 5 disks
  - 32 petals/disk
  - Large number of sensors/petal

Petals with constant Rφ overlap

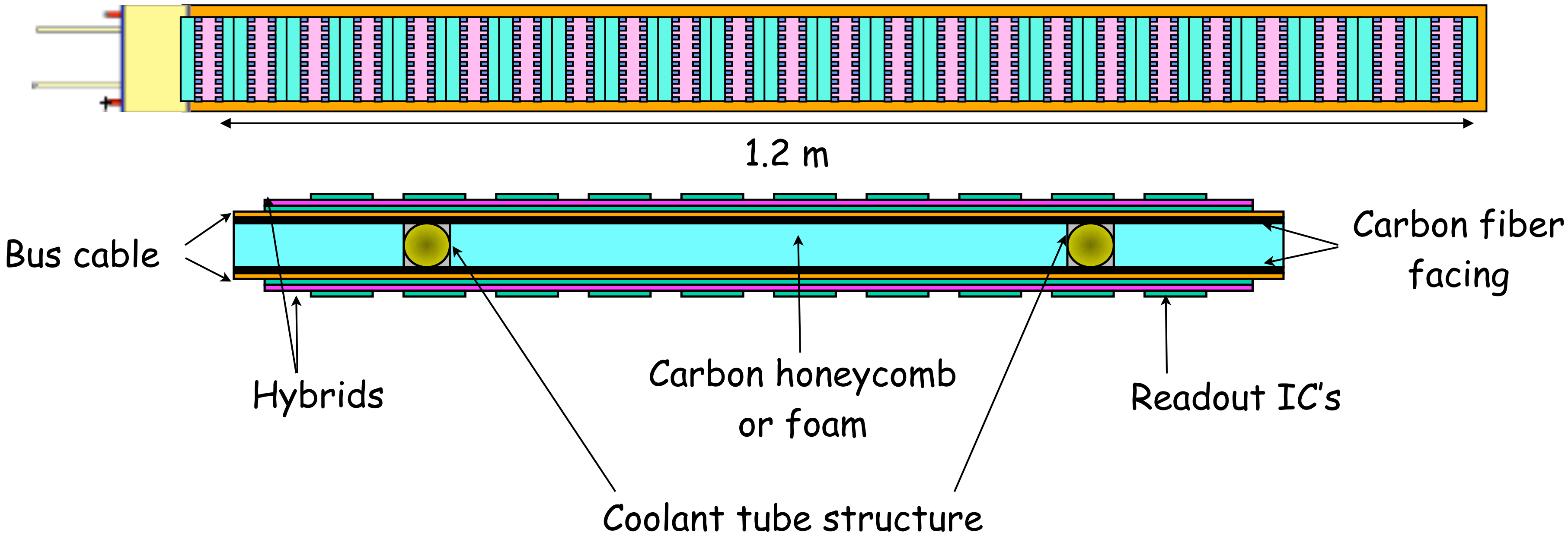




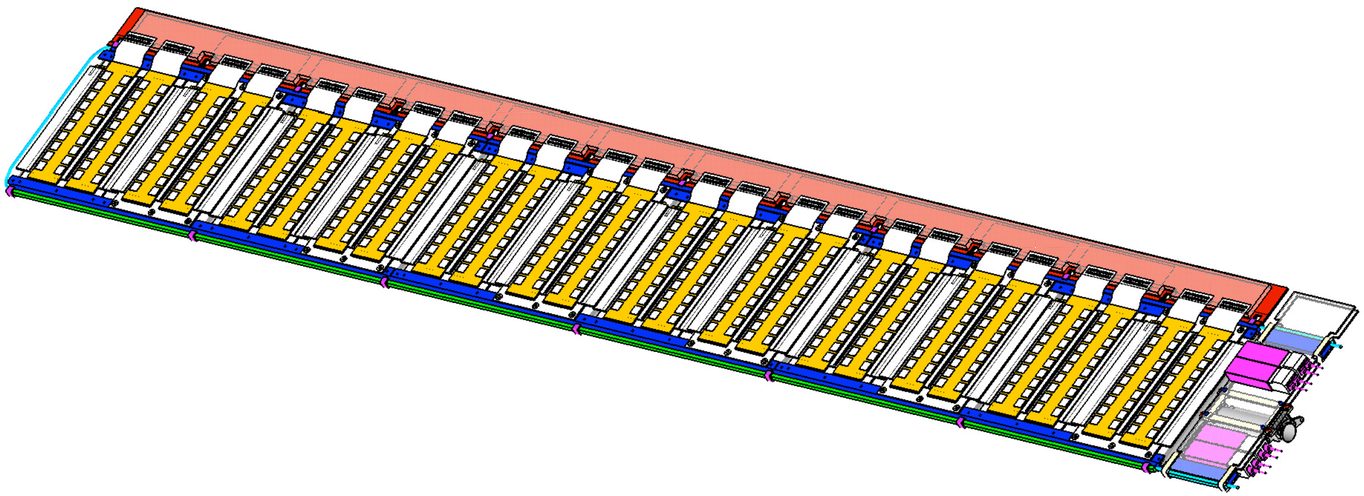


Barrel stave and supermodule concepts

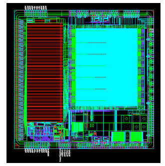
STAVE

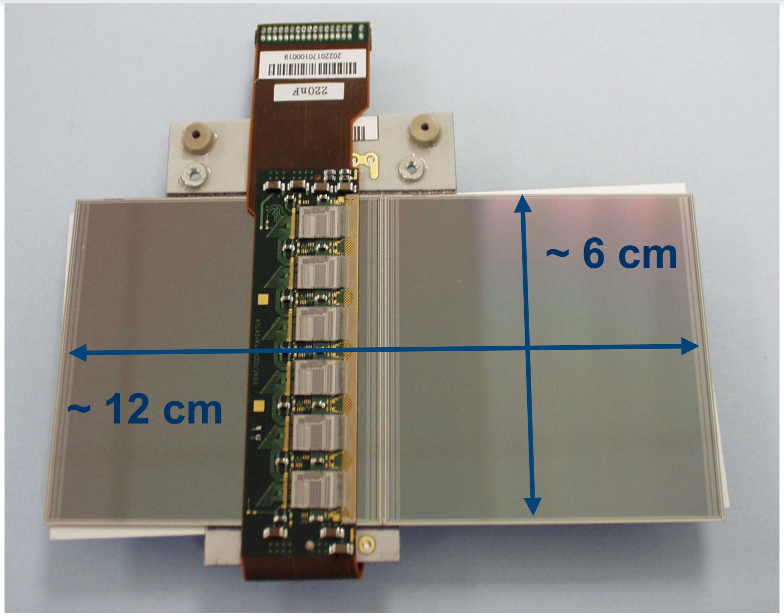


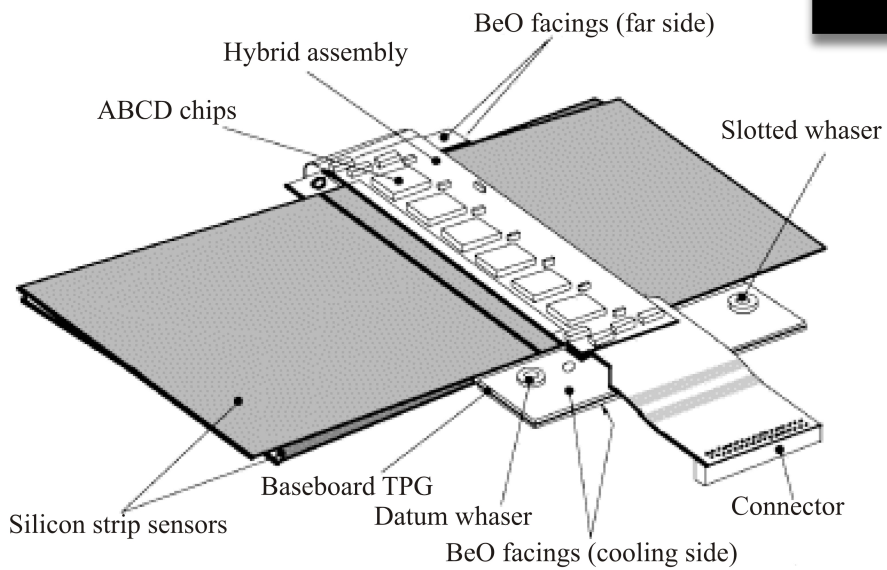
SUPERMODULE

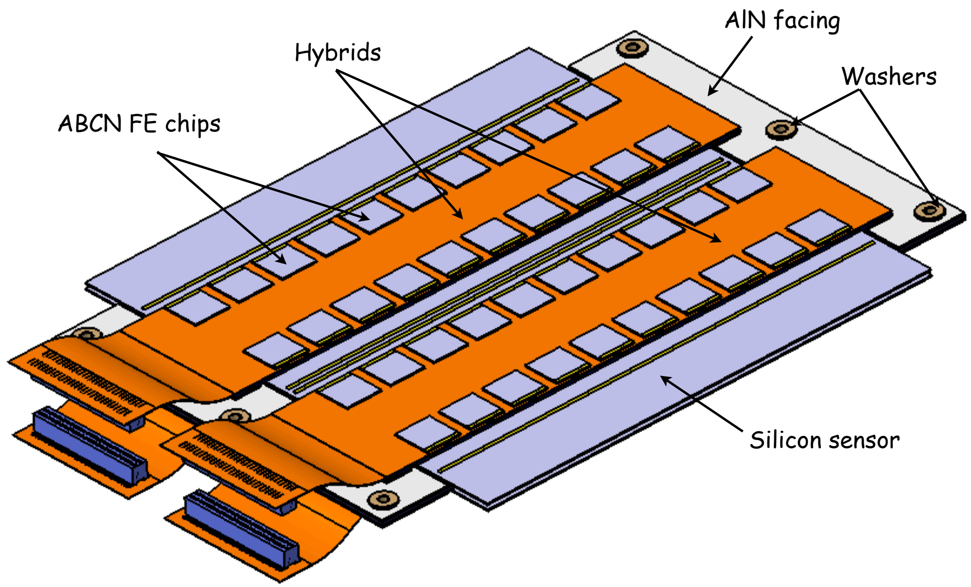


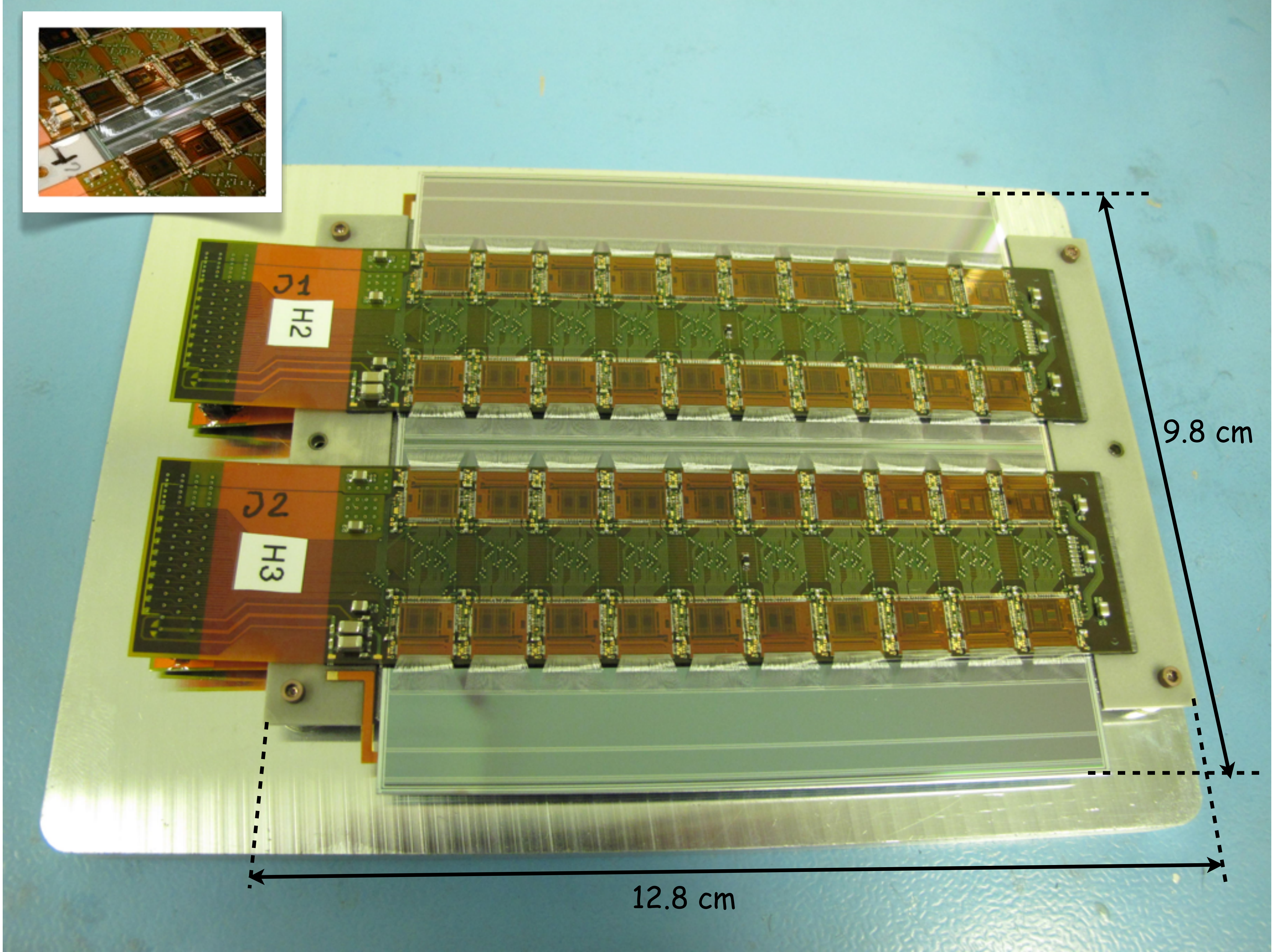
Silicon double-sided module





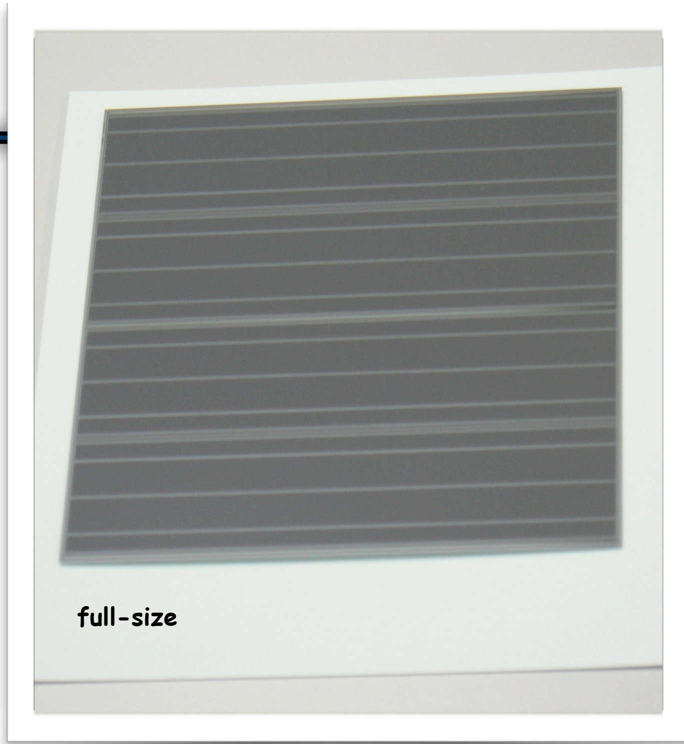





J1
H2
J2
H3
9.8 cm
12.8 cm

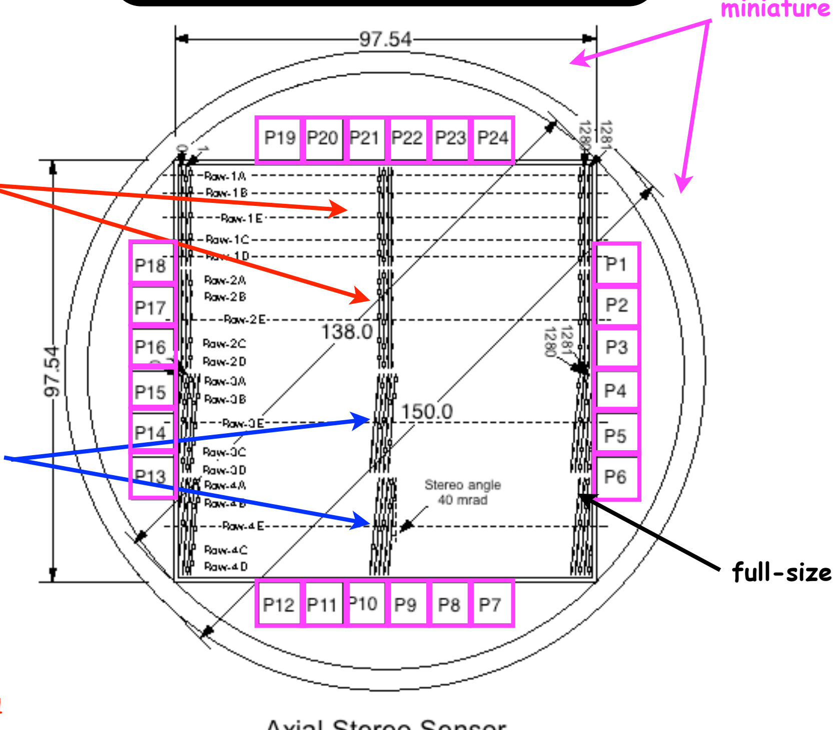
Strip barrel sensors

- n-strips in p-type substrate silicon (n-on-p)
  - always depleting from strip-side
    - no full-depletion required
  - collection of electrons
    - faster signal, less charge trapping
  - single sided process with n^+-side readout
    - “low” cost, greater potential of suppliers
  - no delicate back-side implanted structures

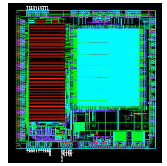


- 6-inch (150 mm) wafers
  - Hamamatsu Photonics HPK
  - full-size prototype sensors
    - 9.75 x 9.75 cm^2
    - 4 segments, short strips
      - two axial and two stereo (inclined 40 mrad) strips
    - pitch: 74.5 m, 1280 strips
  - miniature sensors
    - 1 x 1 cm^2, axial strips
      - irradiation studies

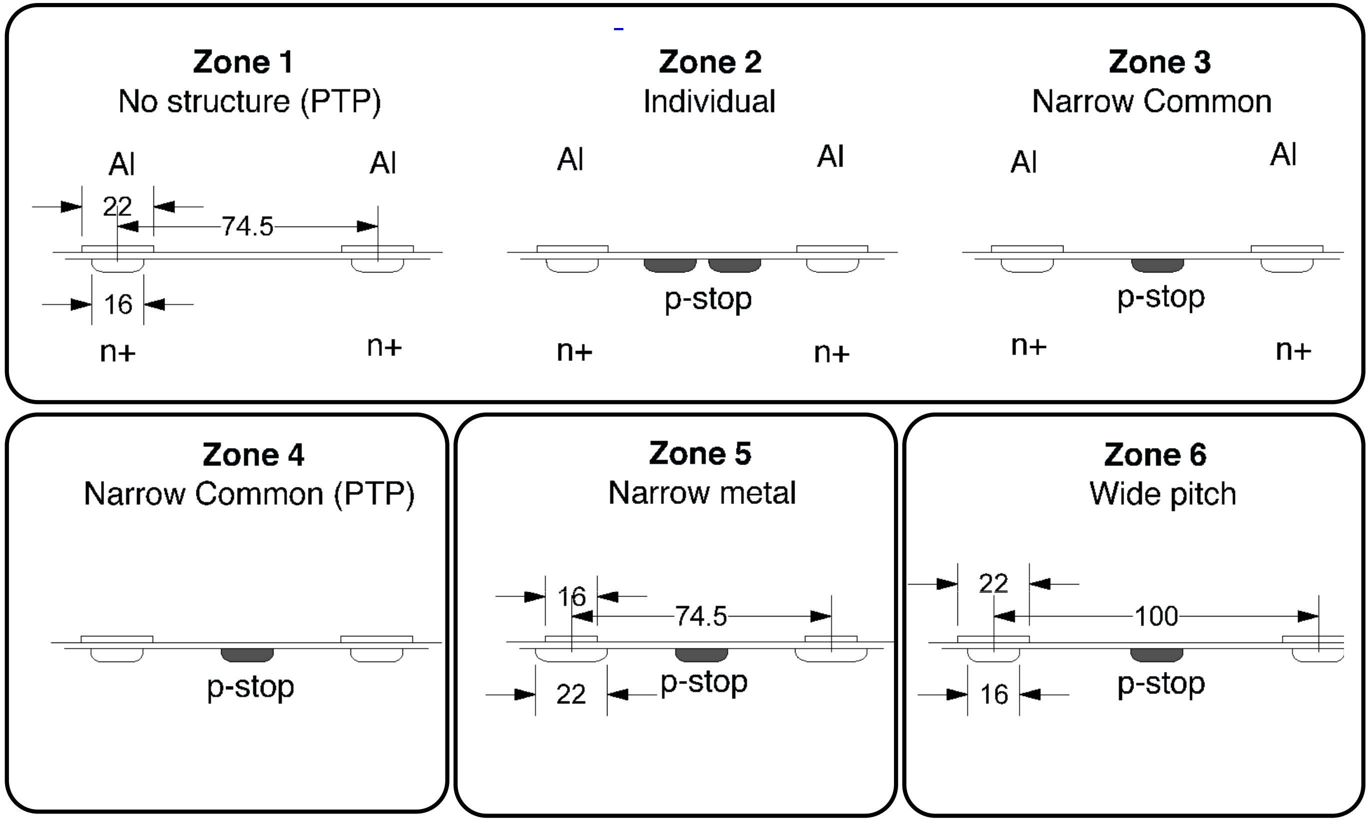
Detector mask layout

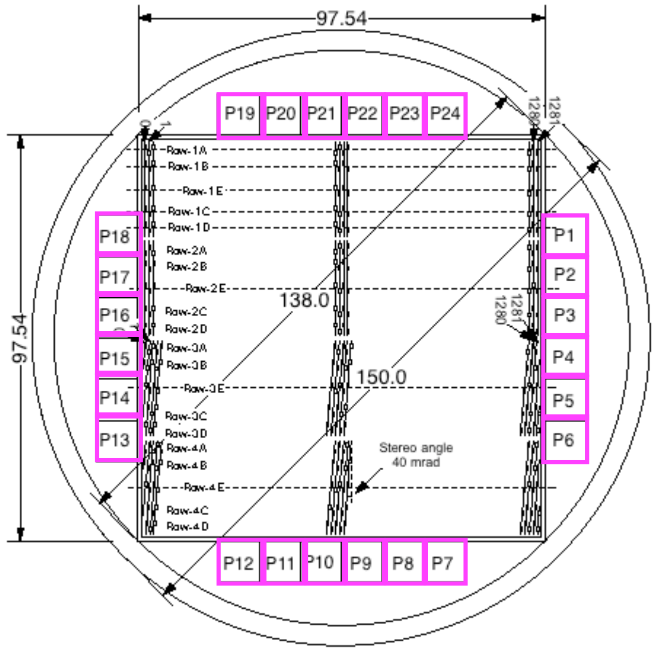


ATLAS07 miniature sensors



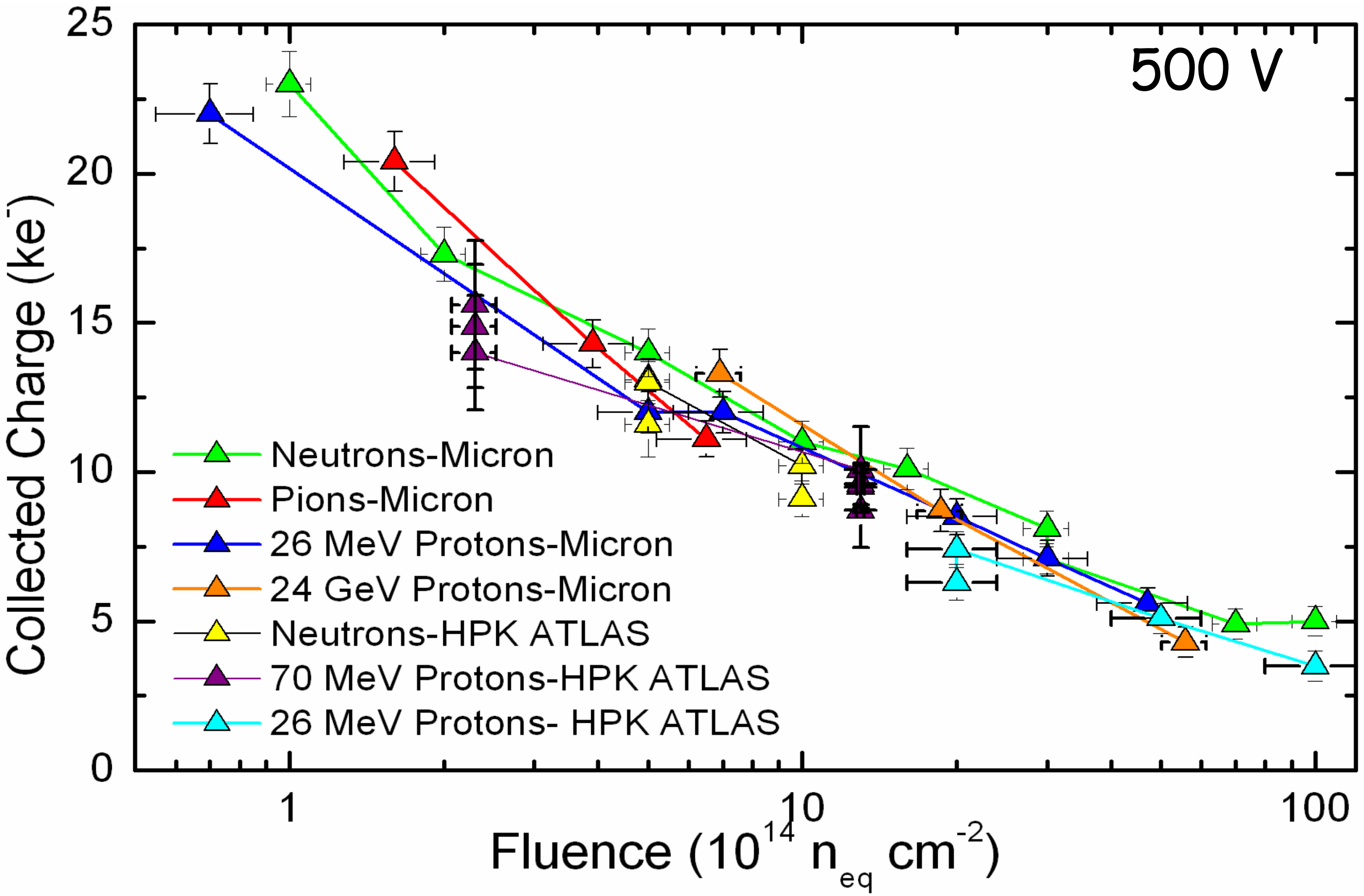
- Radiation damage study
  - Strip isolation (zones 1, 2, 3)
    - structure: p-stop, p-spray, p-stop+p-spray
    - densit: 1x, 2x, 4x, 10×10^{12} ions/cm^2
  - "Punch-Through Protection" (PTP) structures (zone 4)
  - Narrow-metal effect (zone 5)
  - Wide-pitch effect (zone 6)





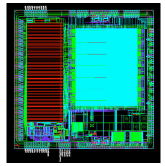
Axial-Stereo Sensor

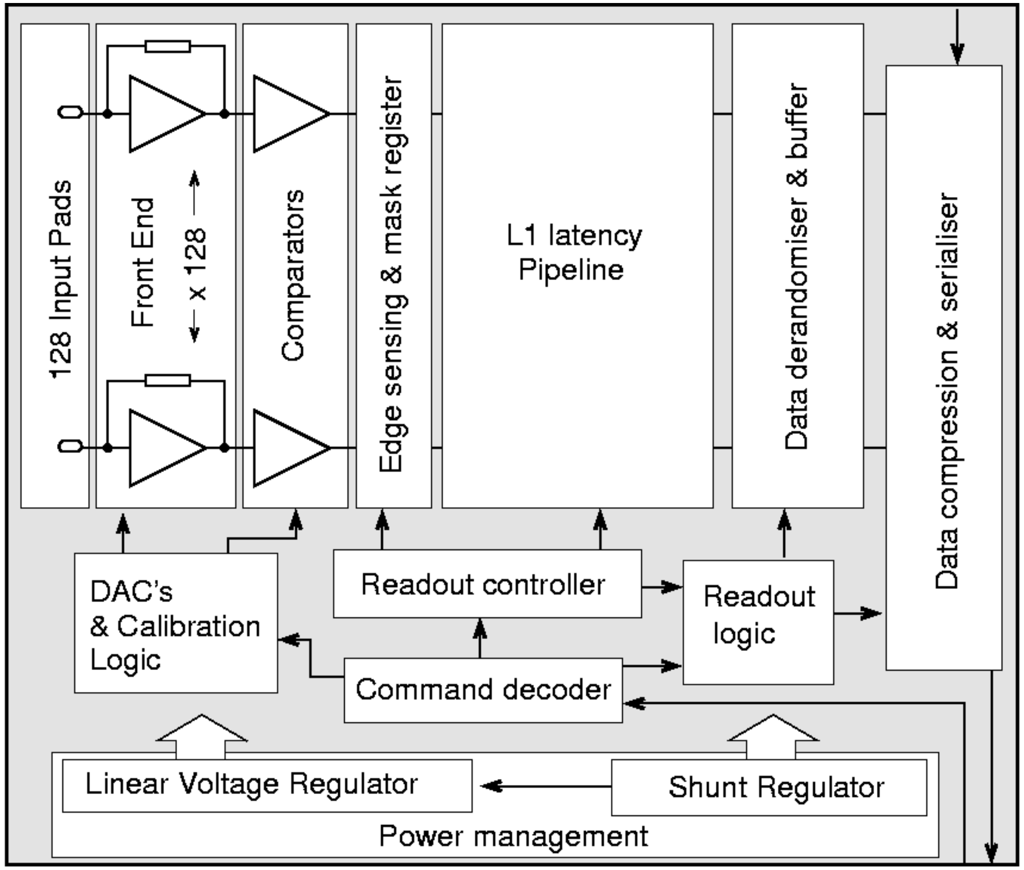
Charge collection

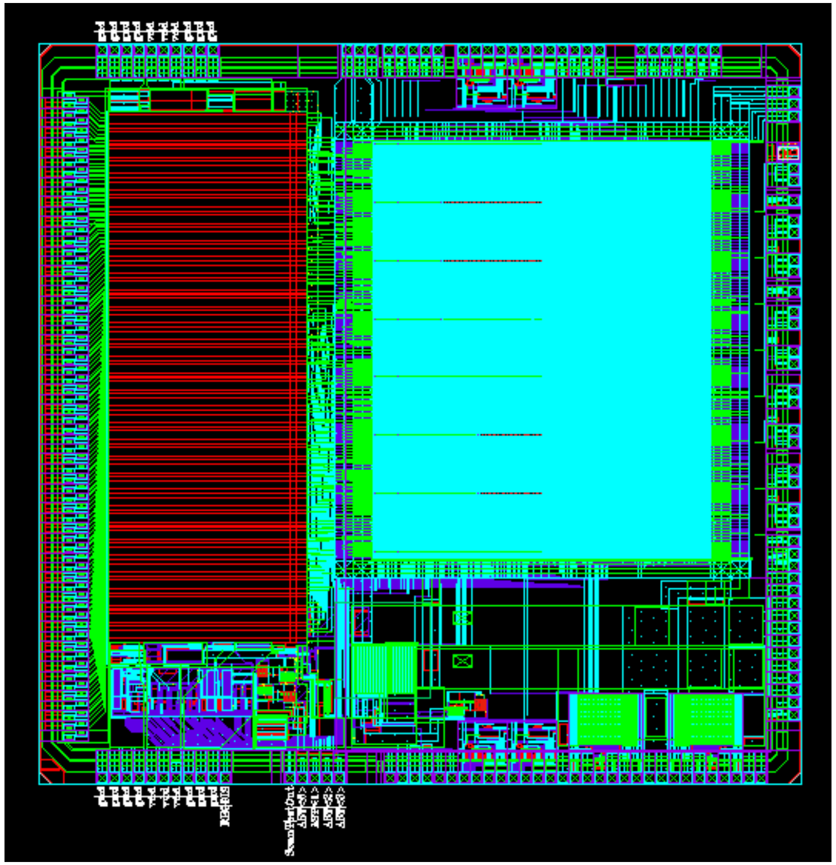


- *Annealing corrections included (CCE reduced by 20%/10%)*
- *NIEL appears to work for charge collection with n-in-p FZ detectors*
- *Micron and Hamamatsu Photonics sensors consistent over measure fluence range*
- *Signal-to-noise ratio ~13 (barrel 4, innermost strip layer)*

ABCN-25

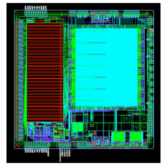


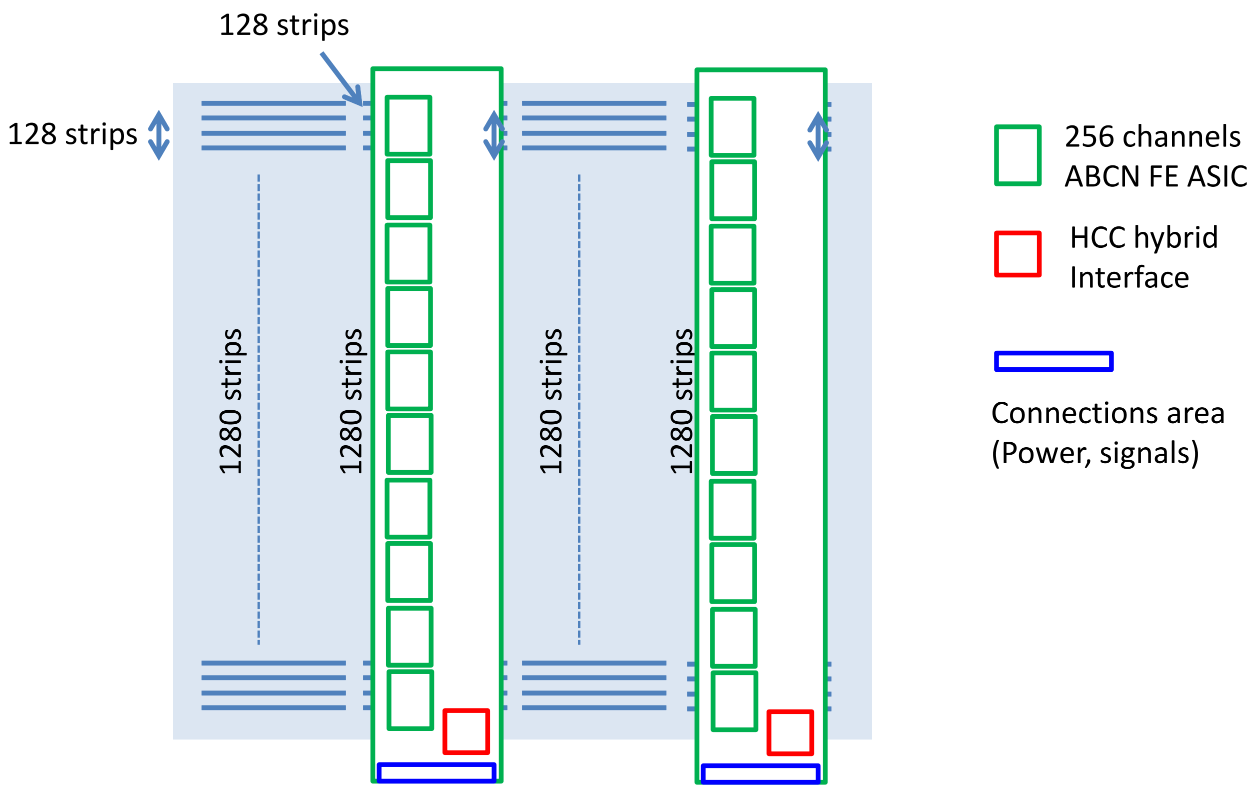




- ABCN-25 ASIC (250 nm IBM CMOS6 technology)
  - binary architecture; 128 channels; internal calibration circuit; both signal polarities; linear voltage regulator on-chip, shunt regulator
  - pipeline length 6.4 μs; two clock shema (40/80 MHz)

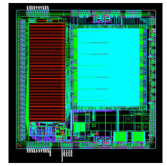
ABCN-130



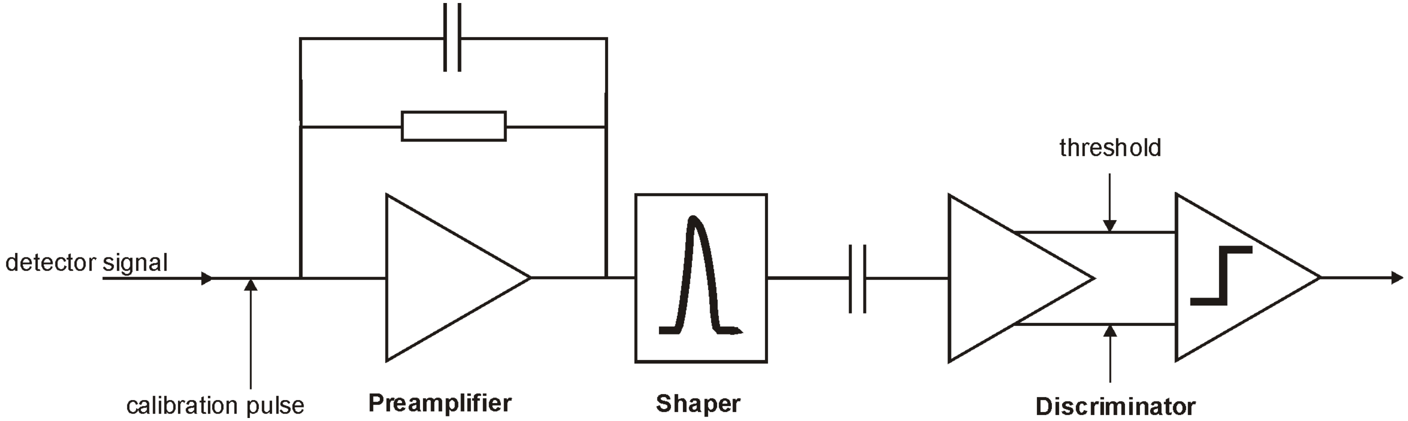


- ABCN 130 nm Front-End ASIC (end 2012)
- Realistic power scheme (1.3 V instead of 2.5 V)
- 256 channels (strips) instead of 128 per ASIC (material reduction)
- Major changes:
  - L0/L1 data-flow control (Track Trigger)
  - Fixed-size data-packet format (1 or 2 cluster /packet, robust against harsh environment)

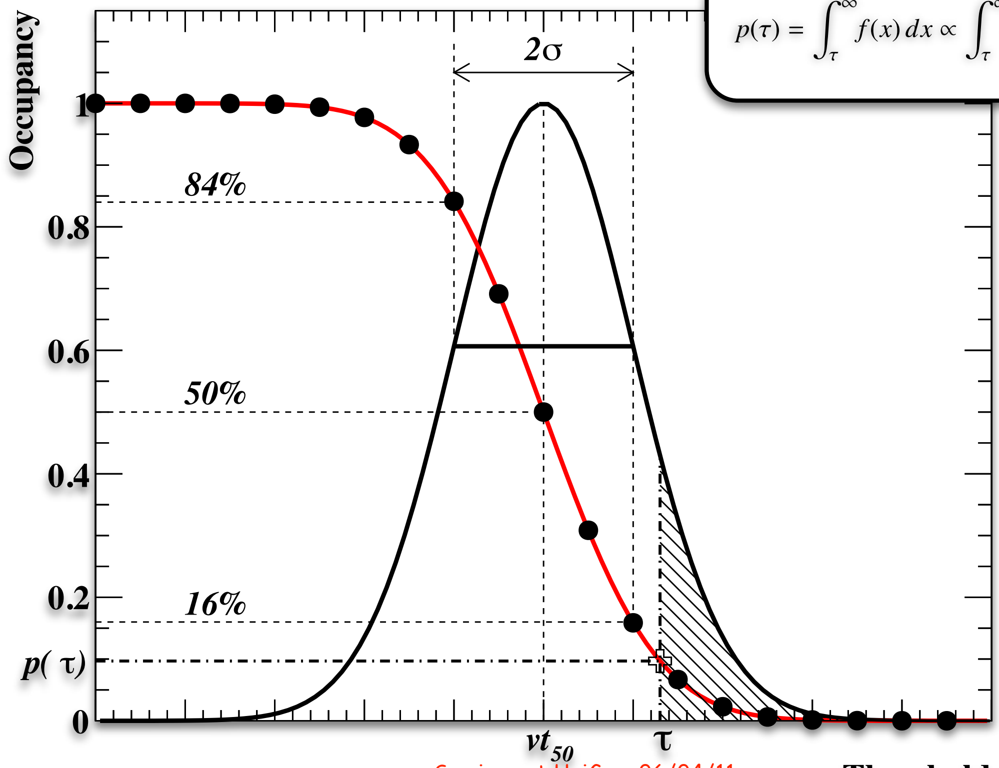
Front-end calibration



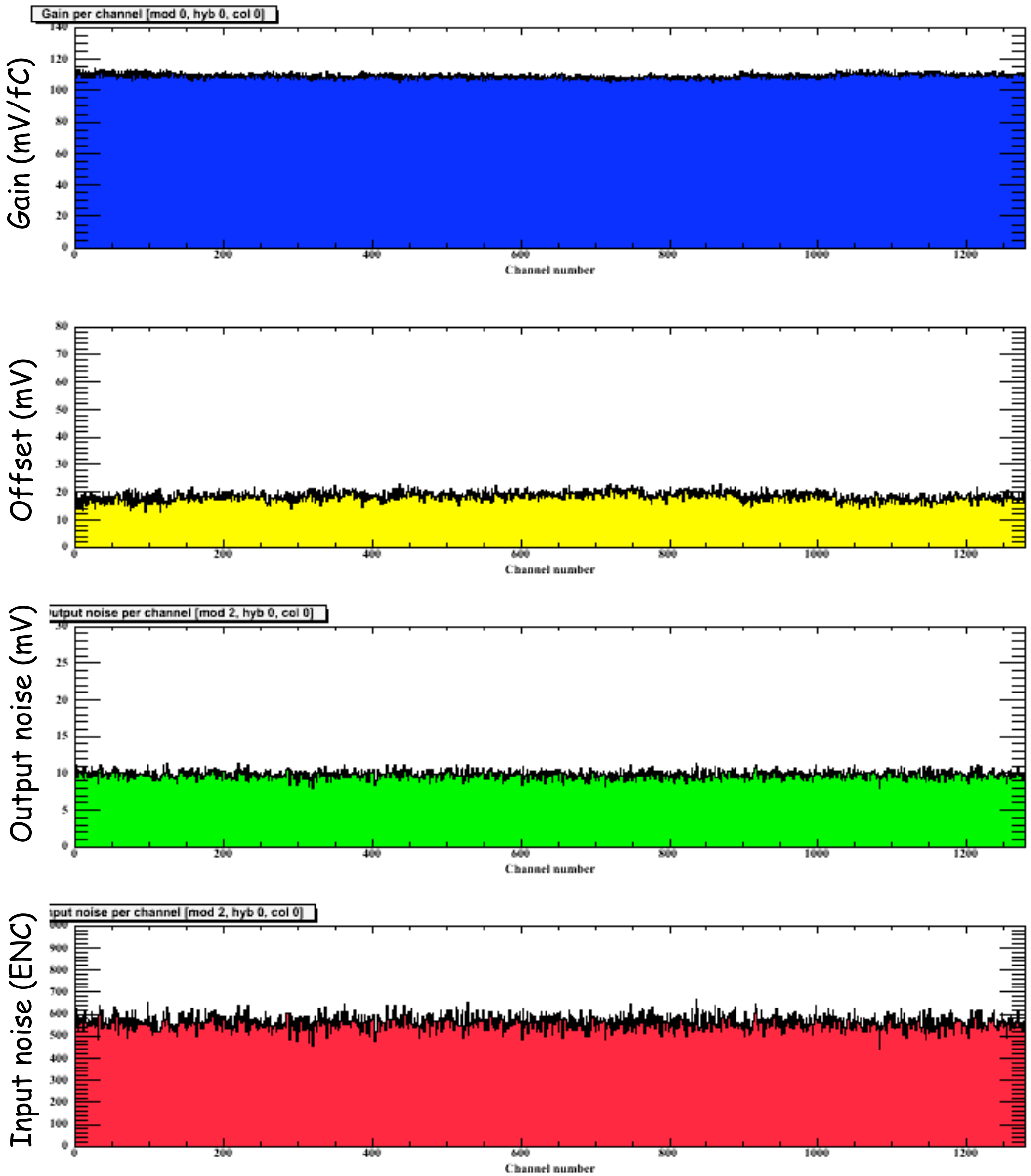
- Per-channel calibration circuitry

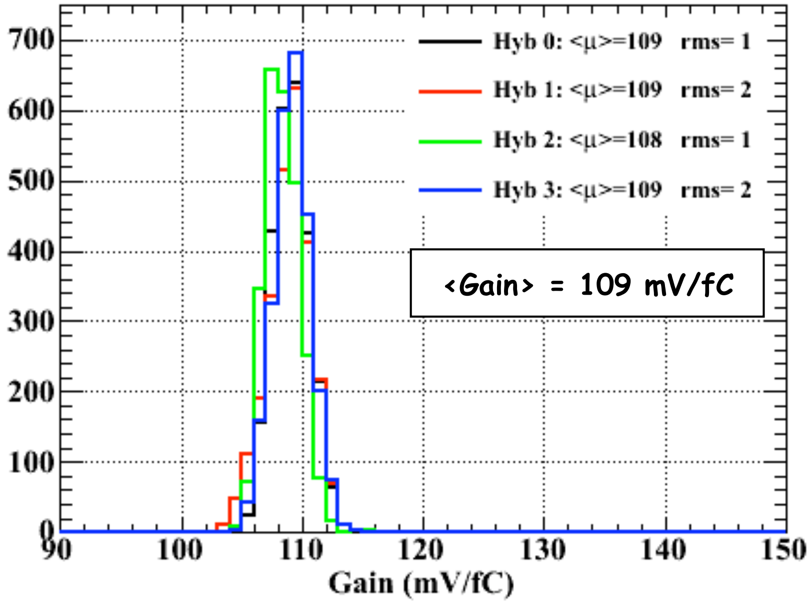


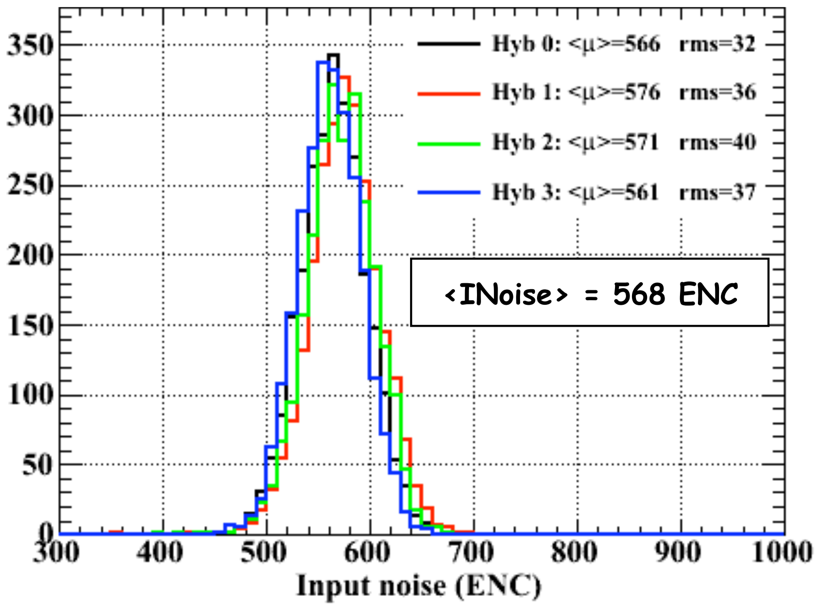
$$p(\tau) = \int_\tau^\infty f(x)\,dx \propto \int_\tau^\infty \exp\left[-\frac{(x-\mu)^2}{2\sigma^2}\right] dx \propto \mathrm{erfc}\left(\frac{\tau-\mu}{\sqrt{2}\sigma}\right)$$



Electrical results: input noise

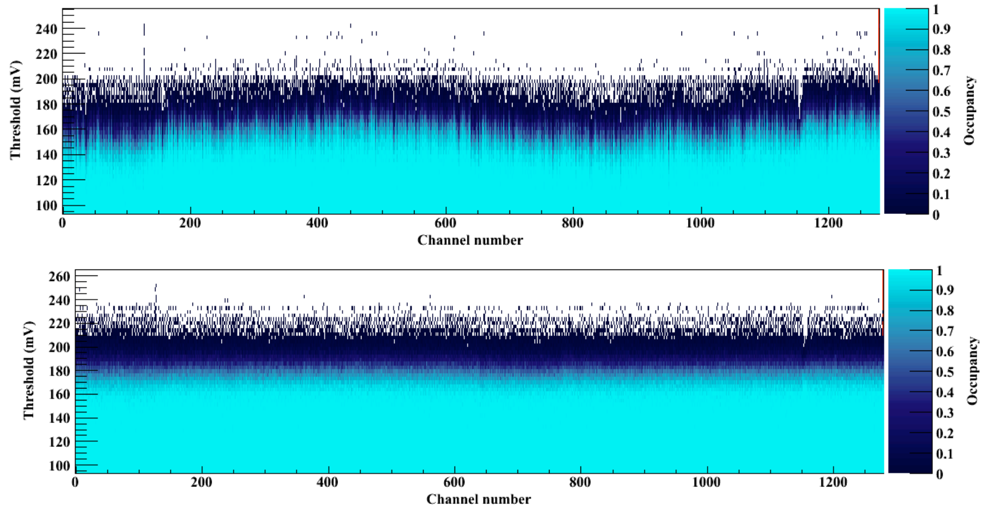




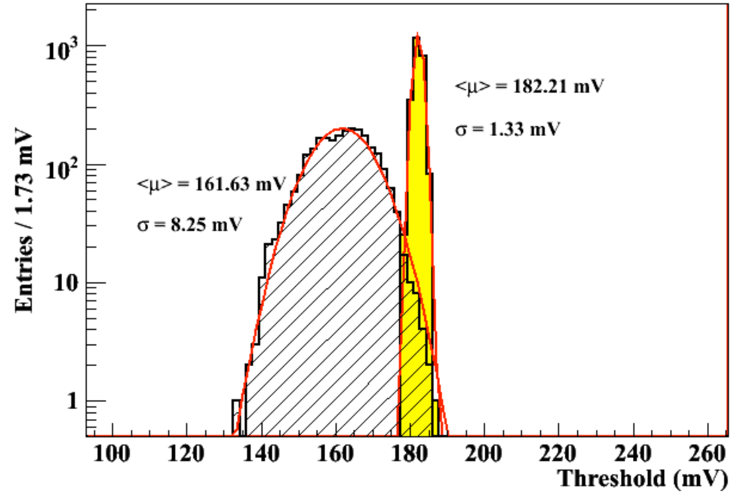


Threshold uniformity and noise occupancy

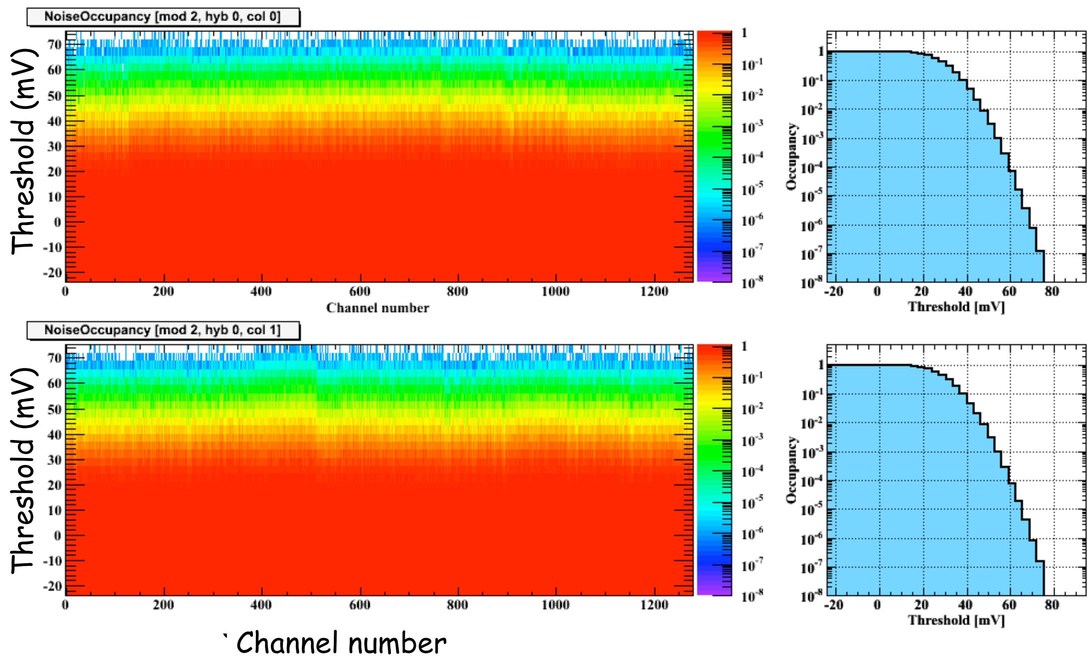
- Trimming procedure
  - threshold uniformization through individual channel threshold corrections

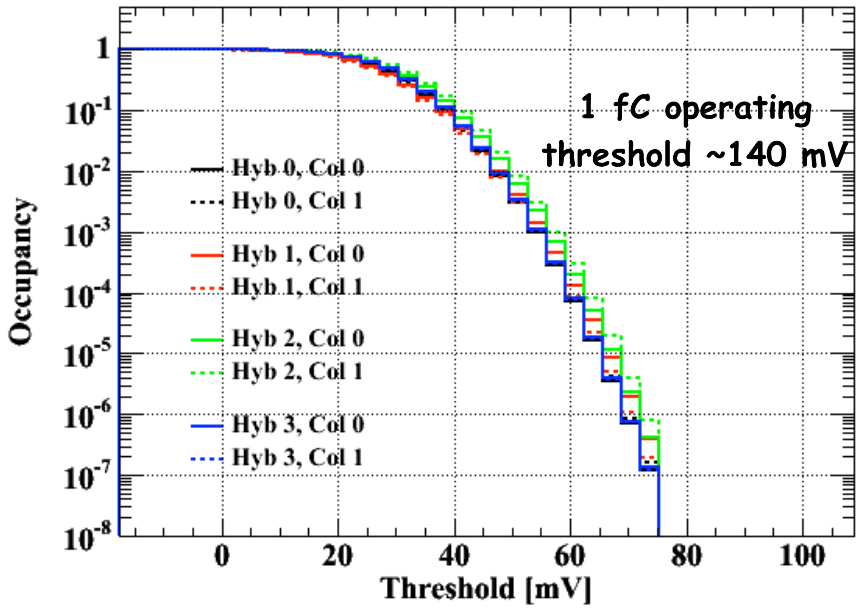


Distributions of vt50 threshold points H1
(all channels in hybrid) before and after trimming

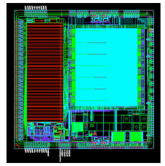


- Noise occupancy test





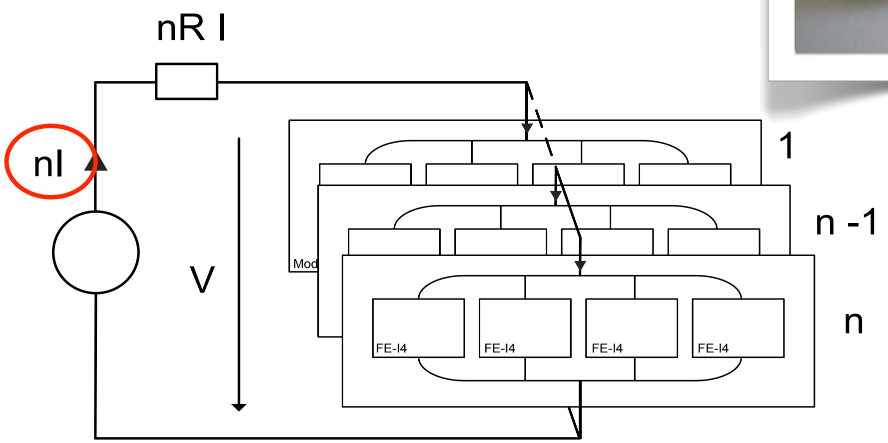
Powering options



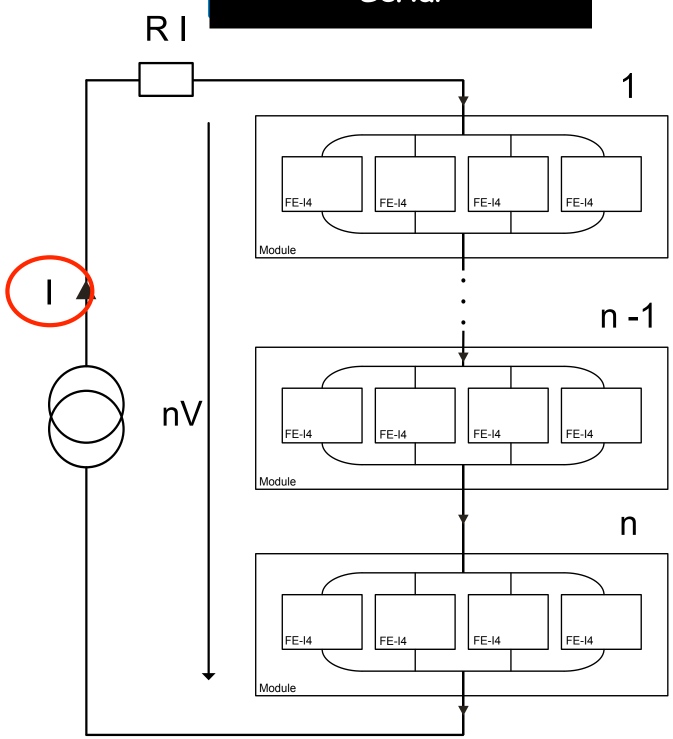
- Current LHC trackers: direct powering
  - high power losses in the cables + significant contribution to material budget

- At the SLHC, assuming 130 nm CMOS ASICS instead of 250 nm
  - almost same total FE power (~ 40-60 kW)...
  - ... but 2-4 times higher total current (30-50 kA) with fixed cable cross-section
  - Need to transmit power at lower current
  - Solutions:
    - Serial powering
    - DC-DC conversion

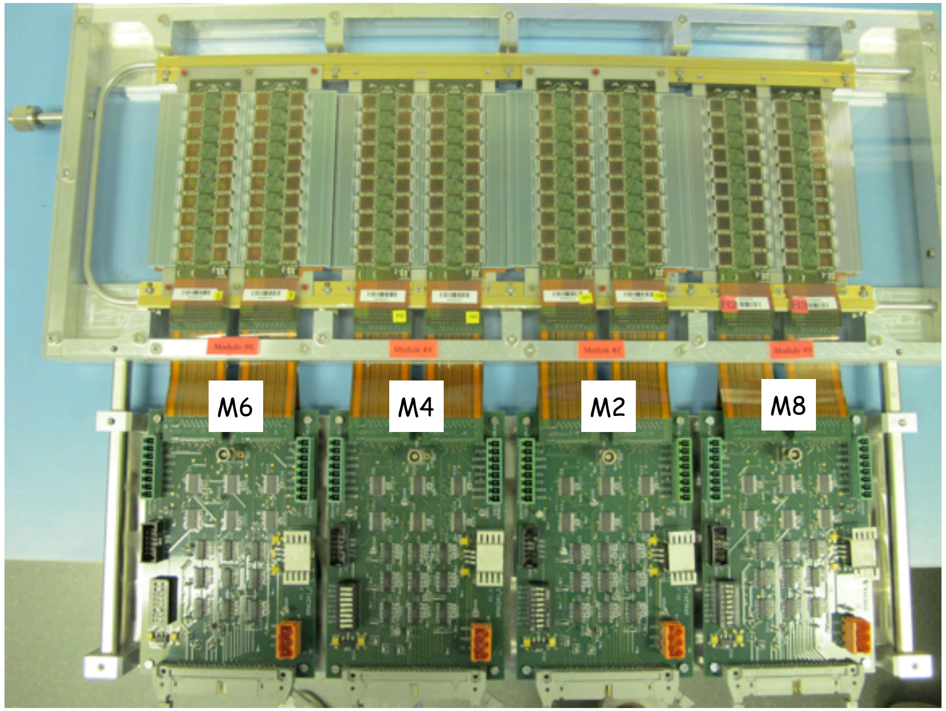
Parallel

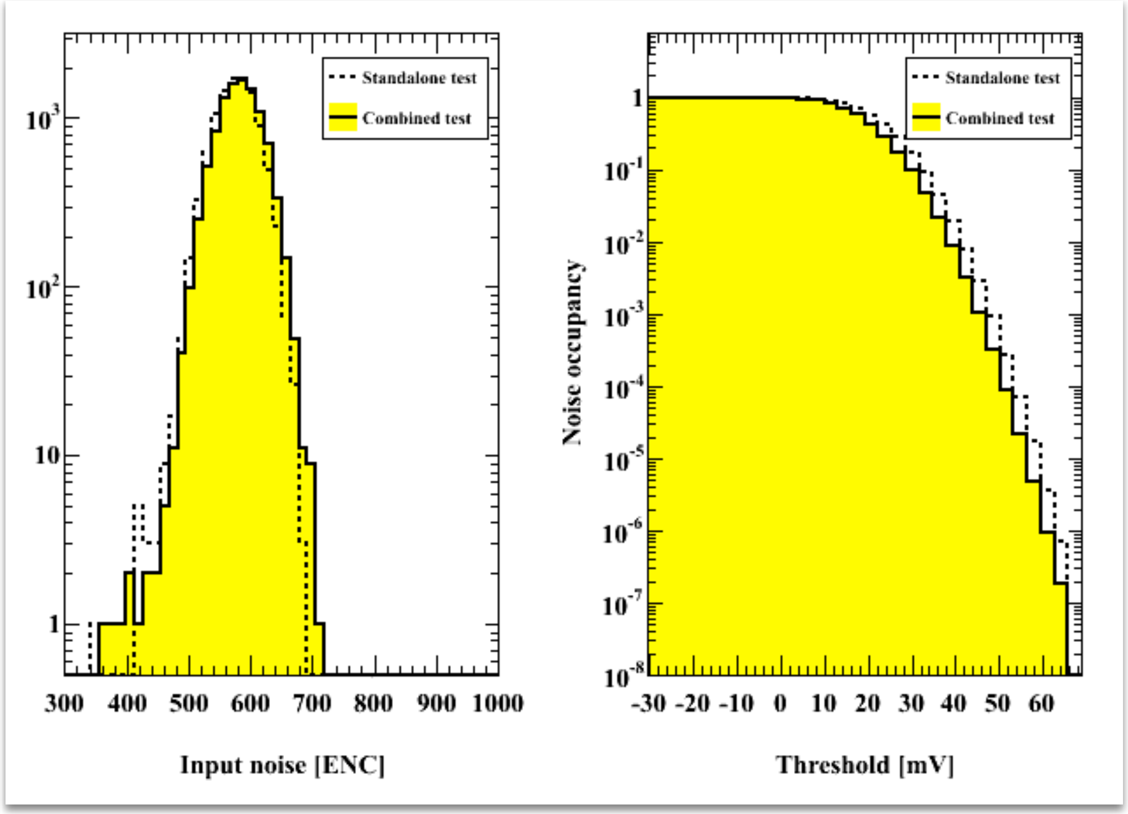


Serial

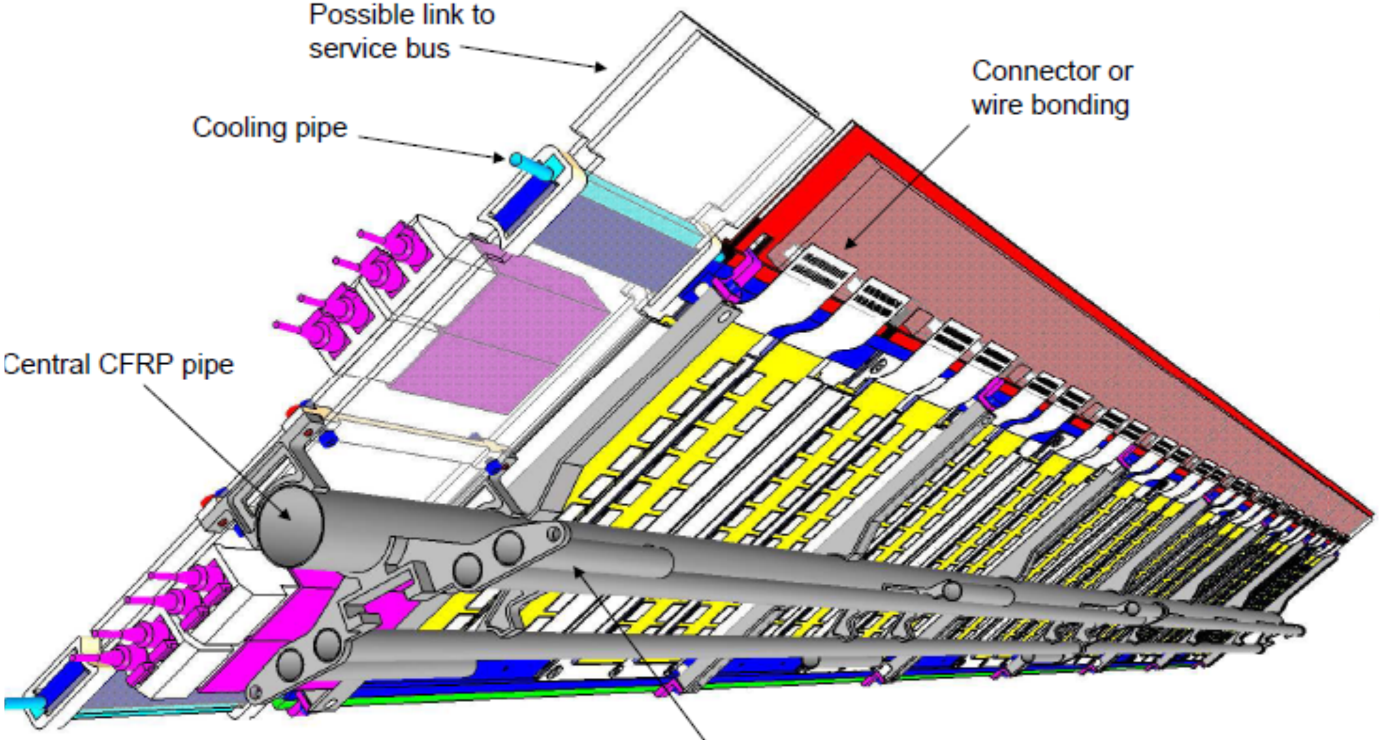


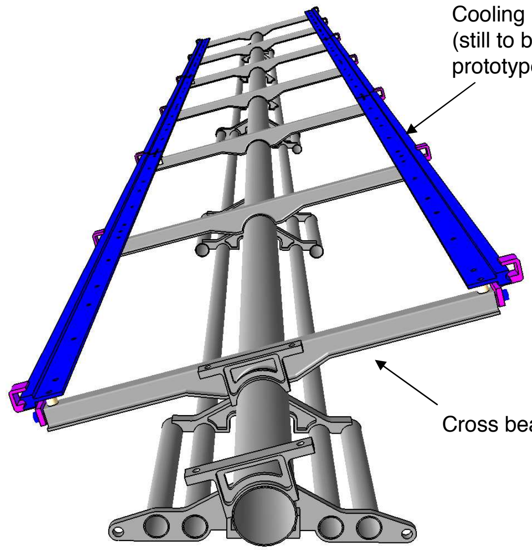
Multi-module systems

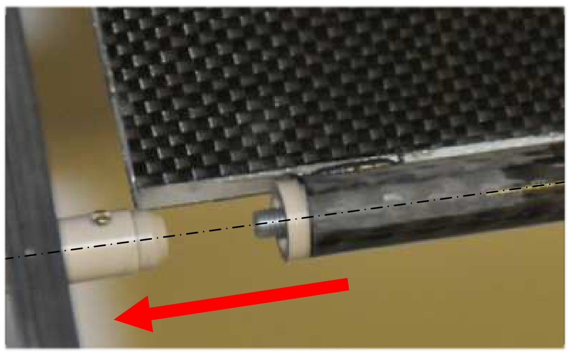


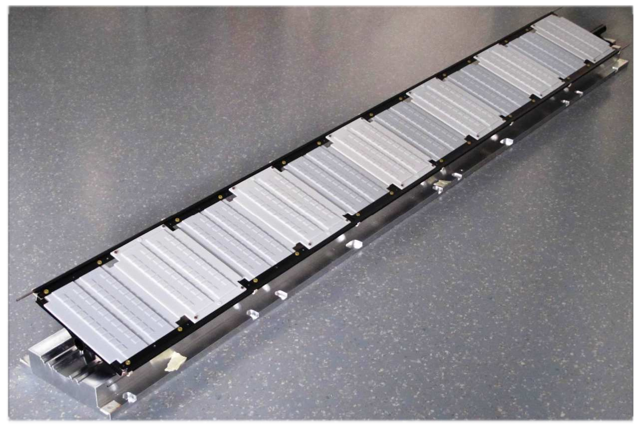


Local support and integration









Summary

- The ATLAS experiment is a wonderful detector that is currently making impressive measurements

- Meanwhile discoveries arrive, the R&D phase for a high-luminosity collider has started and is progressing rather fast
  - though many uncertainties still, simulation is crucial !!!

- Major upgrades for ATLAS are expected, in particular for the tracker
  - fourth Pixel layer IBL
  - completely new silicon inner tracker
  - track-trigger ?

- ATLAS will (of course) be ready for its upgrade in ~2021
  - target is ~3000 fb^{-1}

- A new decade of, hopefully, exciting new measurements, will be ahead of us !!

Thanks for attending !!