



The CMS pixel detector in LS1: a surprise with a happy end

Séminaires de physique corpusculaire
DPNC , 21. Sept 2015

R. Horisberger, PSI

on behalf of BPIX repair groups

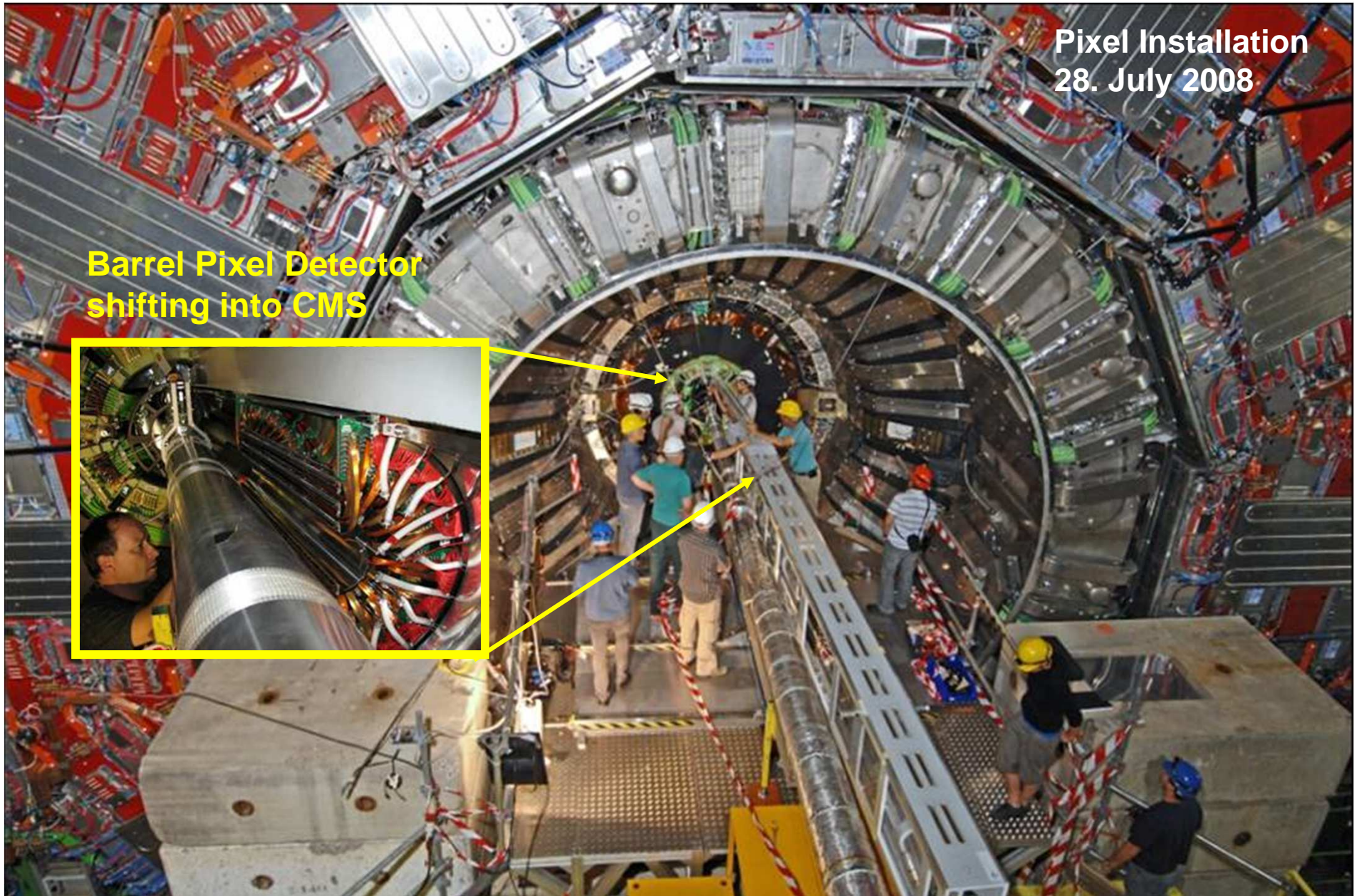
PSI : *W. Bertl, W. Erdmann, R.H., H-C. Kästli,
D. Kotlinski, B. Meier, T. Rohe, S. Streuli*

ETHZ : *A. Starodumov, M. Takahashi*

Uni ZH : *L. Caminada, A. De Cosa*

Pixel Installation
28. July 2008

Barrel Pixel Detector
shifting into CMS



Measured resolution

$$\sigma_{r\phi} = 13\mu\text{m}$$

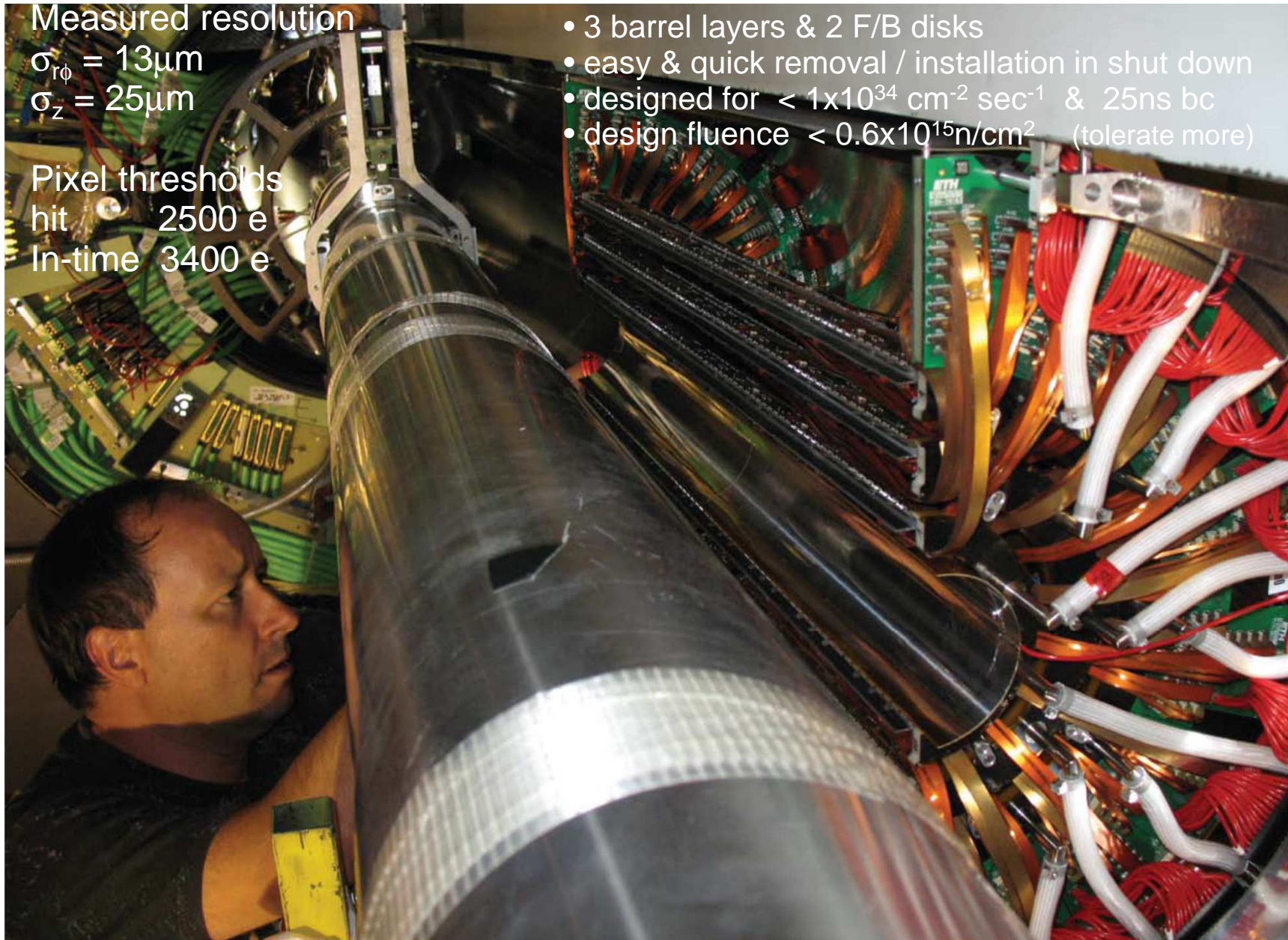
$$\sigma_z = 25\mu\text{m}$$

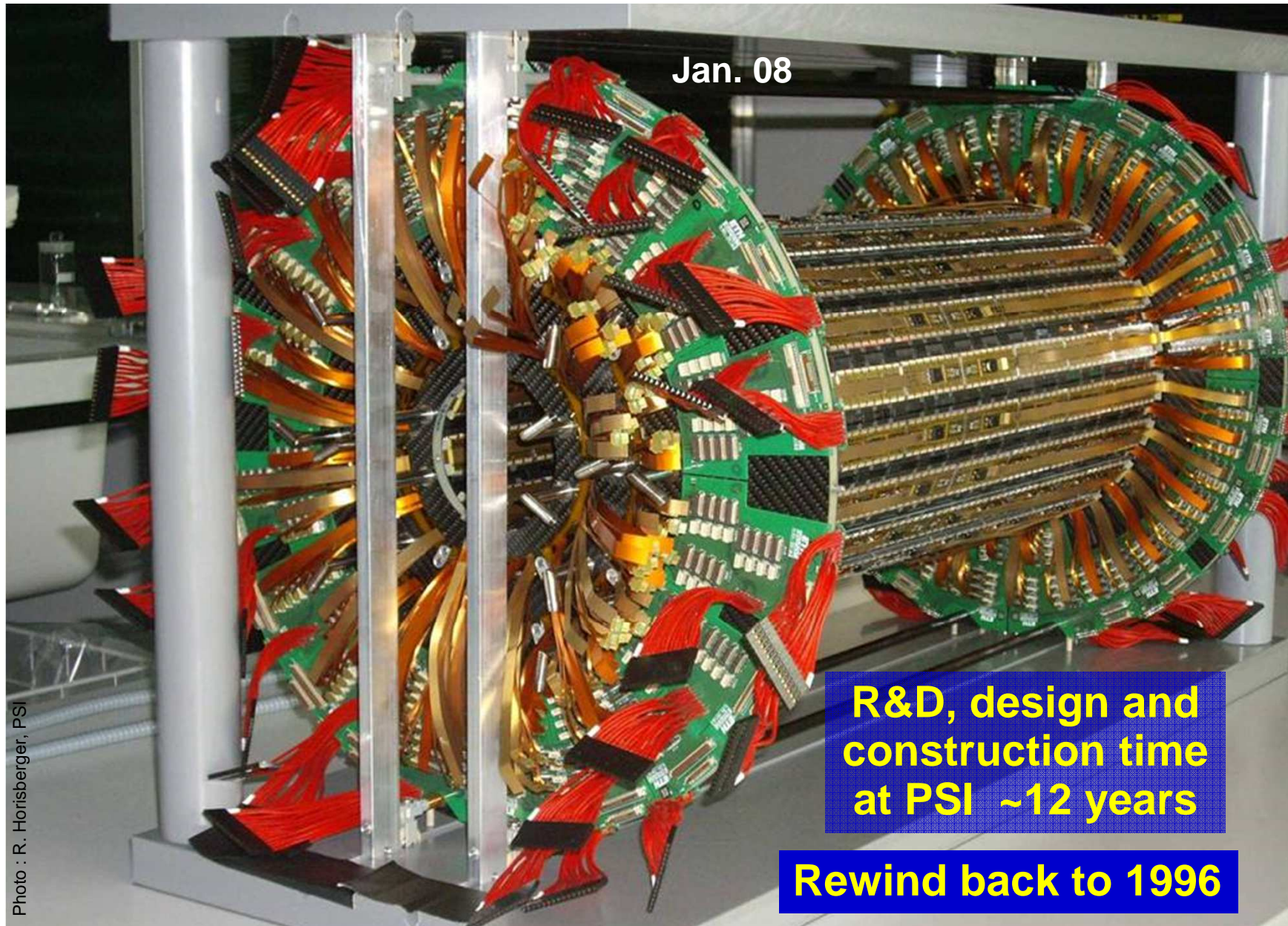
Pixel thresholds

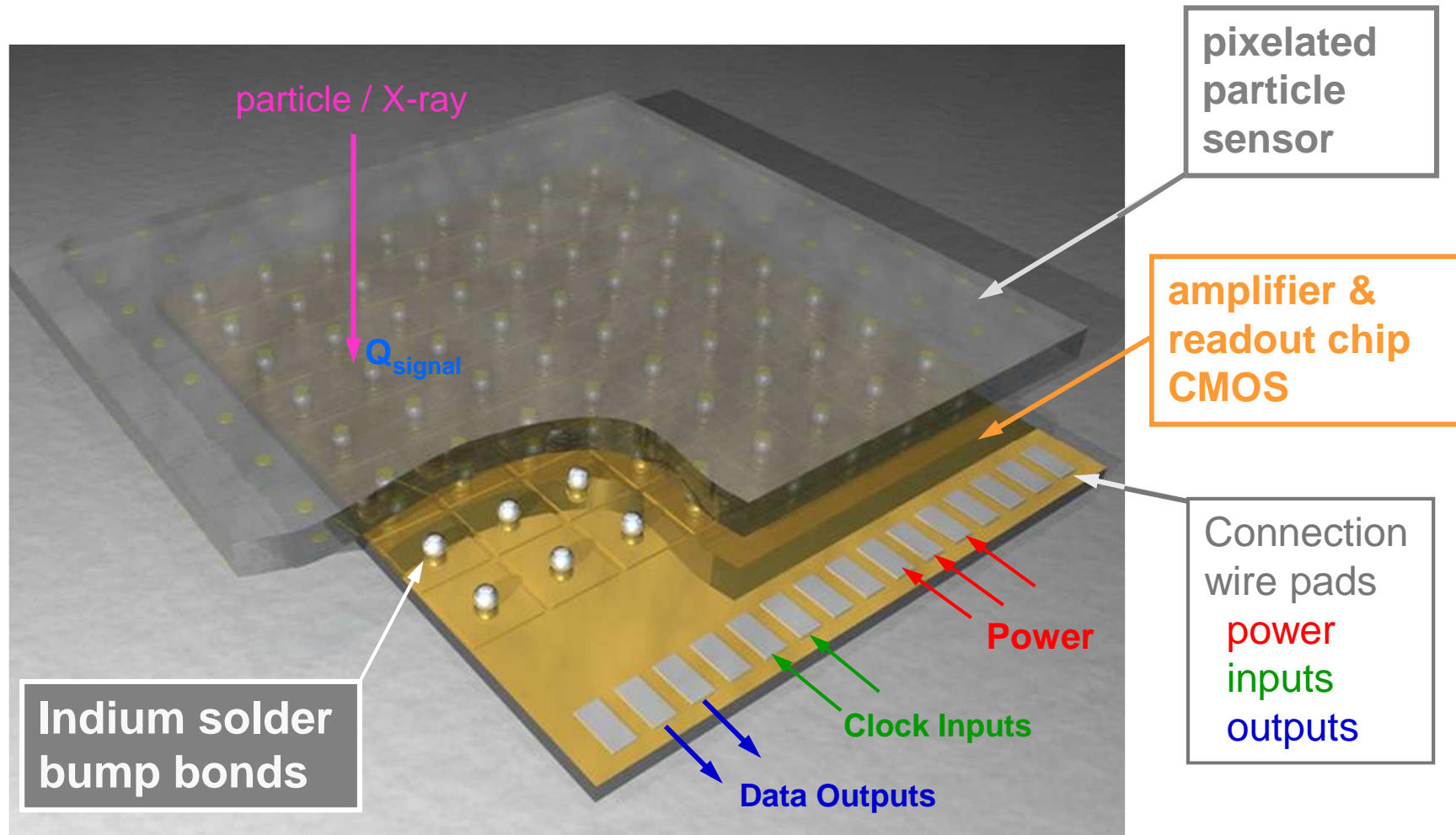
hit 2500 e

In-time 3400 e

- 3 barrel layers & 2 F/B disks
- easy & quick removal / installation in shut down
- designed for $< 1 \times 10^{34} \text{ cm}^{-2} \text{ sec}^{-1}$ & 25ns bc
- design fluence $< 0.6 \times 10^{15} \text{ n/cm}^2$ (tolerate more)





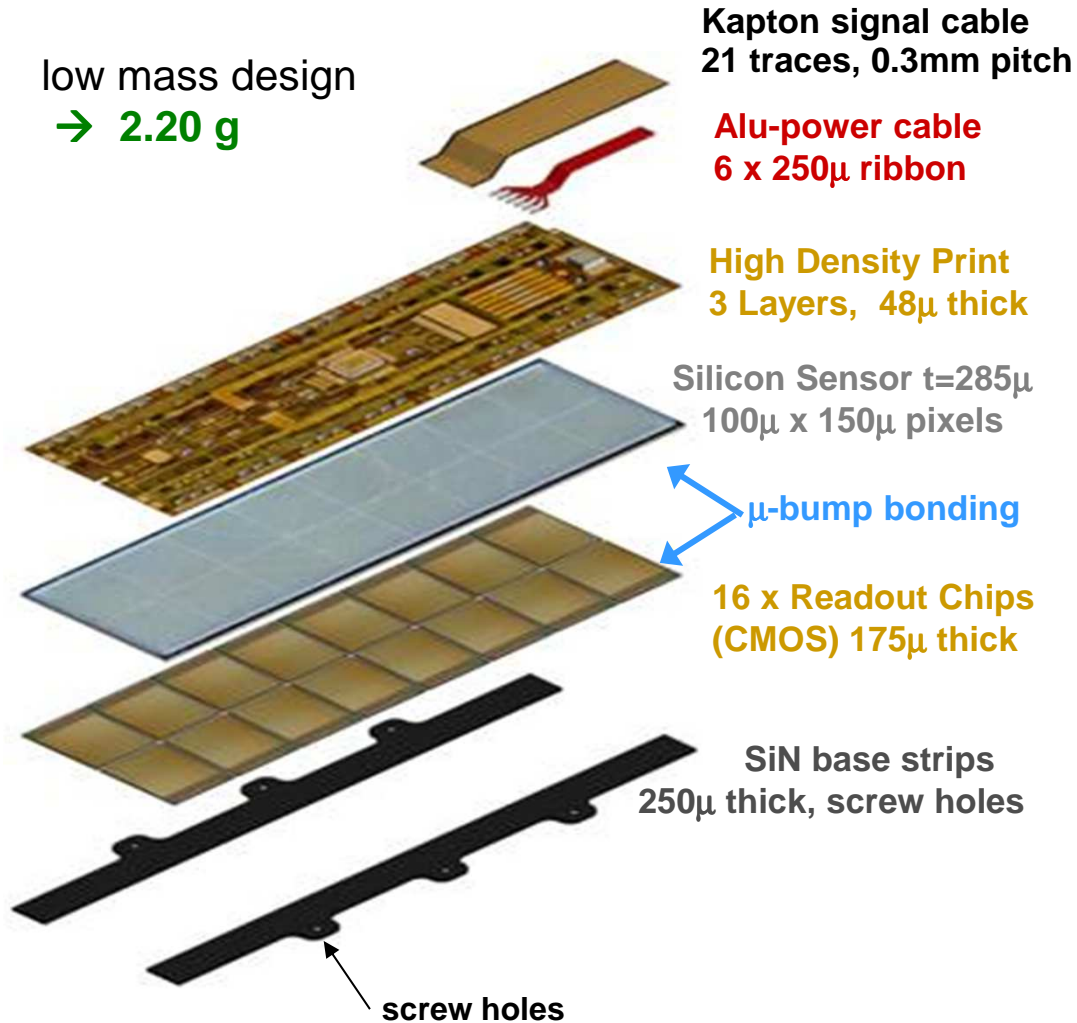


particle / X-ray → signal charge → amplifier → readout → digital data

Module Construction

low mass design

→ 2.20 g



In **1996**, completely crazy project:

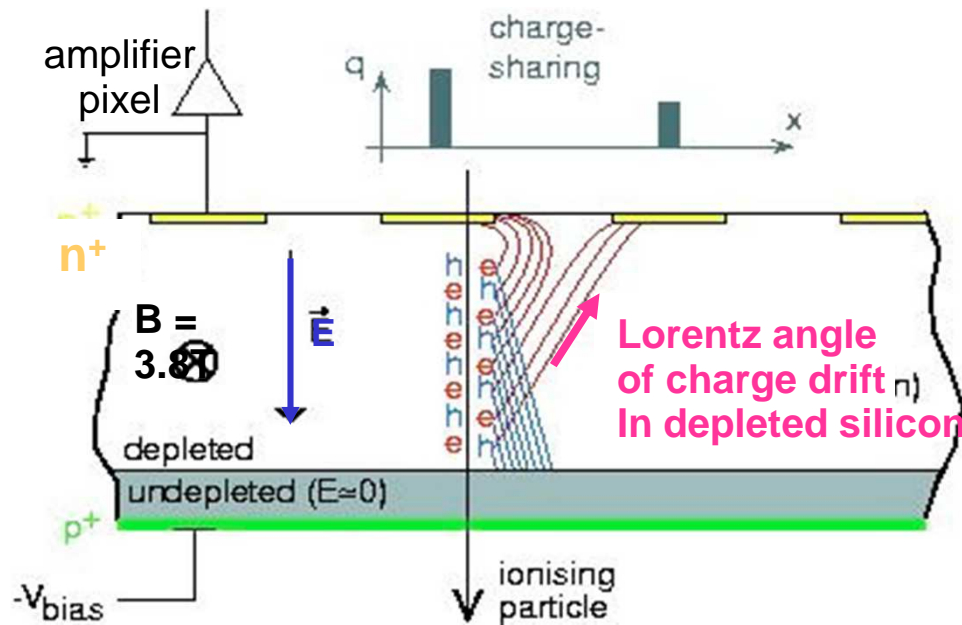
Major uncertainties about:

- 1) rad. hard silicon pixel sensors
for particle fluences to 10^{15} p/cm²
 - signal charge? trapping ?
 - Lorentz angle ?
 - depletion & type inversion ?
 - HV robustness ?
- 2) micro-bump bonding
 - feasibility for <20 μ bumps ?
 - **costs ? → budget ?**
- 3) Pixel Read Out Chip (ROC)
 - low power design, speed ?
 - low pixel noise & thresholds ?
 - rad. hardness? (>100KGy) **costs?**
- 4) Data Rates & Readout
 - 10 Tbit/sec raw data rates
 - ? ? ? ? ? ? ? ? ? ?
- 5) 6).... **Physics performance?**

Sharing of signal charge
by Lorentz angle

ROC with analog pixel readout
→ position interpolation (η -algorithm)

Pixel size $100\mu \times 150\mu$
→ precision coordinates $\sim 10\text{-}20\mu$

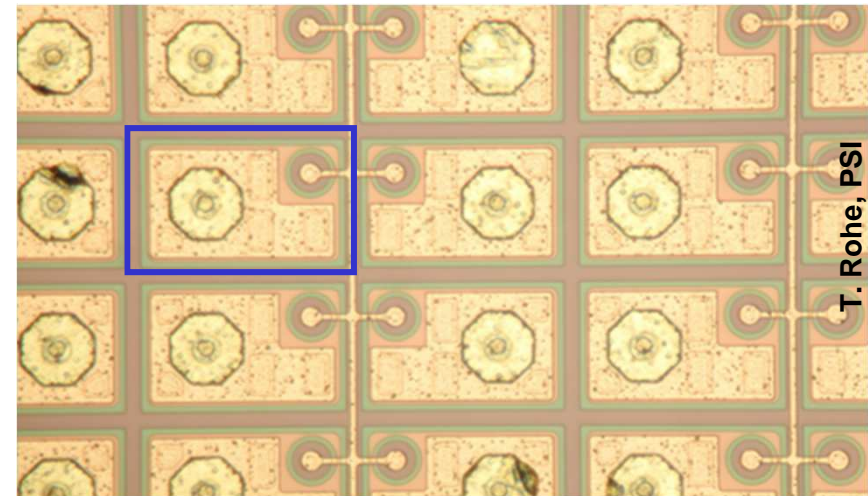


Sensor R&D (PSI)

Design of masks (PSI)

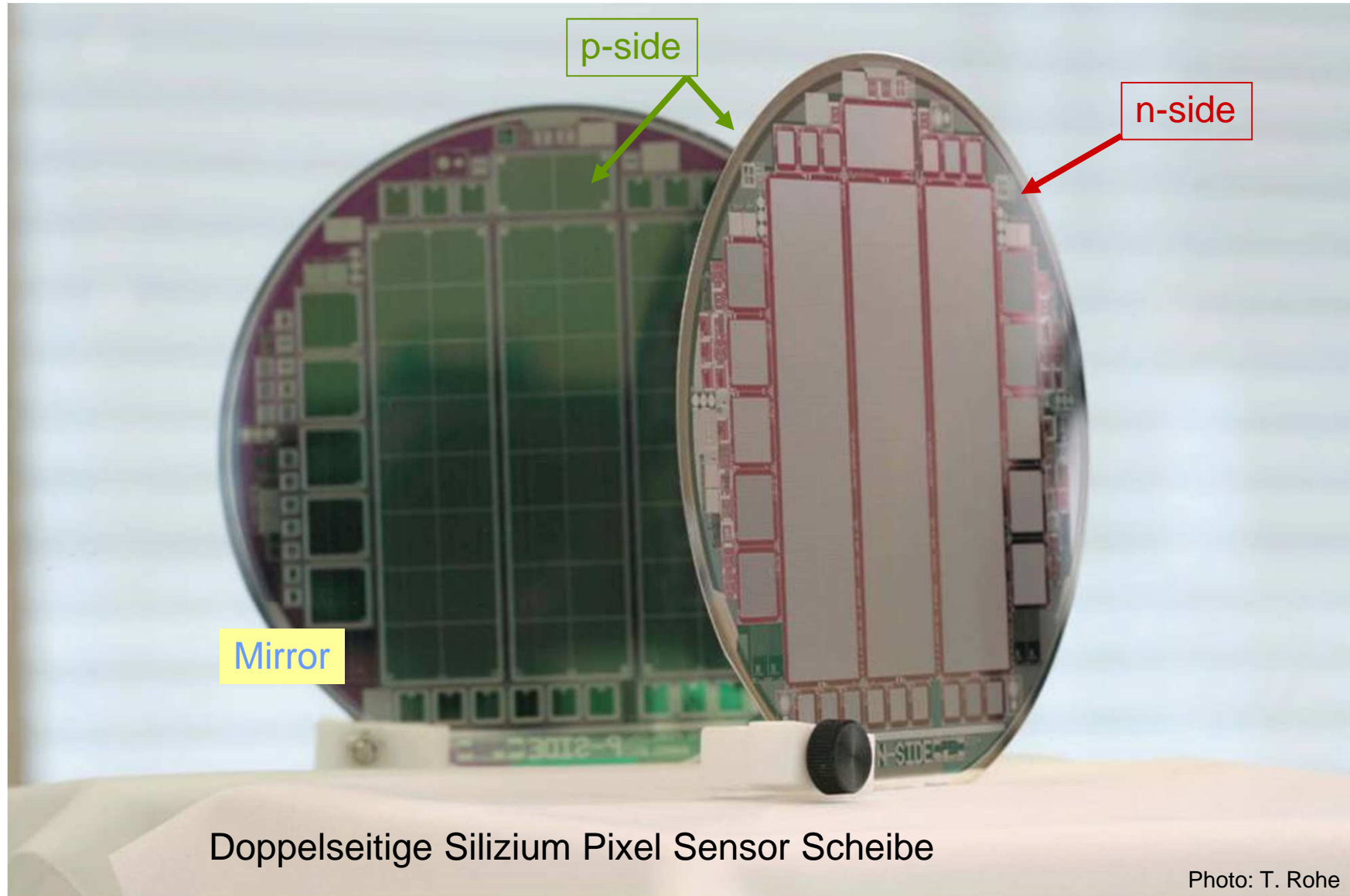
Electrical qualification (PSI)

Sensor test beam @ CERN (UZH, PSI)

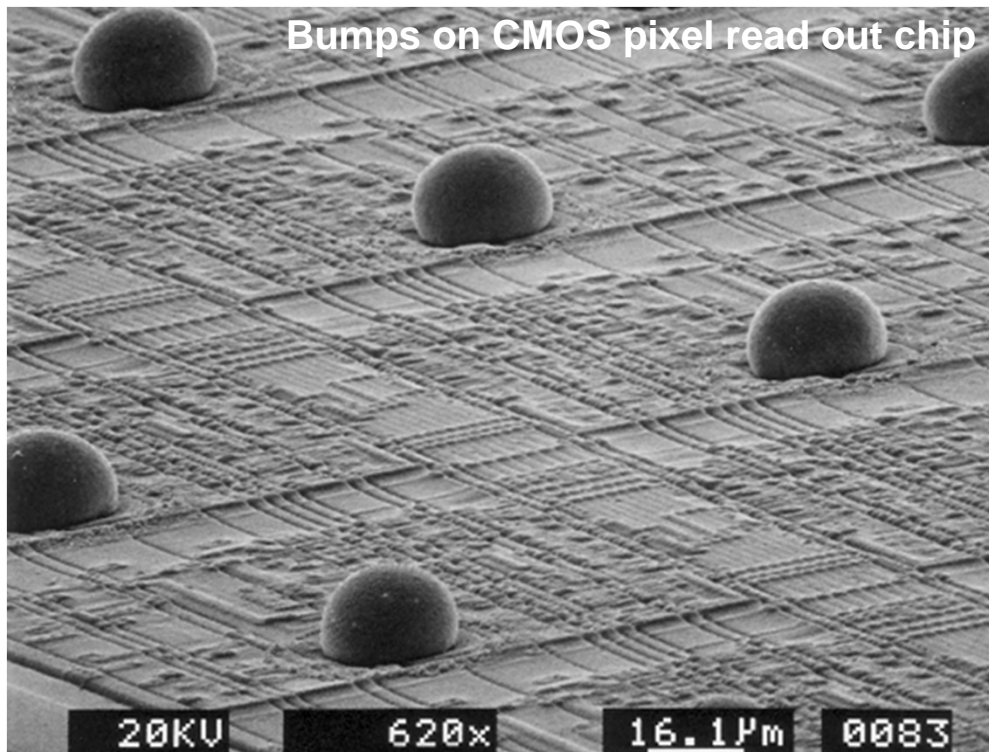


Silicon sensor production

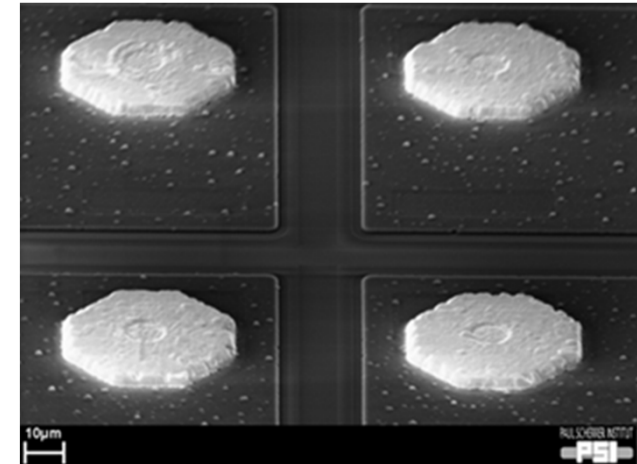
→ CIS, Erfurt Germany



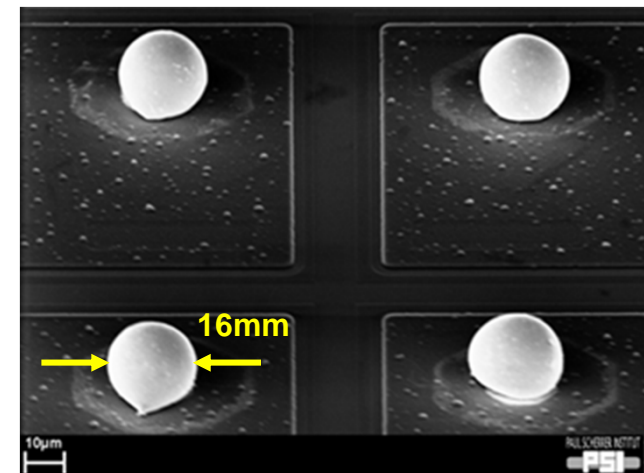
- connecting pixel sensors with ROC electronics
- connection density up to 10'000/cm²
- technique developed at PSI (LMN)
- licensed to spin-off company DECTRIS



Indium “cakes” before reflow



↓ reflow

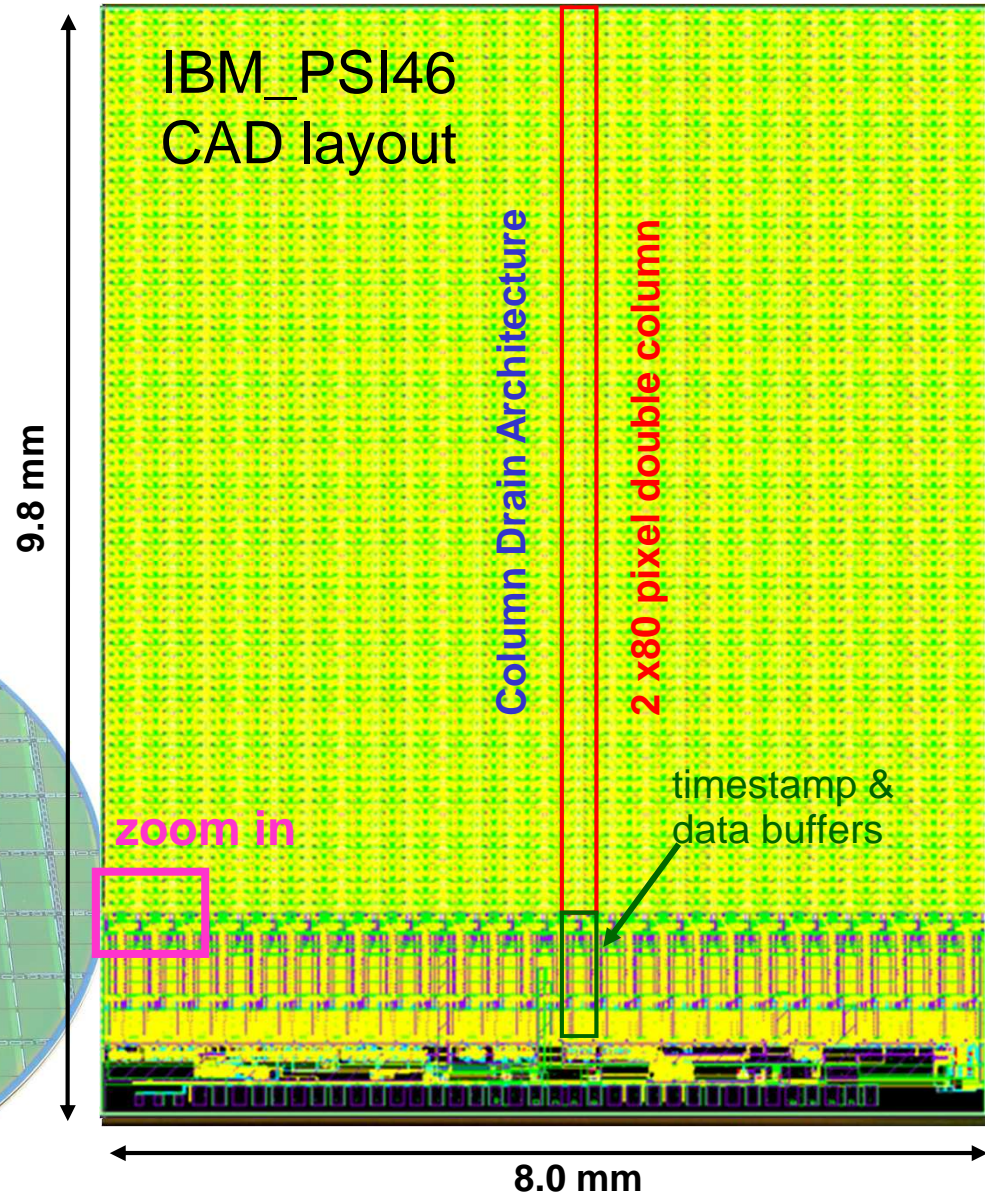
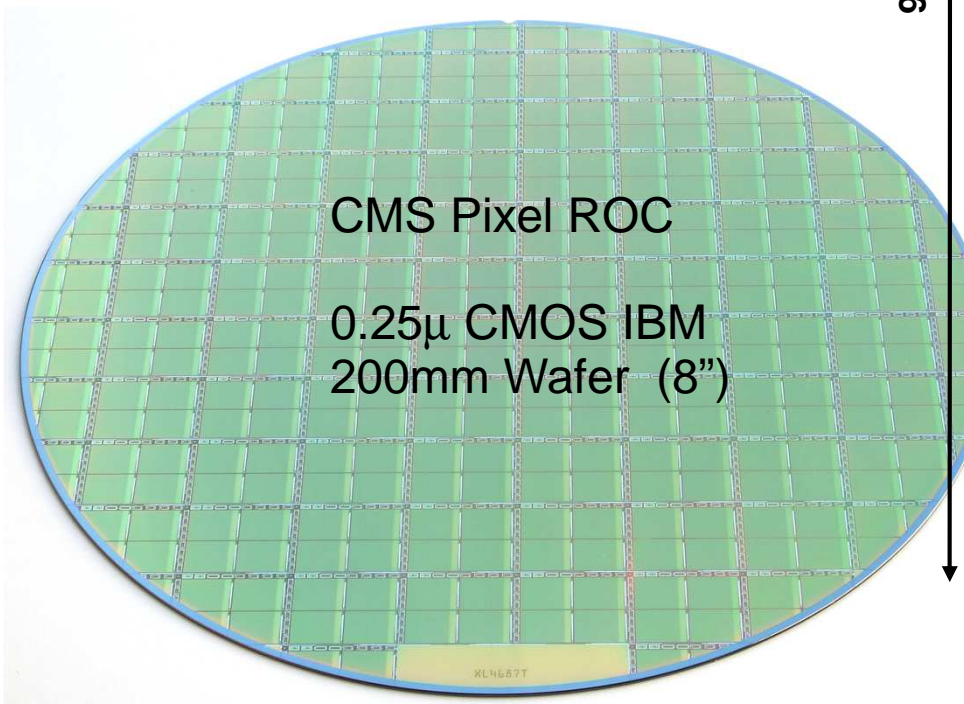


Indium balls after reflow



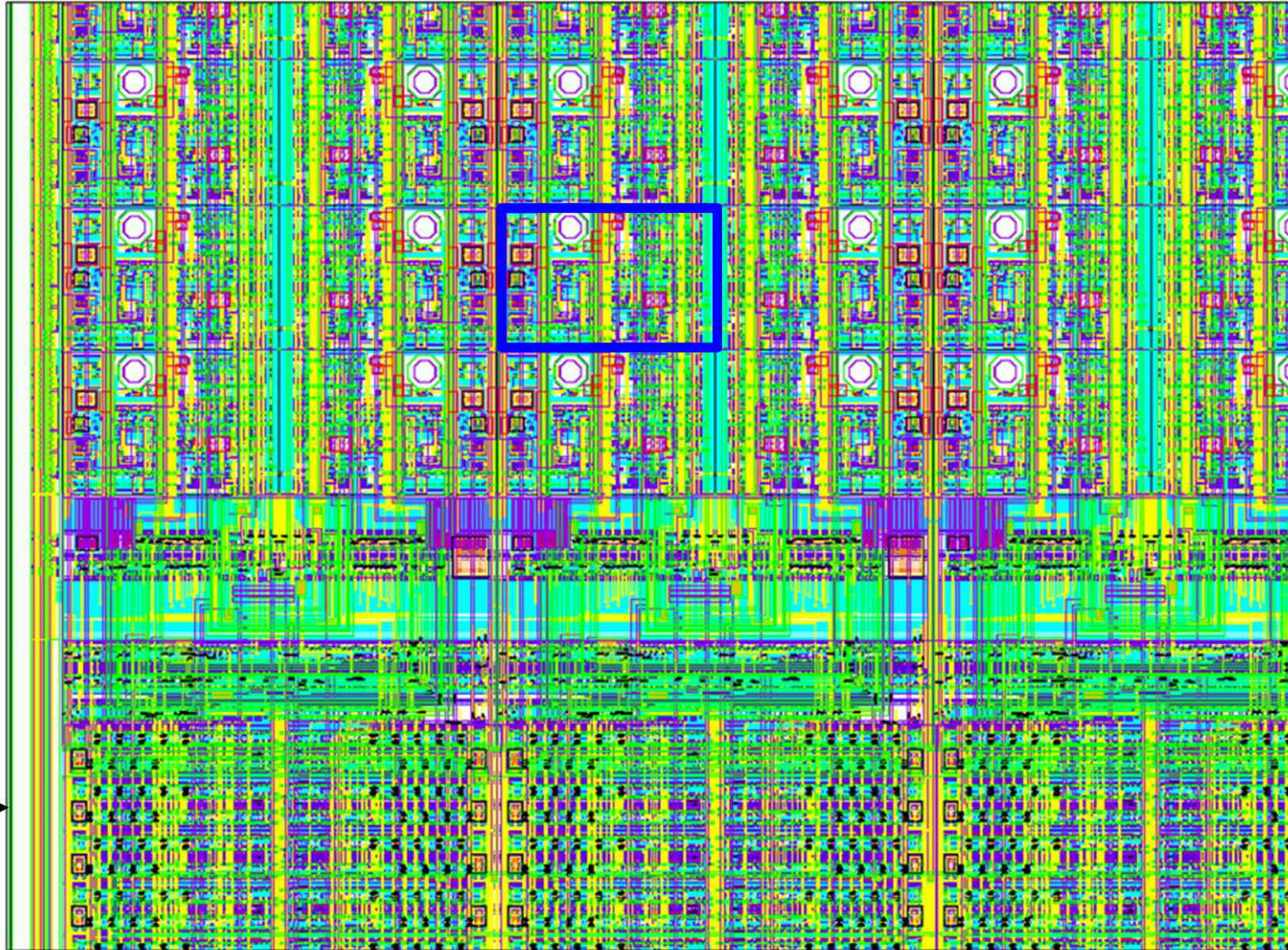
CMS Pixel Read Out Chip

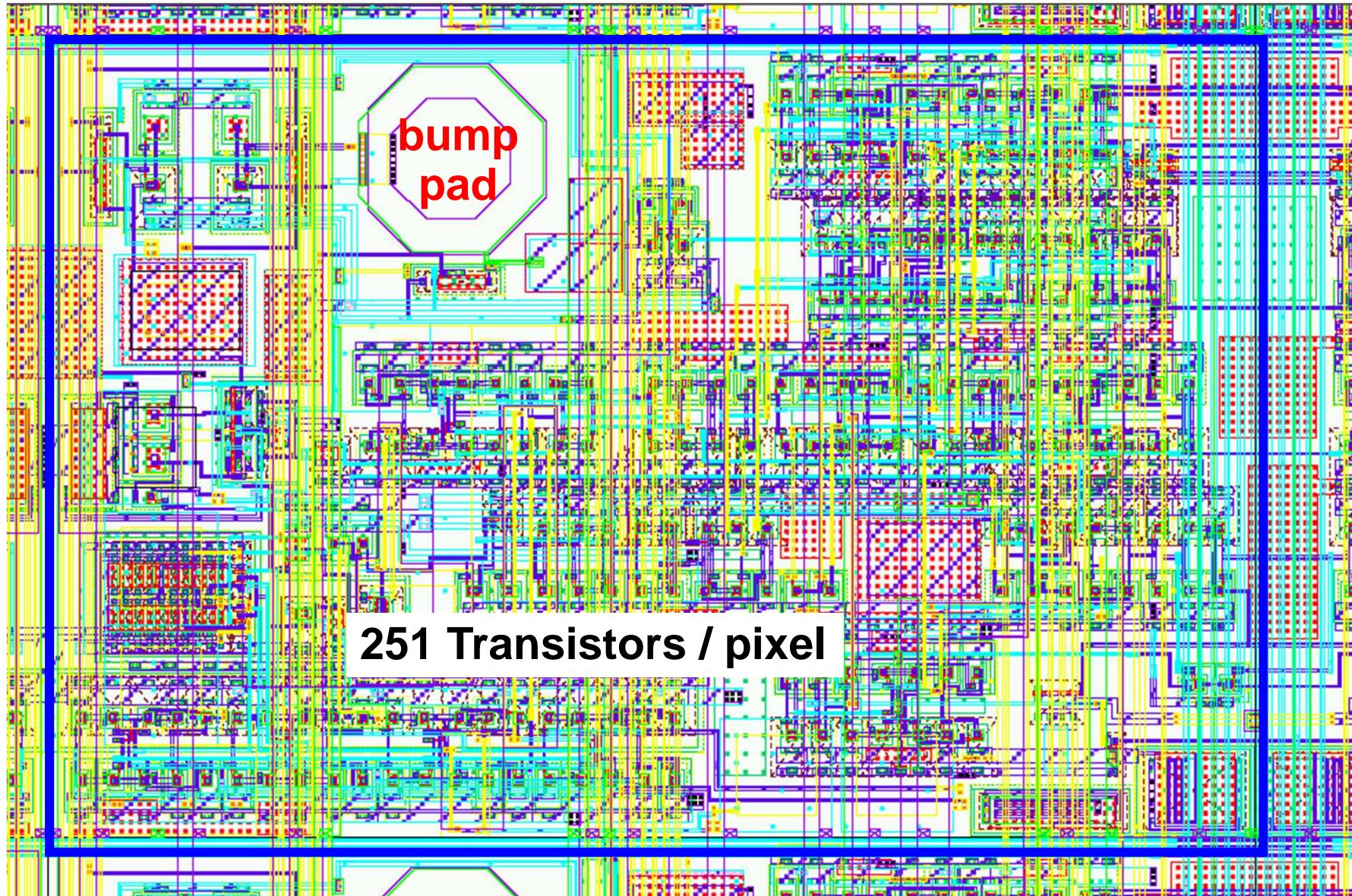
- pixel size $100\mu\text{m} \times 150\mu\text{m}$
- **analog pulse height readout**
- **251 transistors /pixel**
- **$35\mu\text{W}/\text{pixel}$ (very low power)**
- operating **pixel threshold = 2500 e**
- radiation hard design ($\sim 1\text{MGy}$)
- **complete design by PSI group**

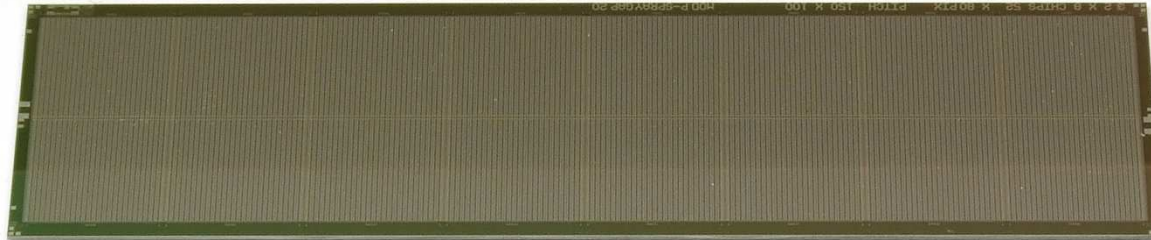


Pixel ROC Zoom (1)

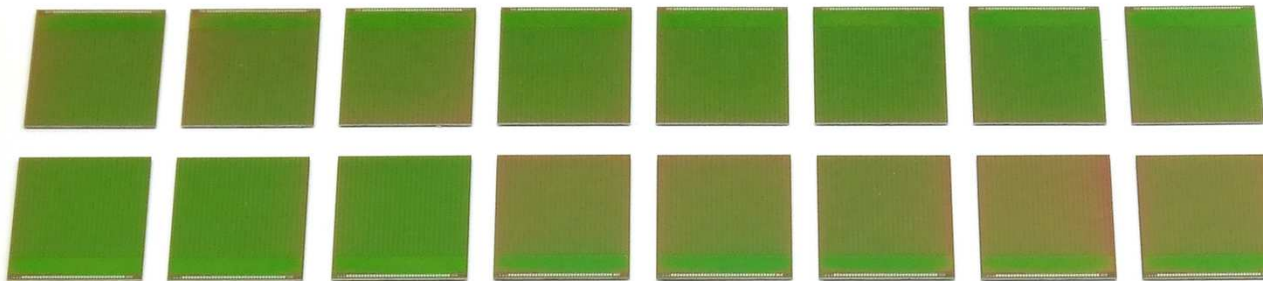
butting chip side, cut within 50μ of transistors !



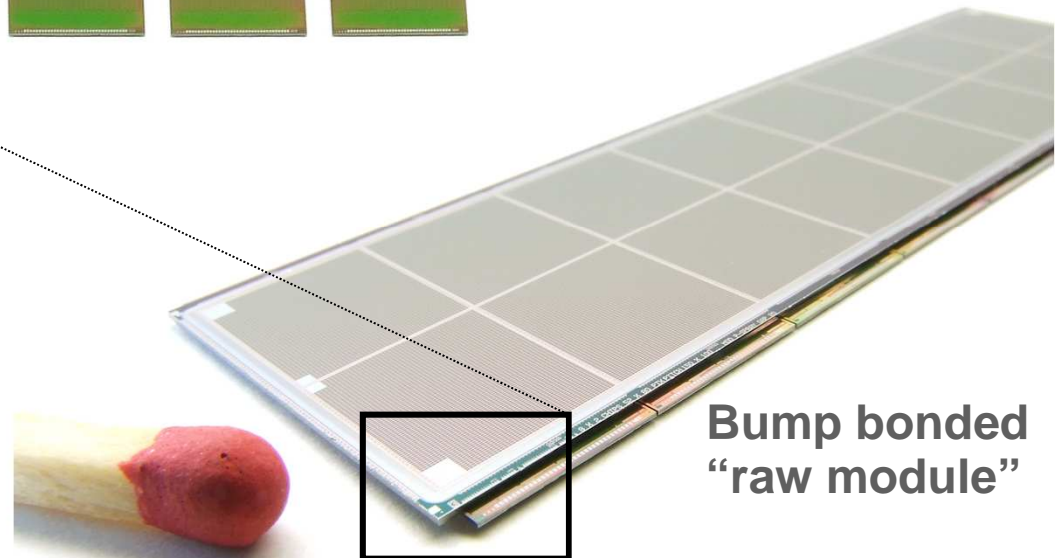
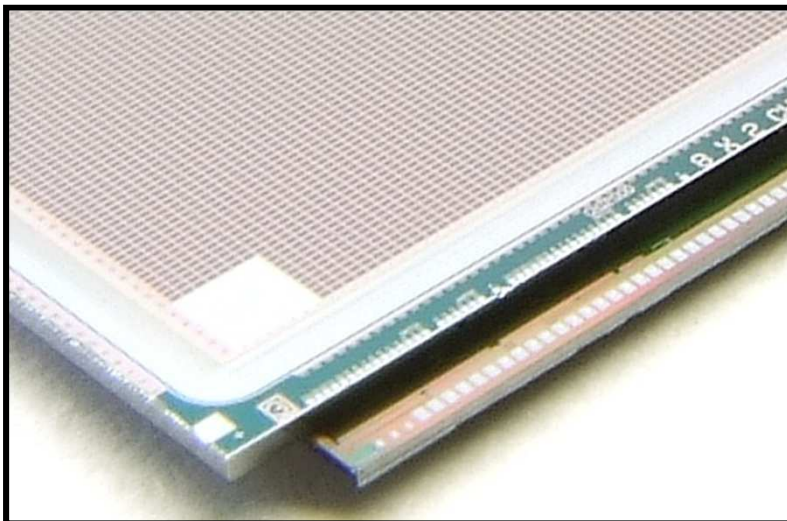




Pixel Sensor with
UBM & Indium balls



16 tested CMOS ROC
chips with UBM & Indium

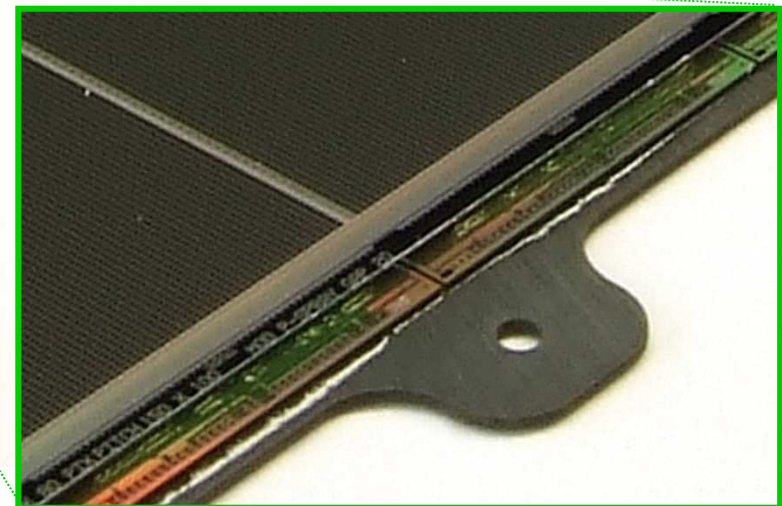
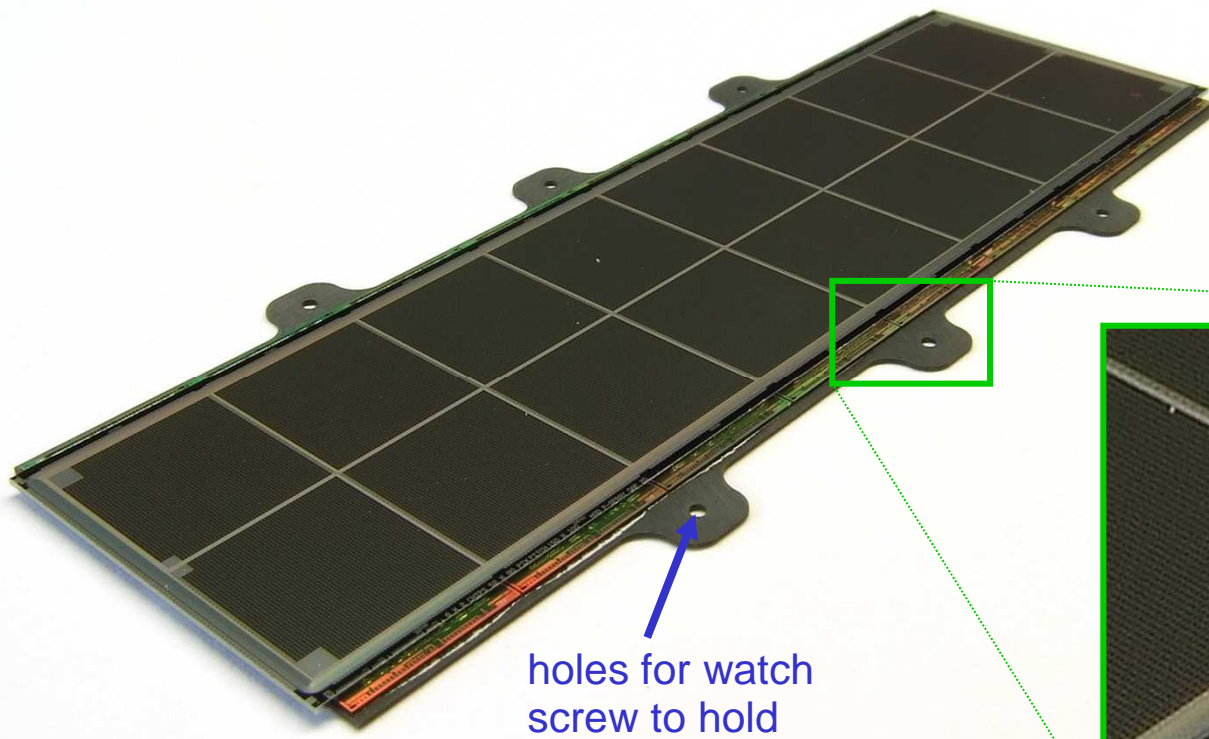


Bump bonded
“raw module”

Now glue ceramic base strips under



Si_3N_4 ceramic is almost identical in thermal expansion to silicon crystals





High Density Interconnect (HDI)
3 layers, 48 μ thick

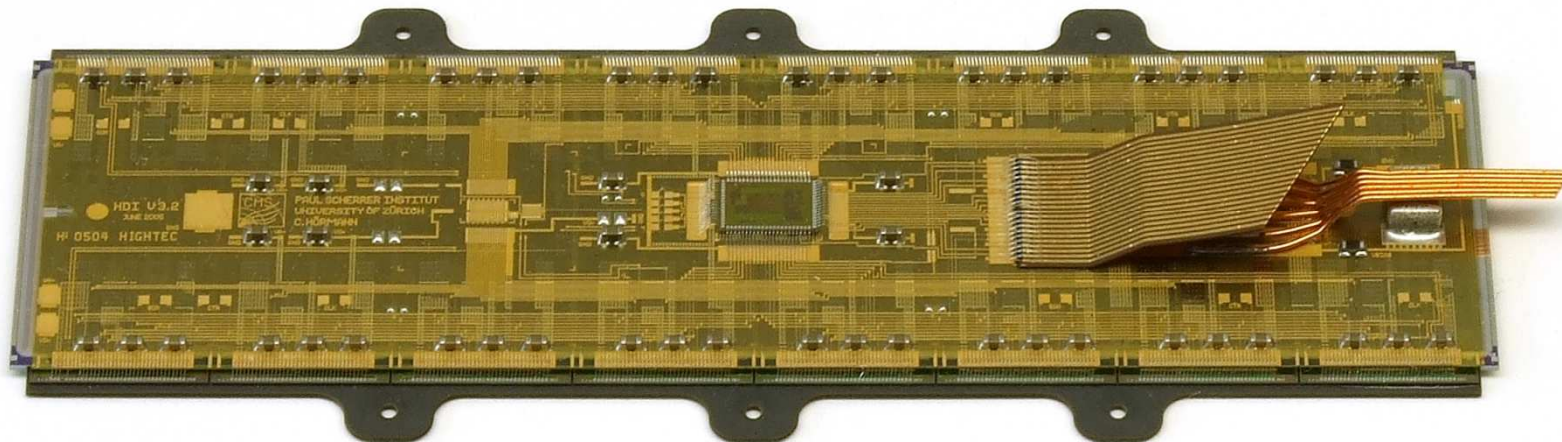
DYCONNEX
Bassersdorf

Kapton signal cable (21 traces, 0.3mm pitch)

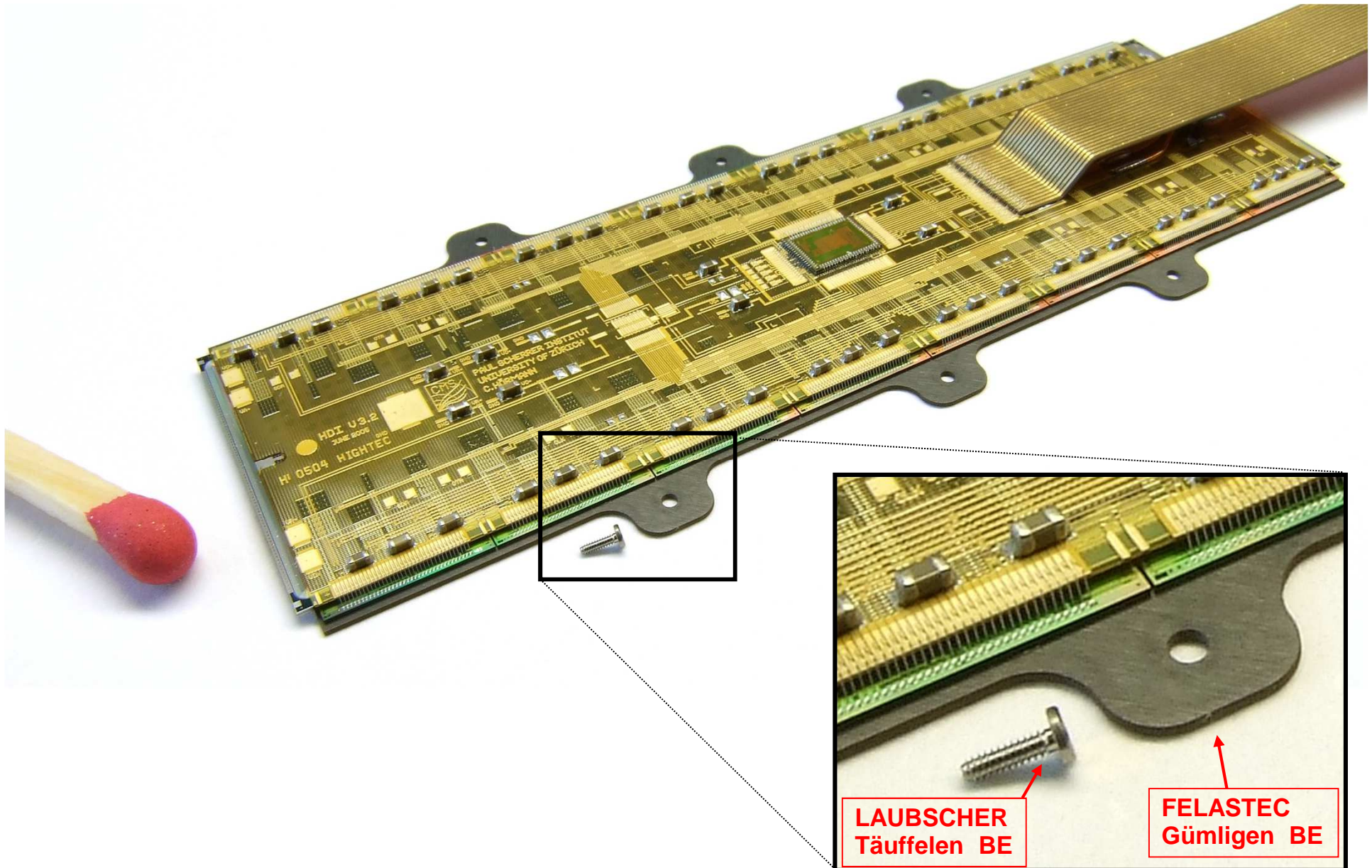
ELECTRISOLA
Eschholz matt

Cu-Claded-Aluminum Power cable (6 wire ribbon) ~1A

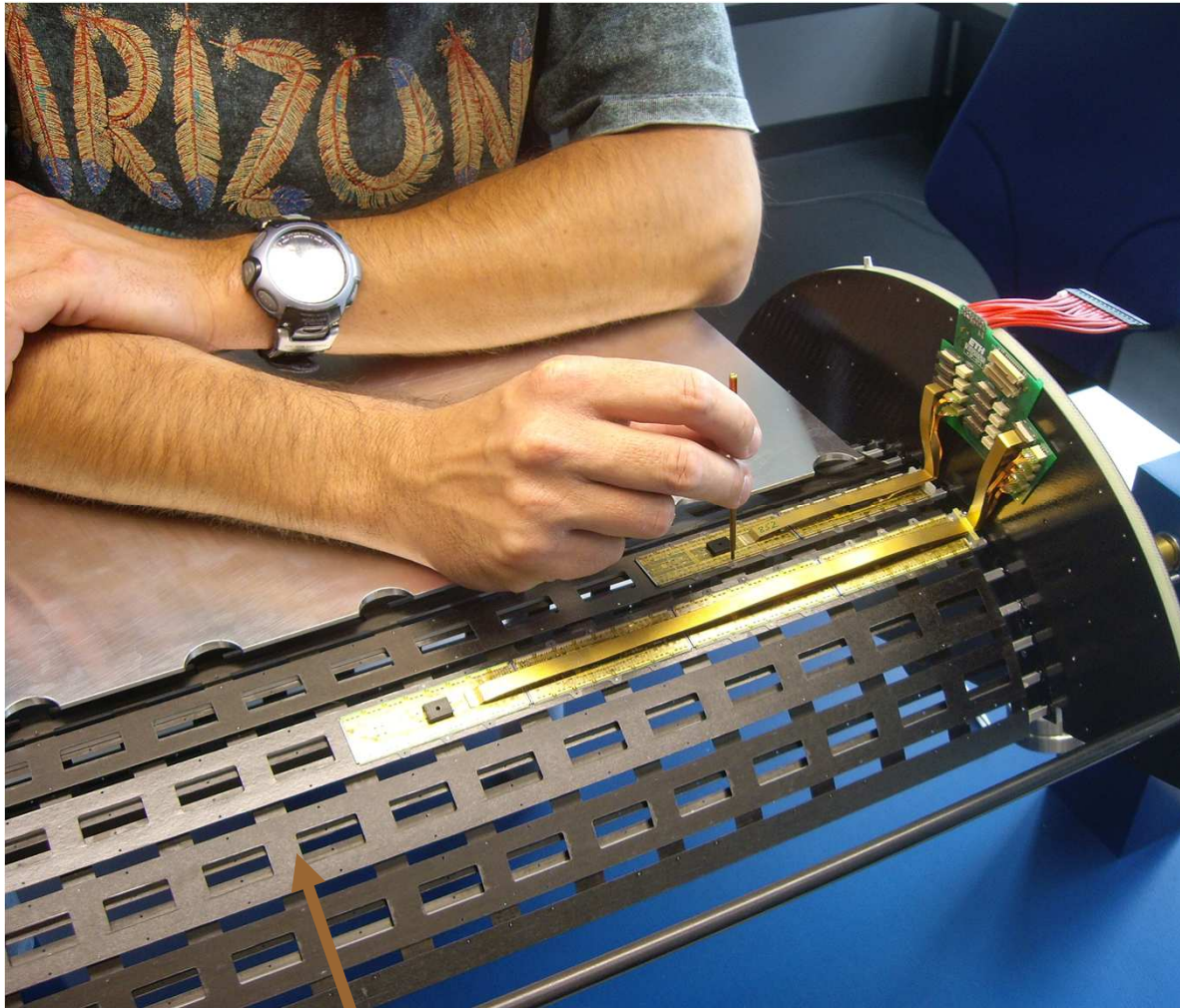
KUK
Appenzell



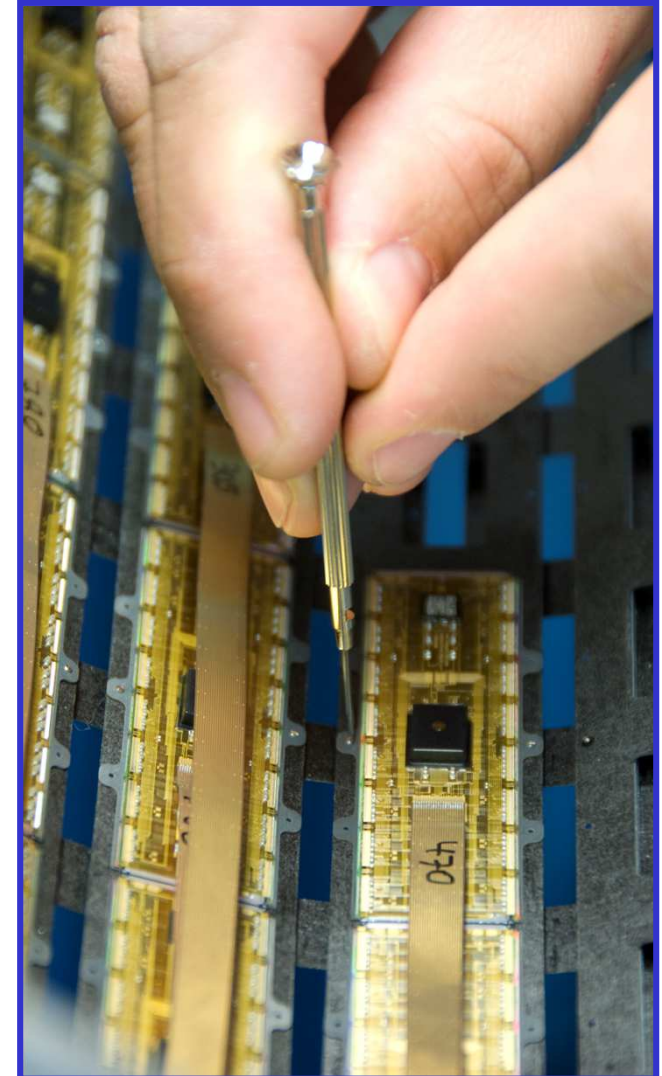
The pixel module will be screwed on



Mounting pixel modules onto C-fibre mechanics with integrated cooling structure



Pixel Barrel mechanics (Carbon-Fibre)
Design & Manufacturing by Uni. ZH



Tightening the Swiss Watch Screw

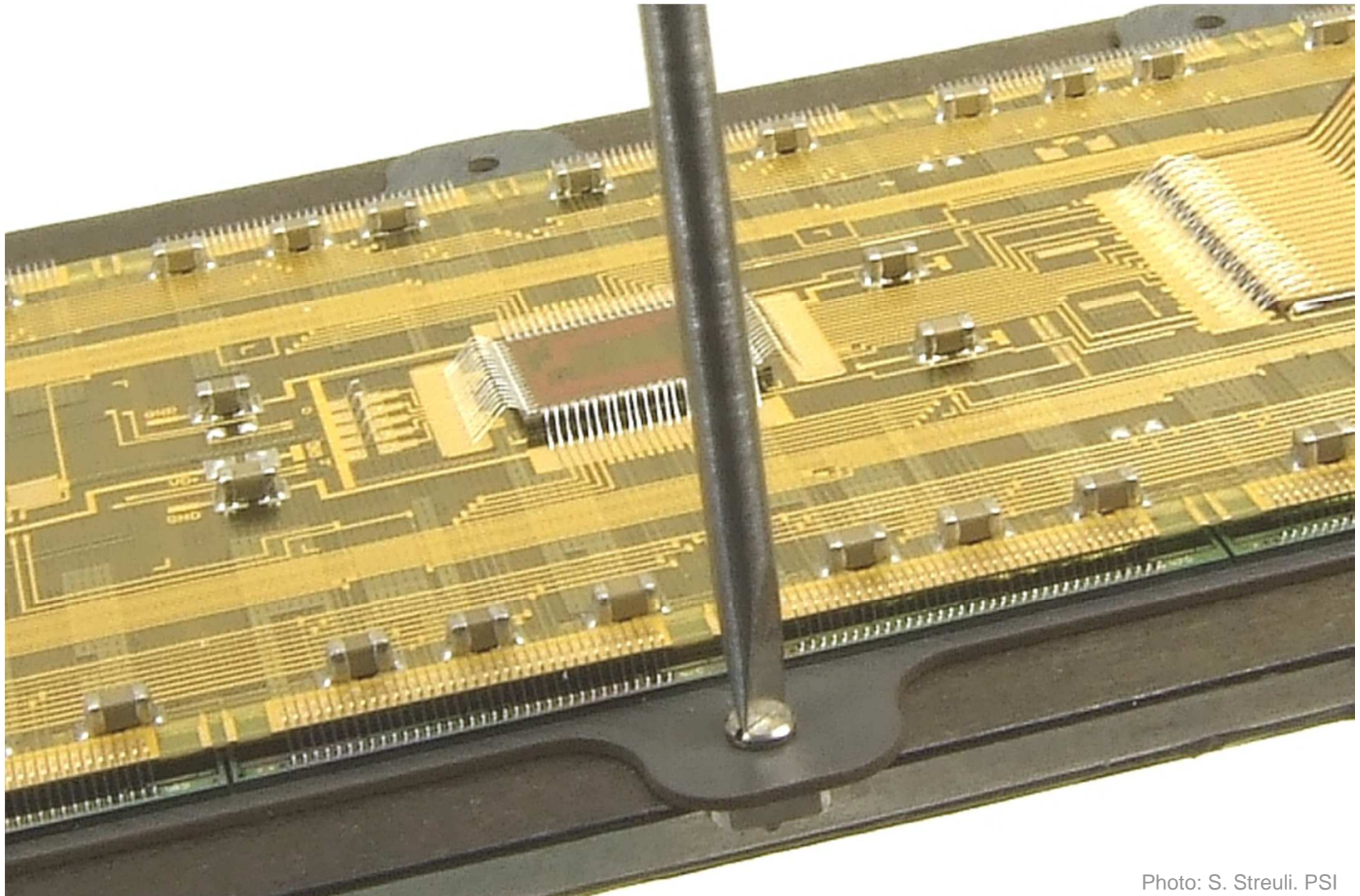
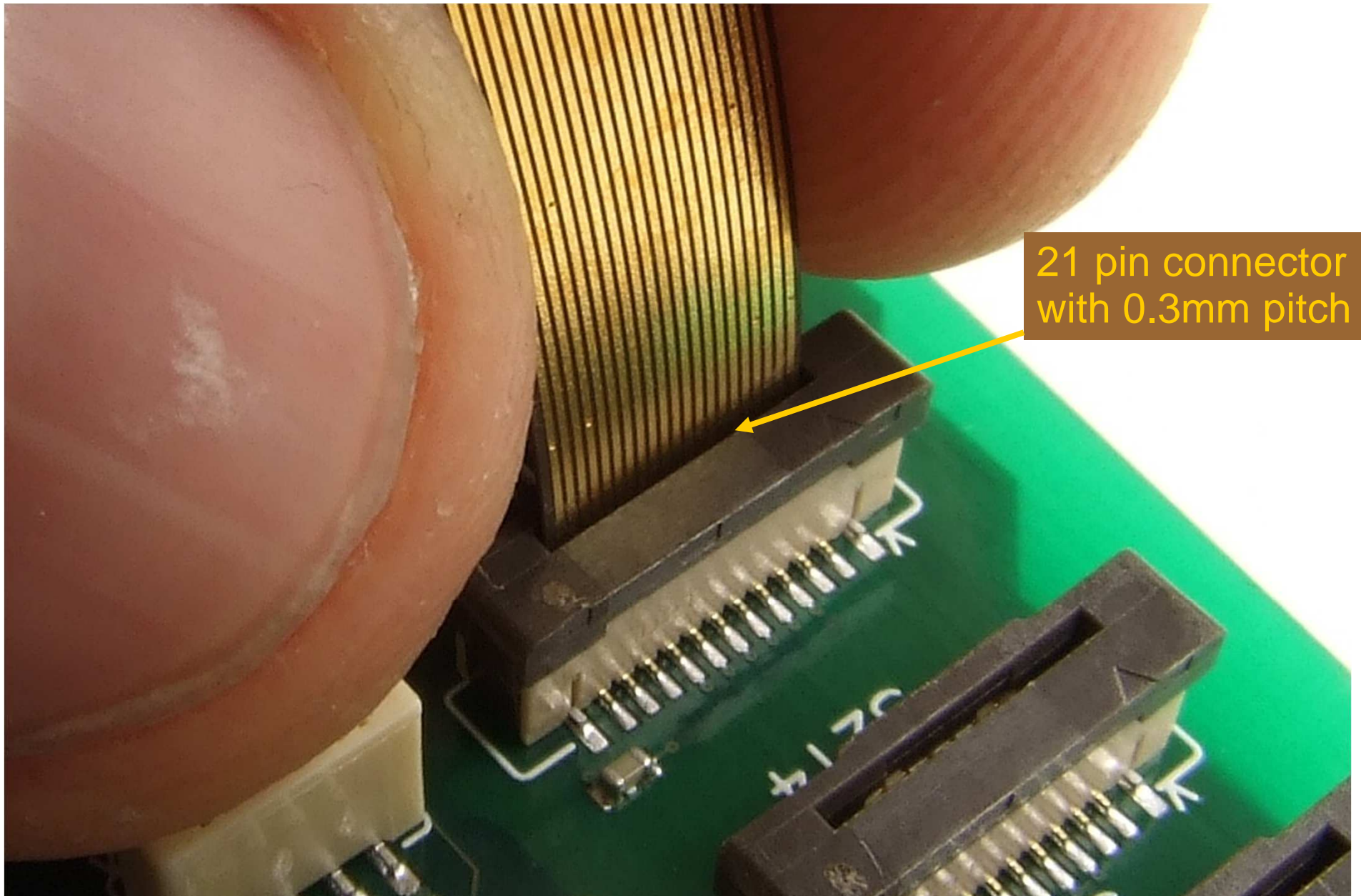


Photo: 12.March 08, 10:23



16128 Contacts must be right



Pixel Barrel & Supply Tube together



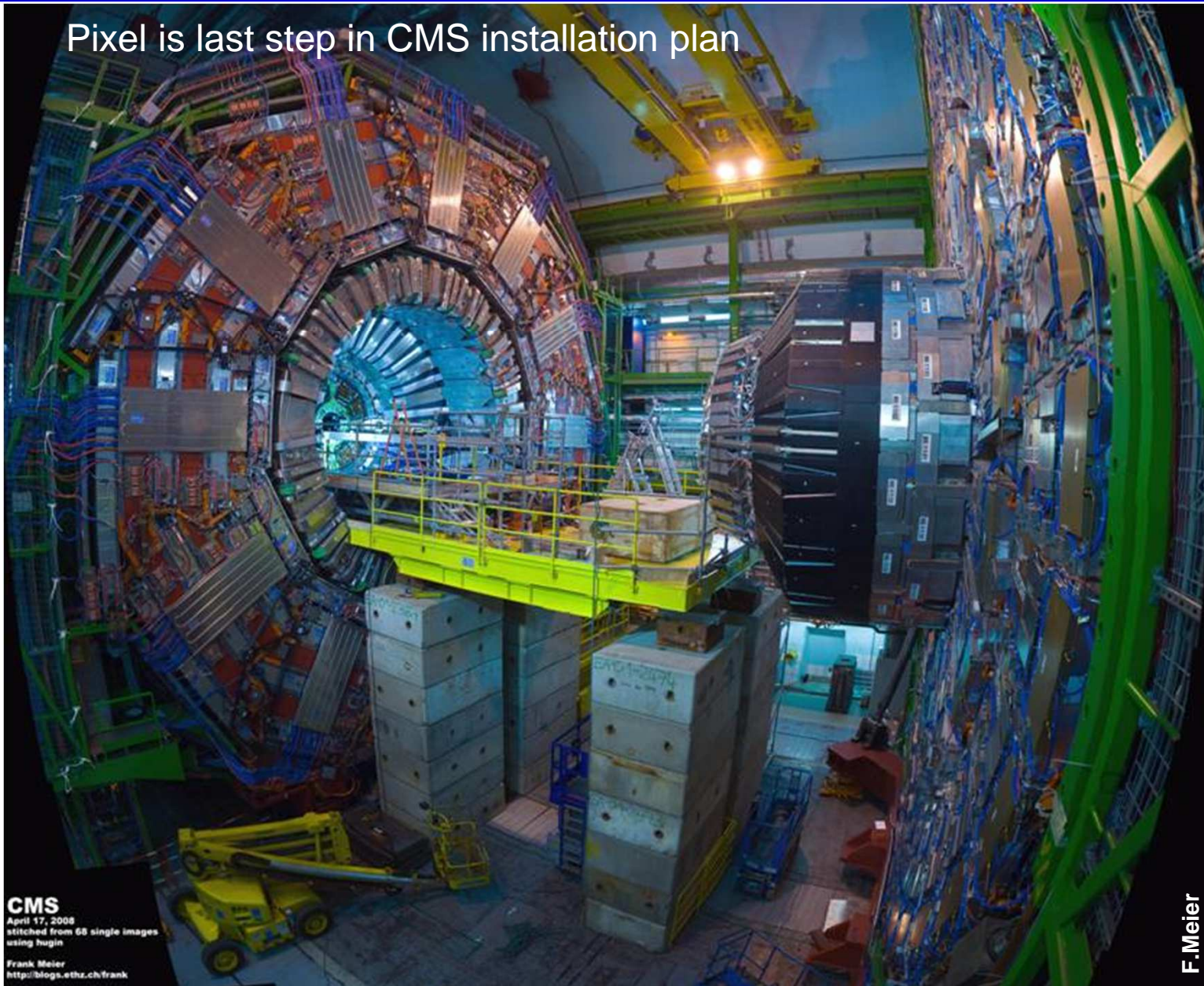
-x side of CMS Pixel Barrel ready !





CMS is ready to install the Pixel System

Pixel is last step in CMS installation plan

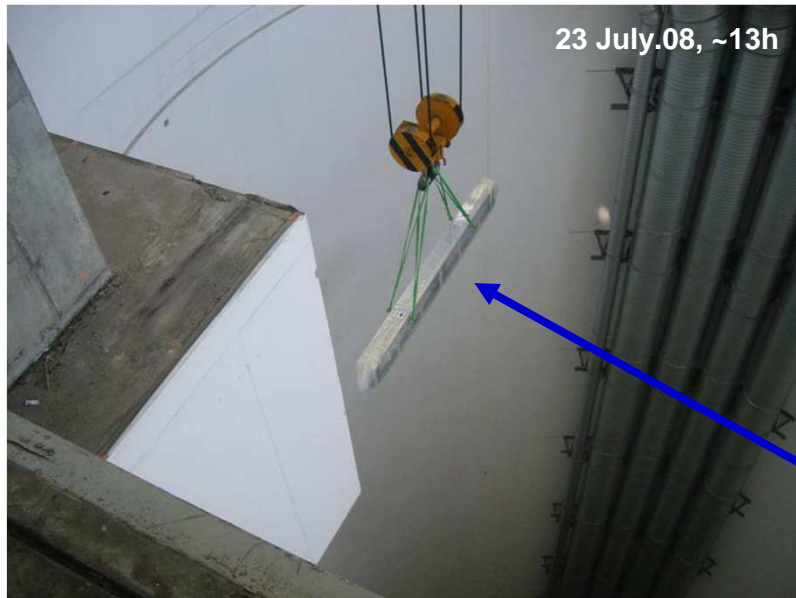


CMS
April 17, 2008
stitched from 68 single images
using hugin
Frank Meier
<http://blogs.ethz.ch/frank>

F.Meier



Our party tent “clean room” at Point 5



It's a big shaft !

BPIX Insertion in 2008

Pixel Installation
28. July 2008

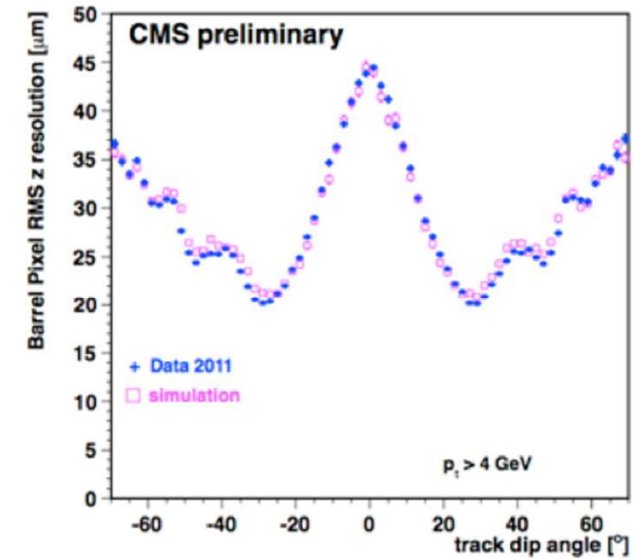


BPIX stayed inside CMS until 2013 LS1
extraction for new beam pipe installation

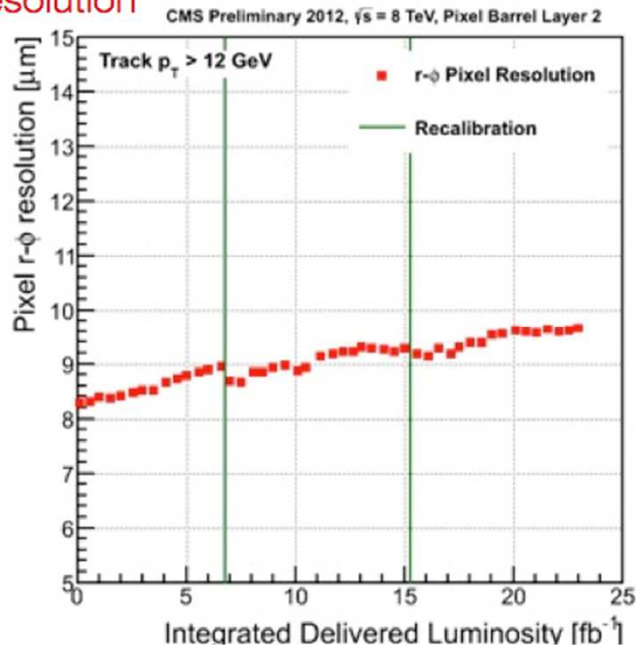


Pixel Performance in Run 1

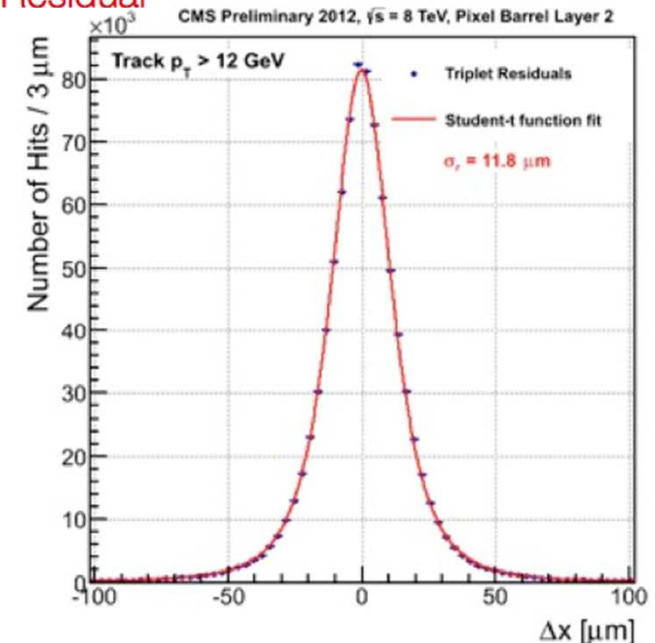
- Spatial resolution measured with the triplet method
- Degradation observed with integrated luminosity
 - ▶ Partially recovered after re-calibrations
- Measured resolution better than 10 μm at the end of Run 1
 - ▶ Consistent with design goals

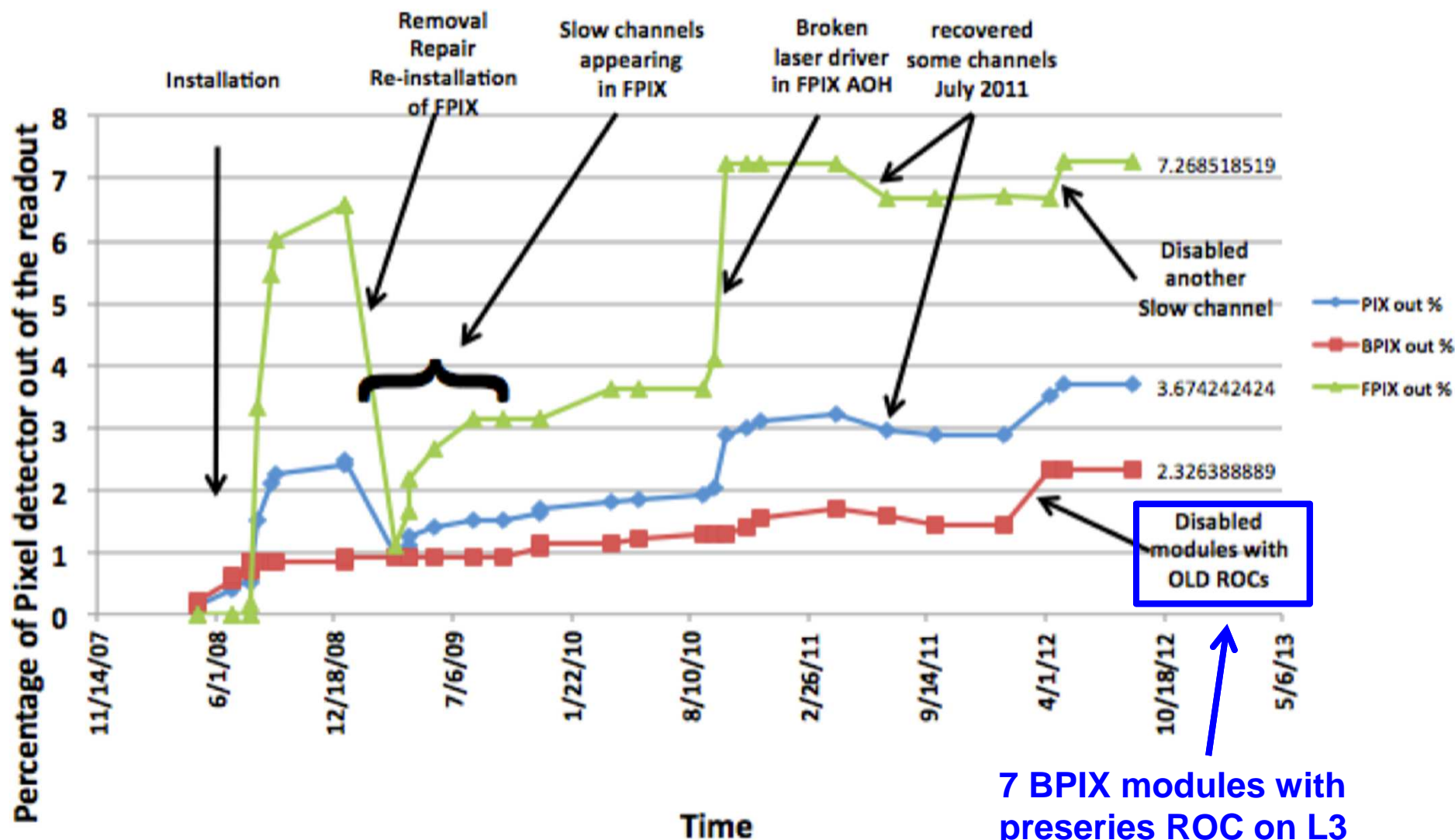


Pixel Resolution



Example of Residual Distribution





7 BPIX modules with preseries ROC on L3 disabled, replace in LS1



BPIX Extraction in LS1 for new beam pipe



BPIX extraction May 2013



Storage in BPIX cold boxes in Pixel Lab (P5)

BPIX low temperature calibrations at -16°C in Pixel Lab during LS1

- test 32 sectors one by one
- open thermal box & swap cables
- testing done over 12 month
- thermal boxes opened many times
- each time re-sealing required



BPIX damage apparent in last check-out



Monday, 11. Aug 2014: Danek & Lea replace pre-series modules in layer 3.

→ Tests of BPI-quadrant shows serious damage → ~1/4 modules (55) do not work

Wednesday, 13. Aug 2014: Inform BPIX team and tracker community on the situation

Friday, 15. Aug 2014: production of new pixel module HDI launched at HighTec

→ launch production of new modules

Friday, 22. Aug 2014: transport inner BPIX half-shell (+x) from CERN to PSI

Thursday 28. Aug 2014: complete half-shell tested with sector testboard electronics

→ confirm damage map from P5 pixel lab.

Friday , 5. Sept 2014: express production of new BPIX HDI by HighTec is finished

Monday, 8. Sept. 2014:

- start production of pixel modules at PSI
- bump-bonding of new pixel modules at DECTRIS
- module qualification at PSI by ETHZ (Andrei & Maiko)



BPIX Activation Measurement at CERN



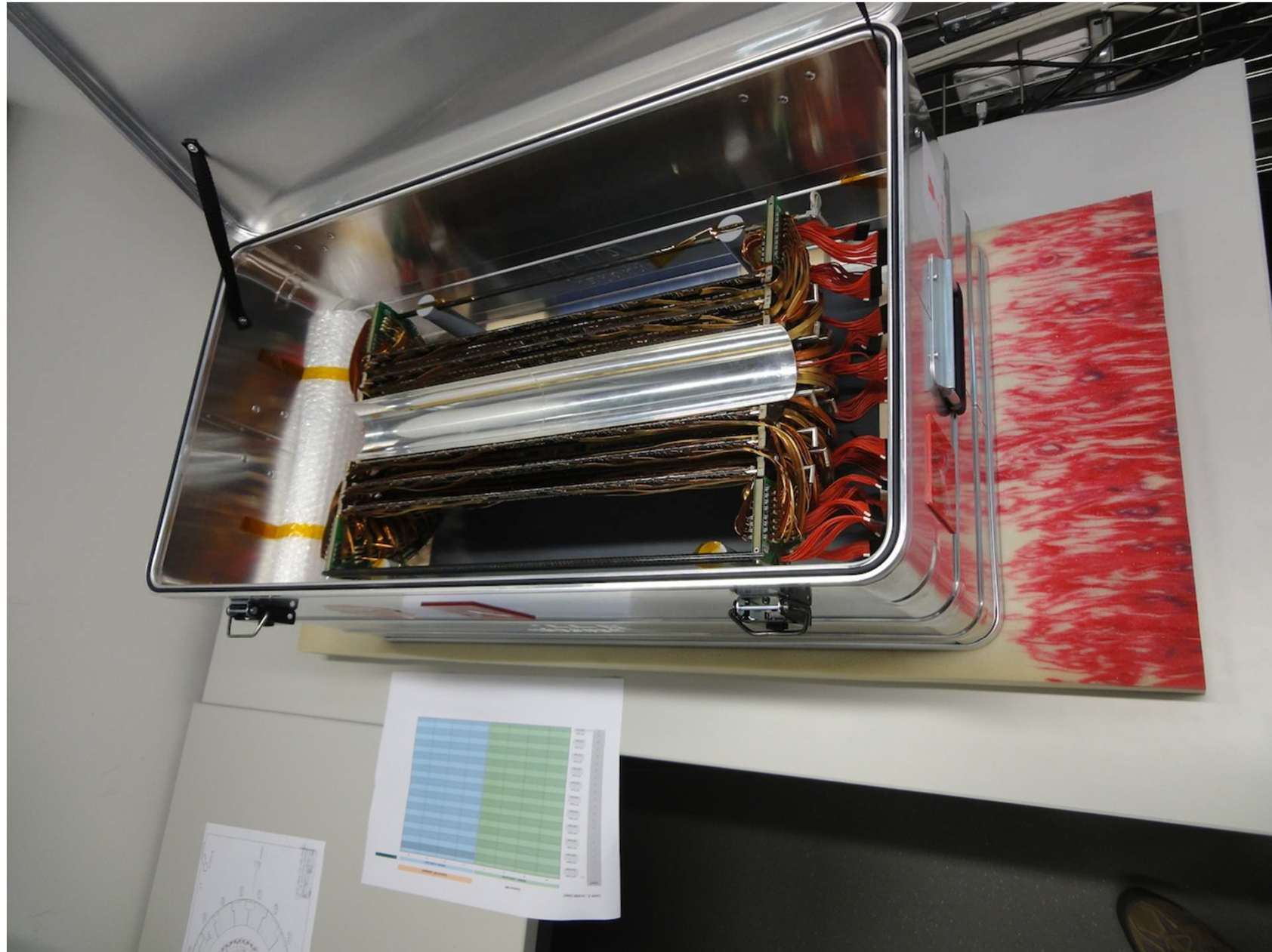


BPIX Transport from CERN to PSI



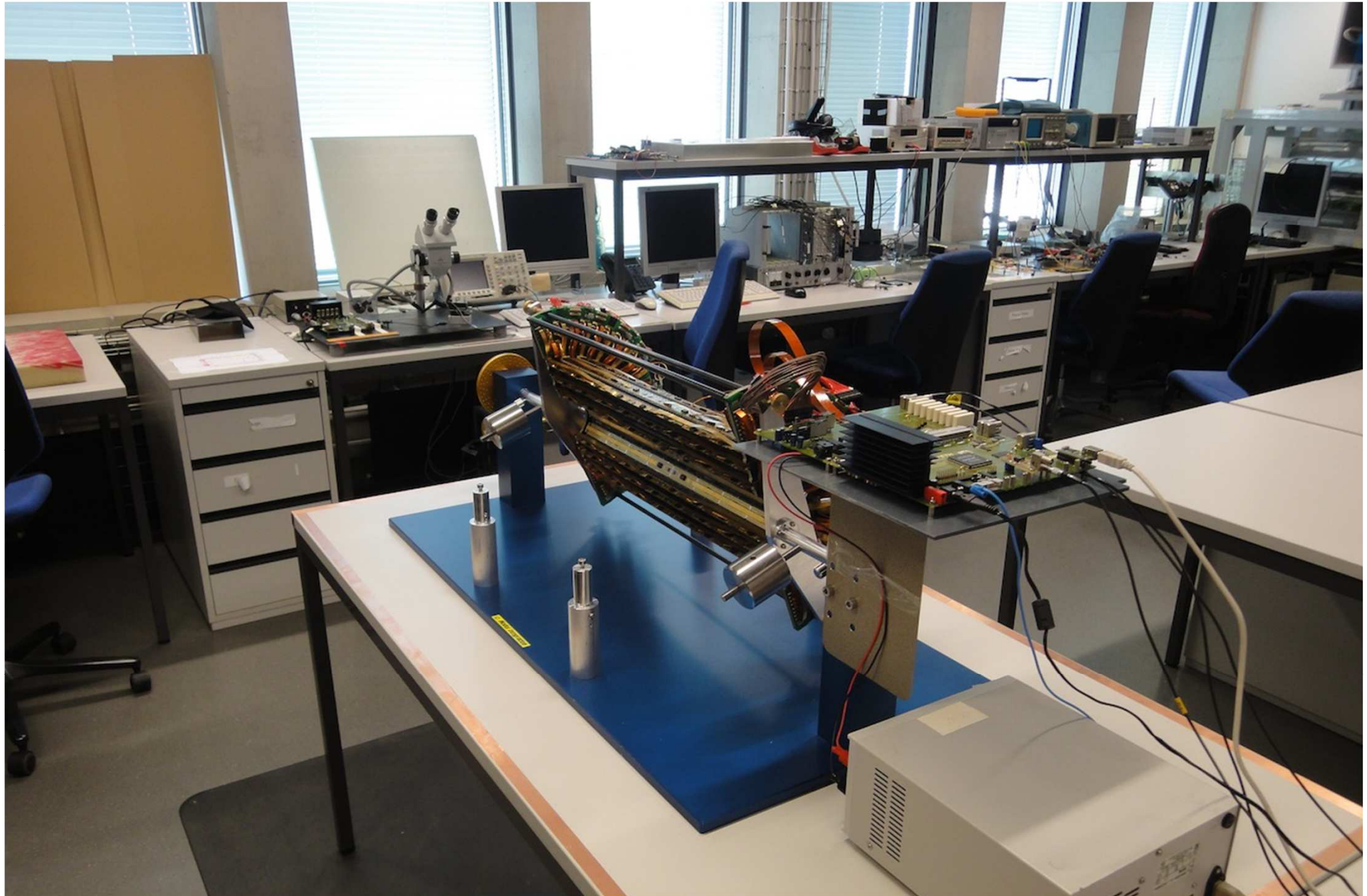


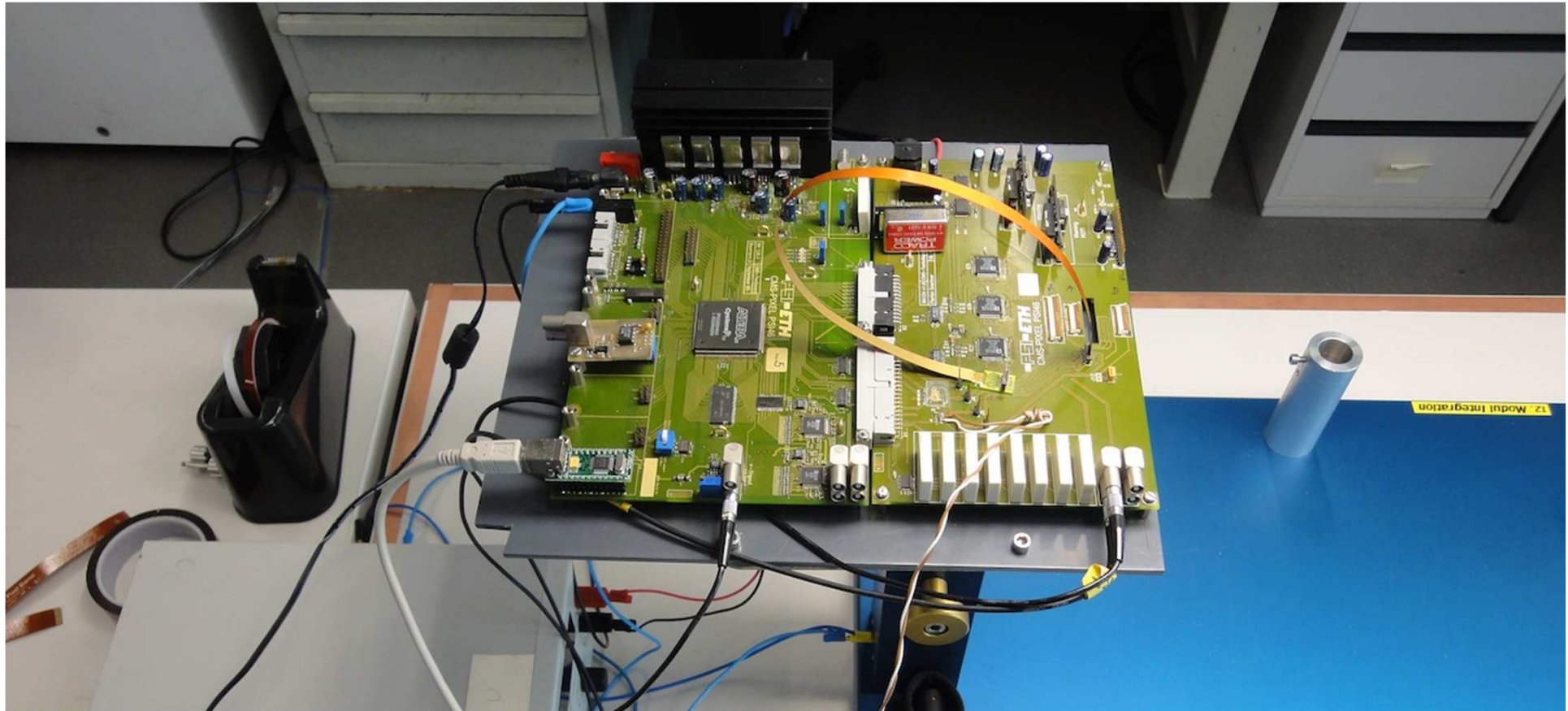
BPIX Transport Box reopened in PSI Lab



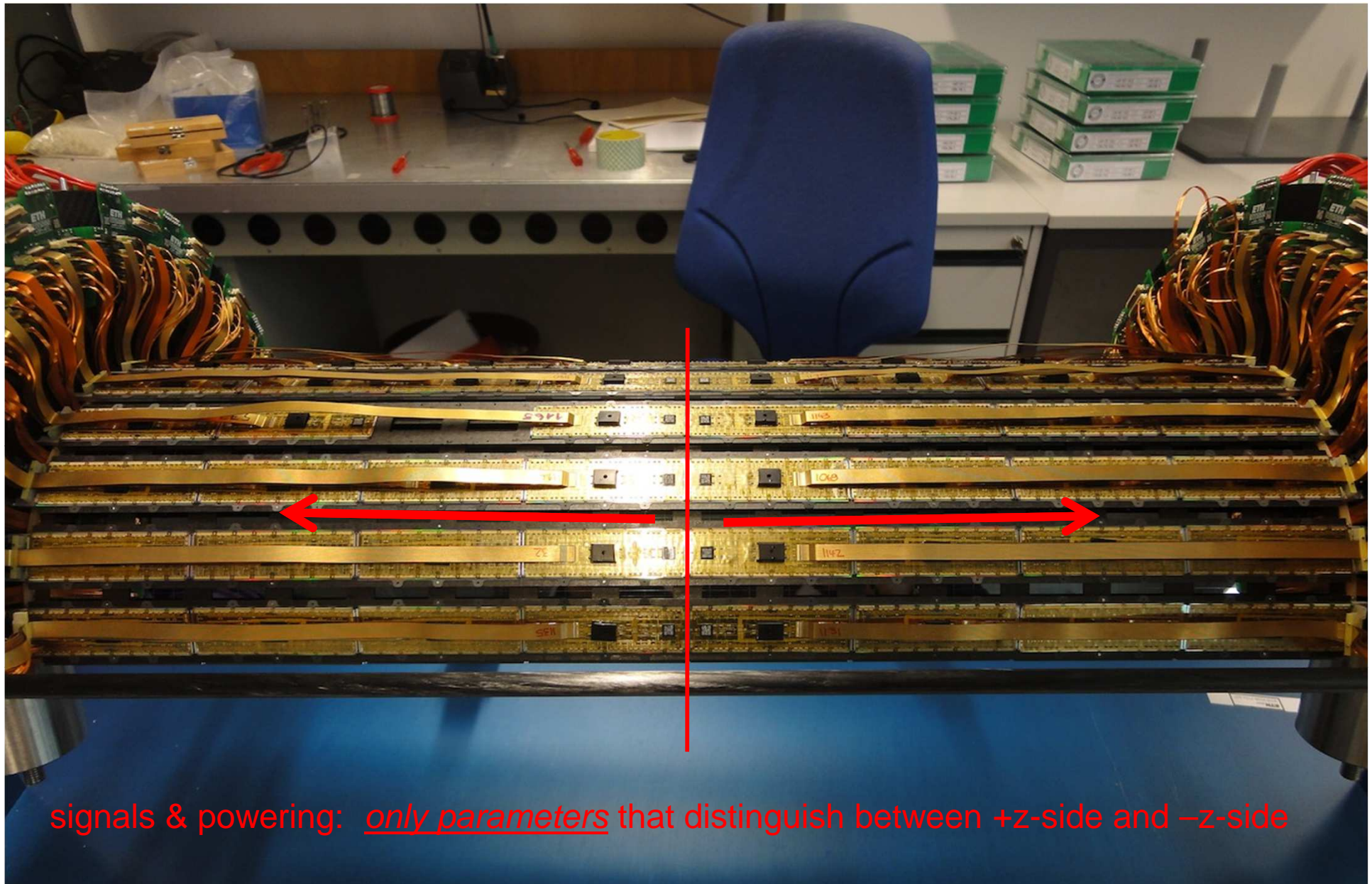


Measure Damage Map with Sector Testboard





- special test board for testing modules & groups of modules (sectors)
- performs functionality of FEC & FEC with parameter scanning software
- **diagnostic signaling** allows **measurement of resulting signal levels by DUT**





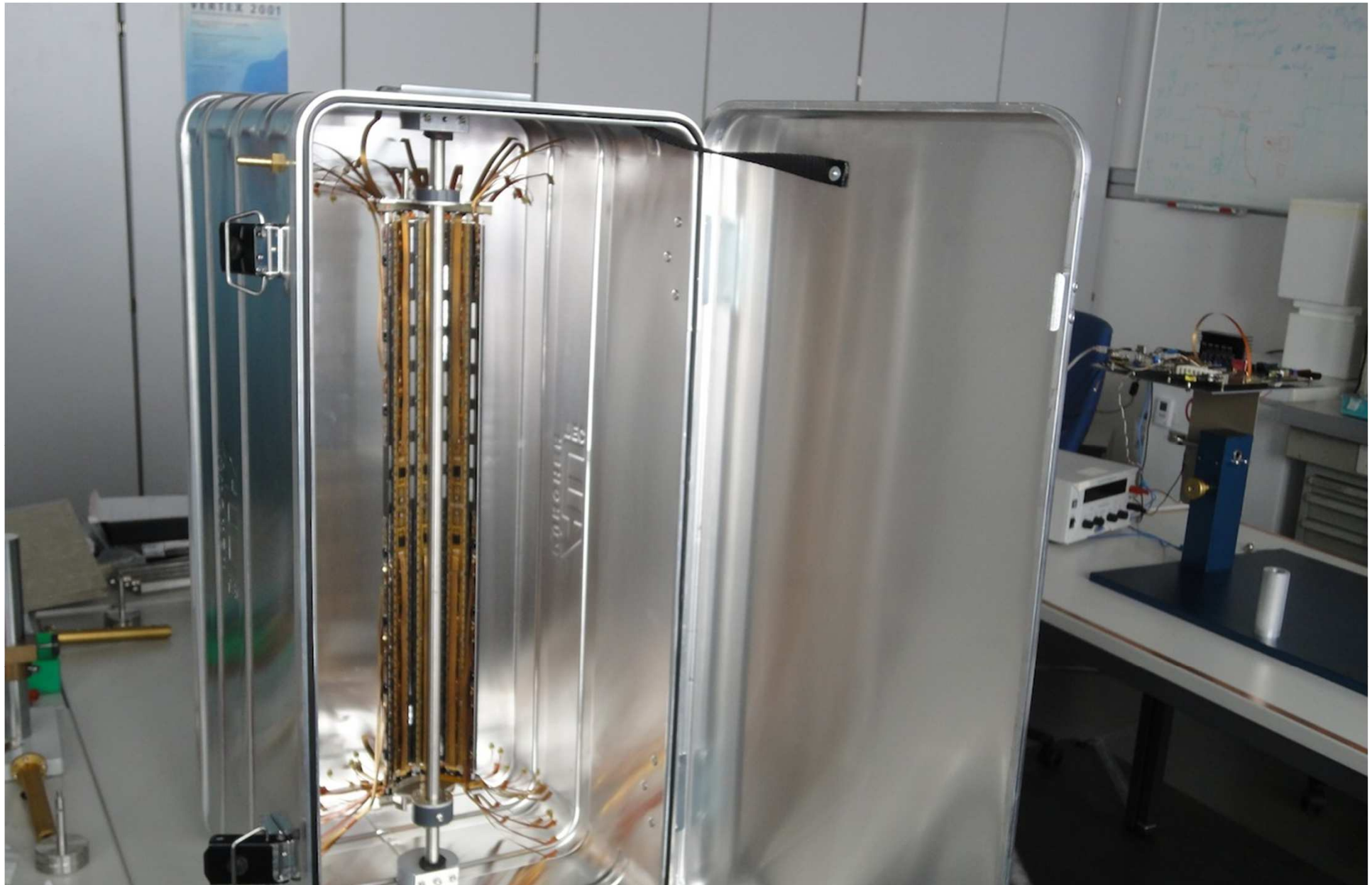
Un-cabling and taking shells apart



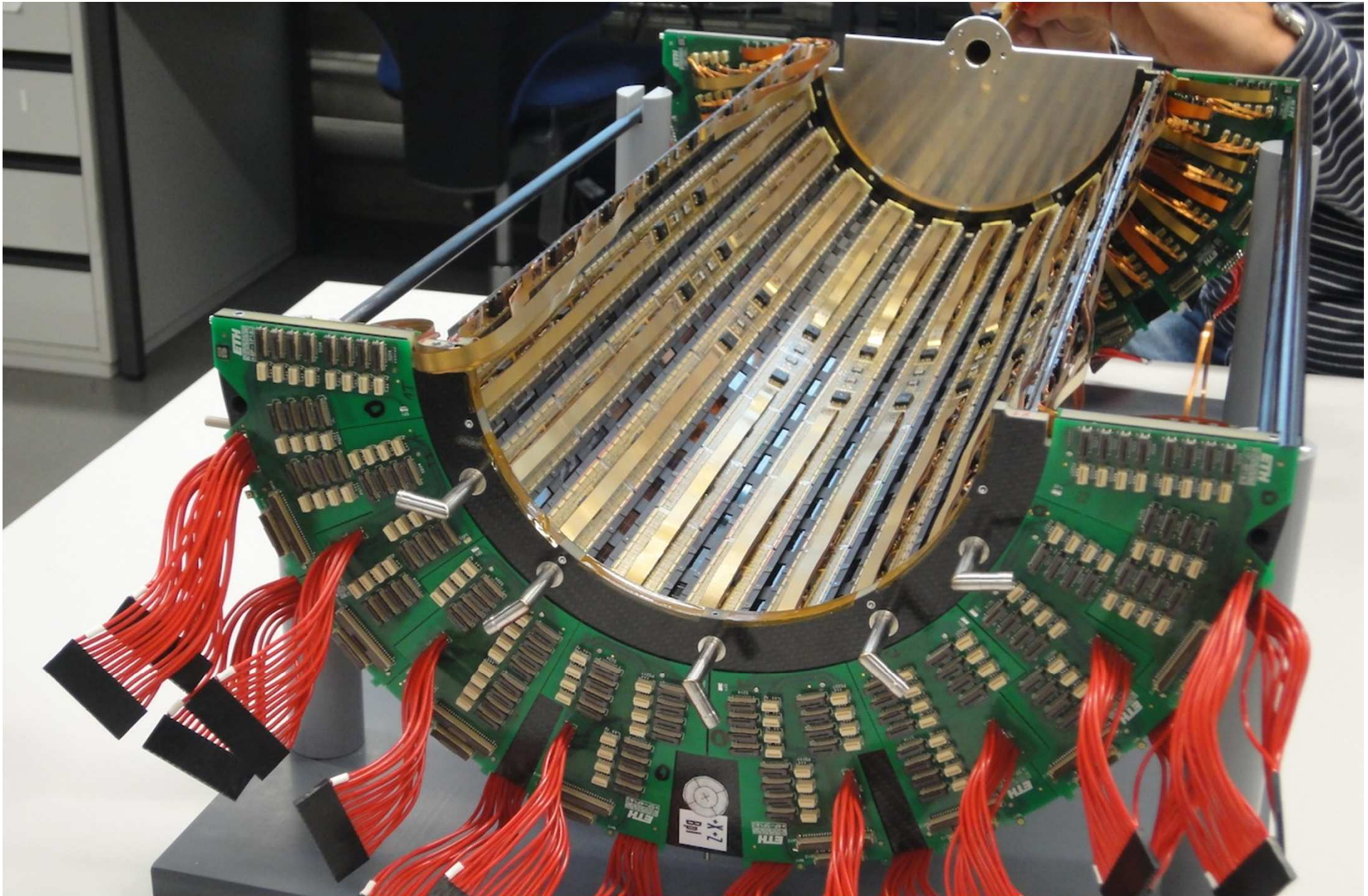


Mounting layer for module removal & testing

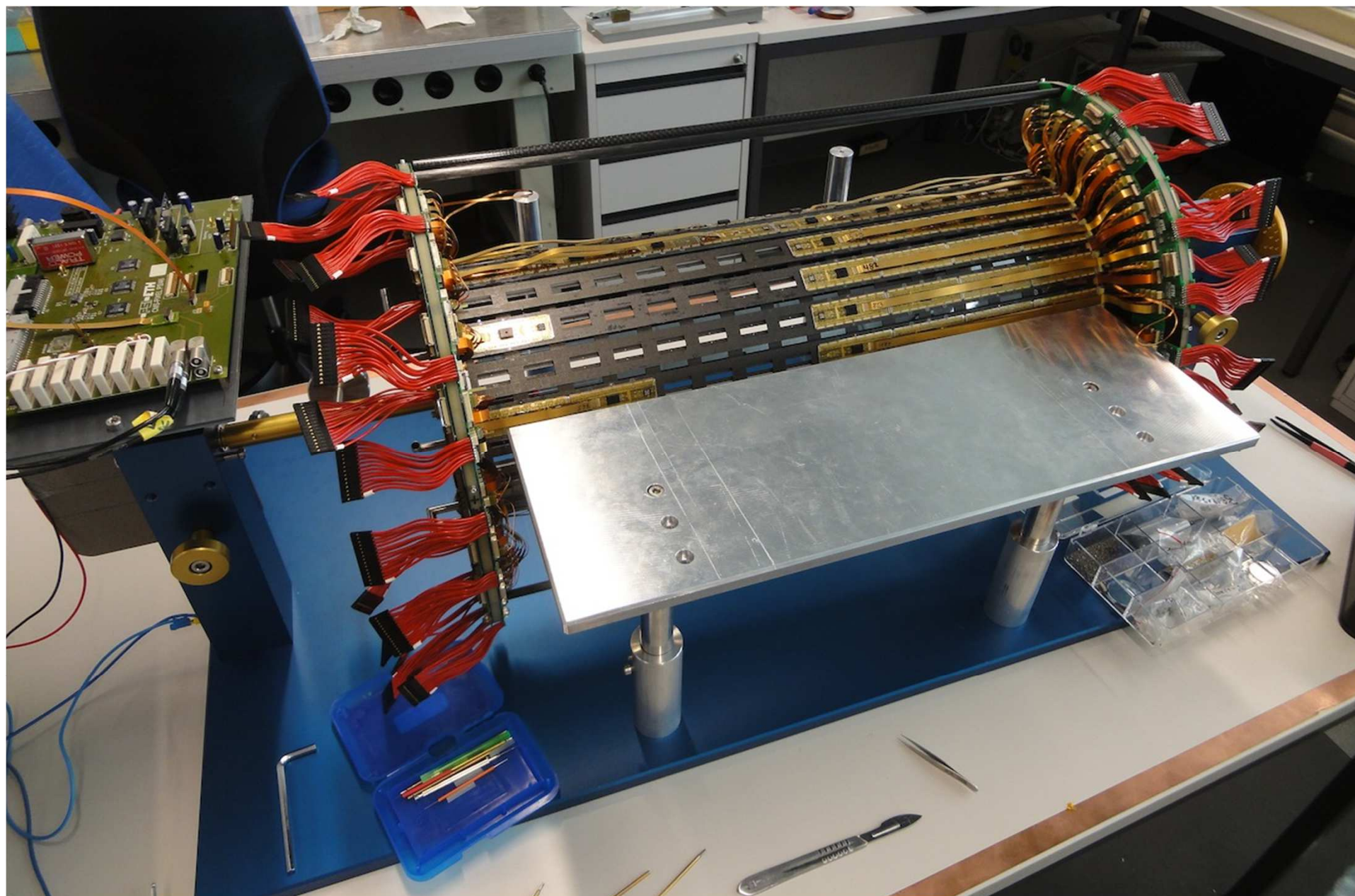




Layer 1&2 done and cold , now do Layer 3

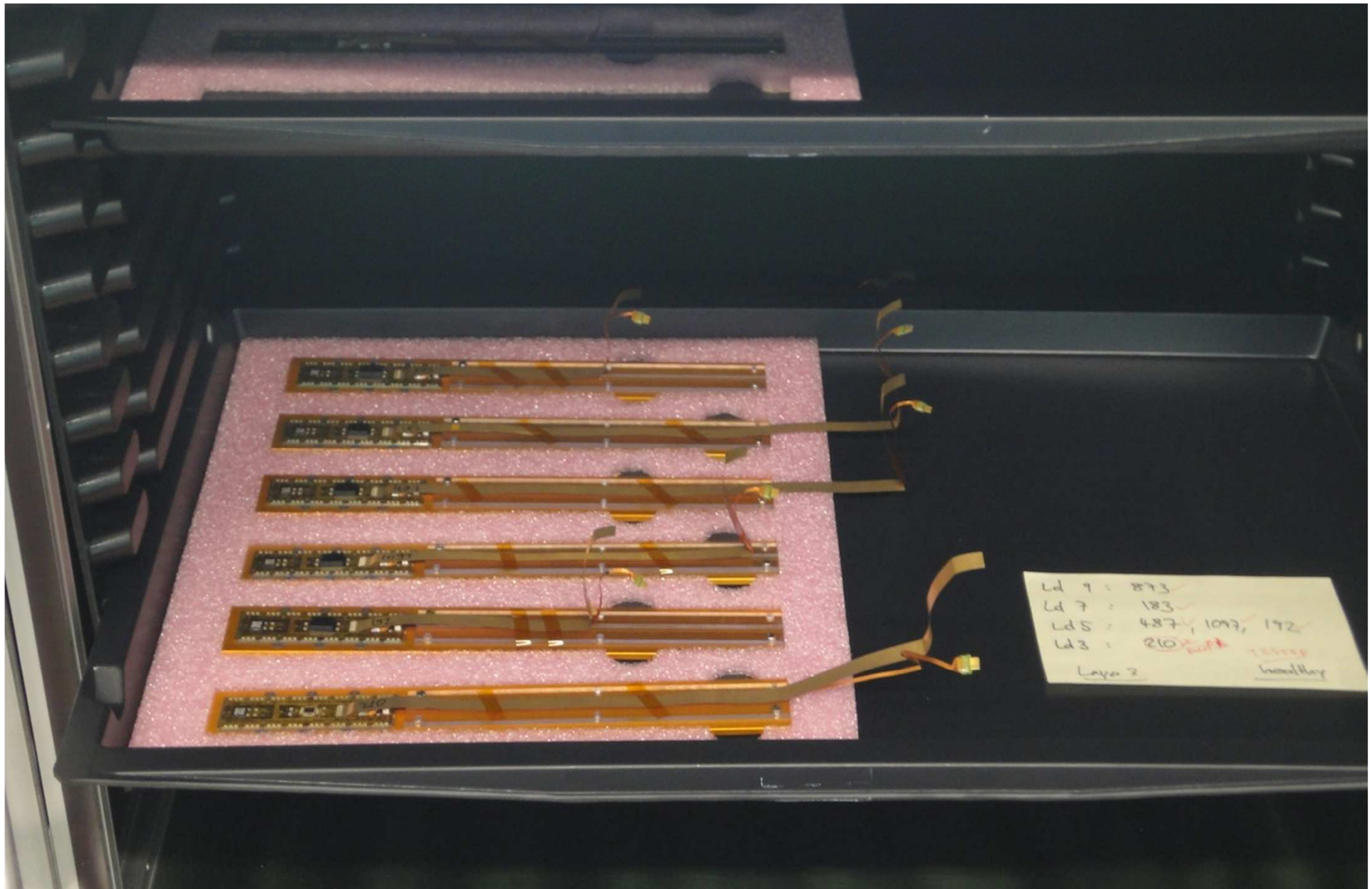


Dismount modules of Layer 3



3 Layers in their own fridges (DP -40° C)





modules of low serial numbers almost always shorts at ROCs between **Reset-pin** & **Aout-pin**

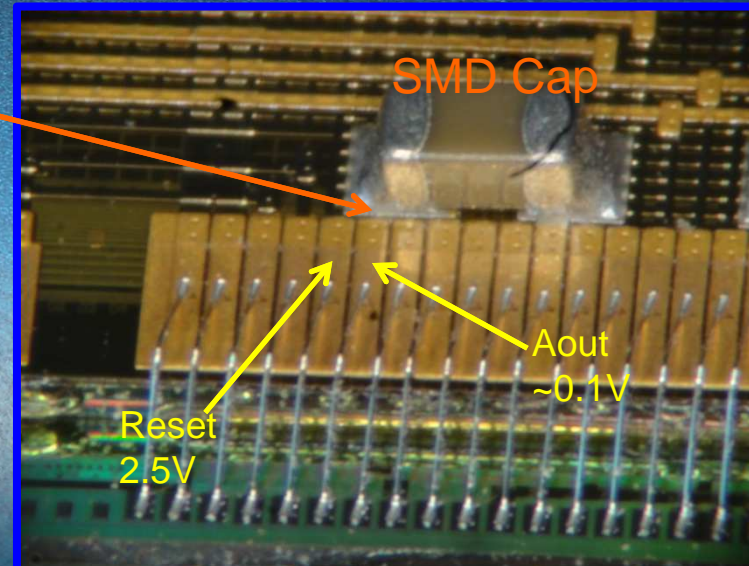
serious damaged modules → multiple shorted modules e.g. also at **TBM-pads** & **cable pads** (very dirty too)



solder footprint
rosin based flux

observe typically shorts between pads with
2-2.5V adjacent voltage differences and
proximity to SMD components

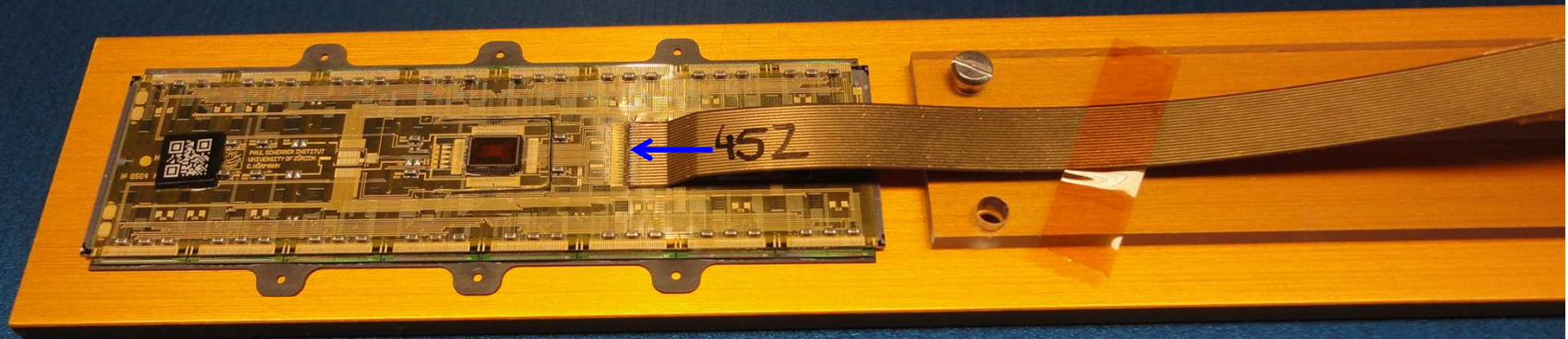
→ observe shorts to disappear when
raising current above ~ 20mA



How to locate shots on HDI

Reset line pulled down by $\sim 5\text{mA}$ by short to ground \rightarrow module reset

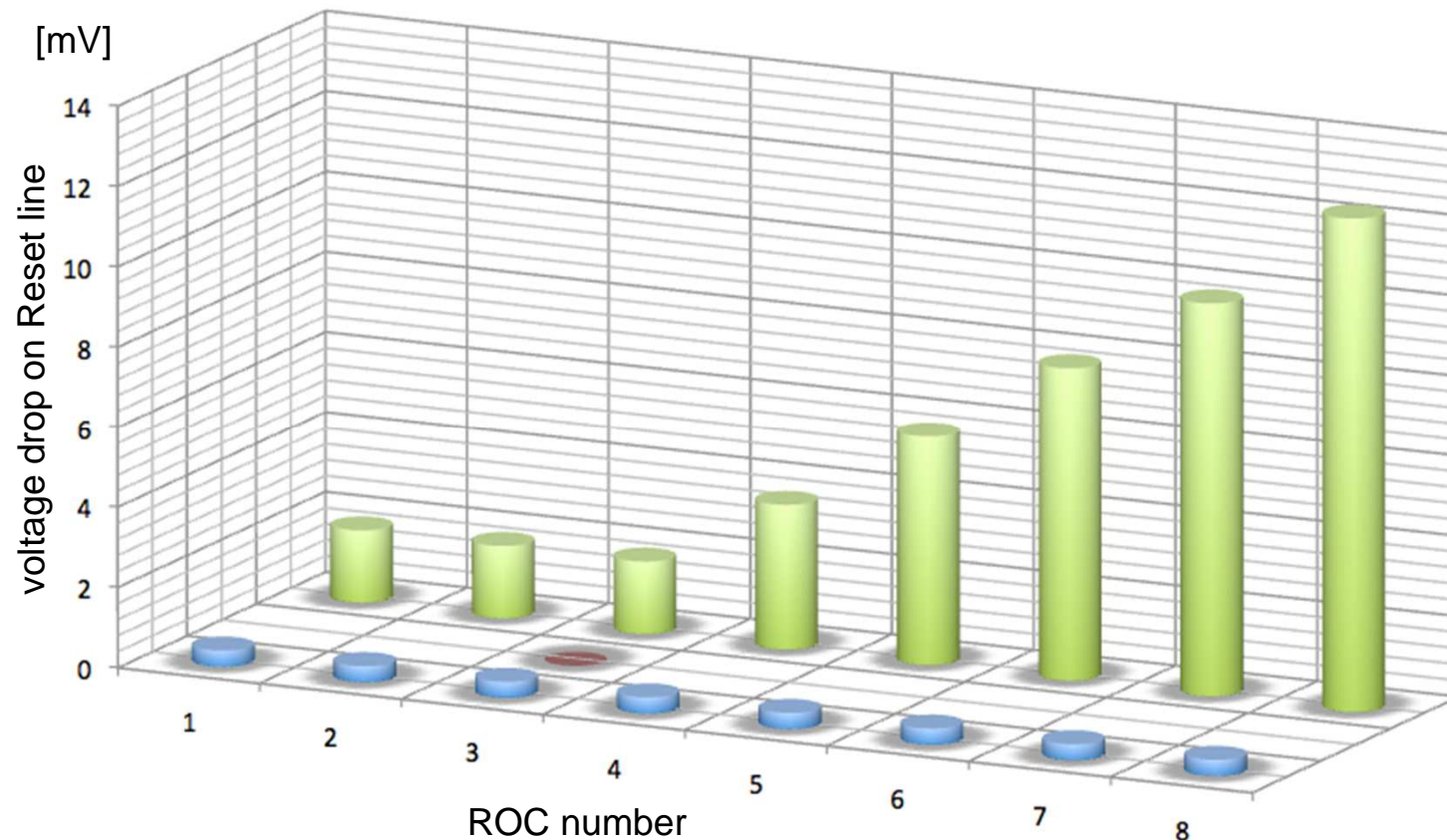
resistive path of reset line $\sim 2\Omega$ \rightarrow locate shorts by precise voltage measurement



Module #69: (Layer 1, Ladder 7, Position +2) Hub ID=30

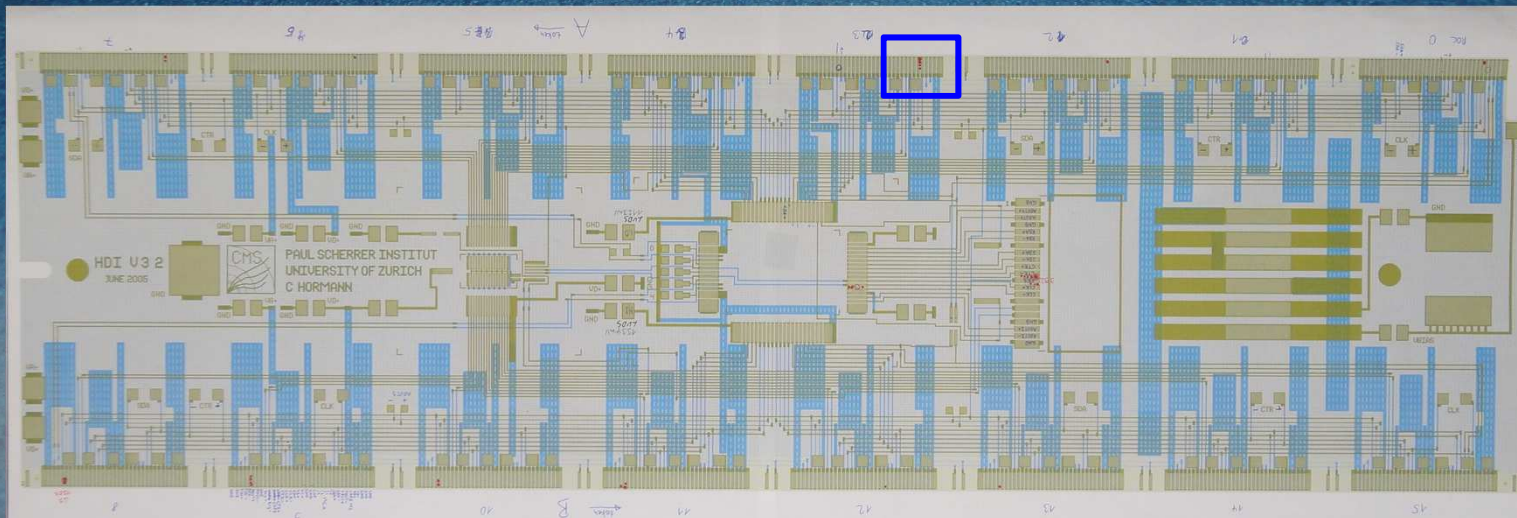
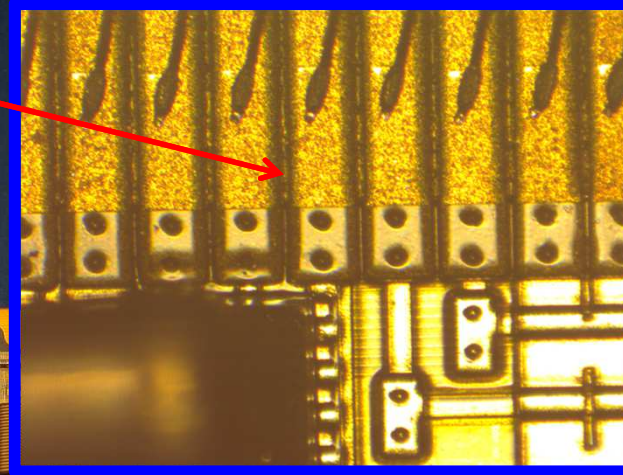
Symptom: Reset line pulled down by ~5mA current to A_{out} pad

→ Precise measurement of voltage drop on Reset line shows **short at ROC 9**

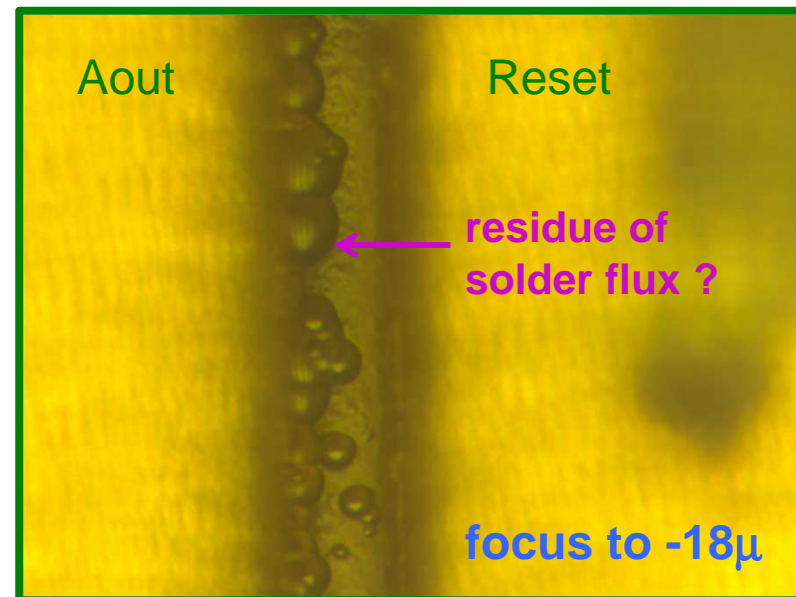
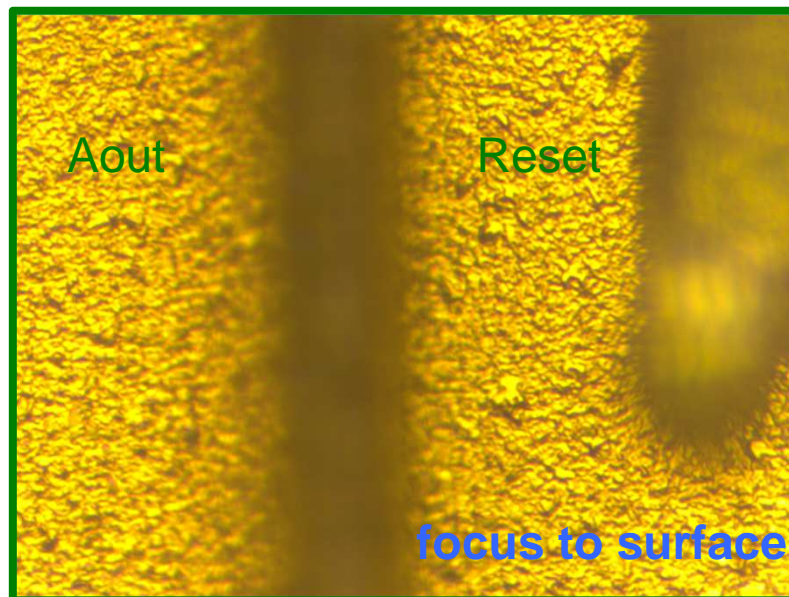
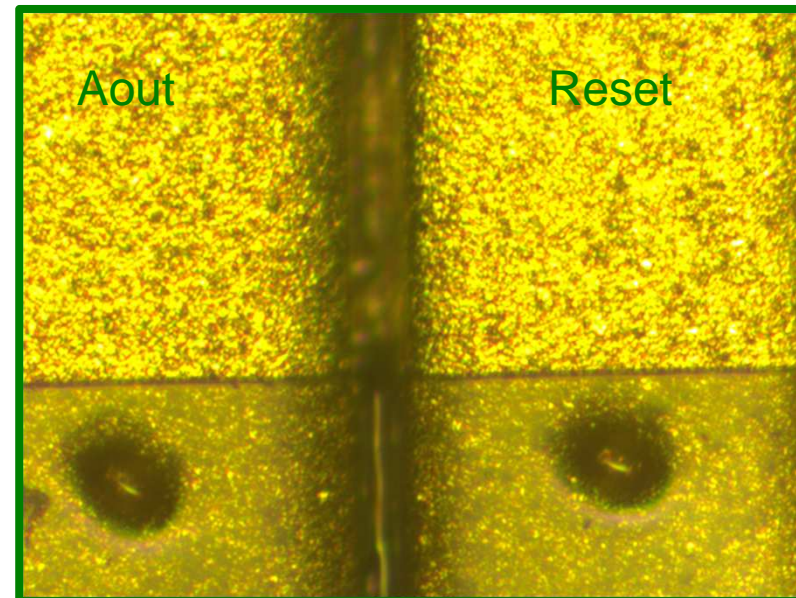
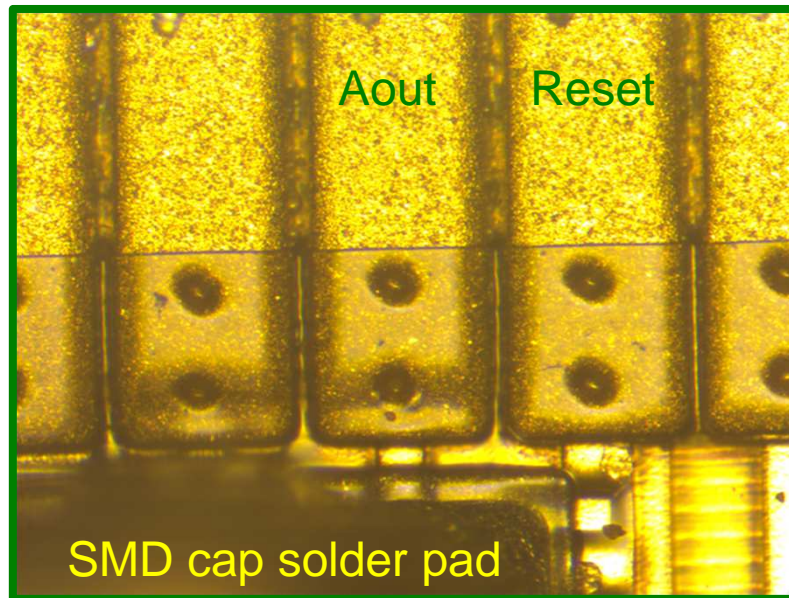


HDI shorts “always” happen at Reset / Aout

typical short
Reset - Aout

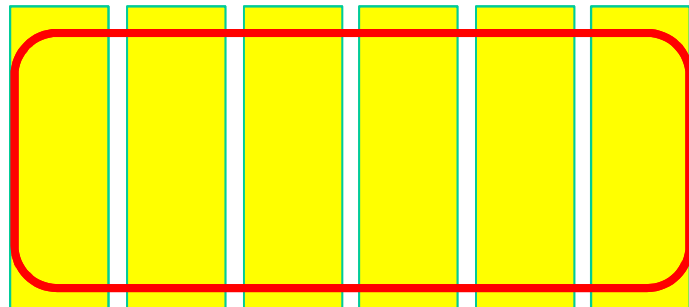


Zoom into cracks between pads

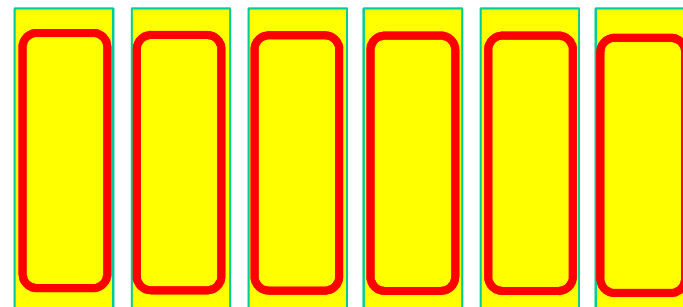


Passivation openings (windows) for ROC, TBM and Cable-pads

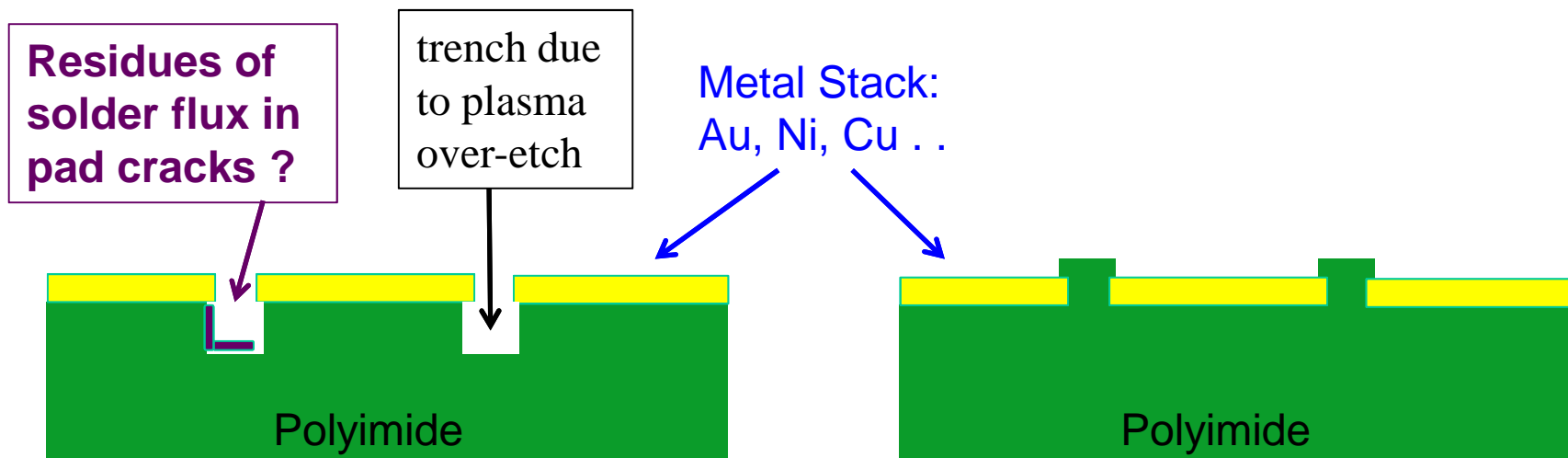
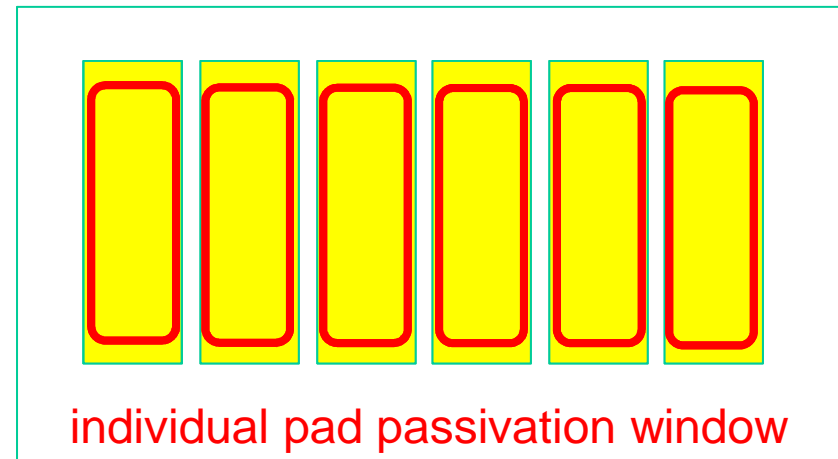
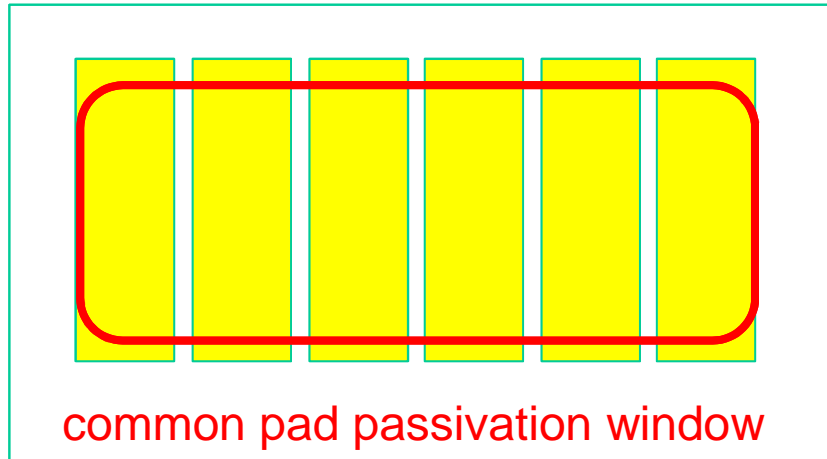
- TBM & Cable-pads with common windows for all HDI produced Dec. 2005 – Aug. 2007
- ROC pads with individual passivation windows for HDI produced Dec. 2006 – Aug. 2007



common pad passivation window

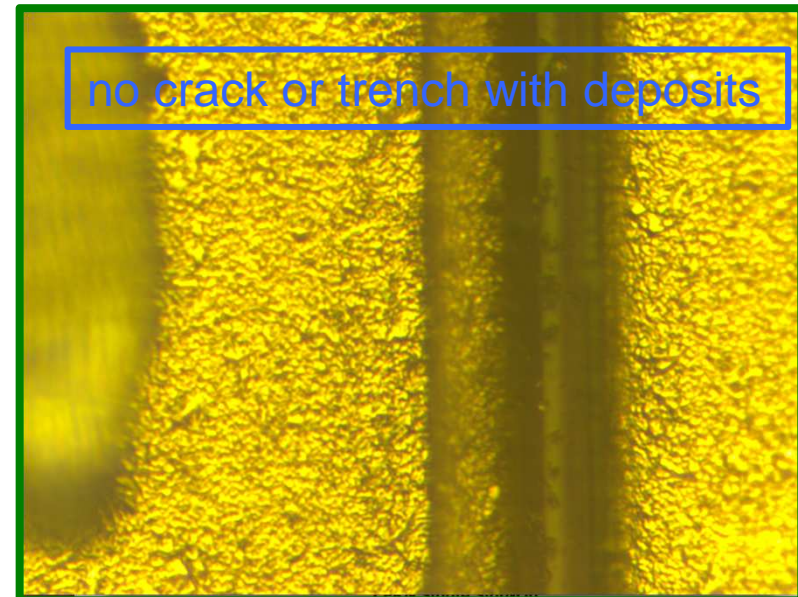
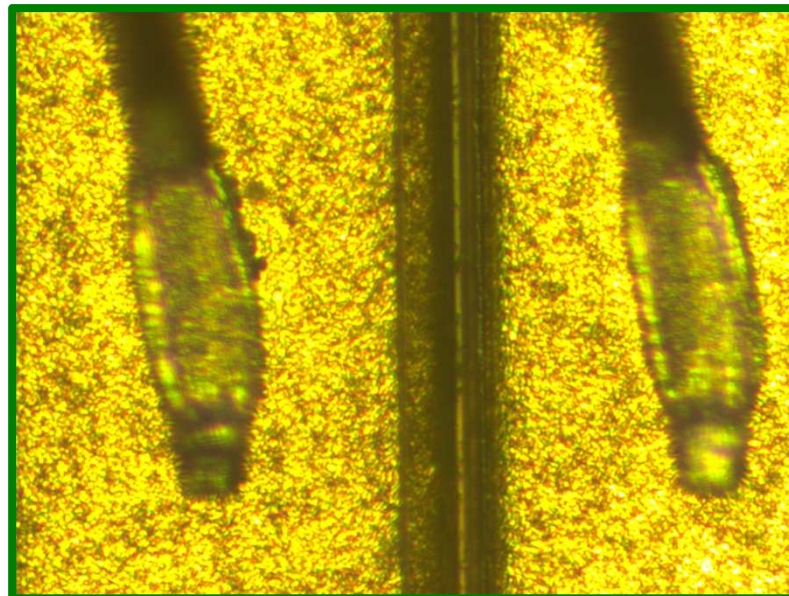
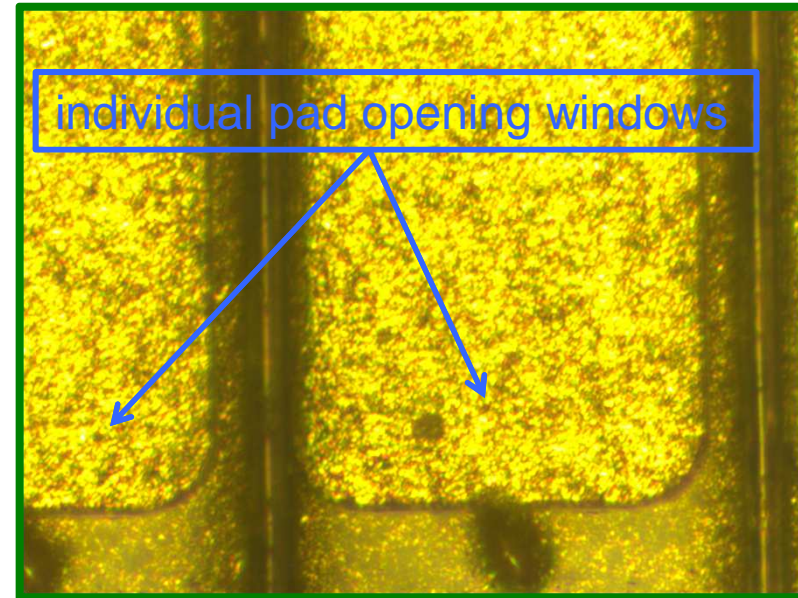
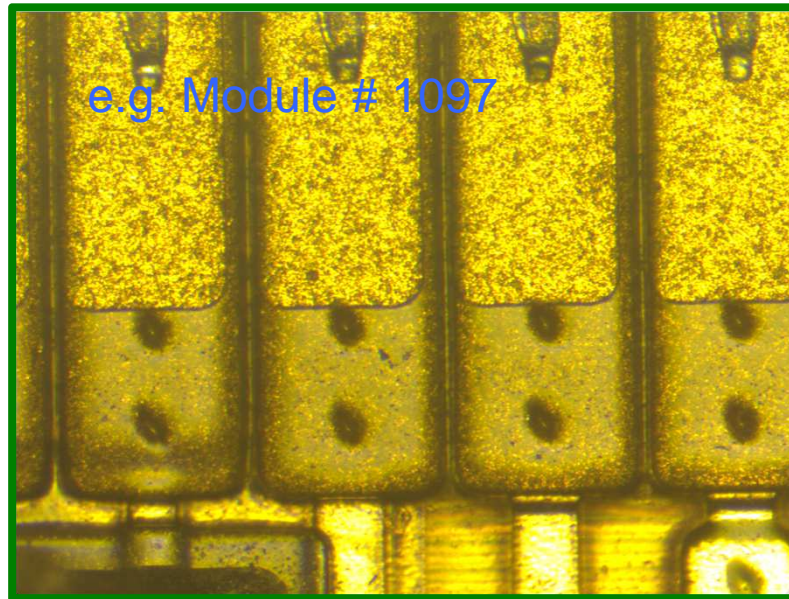


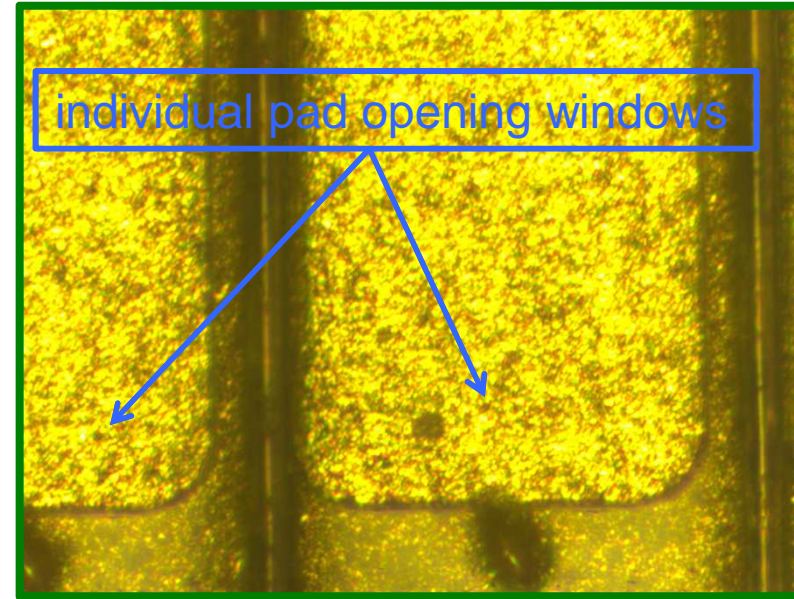
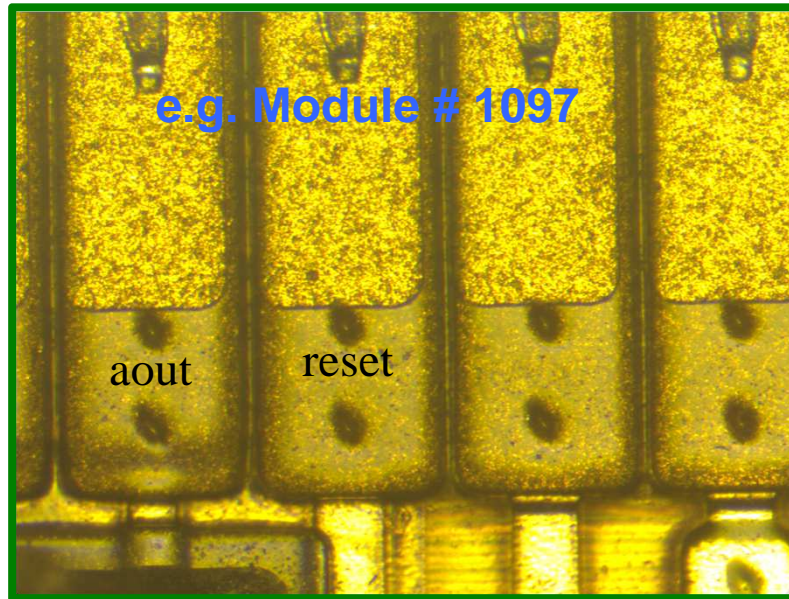
individual pad passivation window



ROC pads of HDI from 2005-2006
→ used till module # ~ 700

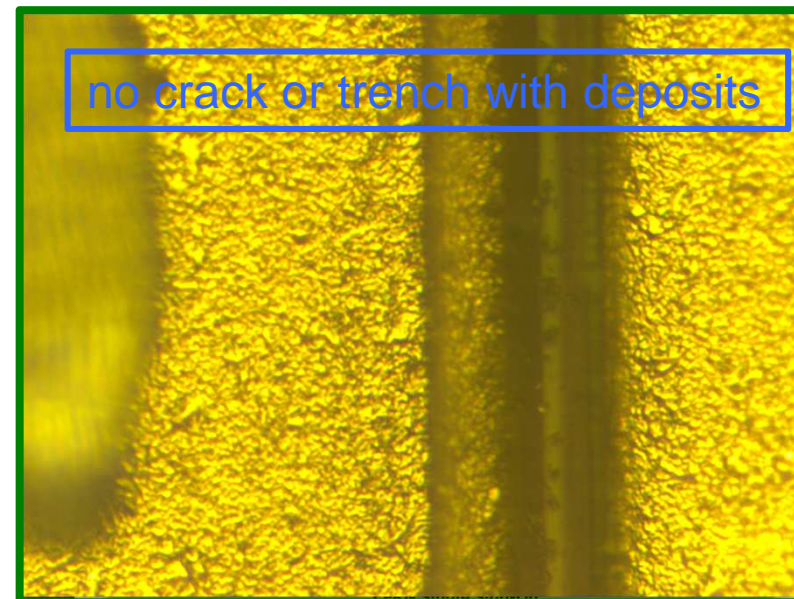
ROC pads of HDI from 2006-2007
→ used in module # ~ 700- 1200





From all the ~50 defect modules (some with multiple shorts) have **not seen a single short** between pads with individual pad openings.

HighTec does not manufacture their HDI like PCBs are done. Process based on build up on substrate, very much like chip manufacturing.





Damage Map of Layer 1

Layer 1, +x-side (near)				Quadrant BMI				Quadrant BPI (damaged)			
				Modules -z-side (Leman)				Modules +z-side (Jura)			
Face #		Ladder		-4	-3	-2	-1	1	2	3	4
1	Top	Half Outer	1				331	418	373		
2		Full Inner	2					757	571	452	1167
3		Full Outer	3				853	759	1197		
4		Full Inner	4								
5		Full Outer	5				818	771	1161	812	1155
6		Full Inner	6								
7		Full Outer	7				1050	130	69	1206	
8		Full Inner	8								
9		Full Outer	9				721	126	284	992	987
10	Bottom	Half Inner	10					376	473	425	387

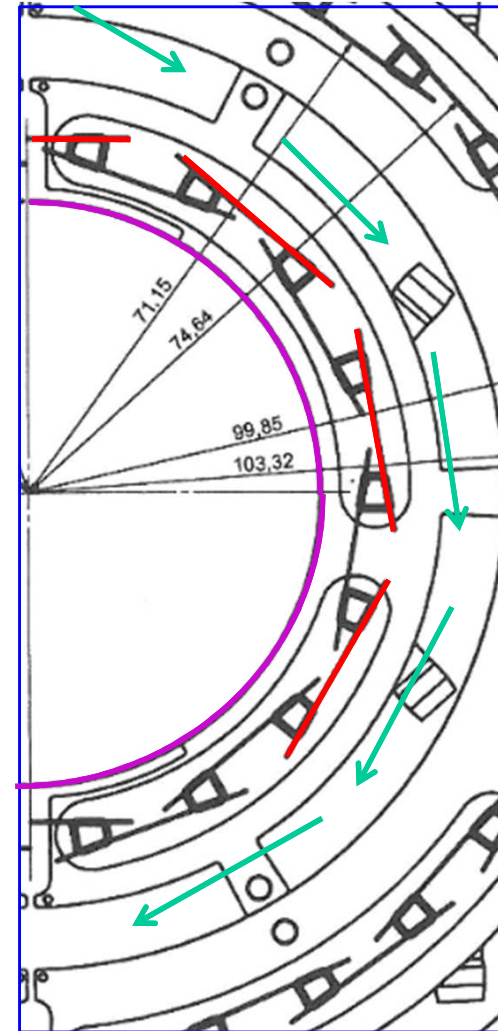
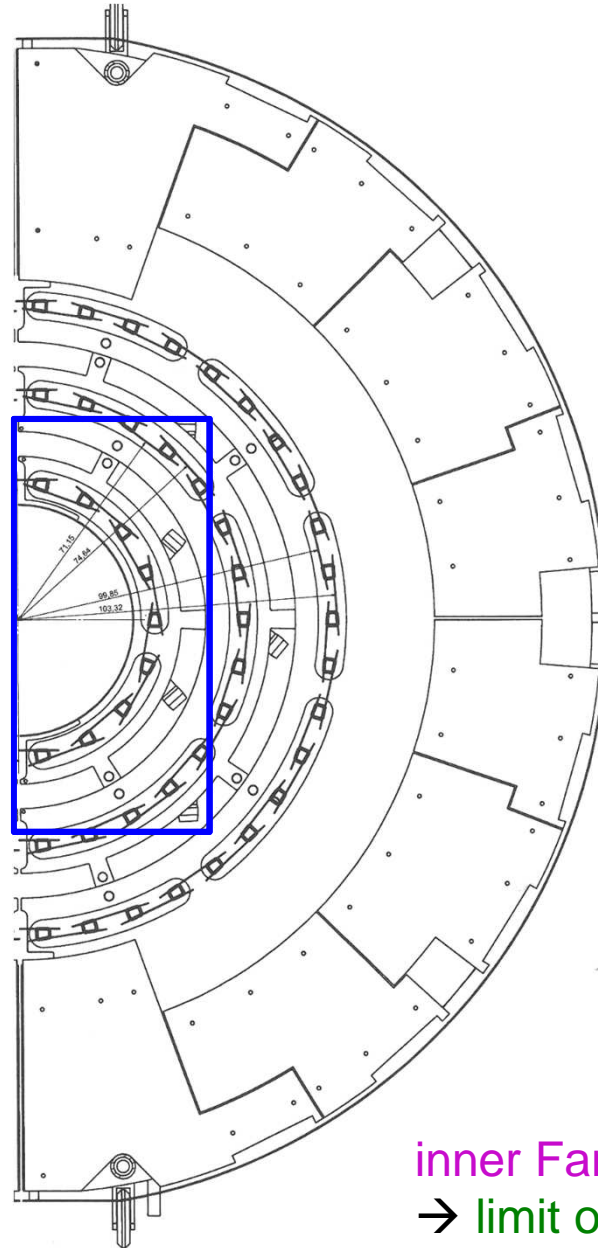
can be ignored

A striking pattern of damaged modules on the same mechanical half-shell !

Module number are scattered through randomly on both sides

Only difference is cabling of power and signals +z-side and -z-side

ventilators underneath create vertically airflow down



inner Faraday shield very close to 1st Layer modules
→ limit of airflow for innermost oriented modules?



Damage Map of Layer 2

Layer 2, +x-side (near)			Quadrant BMI				Quadrant BPI (damaged)			
			Modules -z-side (Leman)				Modules +z-side (Jura)			
Face #			-4	-3	-2	-1	1	2	3	4
1	Top	Half Outer								
2		Full Inner								
3		Full Outer								
4		Full Inner								
5		Full Outer		ignore					?	
6		Full Inner								
7		Full Outer								
8		Full Inner								
9		Full Outer							RDA	
10		Full Inner								
11		Full Outer								
12		Full Inner								
13		Full Outer								
14		Full Inner								
15		Full Outer								
16	Bottom	Half Inner								



Damage Map of Layer 3

Layer 3, +x-side (near)			Quadrant BMI				Quadrant BPI (damaged)			
Face #			Modules -z-side (Leman)				Modules +z-side (Jura)			
			-4	-3	-2	-1	1	2	3	4
1	Top	Half Outer		422	412	374	361		397	417
2		Full Inner								
3		Full Outer				95	210	ignore		
4		Full Inner		ignore						
5		Full Outer				573	487			
6		Full Inner								
7		Full Outer				482	183			
8		Full Inner								
9		Full Outer					477			
10		Full Inner								
11		Full Outer								
12		Full Inner								
13		Full Outer								
14		Full Inner								
15		Full Outer								
16		Full Inner								
17		Full Outer								
18		Full Inner								
19		Full Outer								
20		Full Inner					RDA			
21		Full Outer								
22	Bottom	Half Inner								HV



How could this have happened ? A few facts

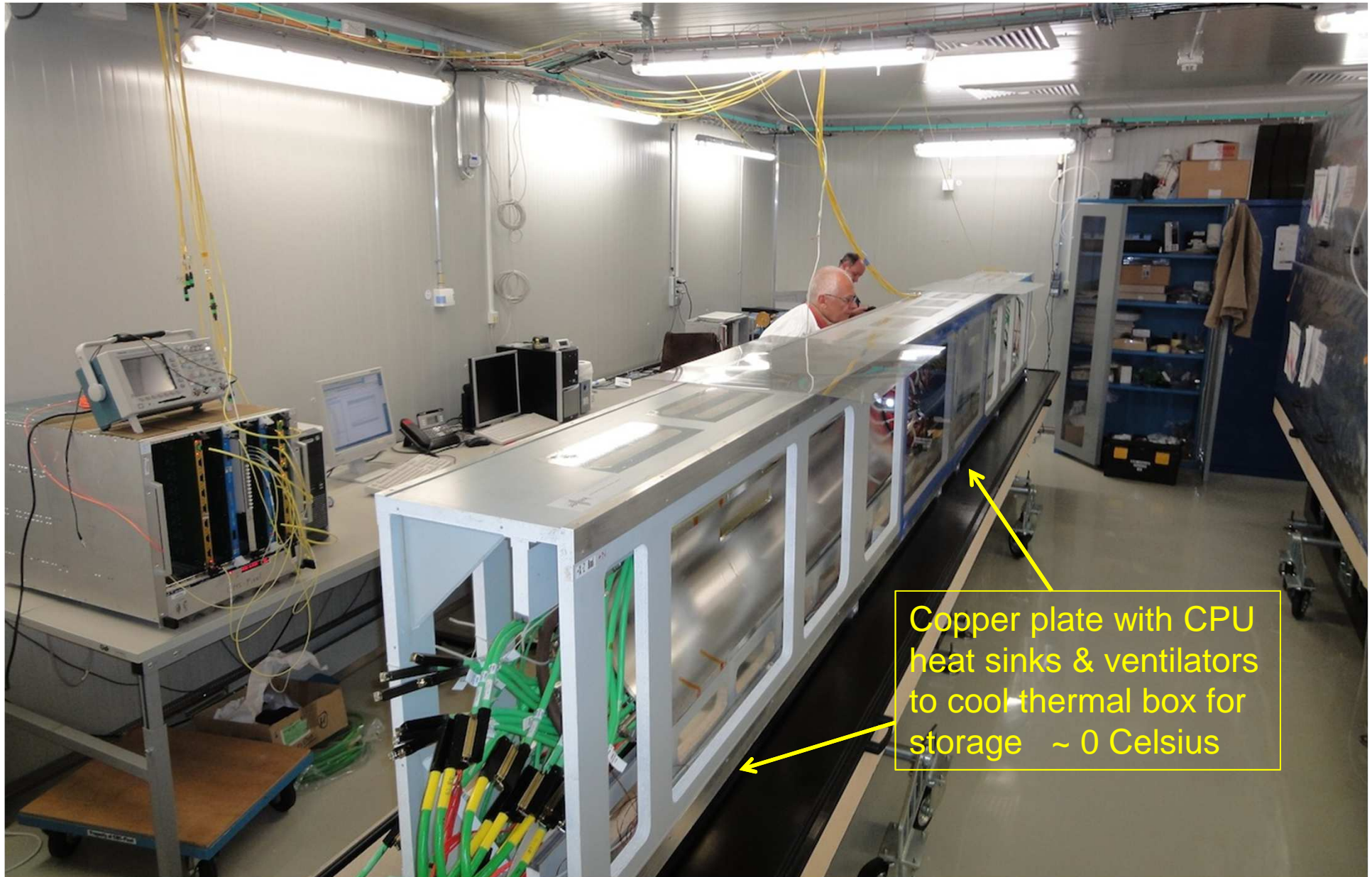


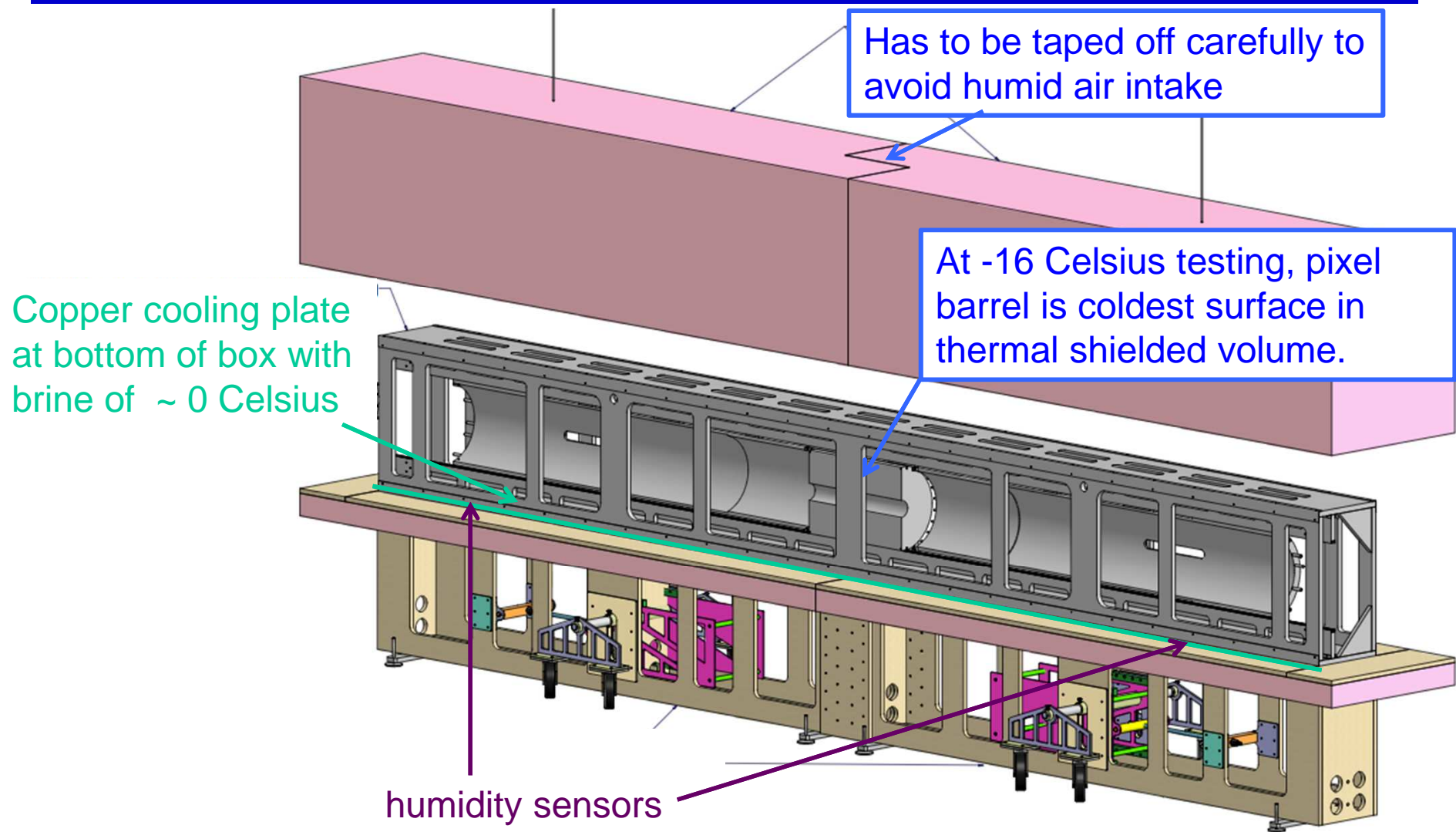
- power & signaling is **only** parameter in BPIX barrel that distinguishes +z-side (damaged) from -z-side (undamaged)
- 3 other quadrants ok and no damage. Same distribution of module#, HDI-batches, ROC #, TBM #, etc. etc. etc.
- all symptoms of damage indicate a defect mechanism that implies **voltage applied** in a crucial (bad) moment
- shorts happen with strong preference between pads of **2V** difference or more.
- **observe “burning away” of shorts** for larger currents → no VDD shorts to GND
- HDI **shorts only** at pads with **common passivation windows** (*trenches*)
- shorts only in close proximity of SMD soldering pads → flux residues (acids)
- Need 3 ingredients for shorts: **humidity (condense), acid (electrolyte) & voltage !**
- **Condensation accident in -16°C calibration runs in cooling box at P5 is most likely hypothesis and consistent with all observed symptoms.**



Cooling Tables of BPIX in P5 Pixel Lab



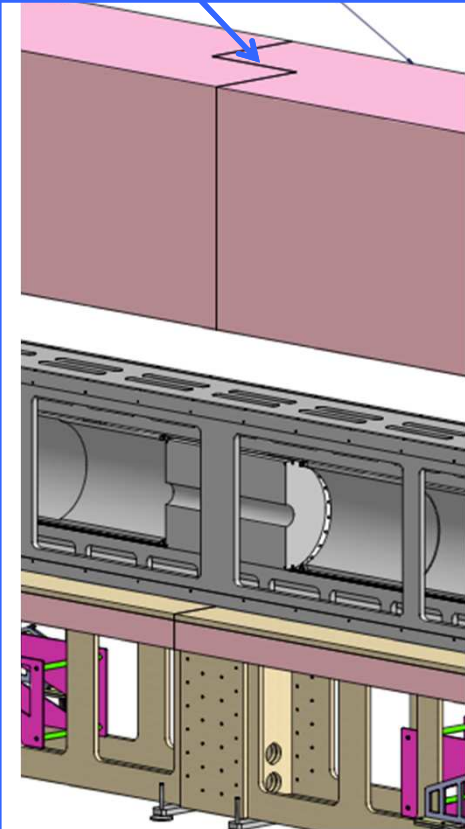




Most likely scenario of events:

- thermal covers opened / closed many times 2013/14
- sealing in Nov/Dec 2013 tests probably left small leak at $z \sim 0$
- small plumes of humid air (\sim liters/min) leak inside volume
- copper cooling plate at $\sim 0^\circ\text{C}$ with air temperature $\sim +8^\circ\text{C}$
- ventilators pull down air flow from gap of thermal covers
- local humidity cloud deposits micron thick ice film on **coldest surfaces** \rightarrow **pixel modules & cooling pipes** (-16°C)
- modules under power melt the ice, since HDI on top of sensor has poor thermal contact to cooling pipes.
- **sectors under test** with **power** gets **damaged** by electro-chemical migration with metalorganic-complexes from flux residues in very narrow, deep HDI cracks of early serial #'s.
- modules without power have inert ice film that will later sublime away again. (no power = no damage)
- humidity sensors at $z \sim \pm 200\text{cm}$ will not see anything !

humid air intake in unclosed gap



(CSI = Crime Scene Investigation)



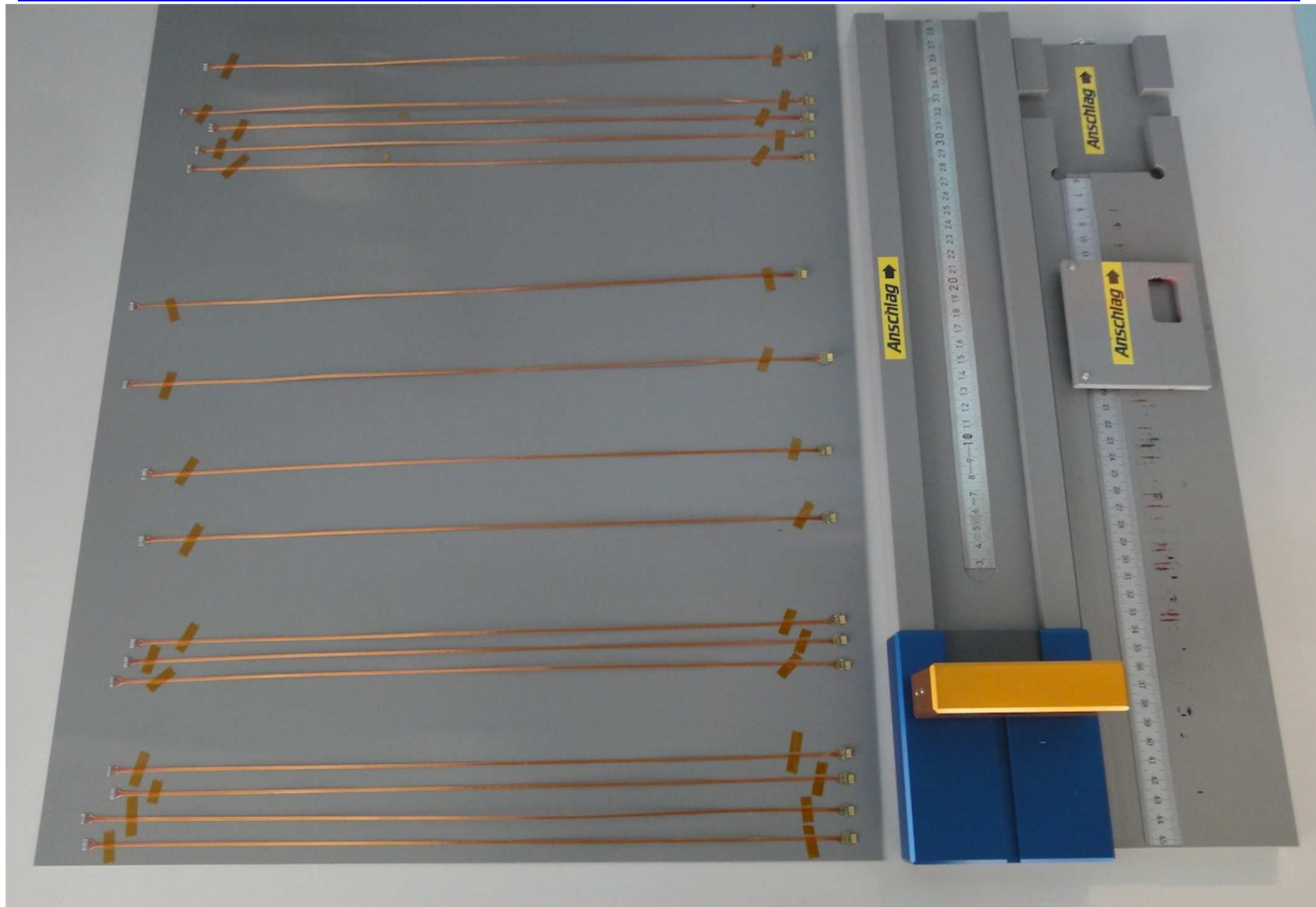
install into CMS

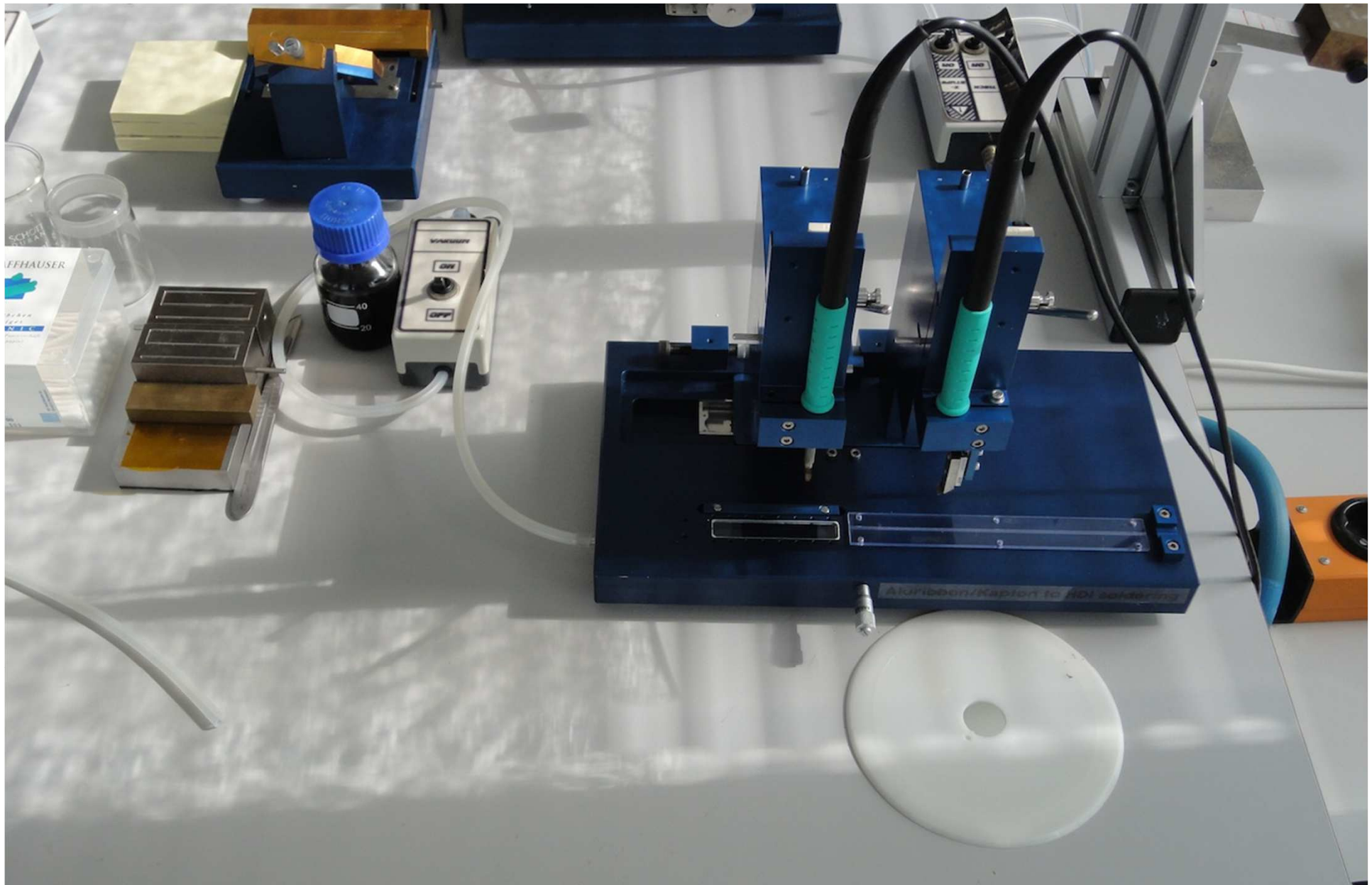


Tasks	Week 39, 22.Sep - 26.Sep					Week 40, 29.Sep - 3.Oct					Week 41, 6.Oct - 10.Oct					Week 42, 13.Oct - 17.Oct					Week 43, 20.Oct - 24.Oct					Week 44, 27.Oct - 31.Oct				
	Mo	Tue	Wed	Thu	Fri	Mo	Tue	Wed	Thu	Fri	Mo	Tue	Wed	Thu	Fri	Mo	Tue	Wed	Thu	Fri	Mo	Tue	Wed	Thu	Fri	Mo	Tue	Wed	Thu	Fri
replace repaired module in layer 3																														
check out & map damaged BPI																														
transport BPI halfshell P5 --> PSI																														
set up lab & testing equipment																														
testing of complete BPI at PSI																														
module production																														
production of old HDI by HighTec																														
HDI & cable & tbm with testing																														
bump bonding 40 modules																														
glue modules & wirebond																														
test & qualify modules																														
uncable & take BPIX apart																														
layer 1 repair																														
remove bad & good obstacle modules																														
diagnose & study defects																														
repair modules																														
test & qualifiy repaired modules																														
prepare cold storage layer 1																														
layer 2 repair																														
remove bad & good obstacle modules																														
diagnose & study defects																														
repair modules																														
test & qualifiy repaired modules																														
prepare cold storage layer 2																														
layer 3 repair																														
remove bad & good obstacle modules																														
diagnose & study defects																														
repair modules																														
test & qualifiy repaired modules																														
assemble BPIX halfshell																														
layer 1 select & remount modules																														
layer 2 select & remount modules																														
layer 3 select & remount modules																														
merge 3 layers & reconnect																														
test & qualify BPIX halfshell																														
transport BPIX from PSI -> P5																														
supply tube testing at P5																														
combine supply tubes & BPIX																														
testing complete BPIX/ST-system																														
install into CMS																														
																</														

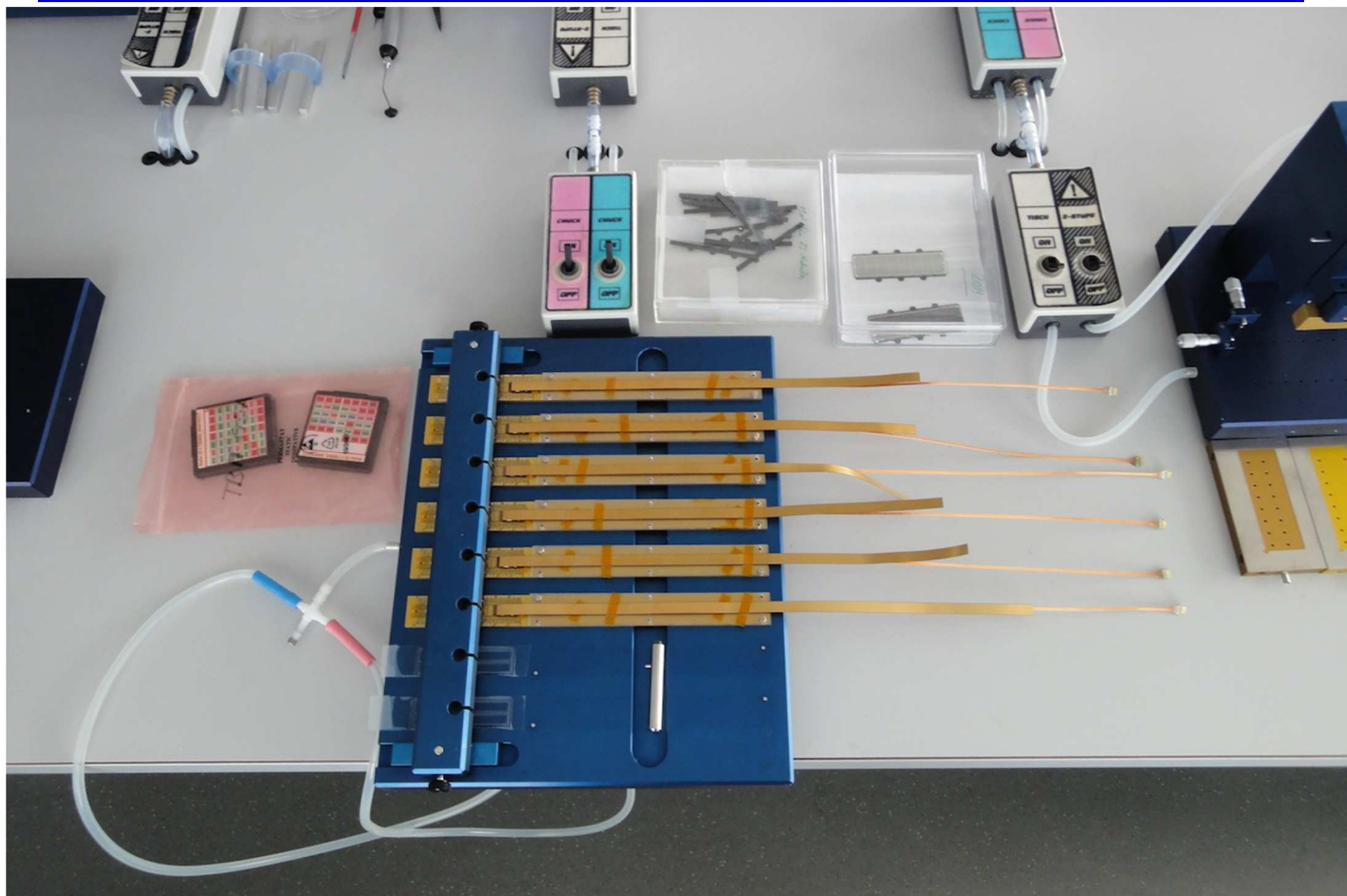


Preparing Cables for Module Production





Glueing TBM to HDI



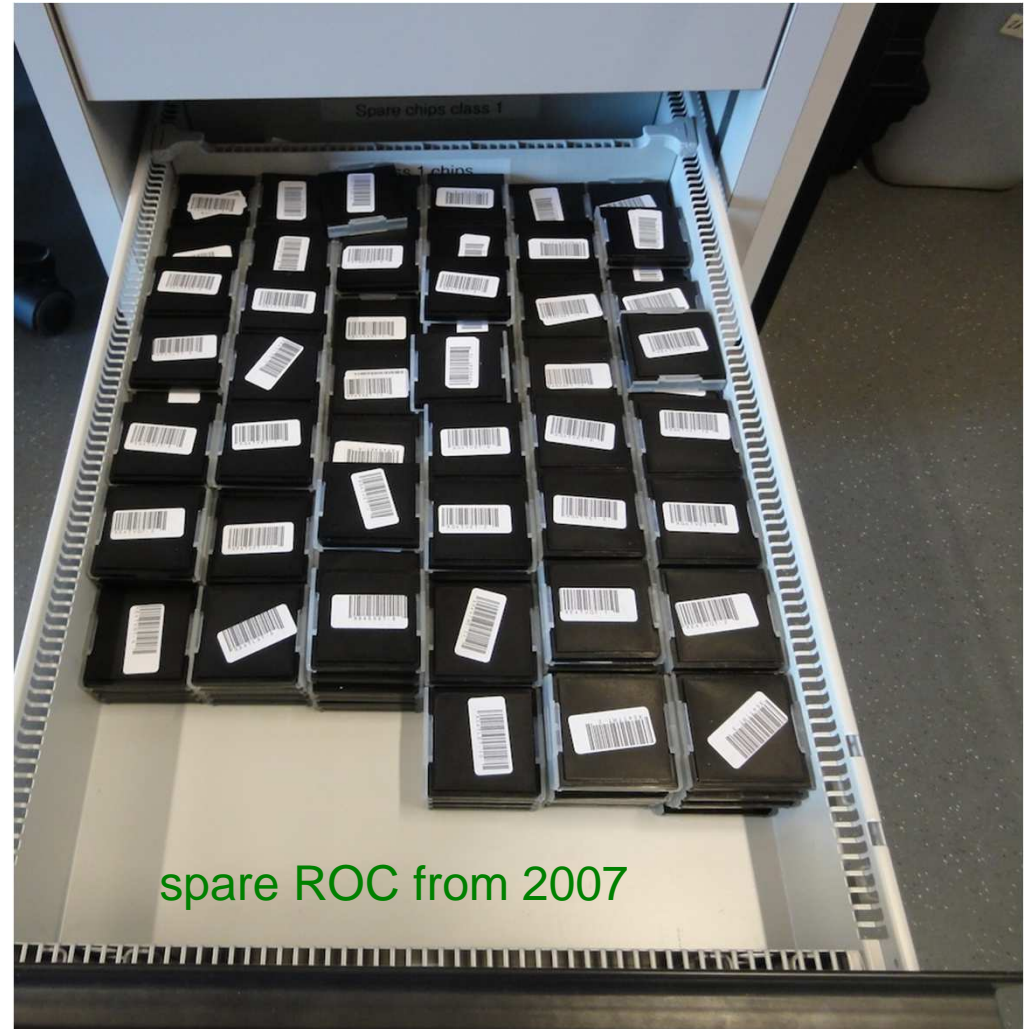


Bump bond ~40 new modules at DECTRIS

spare sensors from 2007

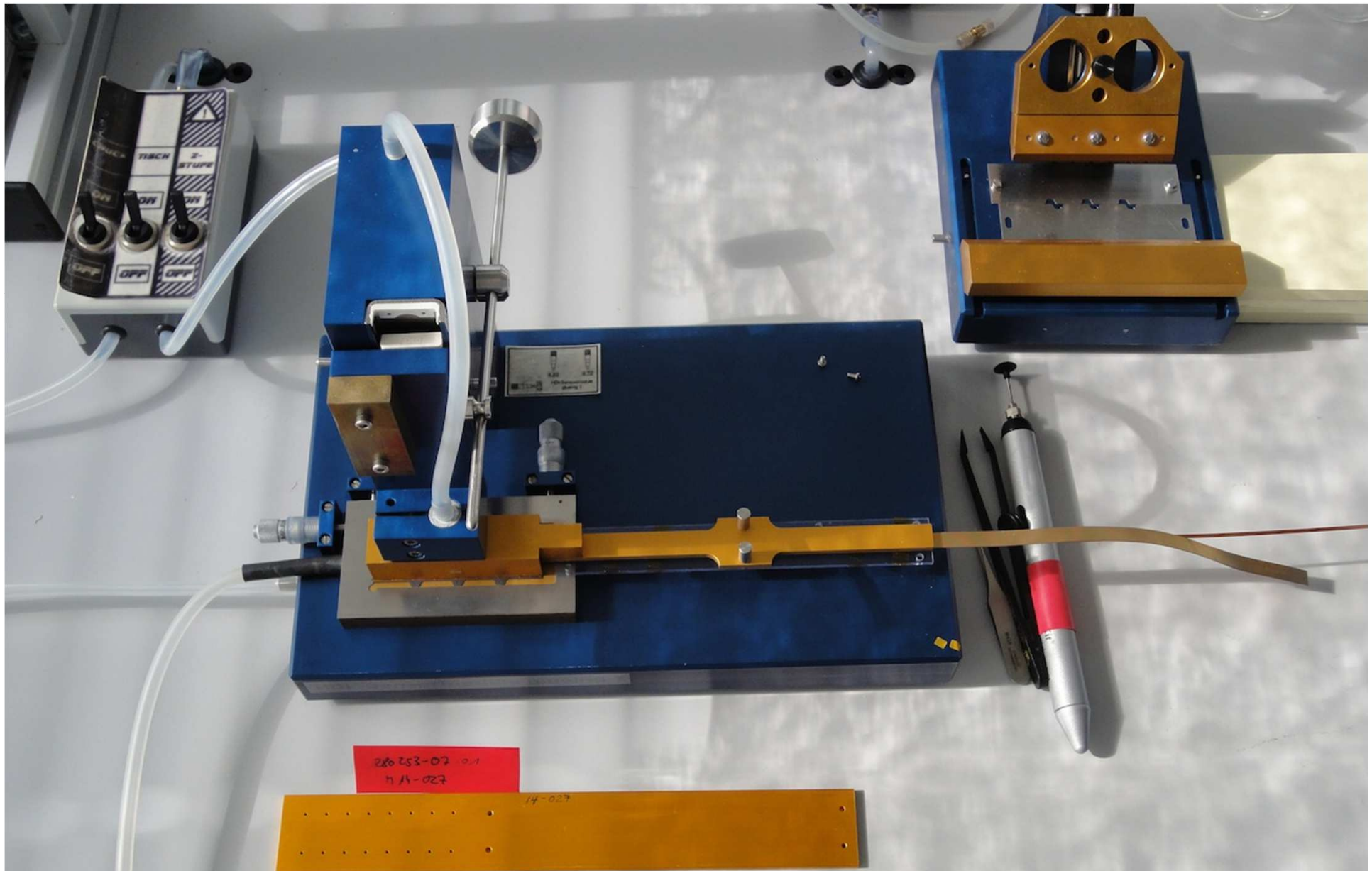


spare ROC from 2007

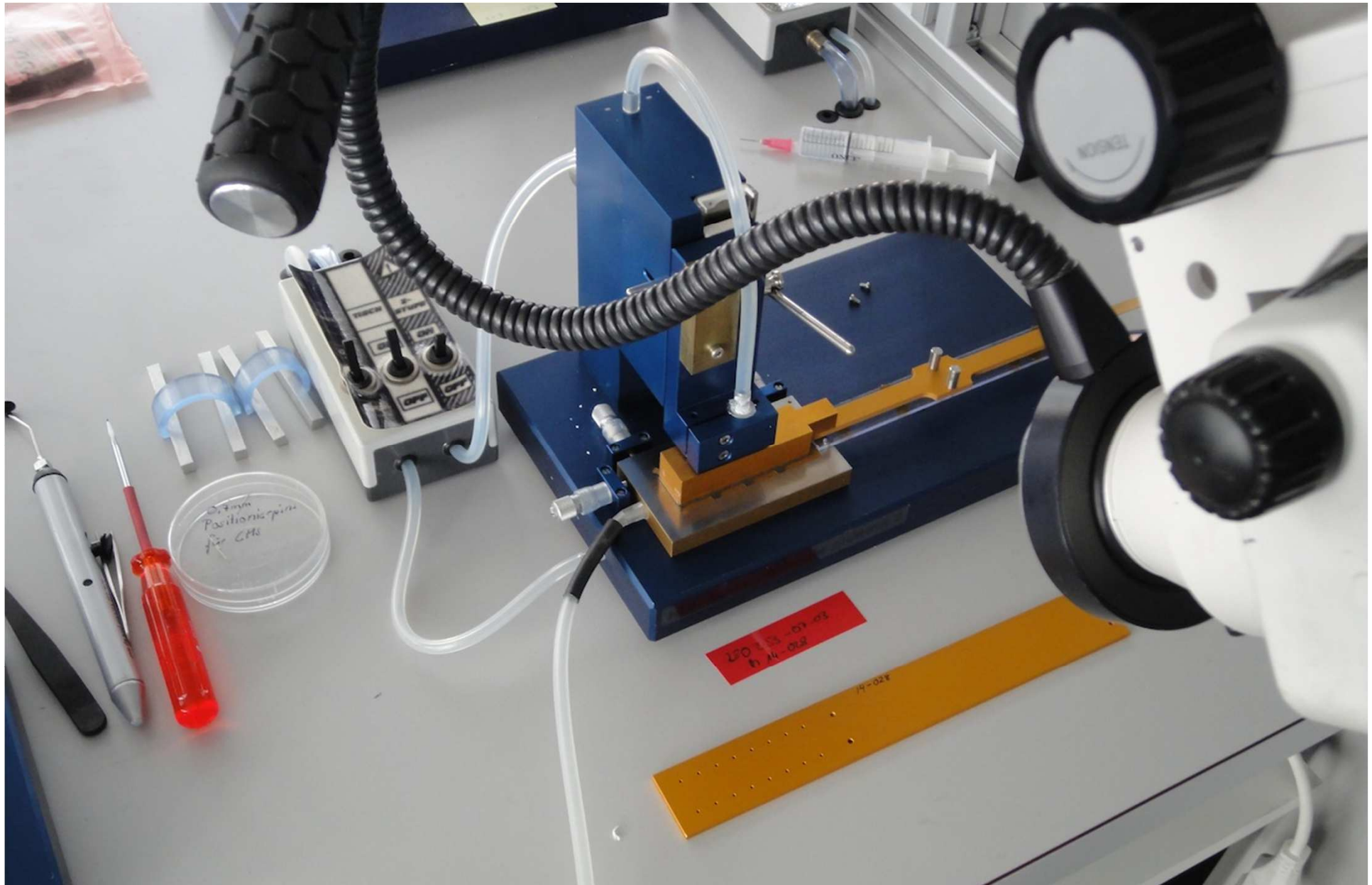




HDI to Bare Module glueing (Station 1)

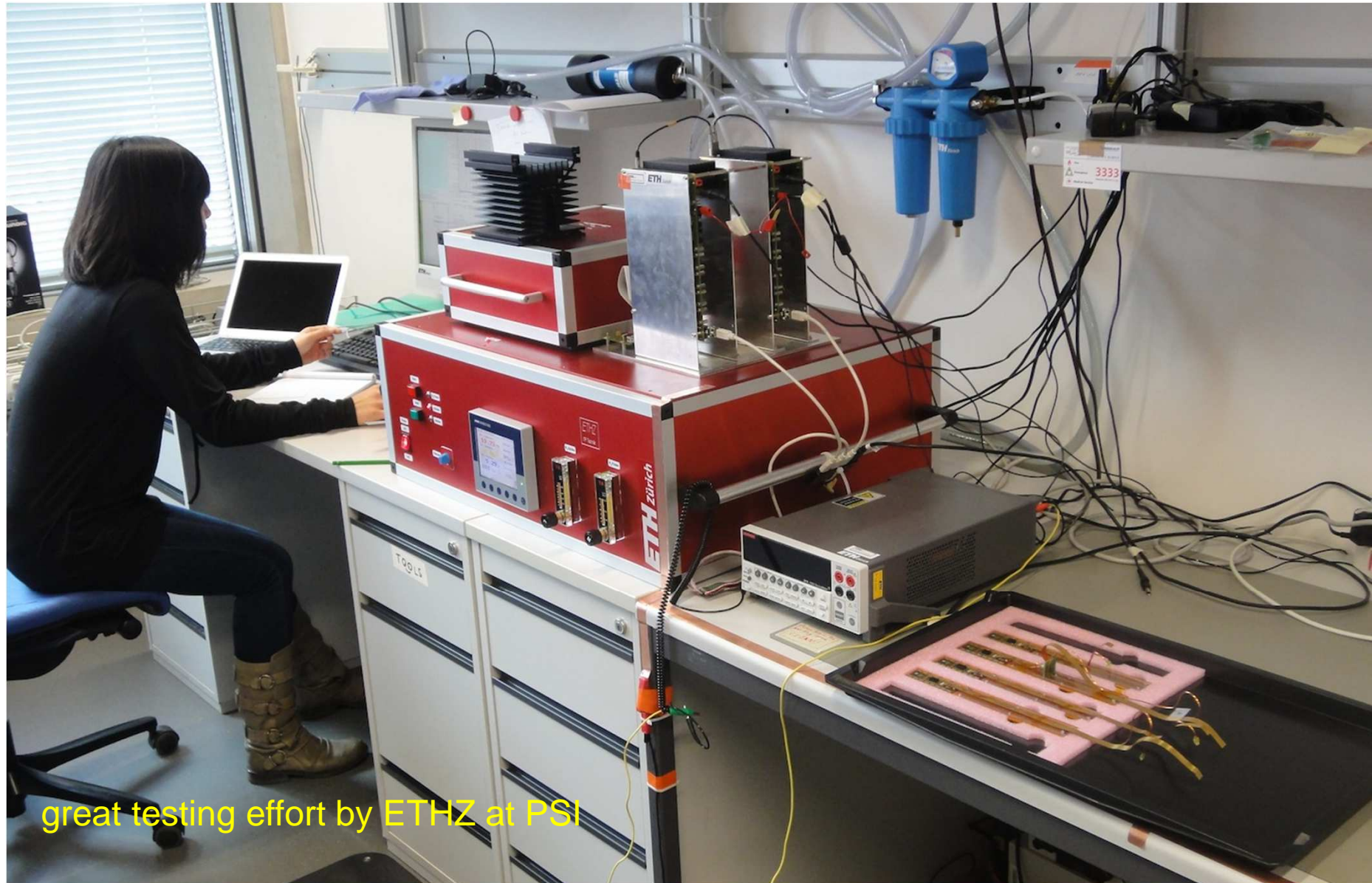


HDI to Bare Module glueing (Station 2)





Testing & Qualification of BPIX Modules



great testing effort by ETHZ at PSI



Statistics of Module Repair and Production



- Damaged and removed modules:
 - 39 repaired
 - 7 worked by themselves or various uncontrolled manipulations
 - 10 not repaired
- Used for final replacement were:
 - 40 new or fresh modules
 - 19 repaired modules , selected by grading scheme
- Module remounting was done in following order:
 - Layer 1 with mostly new modules → back to fridge
 - Layer 2 with few repaired modules → back to fridge
 - Layer 3 with ~50% repaired modules → done Friday, 1. Nov. 2014



bold and underline

Module replaced	
Module repaired	
Problem before incident	
Module was dismantled	



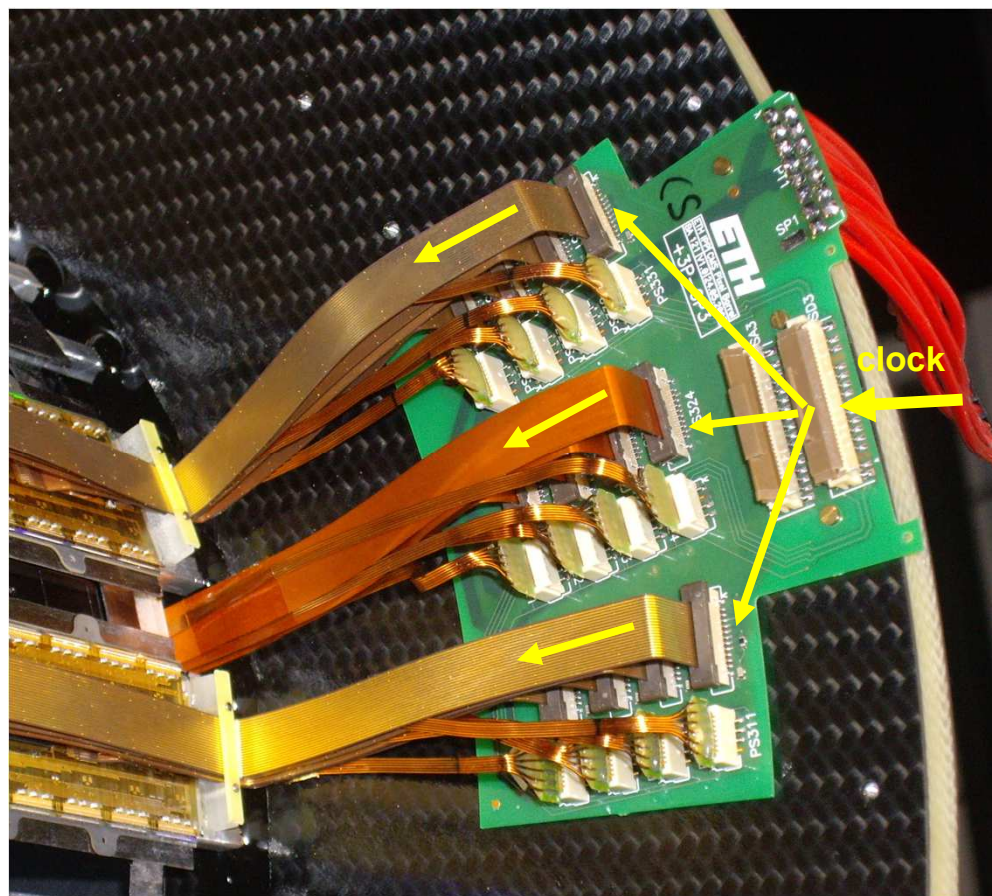
Remounting scheme of Layer 2

Ladder	Quadrant BMI				Quadrant BPI (damaged)			
	Modules -z-side (Leman)				Modules +z-side (Jura)			
	-4	-3	-2	-1	1	2	3	4
1				1012	379	416	385	383 b 391
2				761	672 b 1428	687 b 1418	939	
3				558	283 b 1403	637		
4				743	138	767 b 1446	579	194 b 1432
5		135 b 844	888	809	246	494 b 1452	598	627
6				43	700	860 b 1450	143	
7				444	456	682 b 1441	800	1103
8				944	787	581 b 1454	615 b 1453	473
9				148	242	254 b 1437	460 b 1424	689 b 110
10				113	1180	281 b 1442	289 b 1448	167
11				593	885			
12				301	286 b 1423	564 b 1445	654	
13				549	83			
14				565	47	185	215	31
15				264	636			
16				965	363			

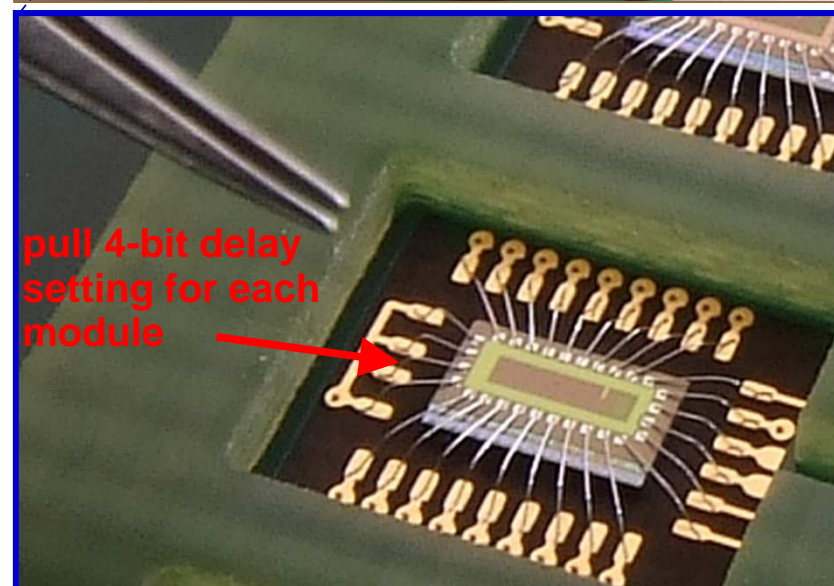
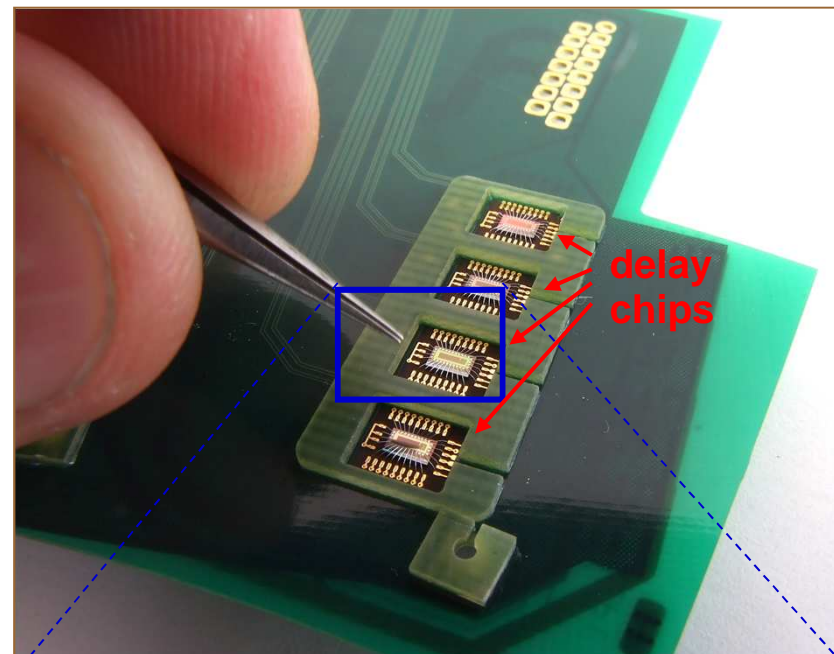


Remounting scheme of Layer 3

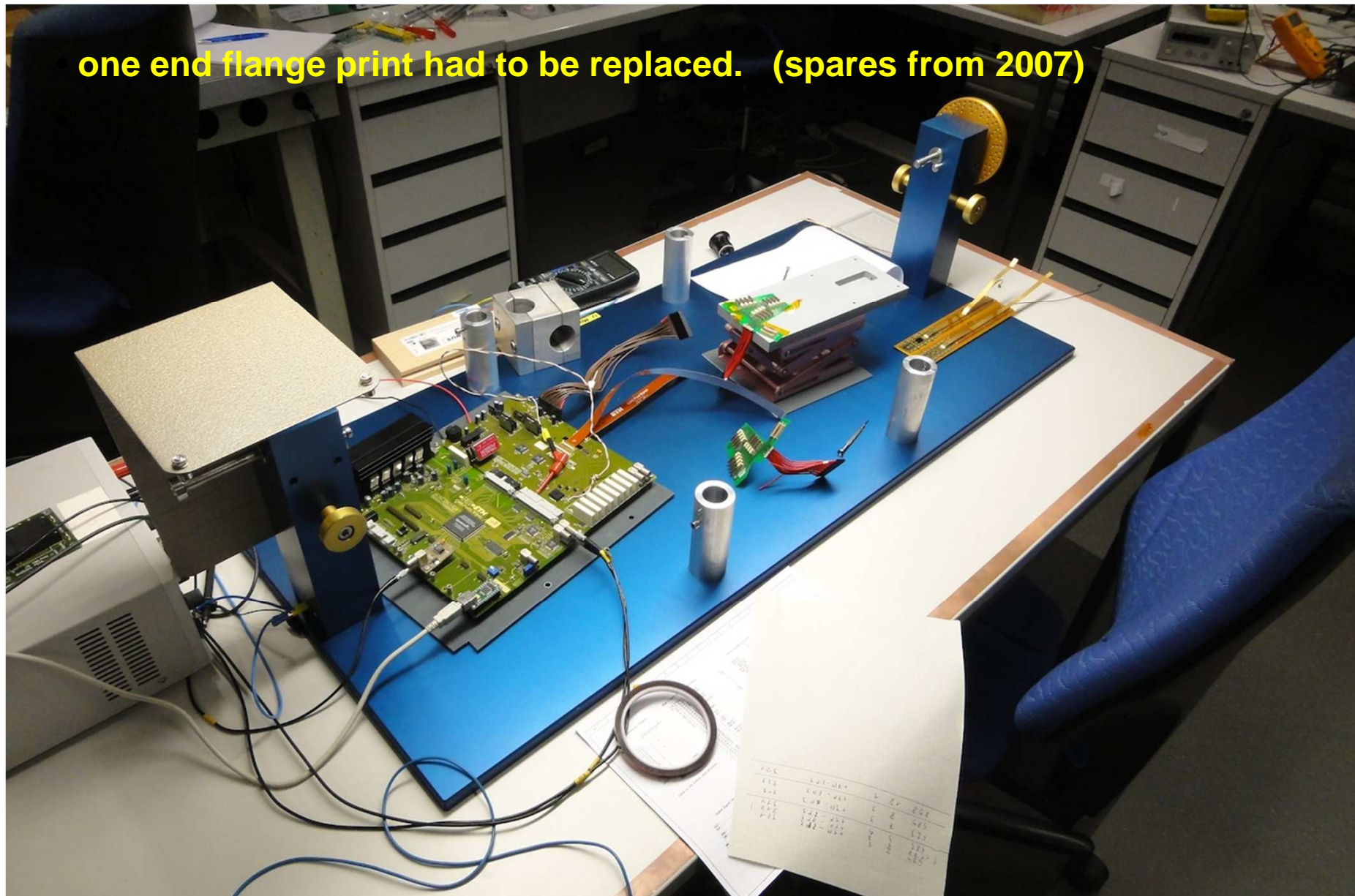
Ladder	Quadrant BMI				Quadrant BPI (damaged)			
	Modules -z-side (Leman)				Modules +z-side (Jura)			
	-4	-3	-2	-1	1	2	3	4
1		422	412	374	361		397	417
2				430	524	1117	41	218 ▸ 1416
3				95	210 ▸ 570	1178	236	685 ▸ 273
4		128 ▸ 1172	448	789	707			
5				573	487	1097	192	447
6				776	705 ▸ 830	981	706	747
7				482	183	486	623	911
8				1146	523	752	589	676 ▸ 1414
9					477	624	873	1063
10				715	648	882	241	521
11					827	70		
12				788	713	895 ▸ 832	155	165
13					1140	497	1211 ▸ 490	262 ▸ 1415
14				305	1101	1119		
15					1165	1163 ▸ 1205	577	1144
16				463	975			
17					1186			
18				483	898 ▸ 674	1067		
19					1132			
20				59	582 (RDA)	712	890	
21					1135			
22				415	357			370(HV) ▸ 375

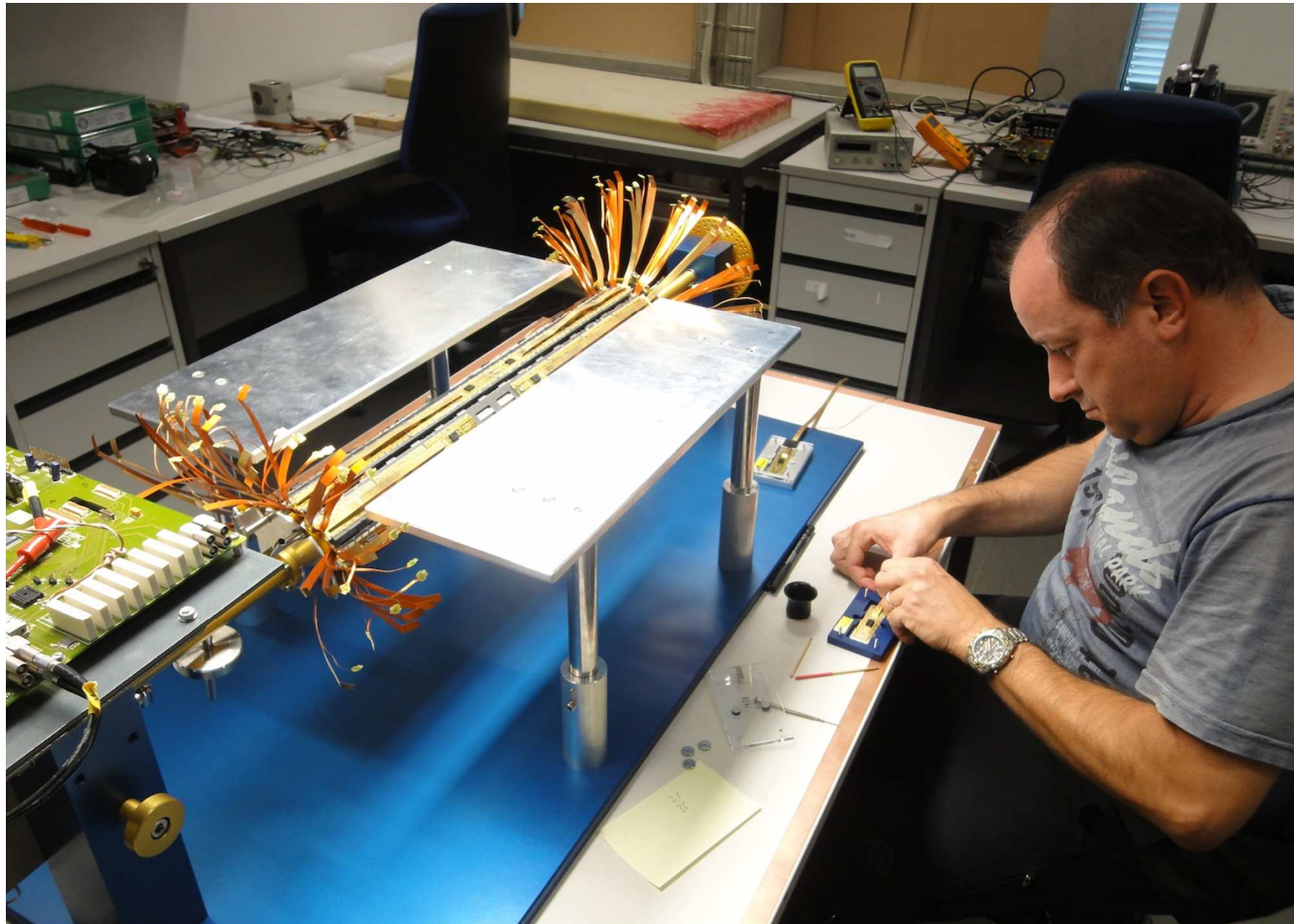


- **delay chips** behind each Kapton cable plug
- delay range 0-3.2nsec, 4-bit \rightarrow 0.2nsec

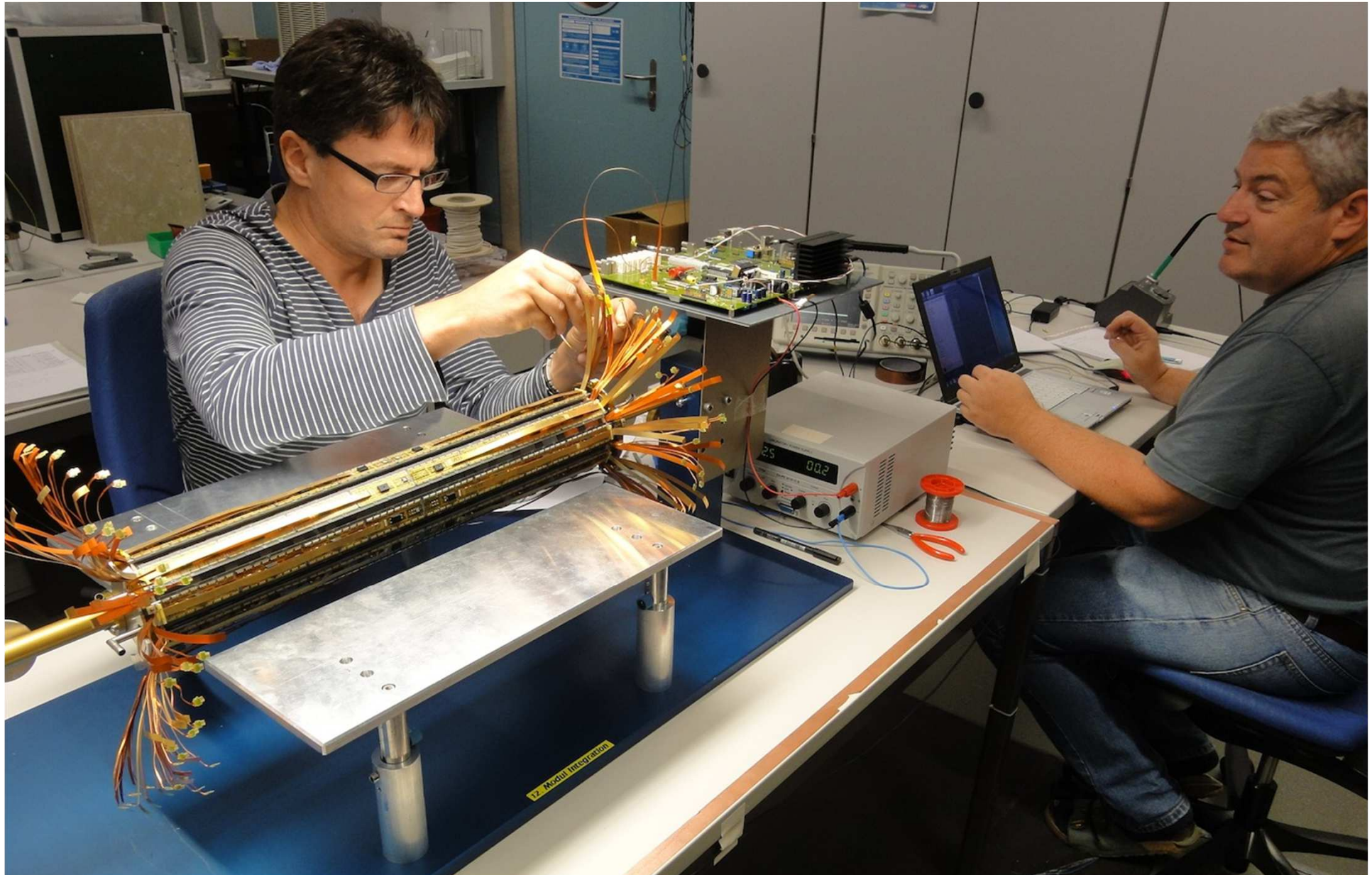


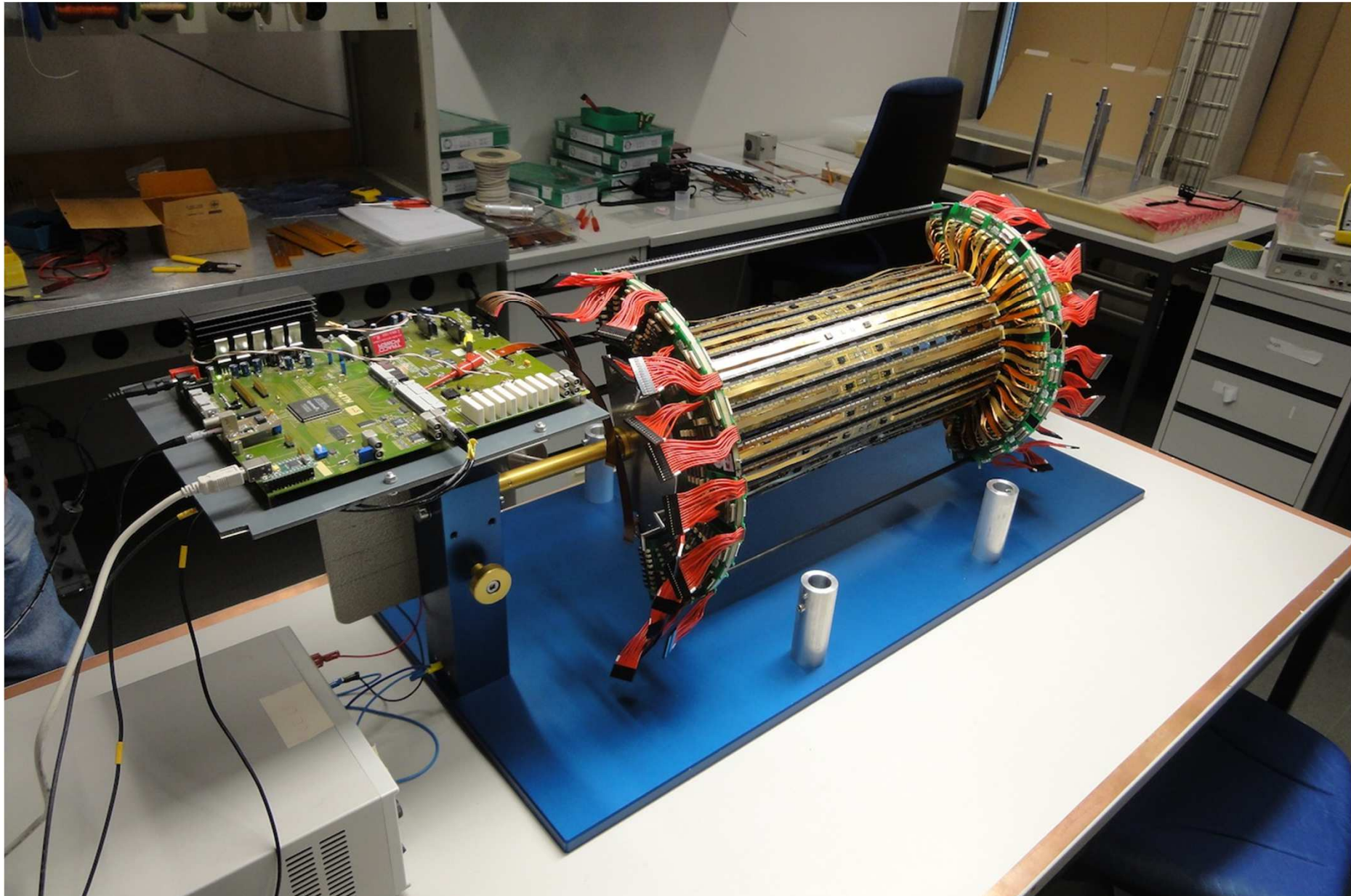
one end flange print had to be replaced. (spares from 2007)





Module testing of remounted Layer 1







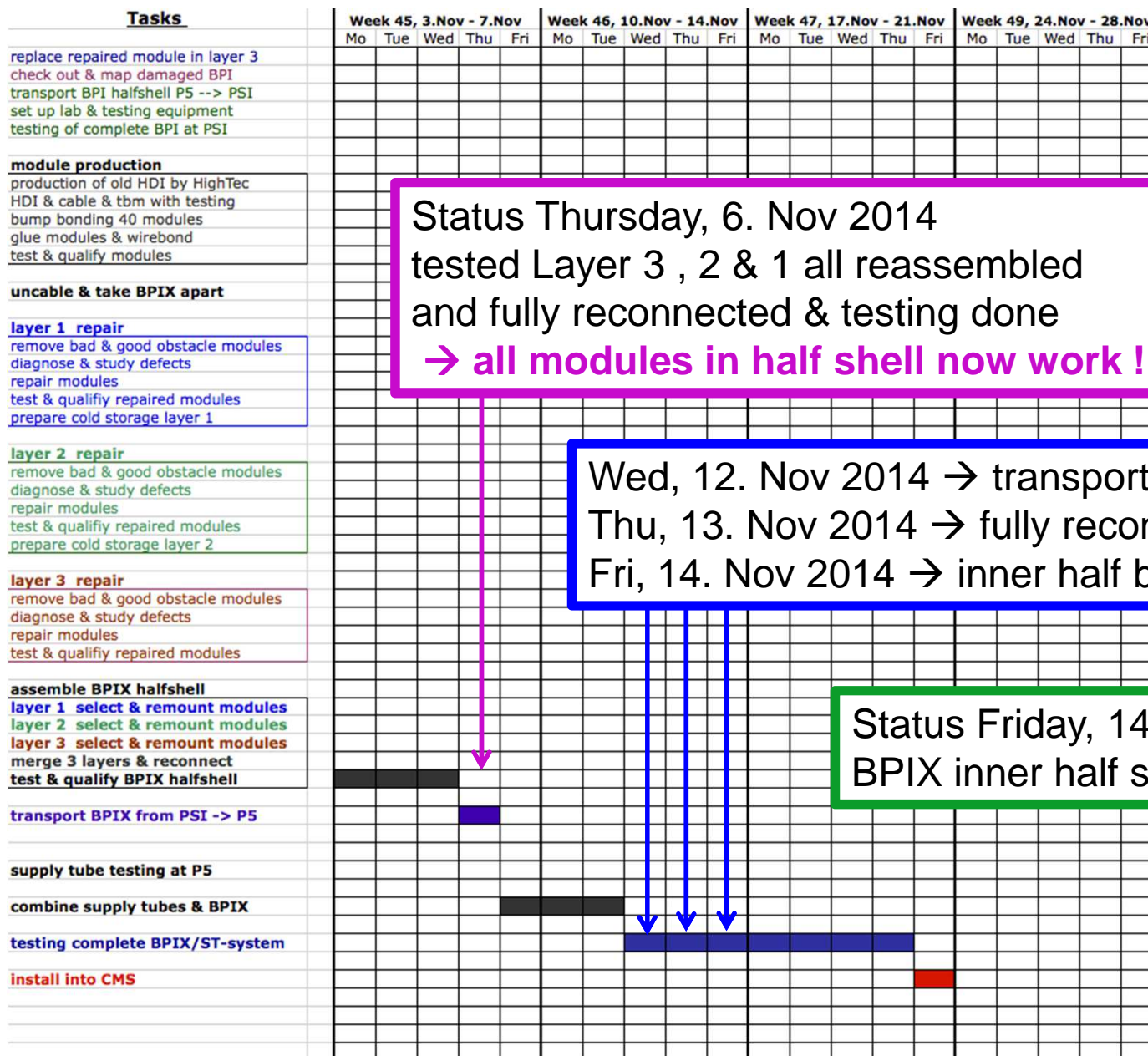
Testing of complete module groups of Layer 3





BPIX Repair Schedule (3)

this is still the original
schedule from begin
September





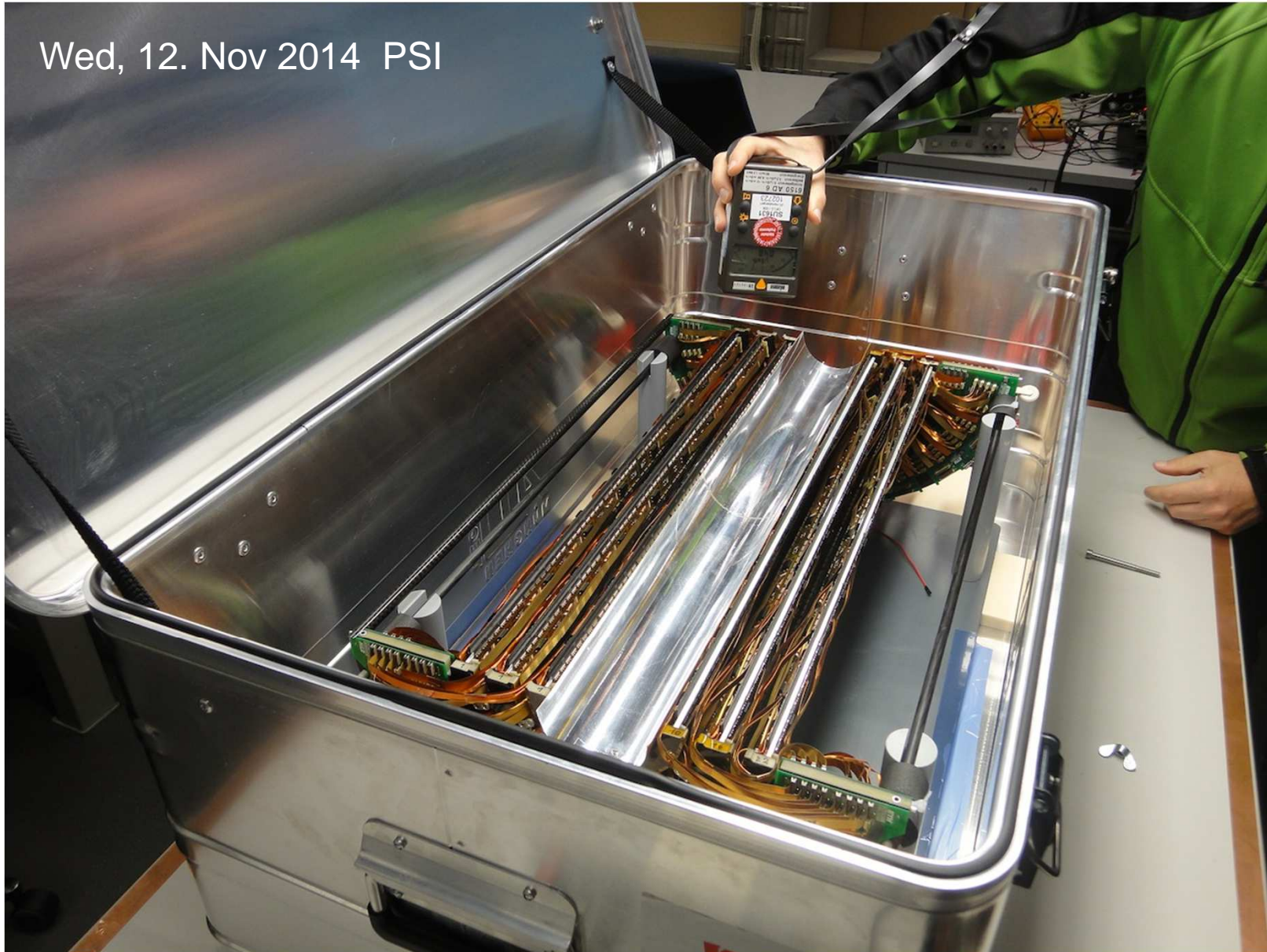
Spare Supply Tube for Power Supply Testing



Testing of Supply Tubes at P5 has been done before re-integration (*Uni ZH*)



Wed, 12. Nov 2014 PSI

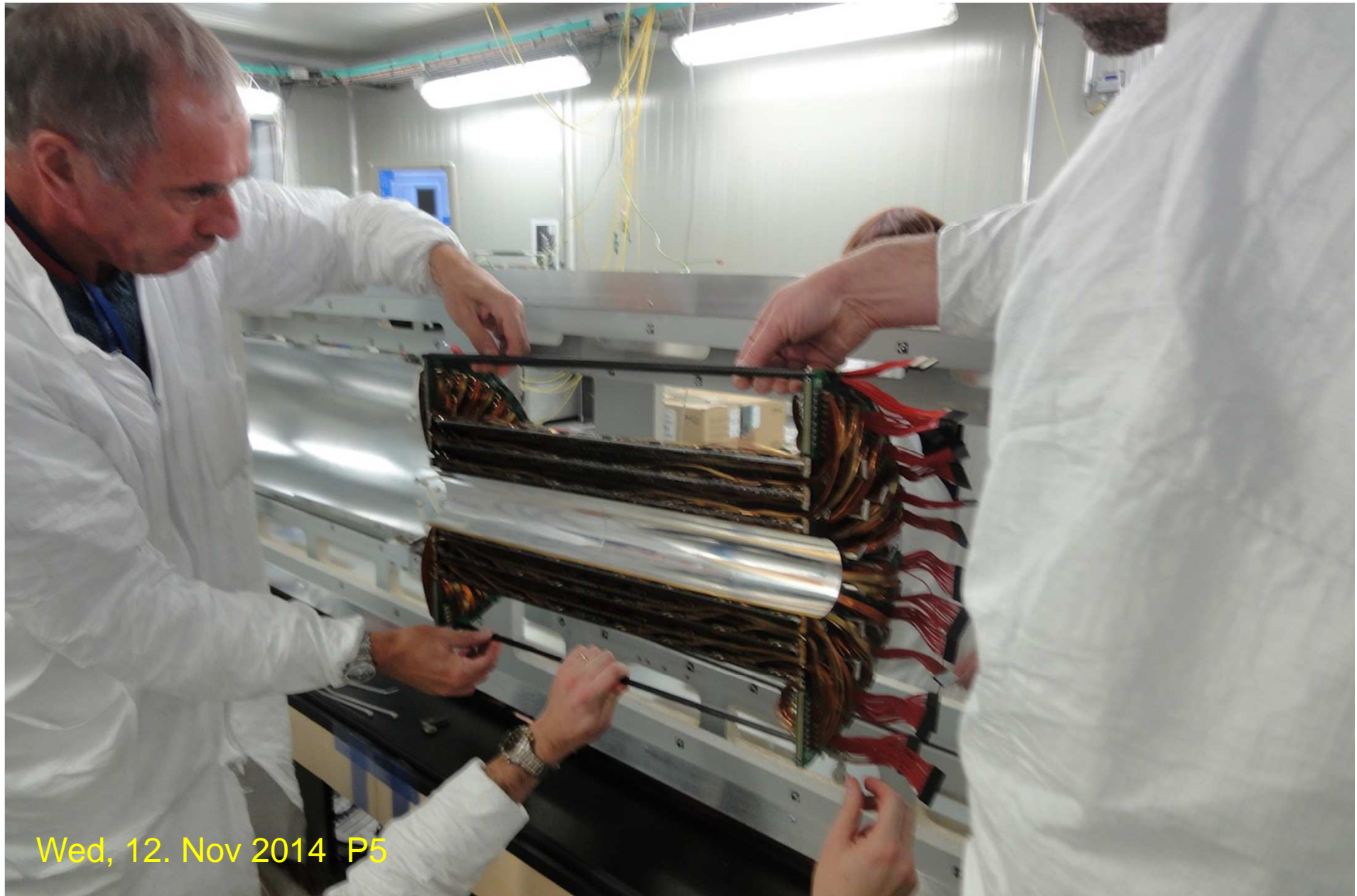




Getting Ready for PSI → P5 Transport



Reinserting Barrel into Rails in Cassette



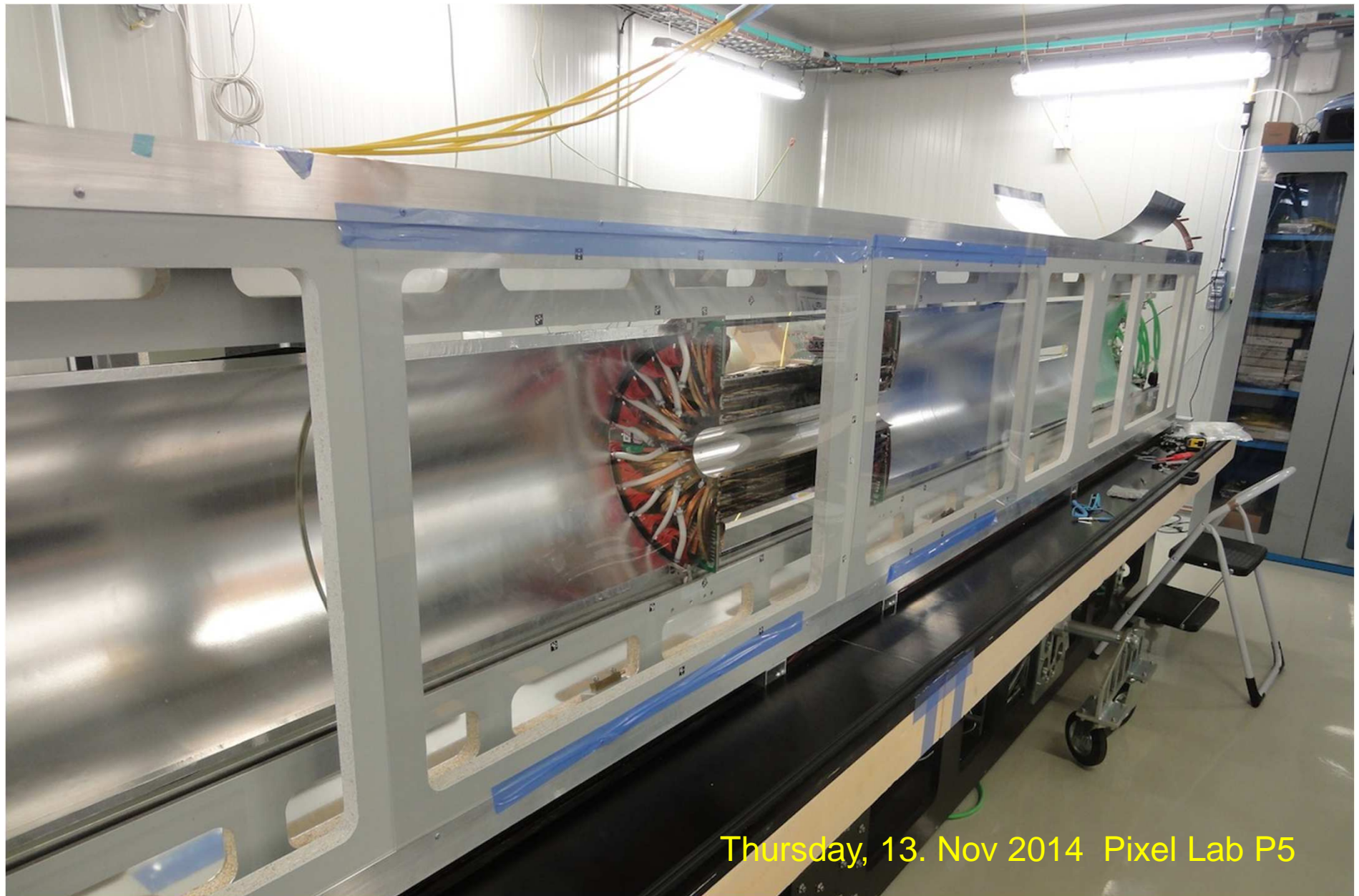
Wed, 12. Nov 2014 P5



Thu, 13. Nov 2014 P5



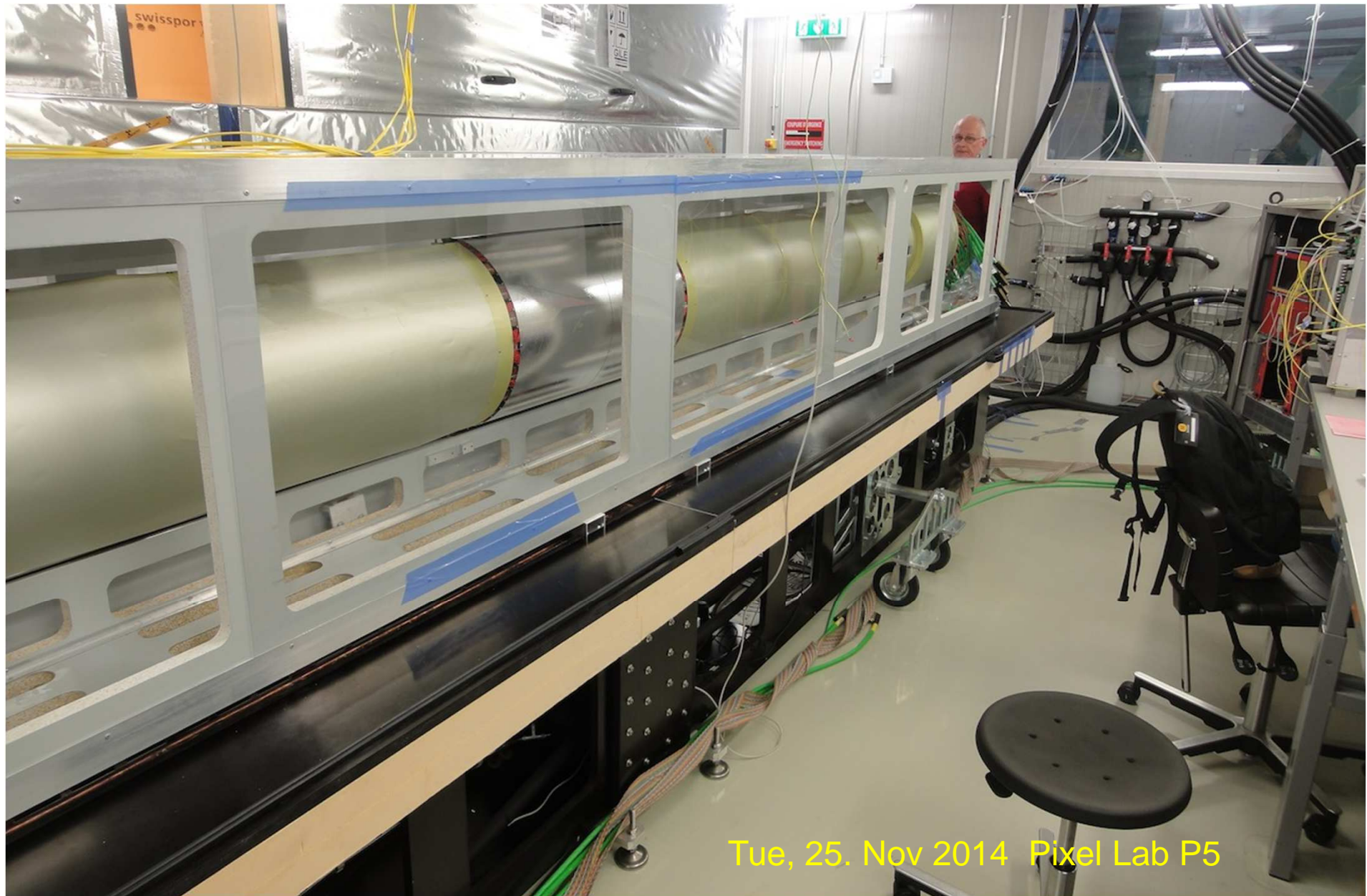
Supply Tubes and inner Barrel reconnected



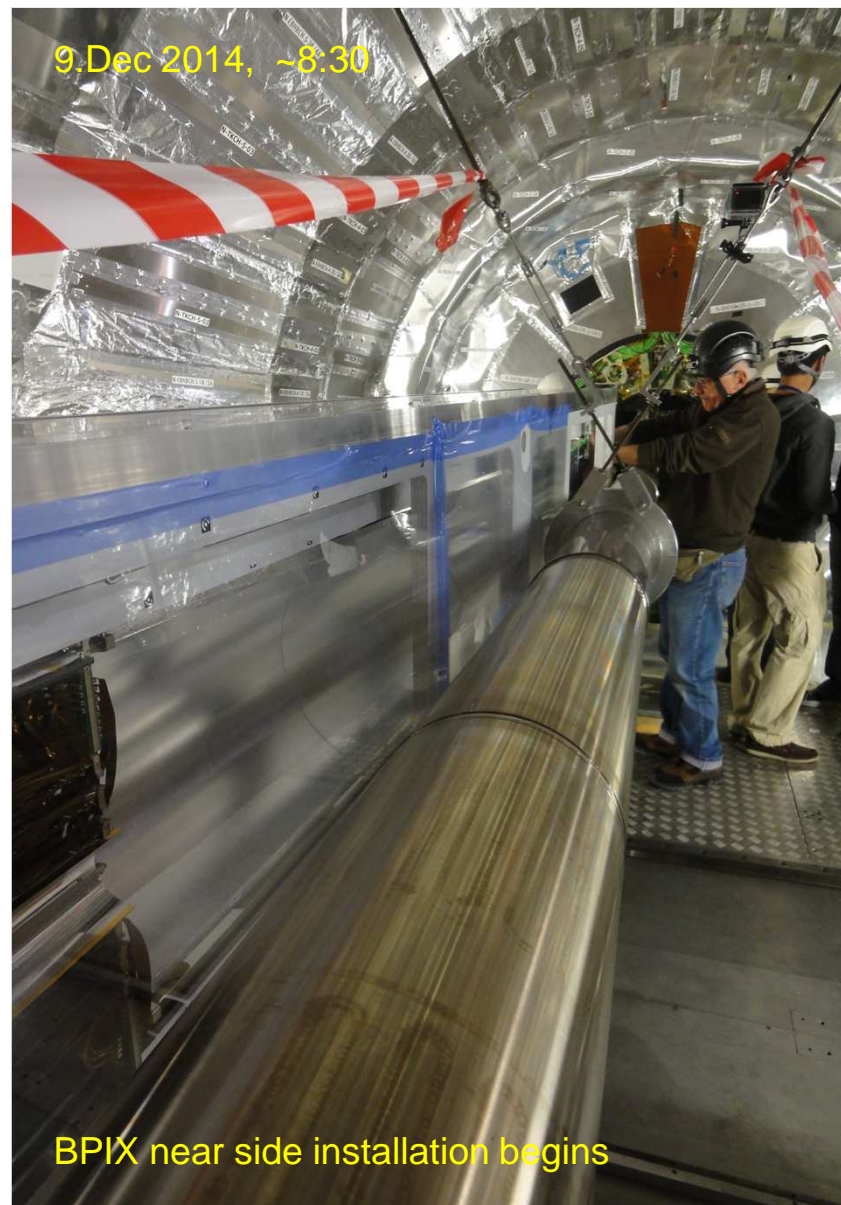
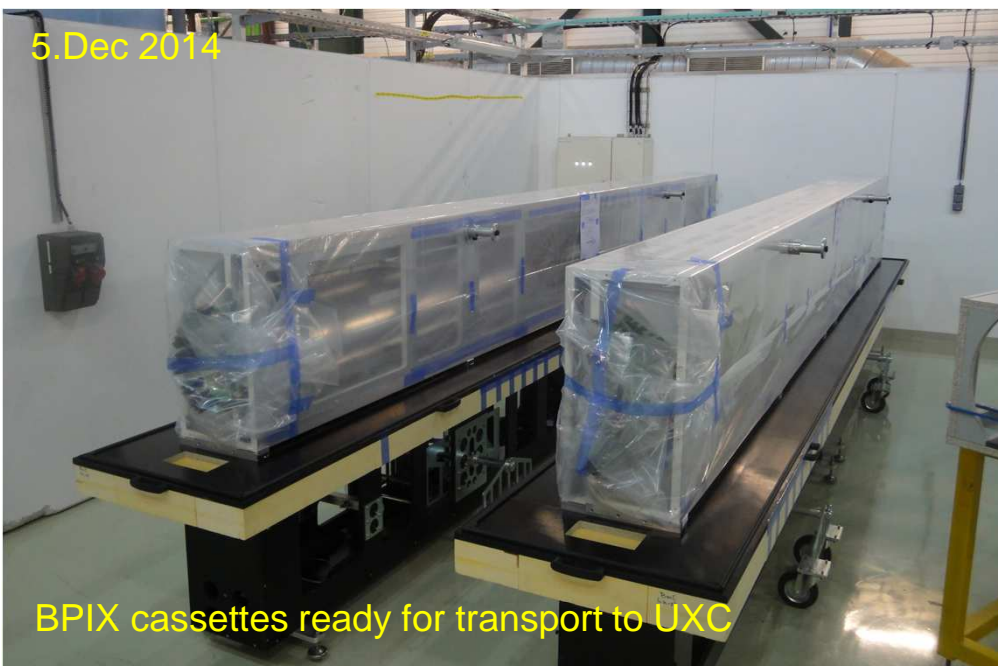
Thursday, 13. Nov 2014 Pixel Lab P5

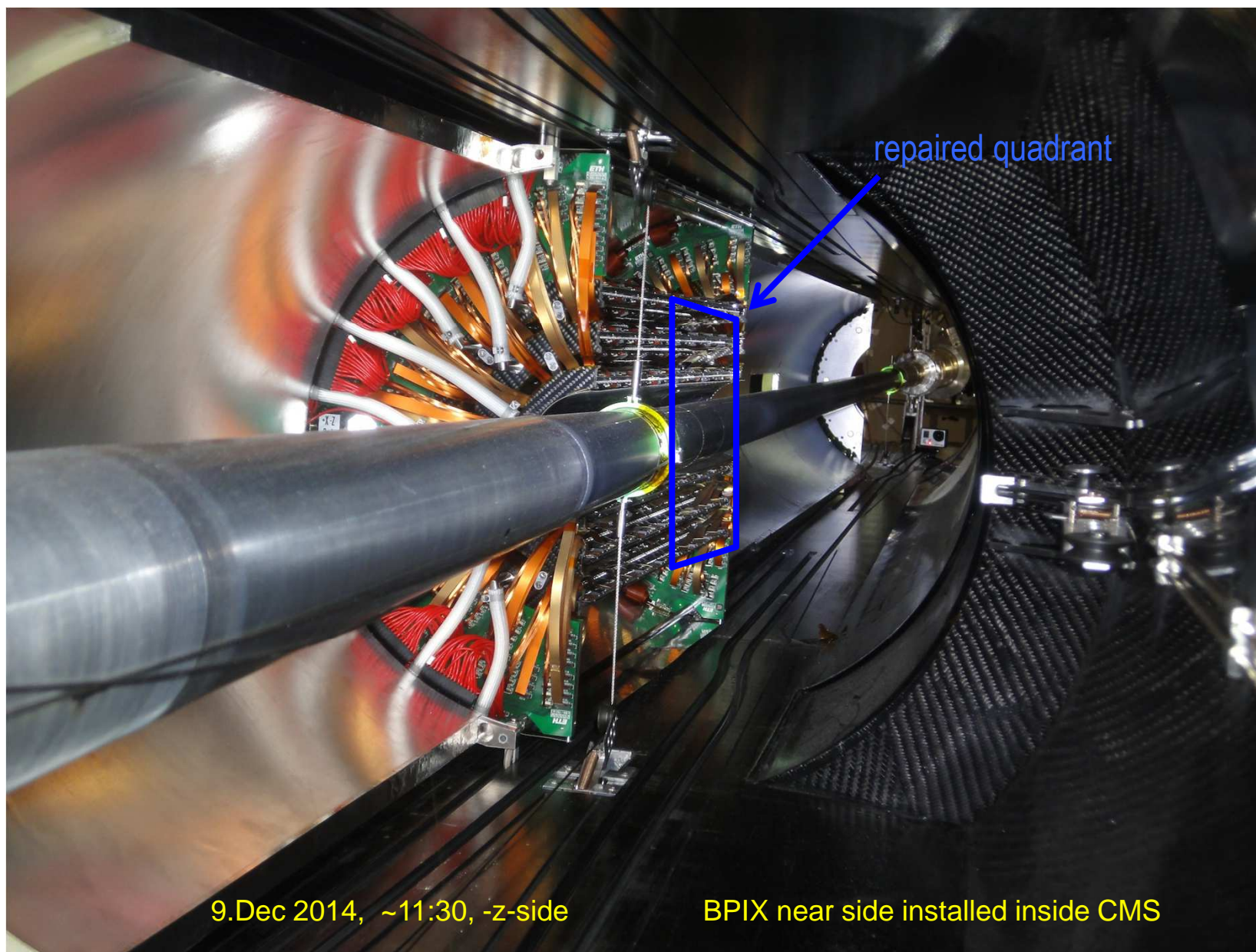


Inner Barrel Half Shell with Shield mounted

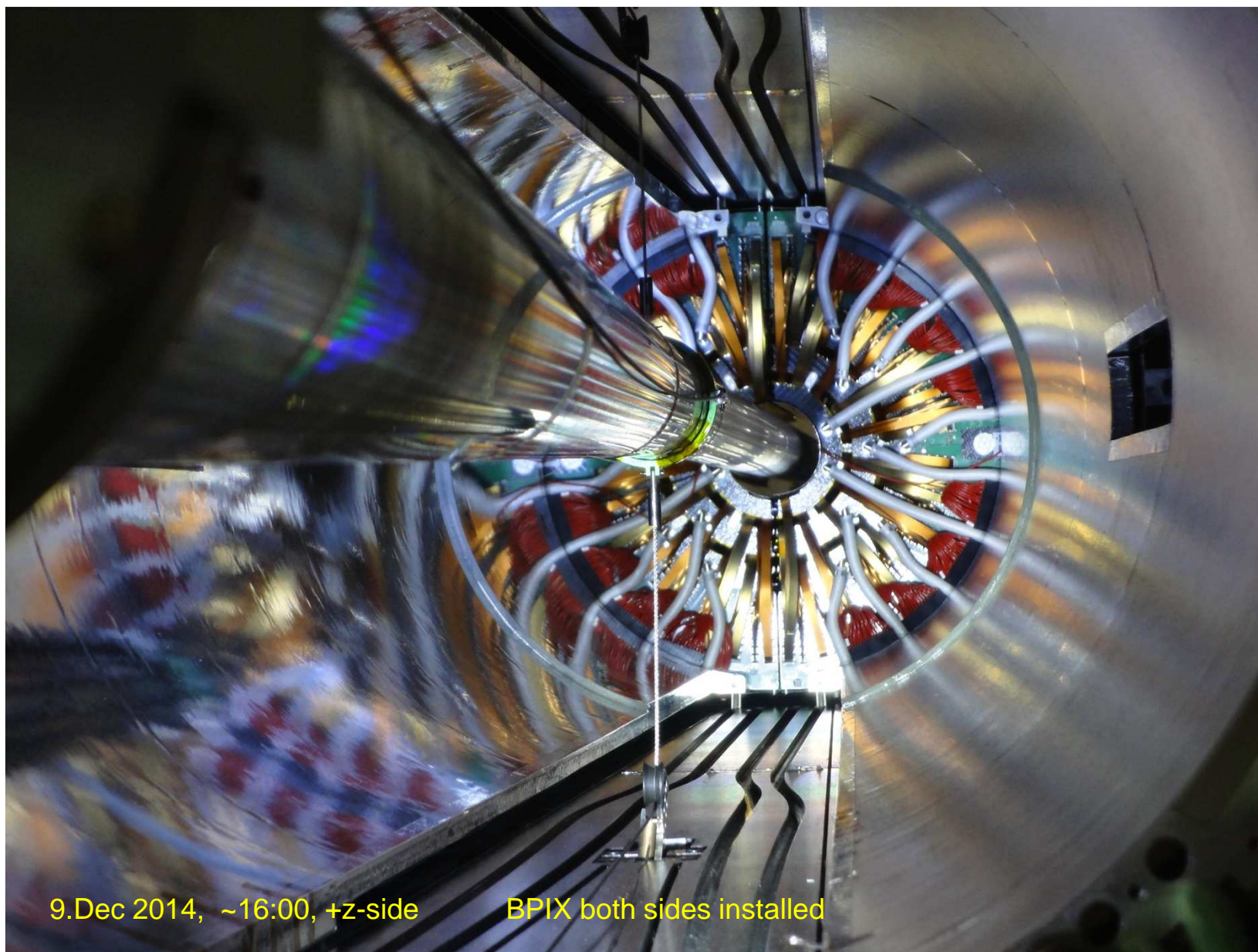


Tue, 25. Nov 2014 Pixel Lab P5



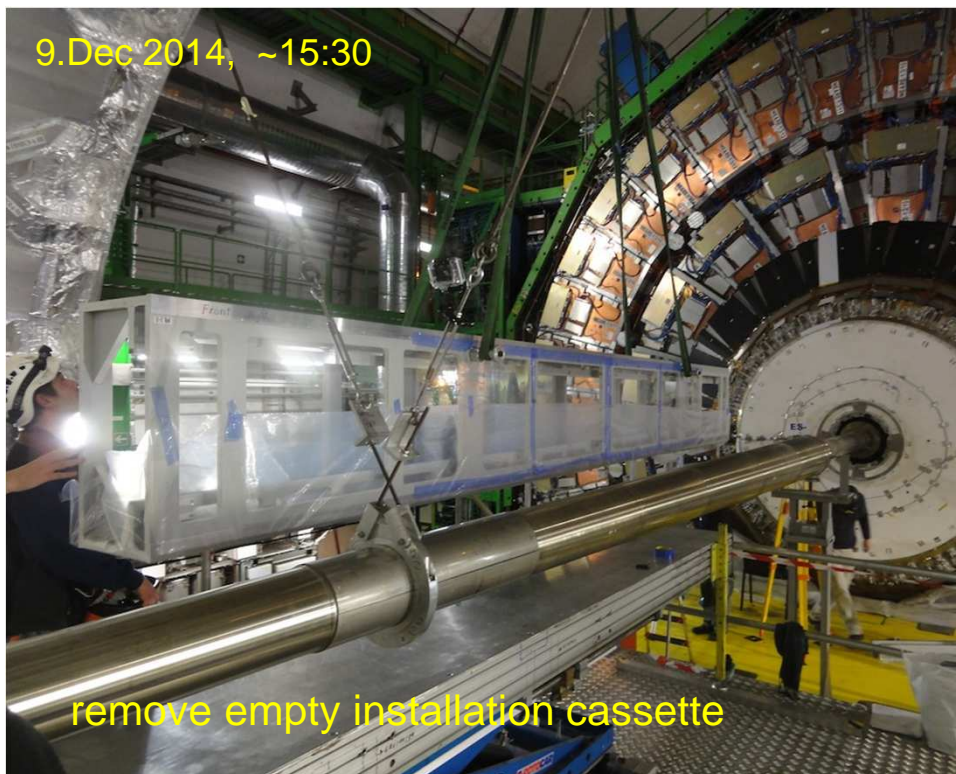


Installation of BPIX System in CMS

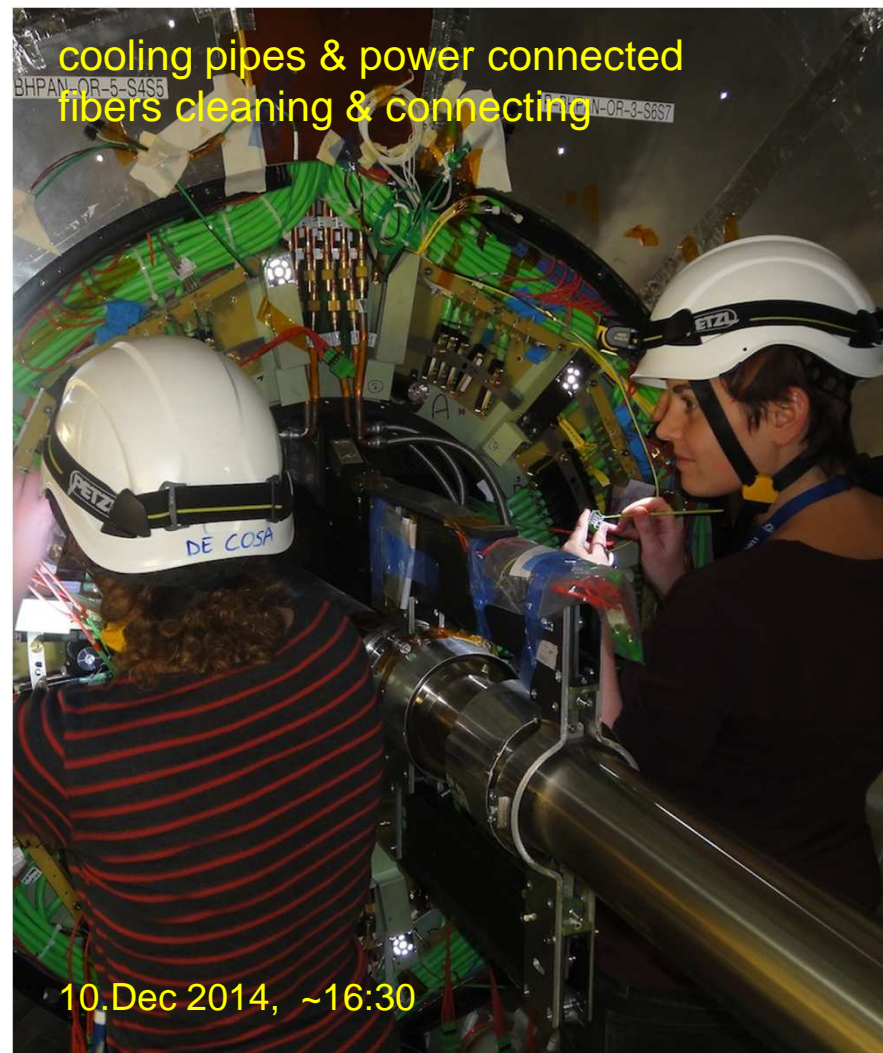
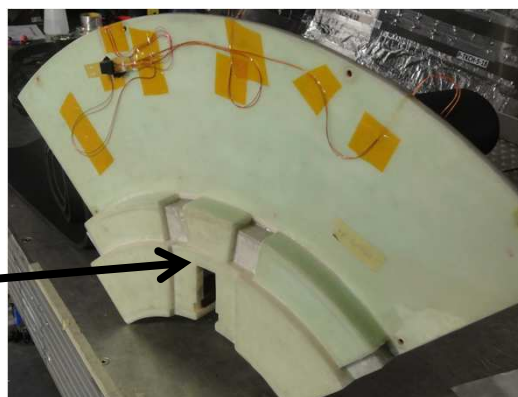


9.Dec 2014, ~16:00, +z-side

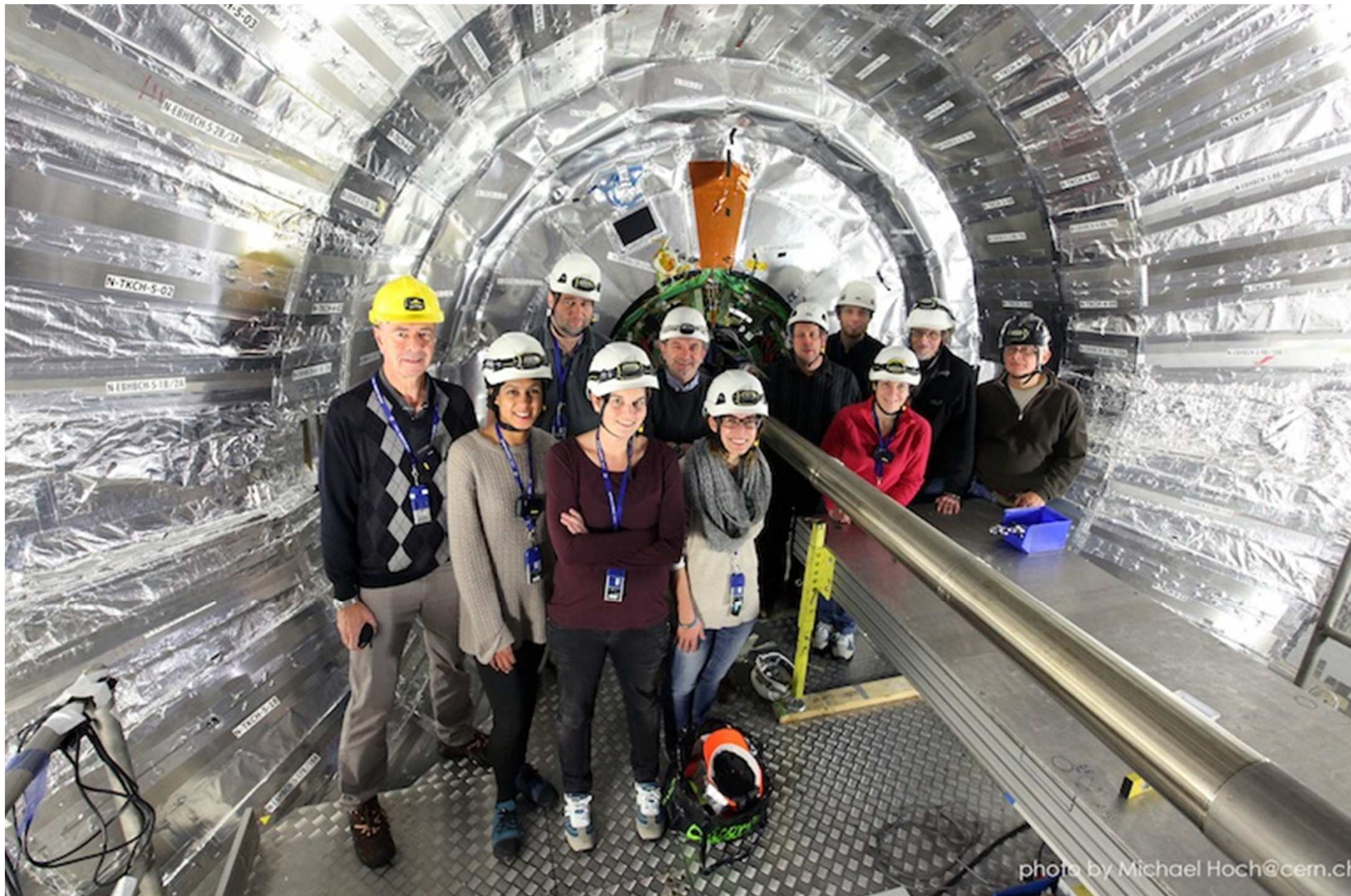
BPIX both sides installed



open issue:
thermal shield PP0
has no space for
cooling pipes



10.Dec 2014, ~18h BPIX fully cabled





Conclusions & Outlook

- repair of damaged BPIX quadrant 100% successfully completed in time
- **humidity, power** and **pockets of electrolyte** residues are cause of shorts
- big effort to re-launch the full module production of “old” modules
- repair was a major effort for the original BPIX team (PSI, ETHZ, Uni ZH)
- long term tests with repaired non-installed modules show no negative results
- BPIX is re-installed and works fine
- FPIX (including Pixel Upgrade Pilot Blades) are also re-installed and work fine.
- Pixel back in CMS and excellent shape for Run 2 and will do great physics !
- **Success possible thanks to :**
 - lasting institutional memory (people, equipment, log-books)
 - enough spares in cabinet
 - dedicated team with focus on vital tasks & procedures