

The TT-PET project: a 30 ps Time of Flight PET scanner in silicon pixel technology

Lorenzo Paolozzi



On behalf of the **TT-PET** collaboration





The TT-PET project

A 3-year project started in march 2016 financed by SNSF to produce a PET Scanner for small animals **based on silicon detector technology**, insertable in an MRI machine and with **30ps RMS time resolution**.

Participating institutes:

- University of Geneva → Sensor ASIC design and production. Scanner assembly. Image reconstruction.
- University of Bern → Read Out design and production. Flex design and production.
- Hôpitaux Universitaires Genève → Image reconstruction. Scanner test.

In collaboration with:

- INFN of Roma Tor Vergata, IHP microelectronics, Stanford University, CERN - Ideasquare



TT-PET team - University of Geneva and HUG



Giuseppe Iacobucci

- TT-PET Principal Investigator.



Osman Ratib

- HUG/ITMI



Lorenzo Paolozzi

- Sensor design
- Amplifier design



Pierpaolo Valerio

- Electronics design
- Chip design



Emanuele Ripiccini

- Scanner simulation
- Image reconstruction



Daiki Hayakawa

- Sensor simulation
- Image reconstruction

Collaborators at DPNC

Frank Cadoux

- Scanner mechanic assembly
- Scanner thermal management

Stéphane Debieux

- Board design
- Electronic support at system level

Yannick Fravre

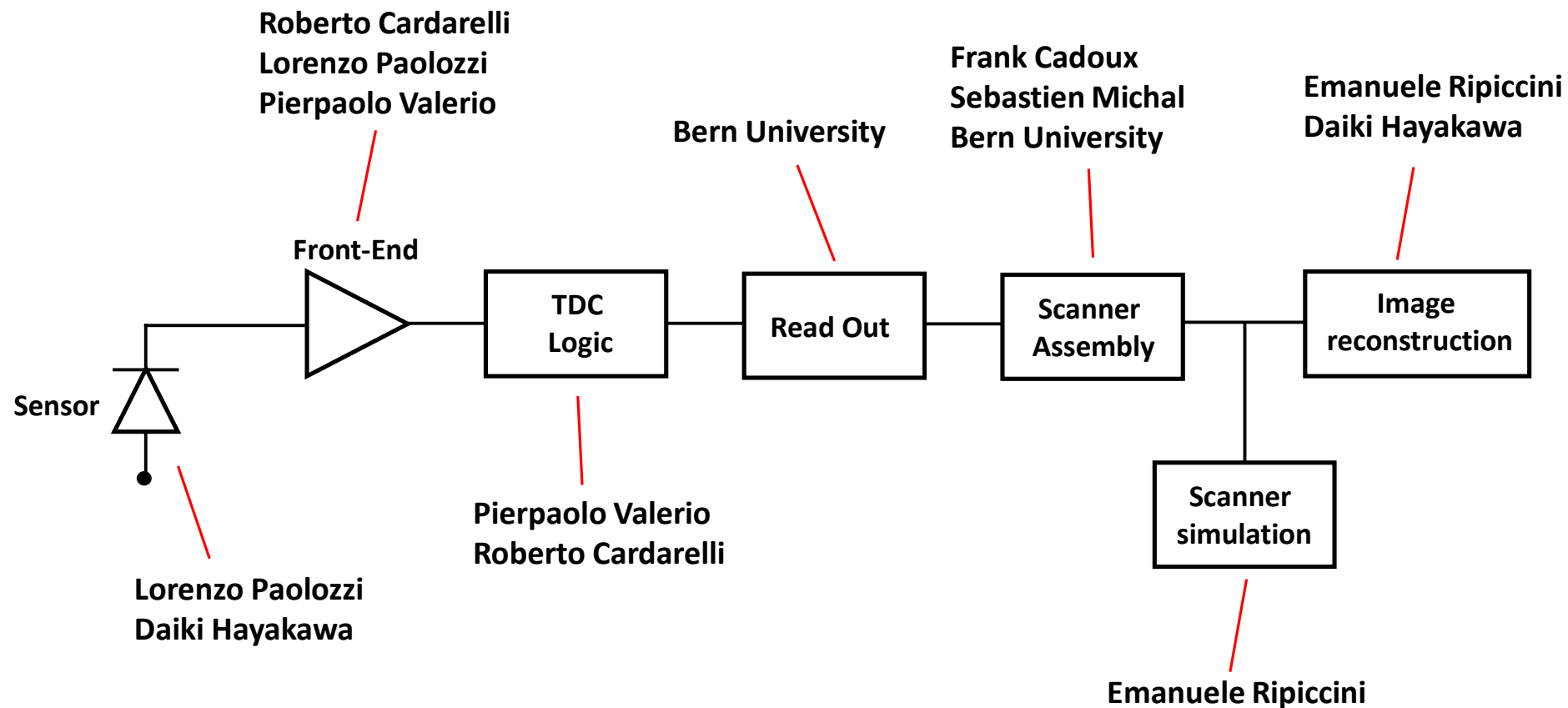
- Electronic support at system level

Didier Ferrere

- Scanner assembly support

Mathieu Benoit

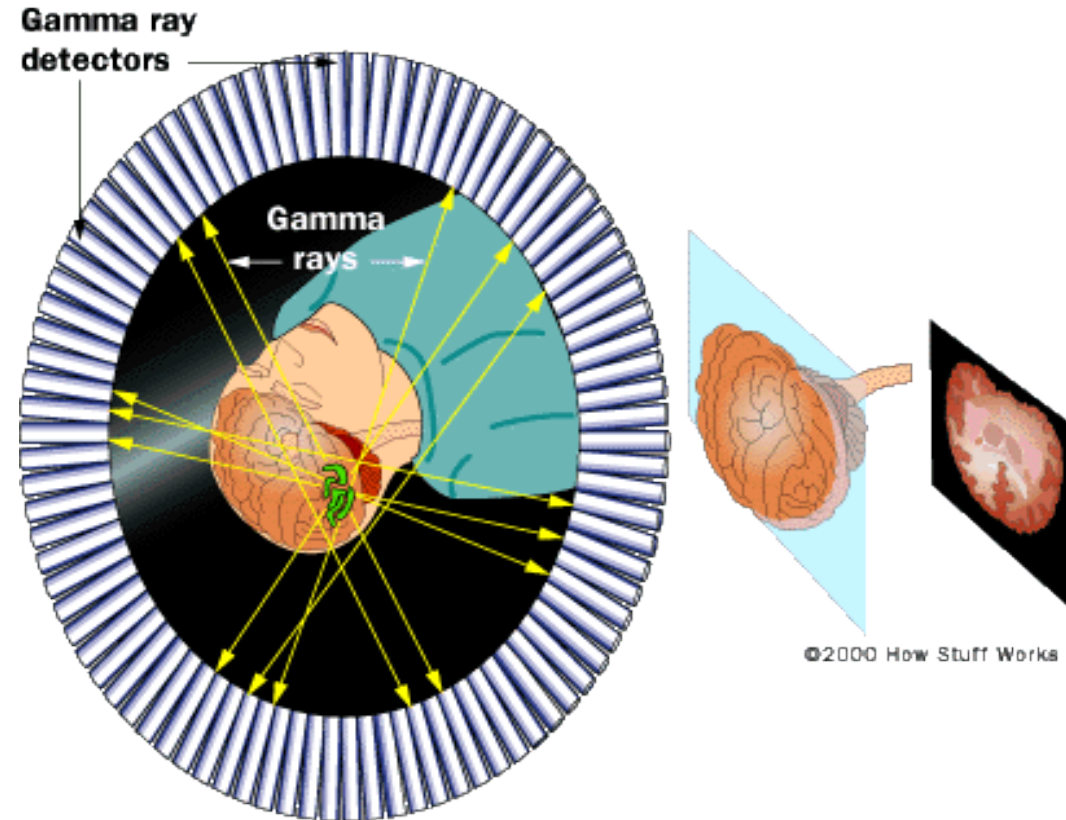
- Sensor and guard ring simulation



The PET technique

A functional imaging technique

- A radiopharmaceutical containing a β^+ **emitting isotope** reaches the target location (ex: tumour cells).
- The positrons annihilate with the nearby tissue, emitting **two back-to-back photons**.
- The photons are detected in coincidence, tracking a **line of response**.





TOF-PET vs Traditional PET

Traditional PET:

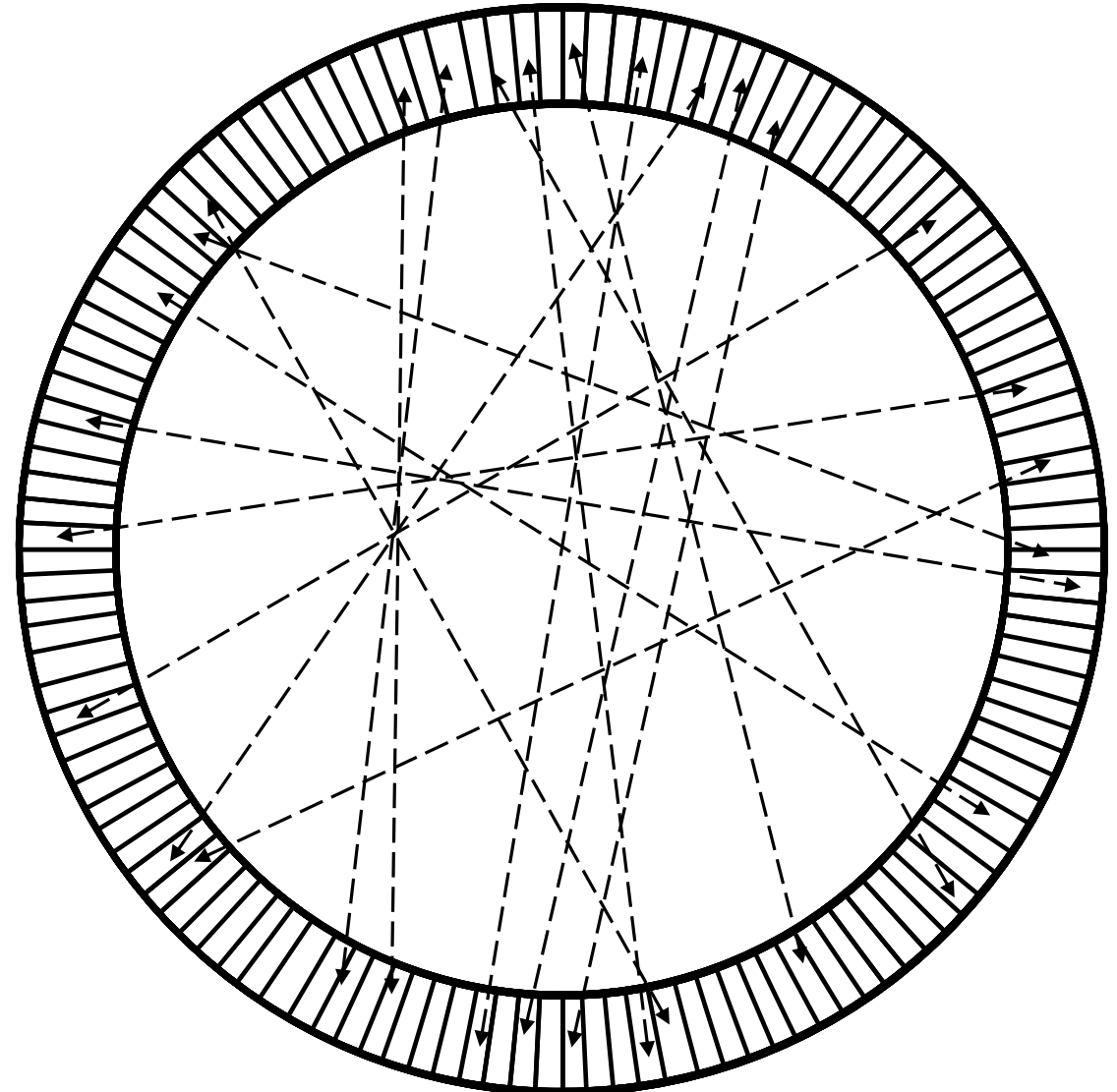
- To each photon couple is associated a **line of response**.
- The background events overlap with the signal.



more statistics is necessary to identify the excess emission point.



Larger radioactive dose.





TOF-PET vs Traditional PET

Traditional PET:

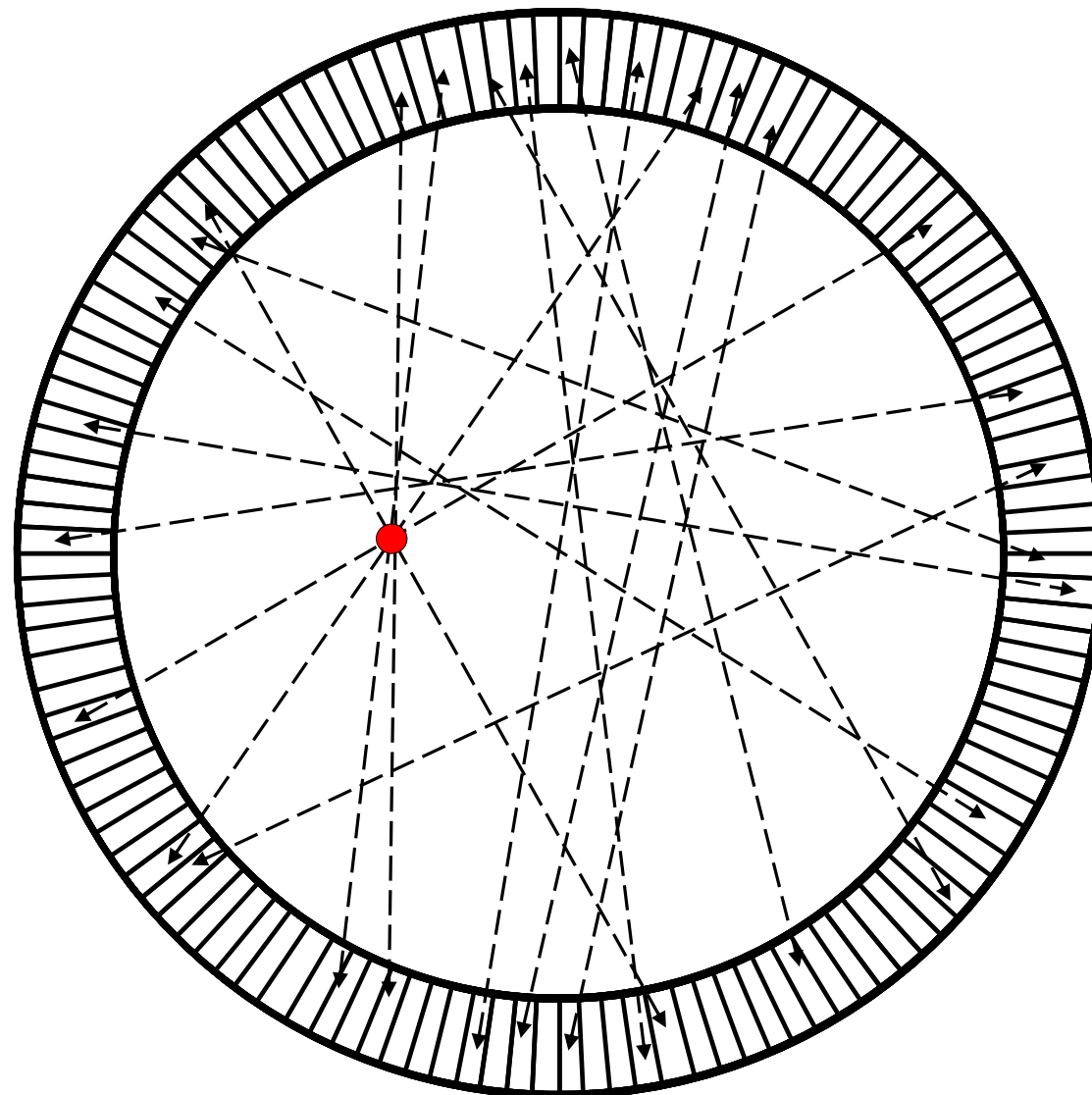
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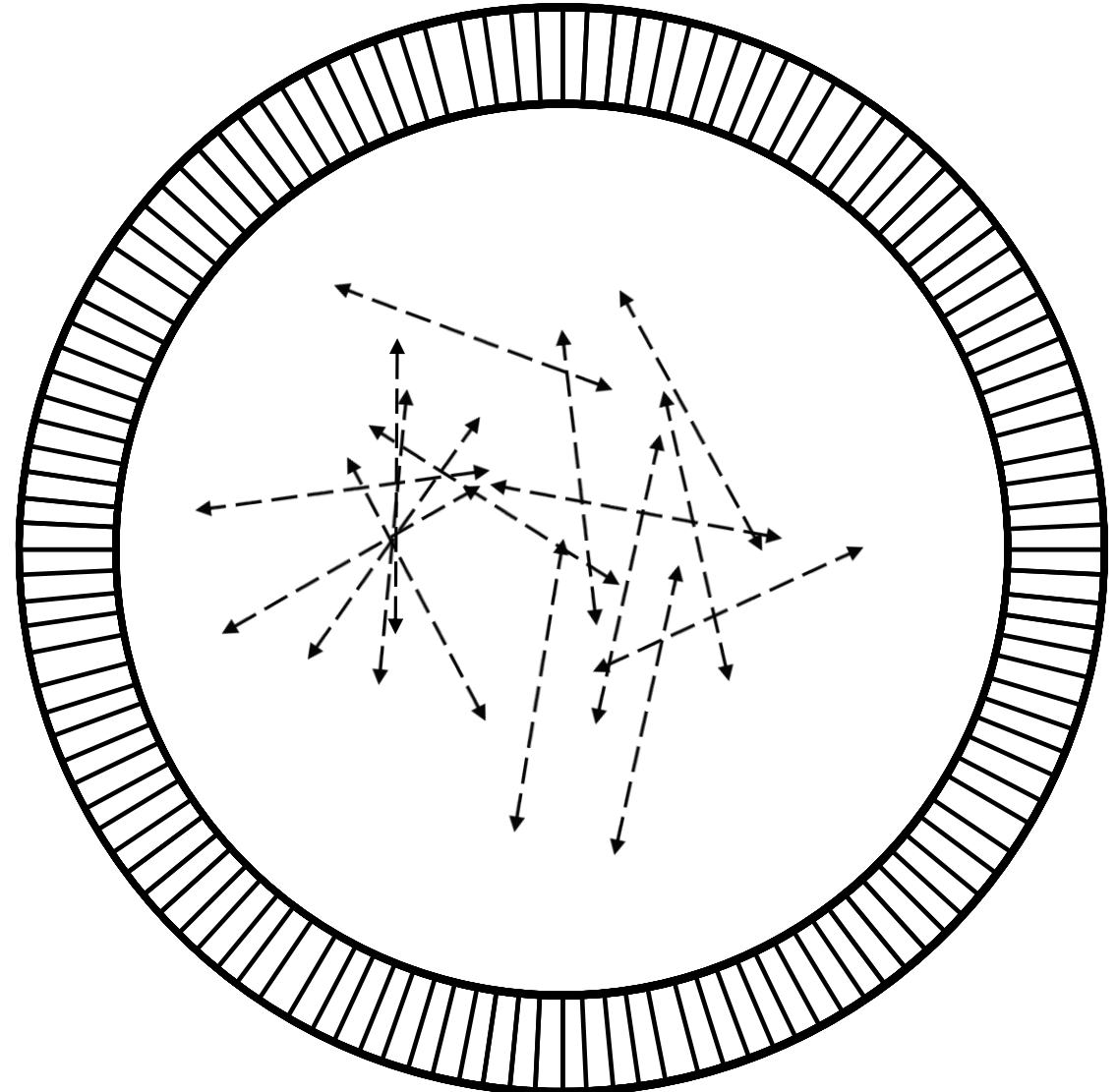
TOF-PET vs Traditional PET

Traditional PET:

- The emission point is **identified along the line of response**.

➡ Reduction of the fake coincidences.

➡ Better scanner sensitivity.





TOF-PET vs Traditional PET

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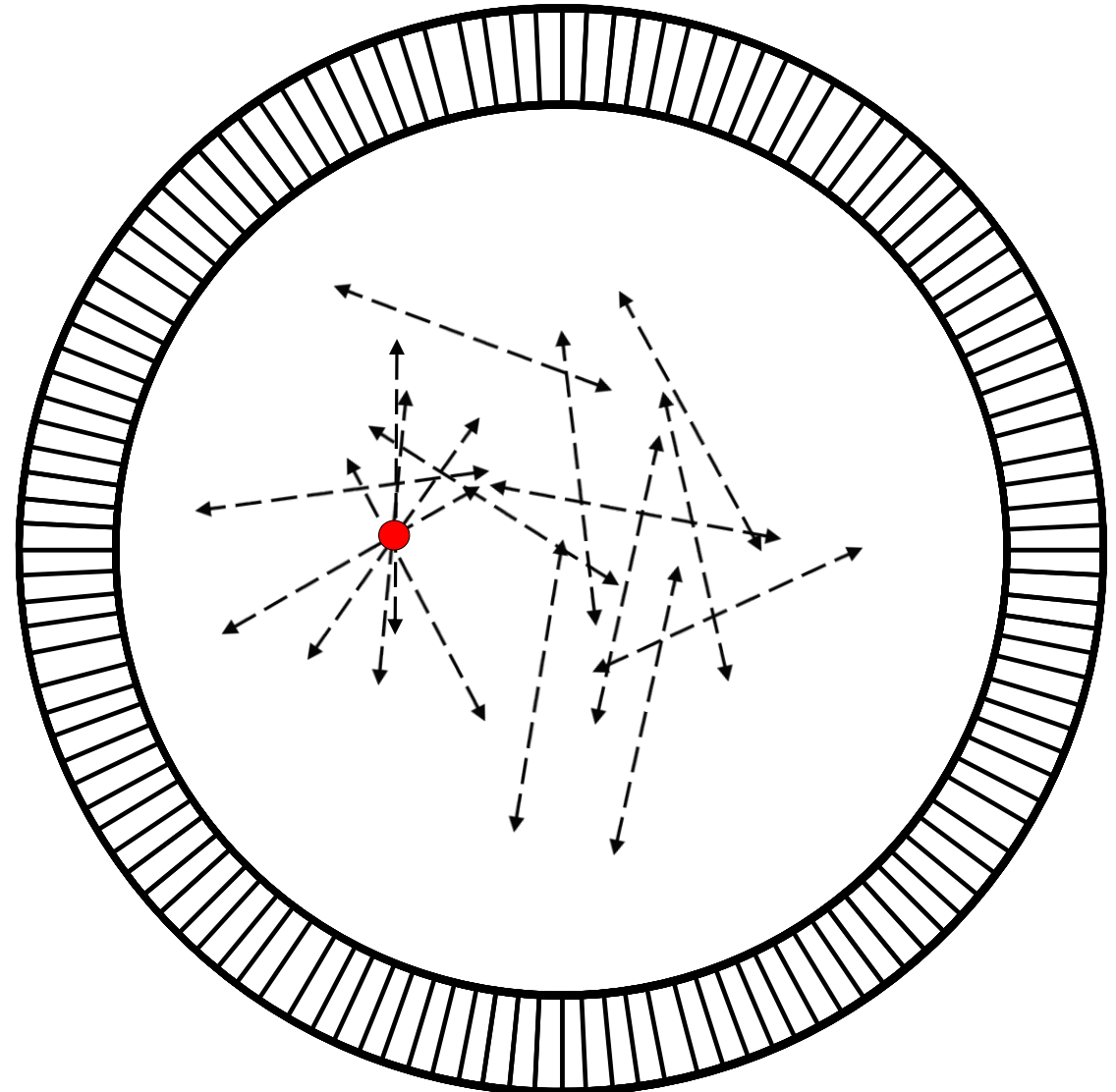
➡ Better scanner sensitivity.

- Best time resolution available on the market:

$$\sigma_t \cong 130ps$$

- Target time resolution for **TT-PET**:

$$\sigma_t = 30 \text{ ps RMS}$$



Depth of Interaction measurement:

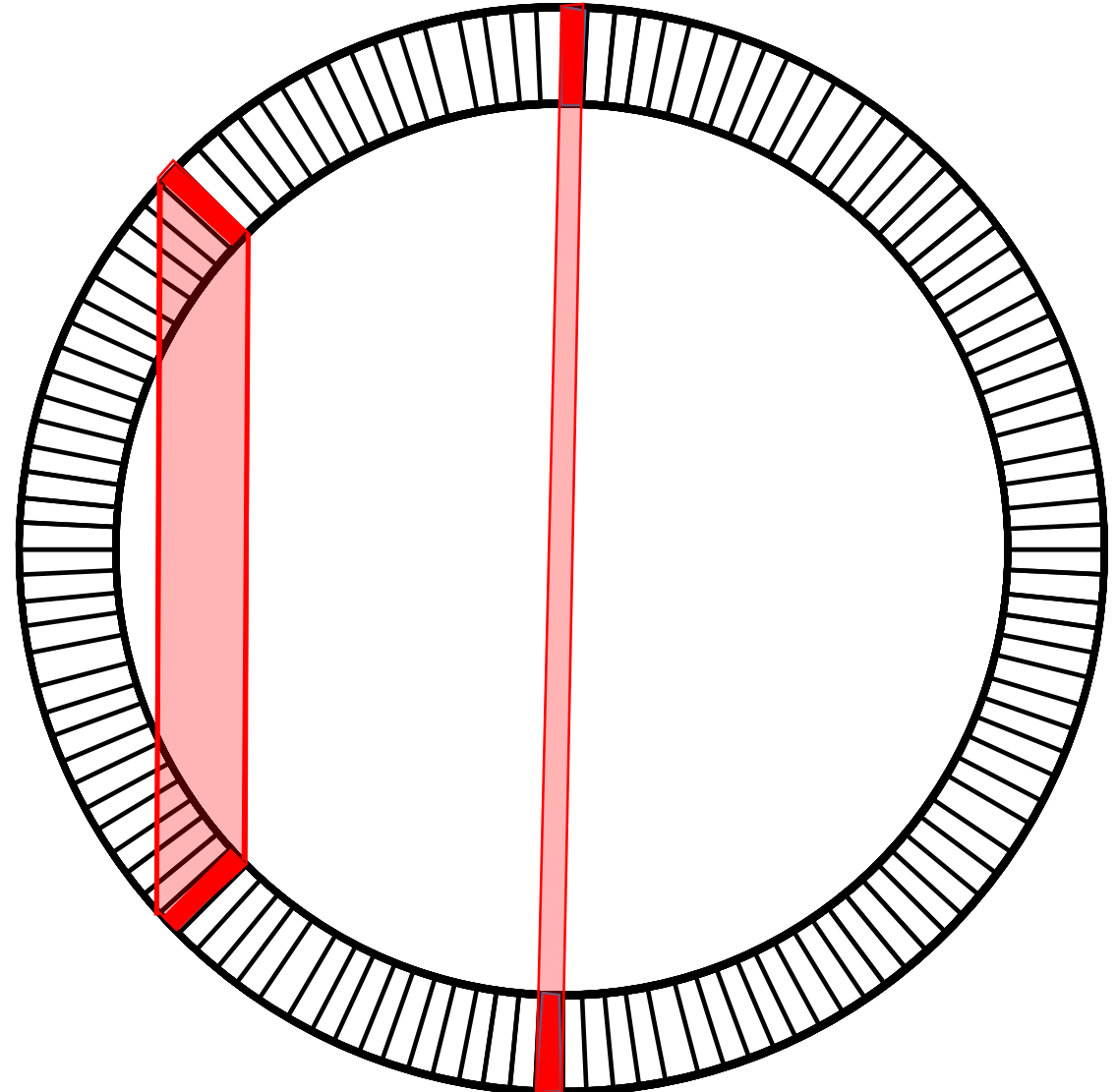
- Uncertainty on the photon interaction point inside the sensor in the radial direction.

➡ Degradation of the time resolution.

➡ Degradation of the space resolution along the radial direction.

- DOI measurement for TT-PET:

$$\Delta r < 250 \mu m$$



The TT-PET scanner

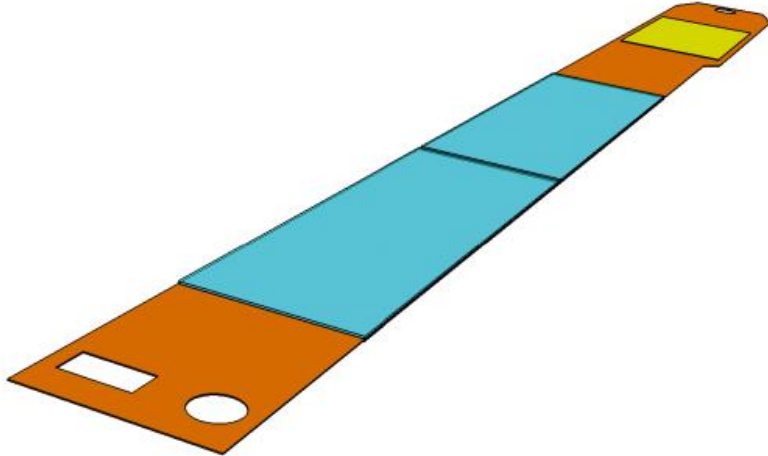
Module



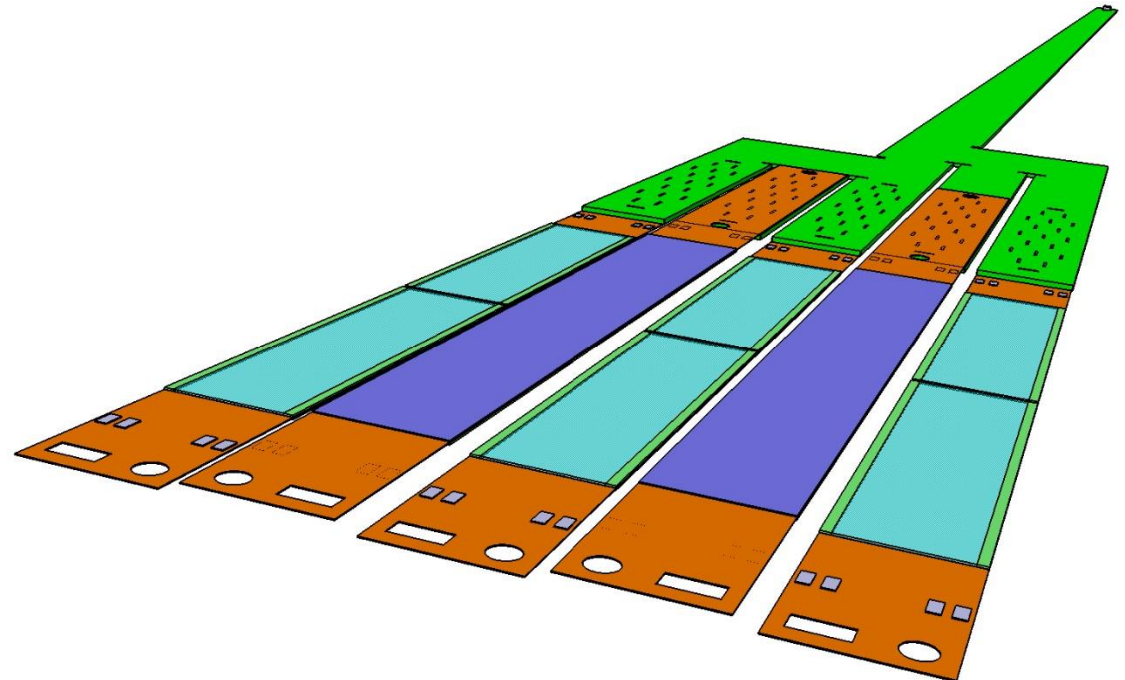
- **Polyimide flex circuit.**
 $55\ \mu m$ thickness
- **Monolithic pixel sensor:**
 $100\ \mu m$ thickness
- **Lead converter**
 $50\ \mu m$ thickness

Signal extraction

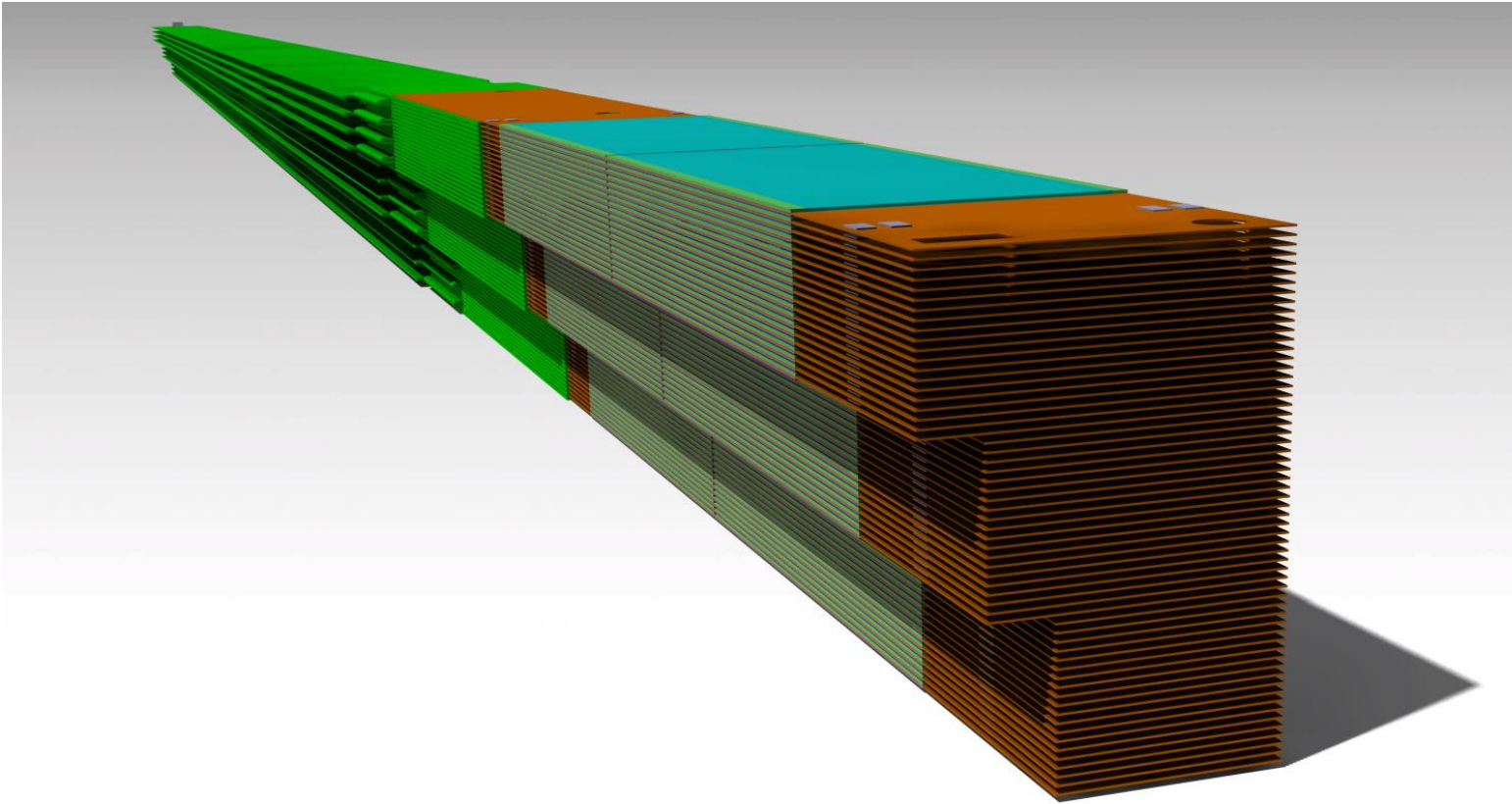
Two chips are bump bonded on a “module flex”



A group of 5 module flexes are then connected to a “data flex”, which sends the data to the read out with a lower density of interconnections.



Scanner “cell”



- A scanner cell is a stack of 60 modules, tightly coupled.
- Total cell thickness will be approximately **1.5 cm**.
- Cell assembly will be possible thanks to the new DPNC flip-chip machine.
- Designed by the DPNC mechanical engineering group.



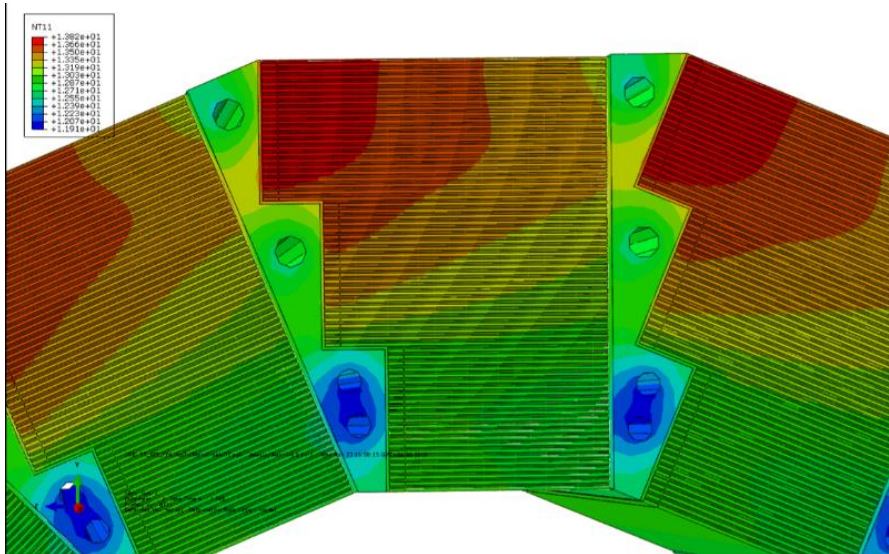
The TT-PET scanner

More than 1 Mpixel.

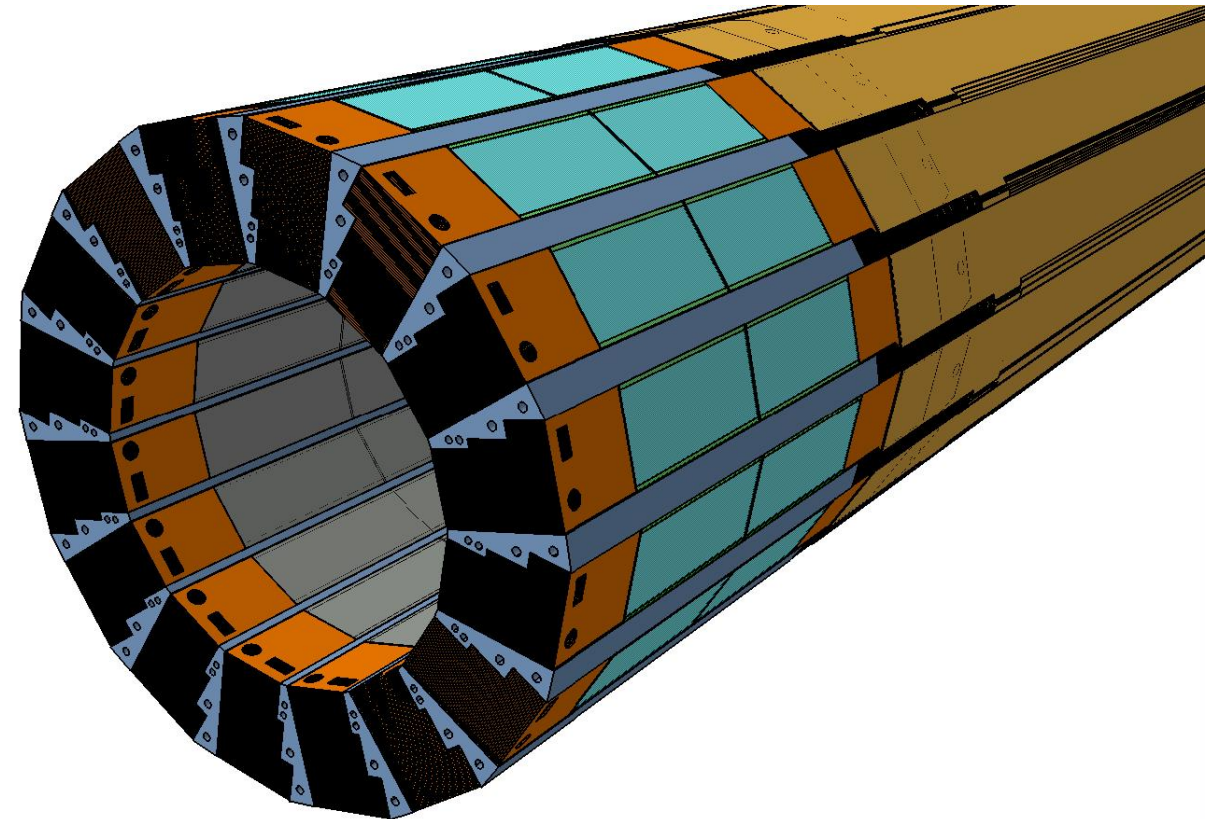
High density of silicon pixel sensors

➡ Sensor power budget $< 80 \text{ mW/cm}^2$

➡ Active cooling: $\Delta T < 1^\circ \text{C}$ in the sensitive volume



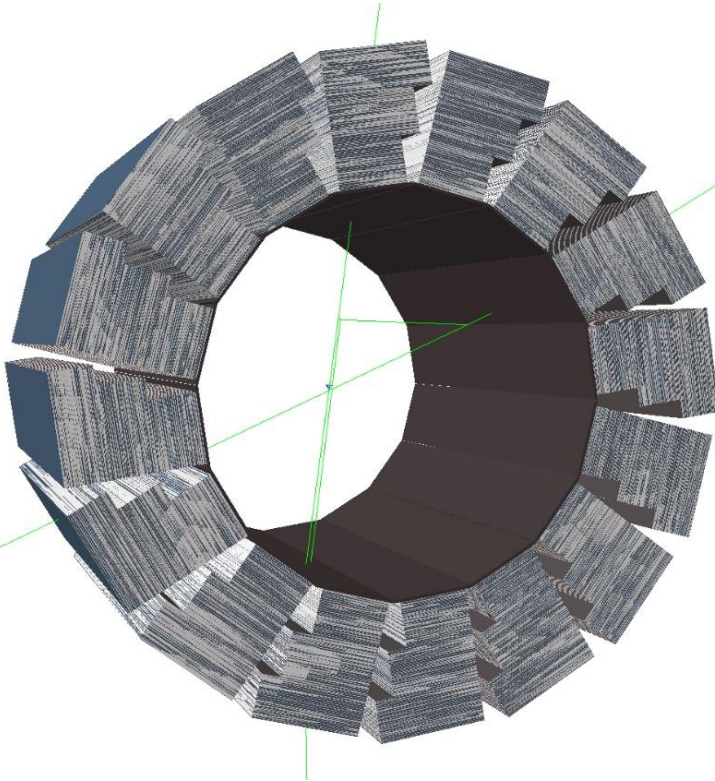
Simulation by F. Cadoux





The TT-PET scanner

A Geant4 simulation has been developed to predict the scanner efficiency to 511 *keV* photons, the expected detection rate per chip and the scanner space resolution.



For 1.5 cm cell thickness

- Scanner sensitivity (coincidences per disintegration): 5 %

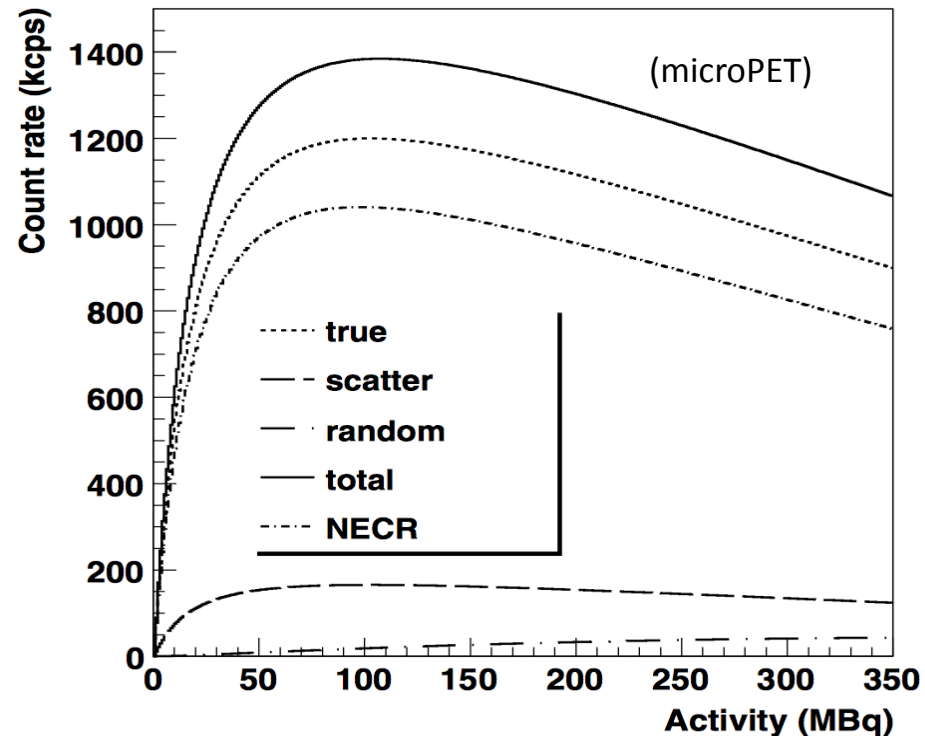
Typical small animal PET sensitivity: from 1% to 10%



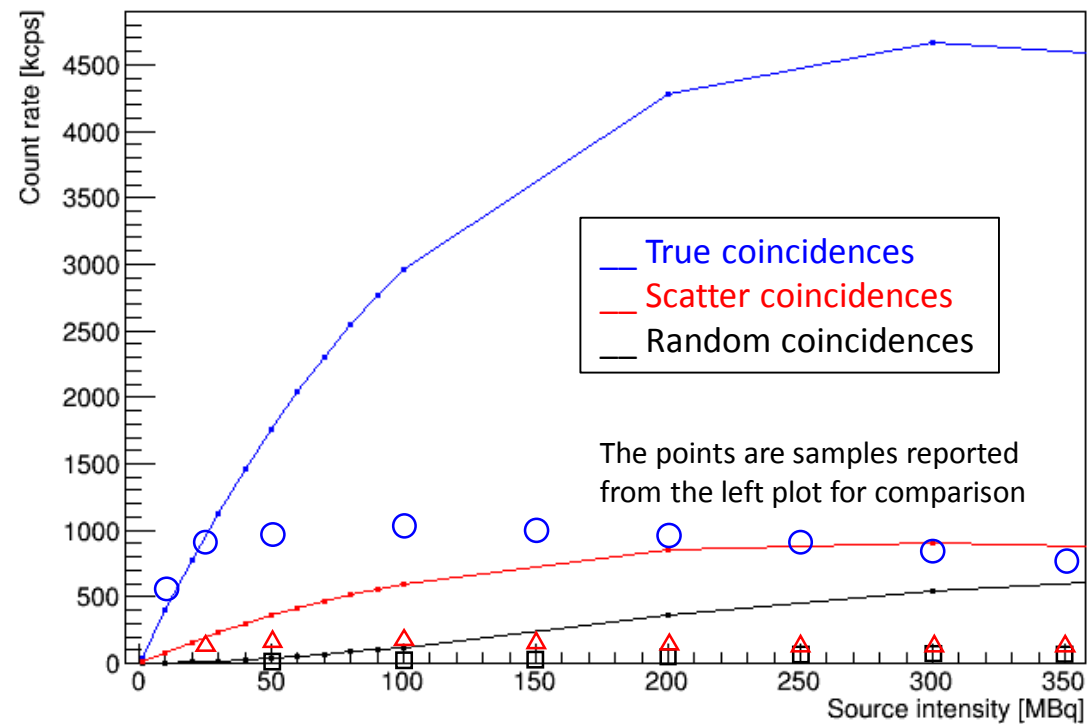
The TT-PET scanner

The high segmentation of the scanner and fast response of the silicon pixel detector allow for a very high counting rate.

Typical performance of a small animal TOF-PET



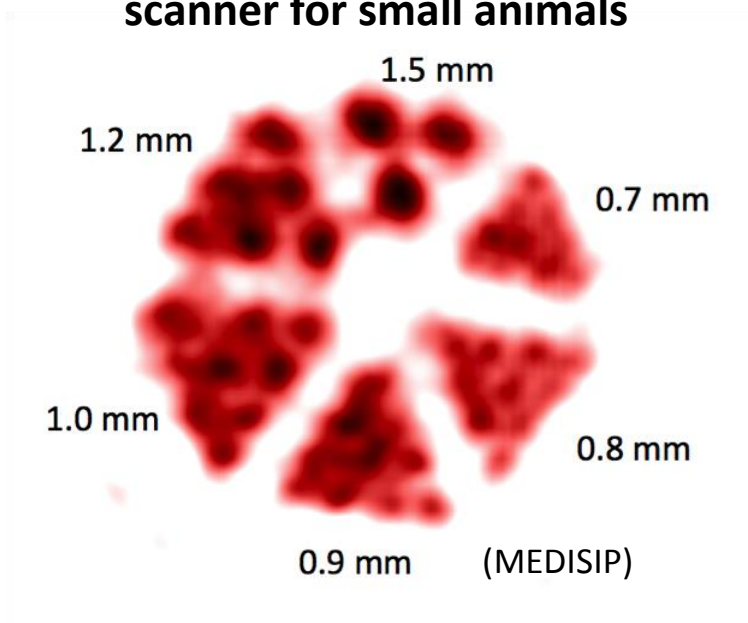
TT-PET scanner counting rates – Geant4 simulation



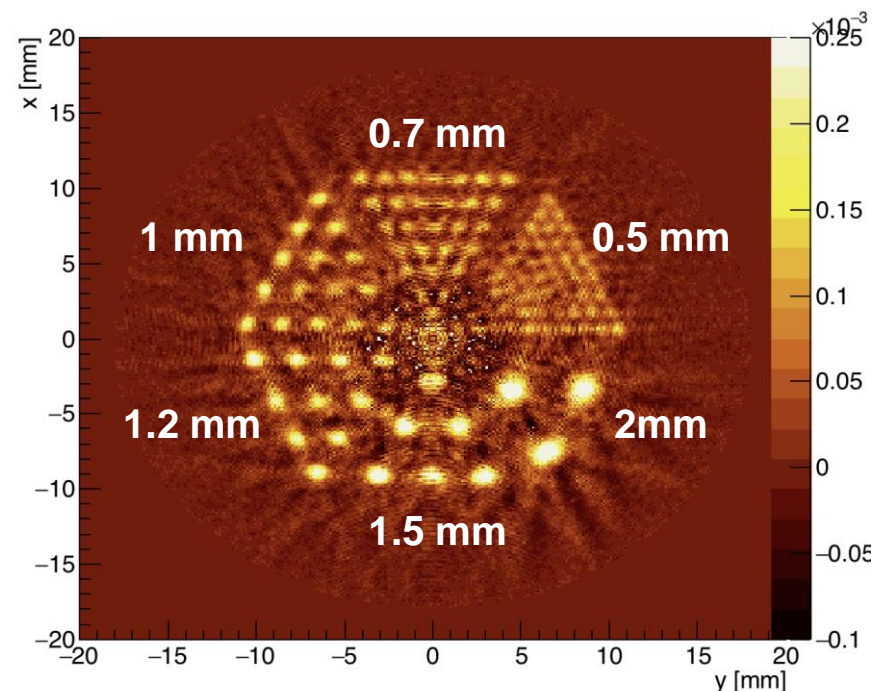
Scanner space resolution in the whole field of view: $< 0.8 \text{ mm FWHM}$

Derenzo phantom Geant4 simulation

Typical performance of a TOF PET scanner for small animals



TT-PET simulation



New image reconstruction algorithms are under development to fully exploit the time resolution and DOI measurement capability of the TT-PET scanner.

The fast, monolithic pixel sensor



What do we need to develop

➔ 1. Make a 30 ps time resolution detector for 511 keV photons...

Two orders of magnitude better
than the existing monolithic
silicon pixel sensors.



- Detector design.
- Electronics technology and design.
- Understanding of sensor physics.



What do we need to develop

1. Make a 30 ps time resolution detector for 511 keV photons...

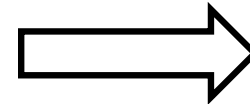
➔ 2. ... and make it monolithic.

Both sensor and electronics **integrated in the same chip**, in a commercial microelectronics process.

Advantages:

- Simplified interconnections.
- Integrated front end, TDC, logic, serializer.
- Cost reduction

BUT



- Requires to adapt to a process that is not optimized for sensor design.
- Experience in ATLAS group at DPNC with other technologies



How do we do it?

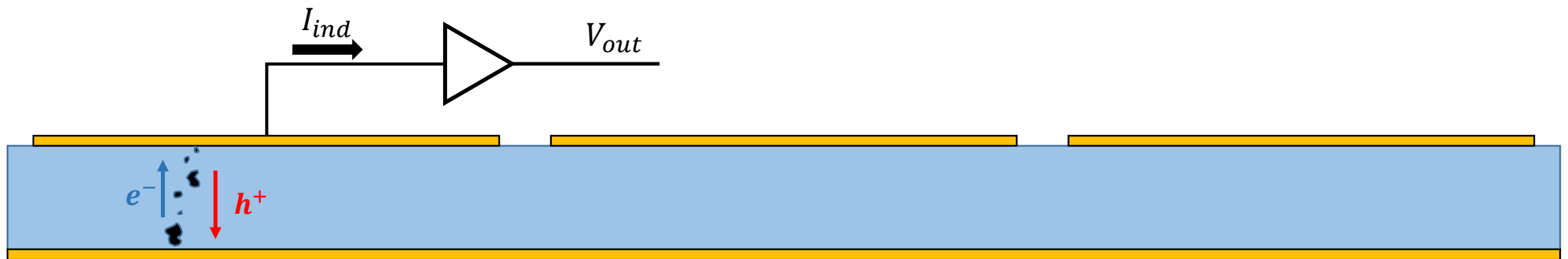
What are the main parameters to improve for the time resolution of semiconductor detectors?

↳ Read out geometry (constraint)

↳ Electronics noise (optimization)

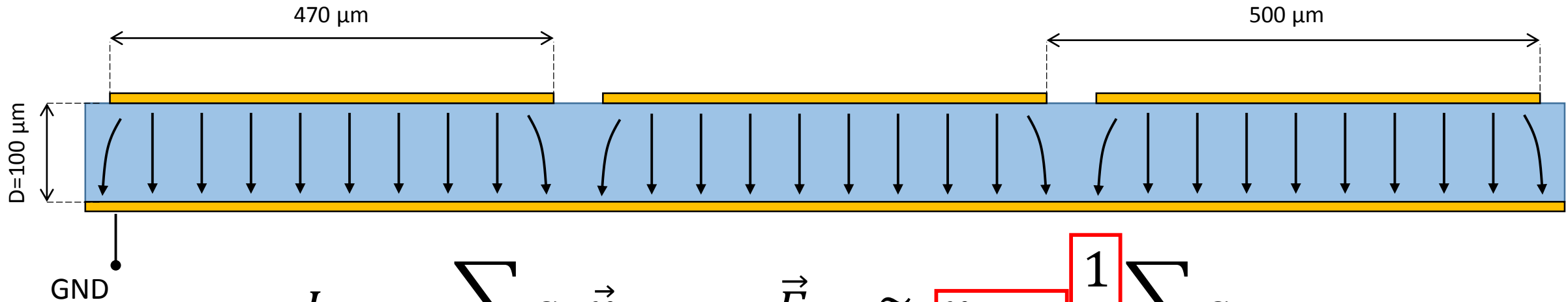
↳ Charge collection noise (limit)

$$I_{ind} = \sum_i q_i \vec{v}_{drift,i} \cdot \vec{E}_{w,i}$$



Read out geometry

The condition of “parallel plate” read out is fundamental to guarantee the uniformity of the weighting and the electric field.



$$I_{ind} = \sum_i q_i \vec{v}_{drift,i} \cdot \vec{E}_{w,i} \cong \boxed{v_{drift}} \boxed{\frac{1}{D}} \sum_i q_i$$

Scalar, saturated

Scalar, uniform

Drawback!

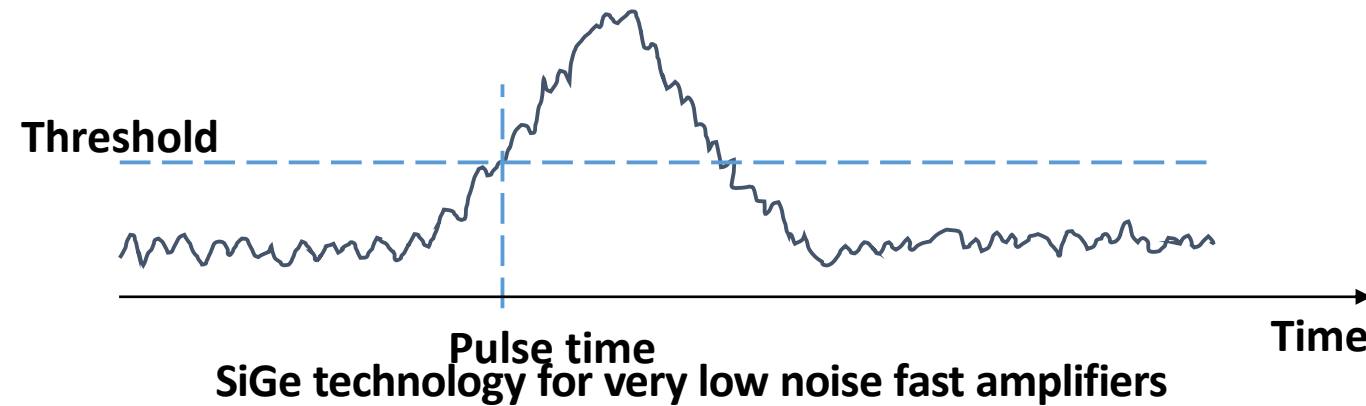
Increase of the pixel capacitance



Larger equivalent noise from the amplifier.

Electronic noise

Detector time resolution depends mostly on the amplifier performance!

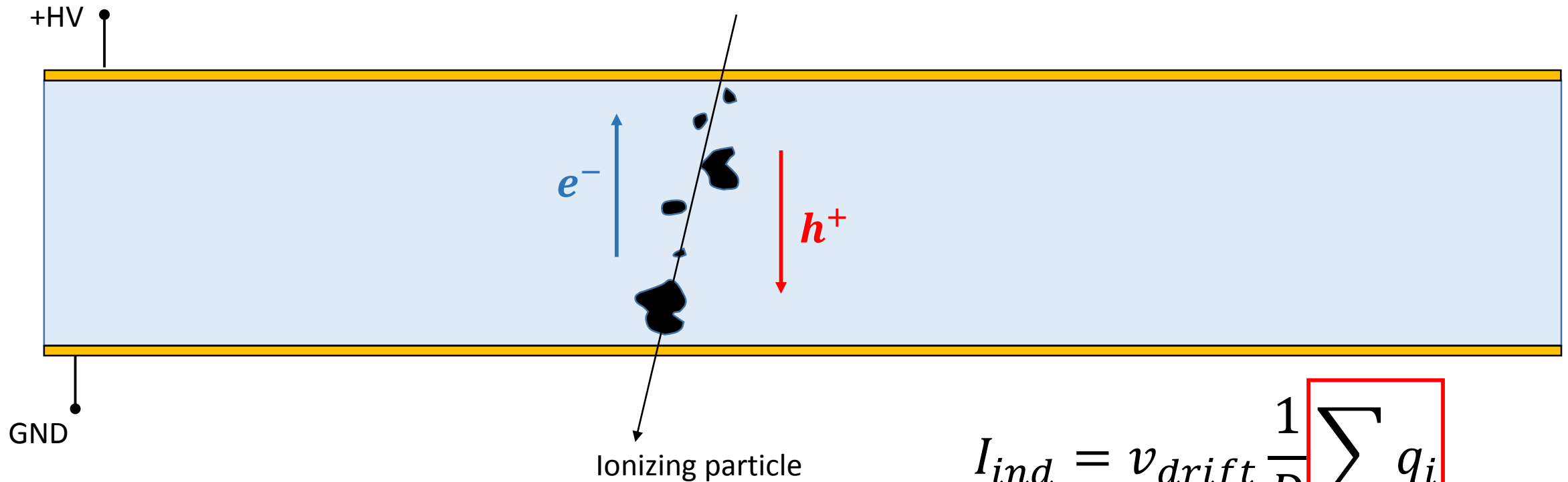


$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} \cong \frac{\text{Rise Time}}{Q/ENC} \quad \boxed{I_{ind}} = v_{drift} \frac{1}{D} \sum_i q_i$$

Need a **fast, low-noise, low power consumption** electronics:

➡ 1 ns rise time, < 1000 e^- ENC on ~ 1 pF capacitance.

Charge collection noise



$$I_{ind} = v_{drift} \frac{1}{D} \sum_i q_i$$

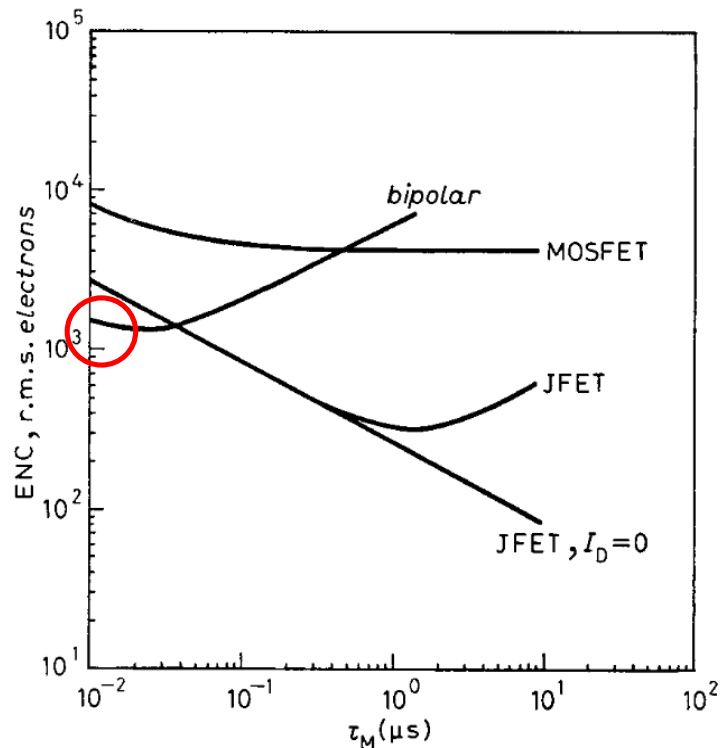
- Produced by the Landau fluctuations on the charge deposition in the sensor.
- **Intrinsic limit to the time resolution for a semiconductor detector!**

Technology choice

The fast, low noise amplifier

$$ENC^2 \propto \left(2q_e I_C + \frac{4kT}{R_P} + i_{na}^2 \right) \cdot \tau + \boxed{(4kTR_S + e_{na}^2) \cdot \frac{C_{in}^2}{\tau}} + 4A_f C_{in}^2$$

Dominating term: series noise (for TT-PET $\tau < 10 \text{ ns}$)



Fast integrator

➔ Minimization of series noise

➔ Low input impedance of the transistor

➔ **BJT technology**

The fast, low noise amplifier

For a fast charge integrator in BJT technology the term is expressed as:

$$ENC_{series\ noise} \propto \sqrt{2kT\langle SNI \rangle \left[(C_{in})^2 \frac{h_{ie}}{\beta} + R_{bb} C_{in}^2 \right]}$$

Maximize the current gain (at high frequencies!) while keeping a low base resistance



The fast, low noise amplifier

Amplifier current gain can be expressed as (NPN BJT)

$$\beta = \frac{i_C}{i_B} = \frac{\tau_p}{\tau_t}$$

τ_p = hole recombination time in base

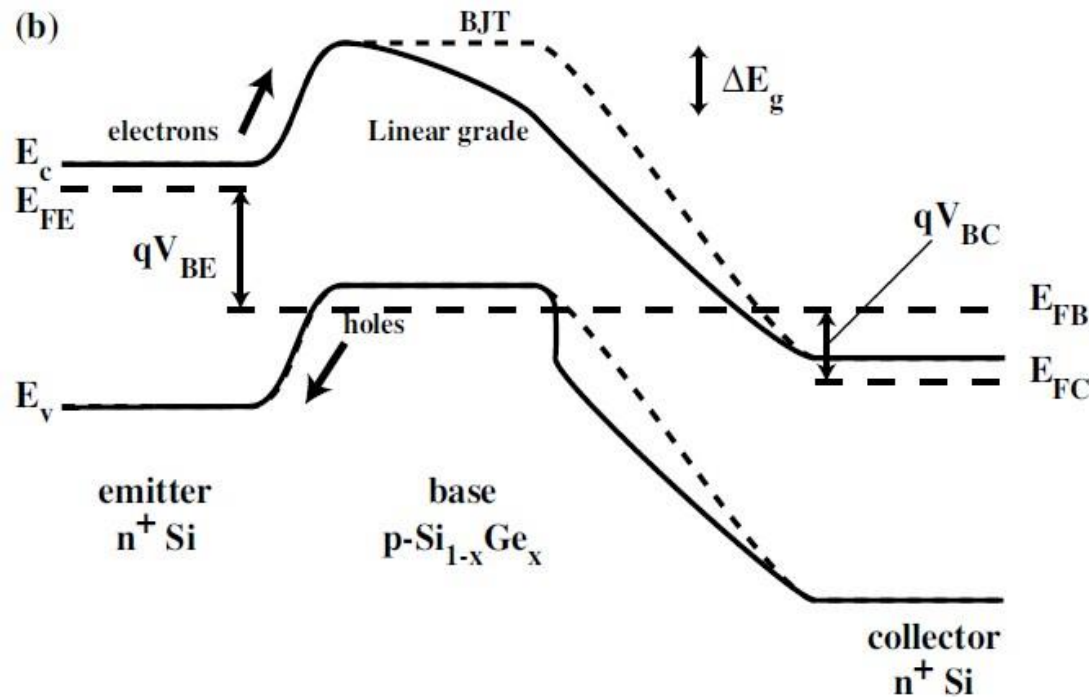
τ_t = **electron transit time (E to C)**

Need to minimize electron transit time in the base

Increase gain \Rightarrow Reduce base width \Rightarrow Reducing base doping

Spreading resistance increases!

A possible approach: **changing the charge transport mechanisms** in the base from diffusion to drift.



SiGe heterojunction bipolar transistor technology.

Our technology choice:

SiGe HBT from IHP microelectronics

$$\beta = 900$$

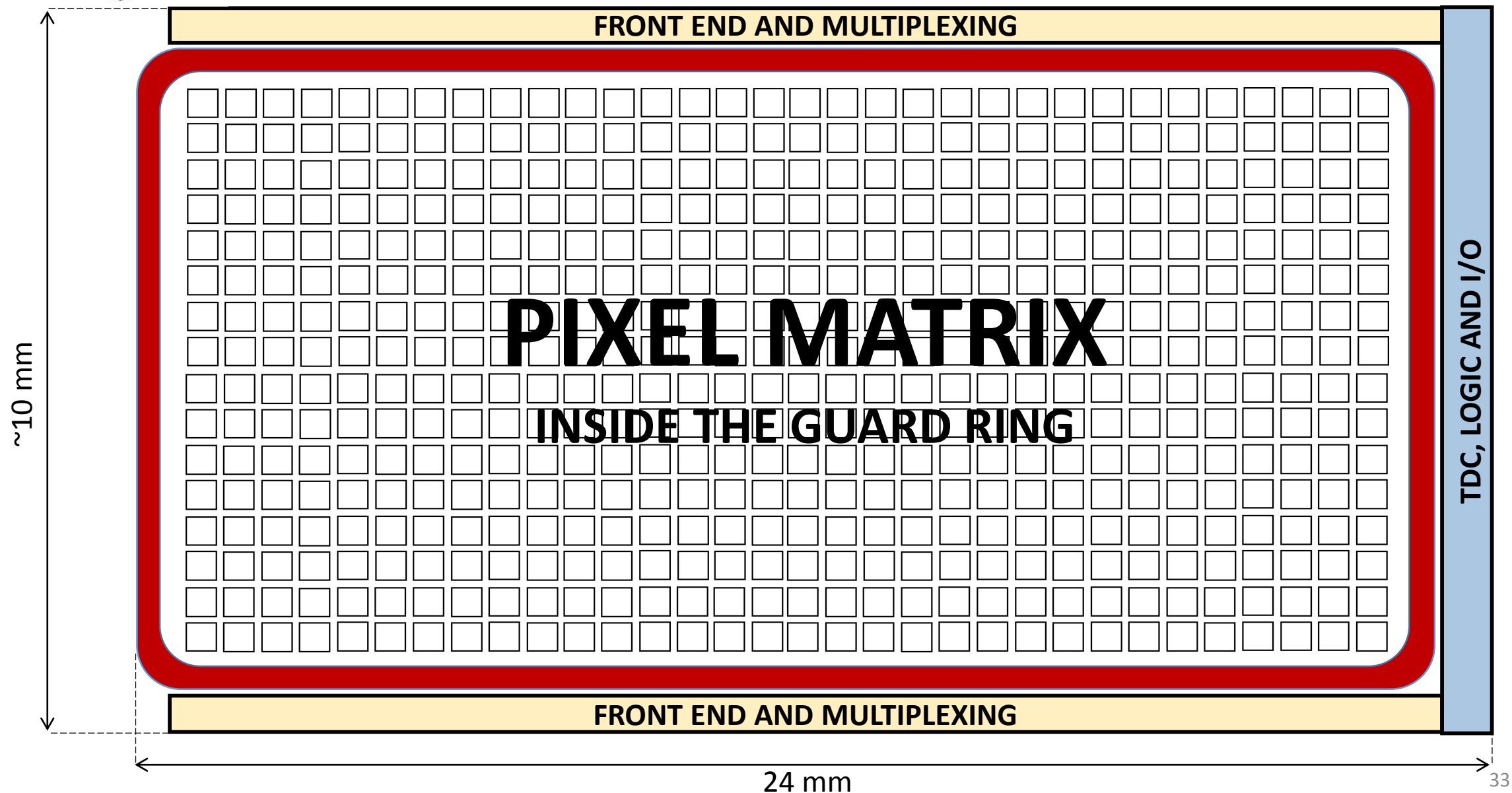
$$f_t = 250 \text{ GHz}$$

Equivalent to introducing an electric field in the base.

ASIC development



TT-PET ASIC conceptual layout





The TT-PET ASIC

A monolithic silicon pixel detector:

ASIC length	24 mm
ASIC width	7, 9, 11 mm
Pixel Size	$500 \times 500 \mu m^2$
Pixel Capacitance (comprised routing)	750 fF
Preamplifier power consumption	$< 80 mW/cm^2$
Preamplifier E.N.C.	600 e^- RMS
Preamplifier Rise time (10% - 90%)	800 ps
Time resolution for MIPs	100 ps RMS
TDC time binning*	20 ps
TDC power consumption	$< 1 mW/ch$

*** NOTE: 1920 chips synchronized at 10 ps precision.**

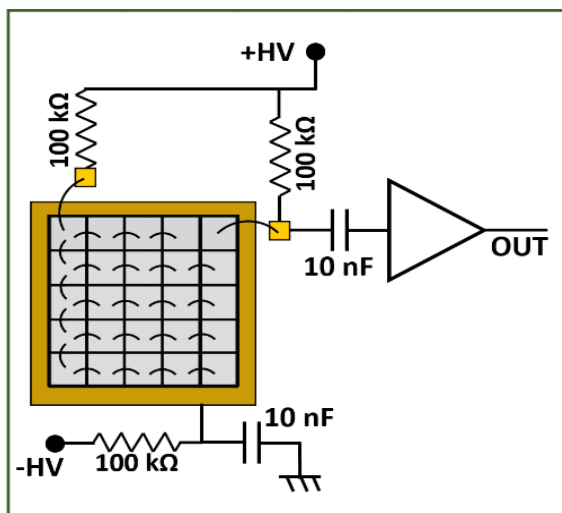
A new TDC synchronization technique developed for this project is being patented by University of Geneva / Unitec and INFN of Roma Tor Vergata.

Proof of principle

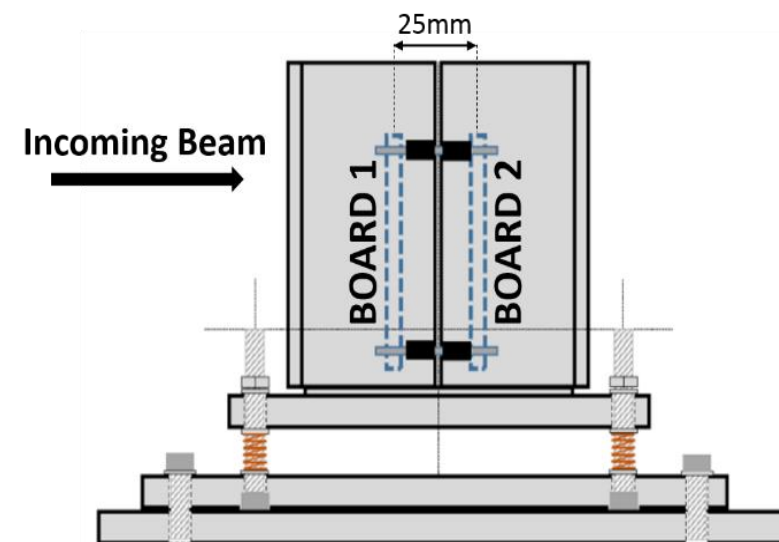
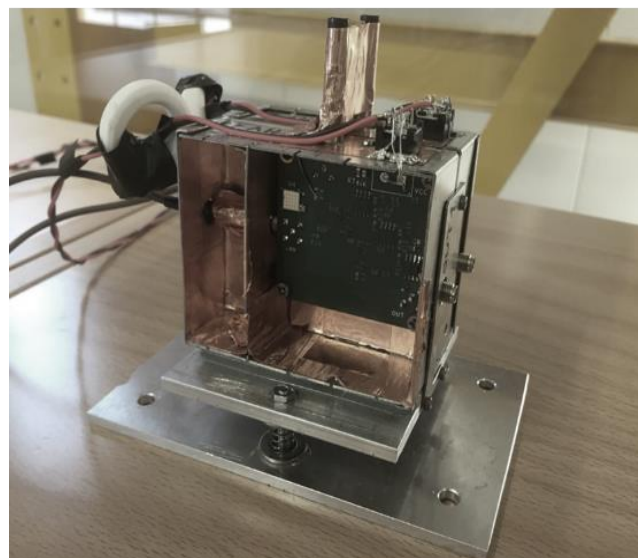
Proof of principle

Test with discrete component SiGe amplifier and external sensor

Board schematic design:

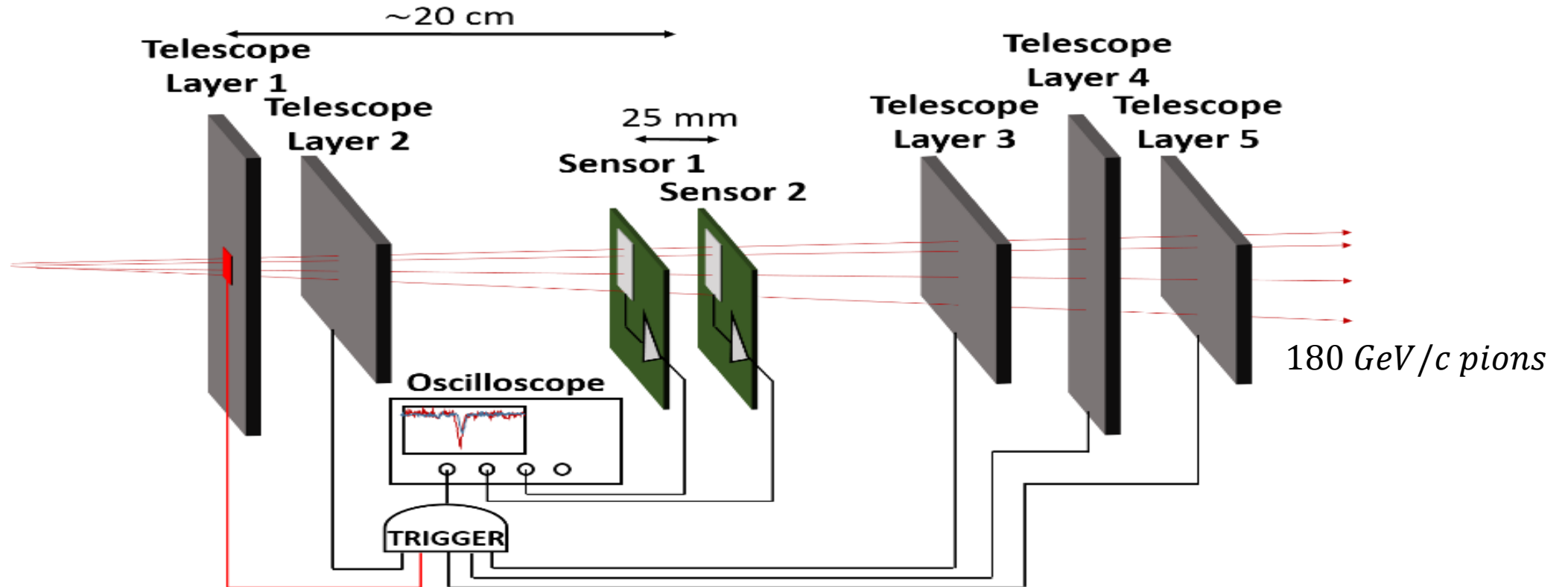


Mechanical support



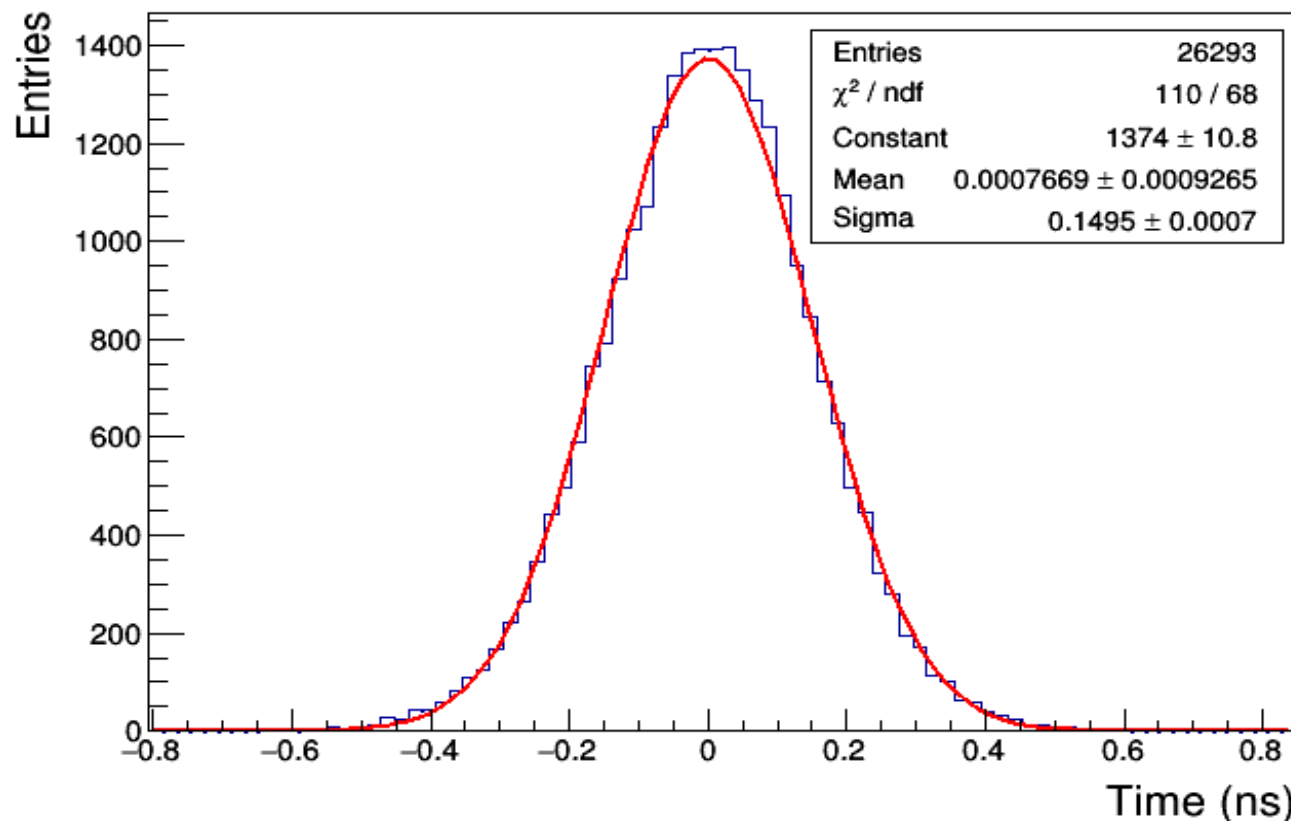
Proof of principle

Test of external sensor and custom SiGe HBT preamplifier at H8 beam line at SPS (CERN).



Proof of principle

Time Difference Detector 1 - 2, MIP, bias 2.3V/um



$$\sigma_t = \frac{(150 \pm 1)ps}{\sqrt{2}} = (106 \pm 1)ps.$$

**100ps time resolution
measured with MIPs
on 1 pF capacitance**

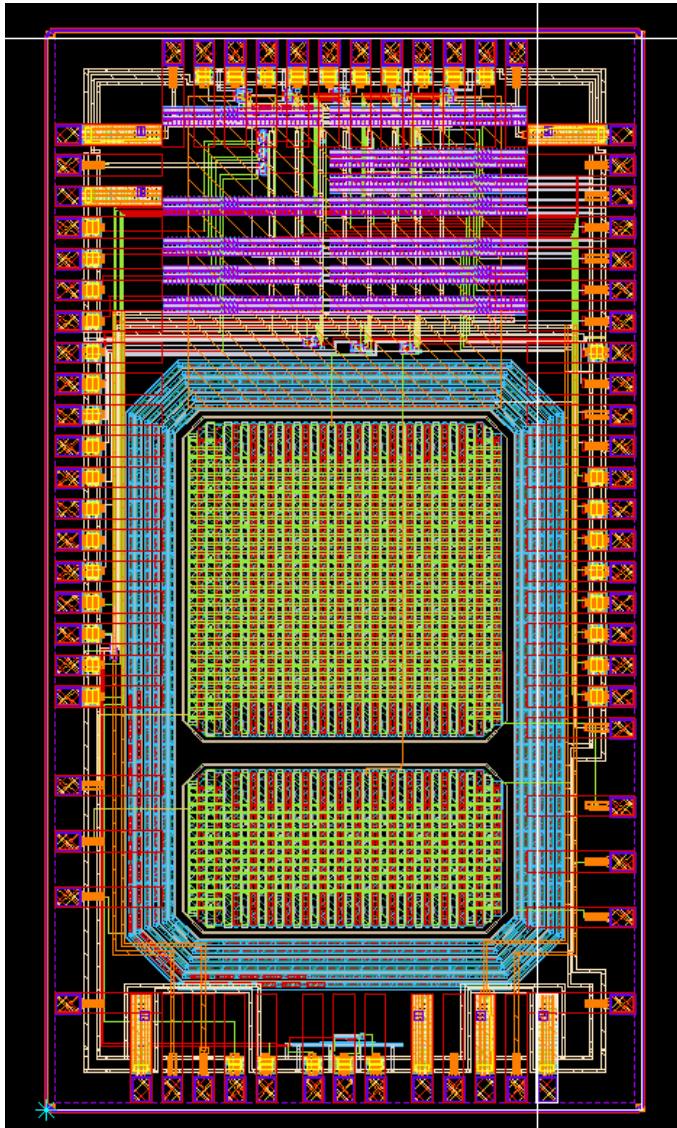
**Record for a silicon pixel
detector, obtained on a
large capacitance!**

Published on JINST:

M. Benoit et al., *100 ps time resolution with thin silicon pixel detectors and a SiGe HBT amplifier*, JINST 11, P03011 (2016)

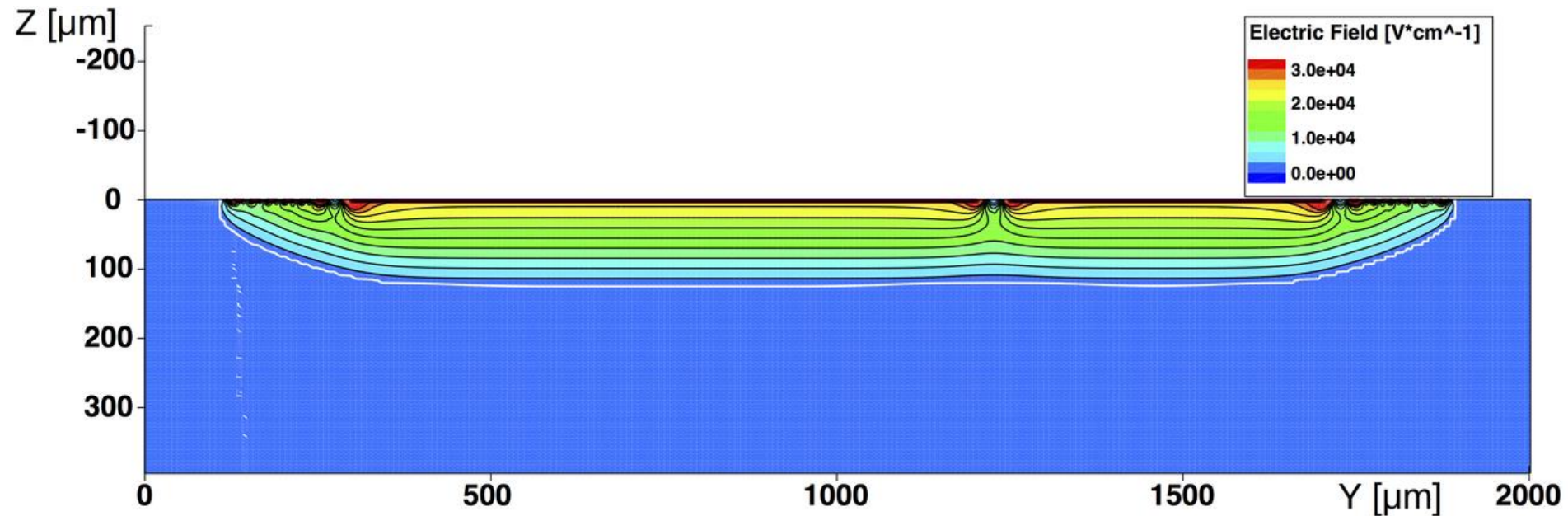
1st monolithic test chip

Chip layout



- Two pixels + amplifier + discriminator in 130 nm IHP process.
- Pixel size: $900 \times 900 \mu m^2$ and $900 \times 450 \mu m^2$.
- Higher wafer resistivity ($1 k\Omega cm$)
- No thinning, no backplane metallization.

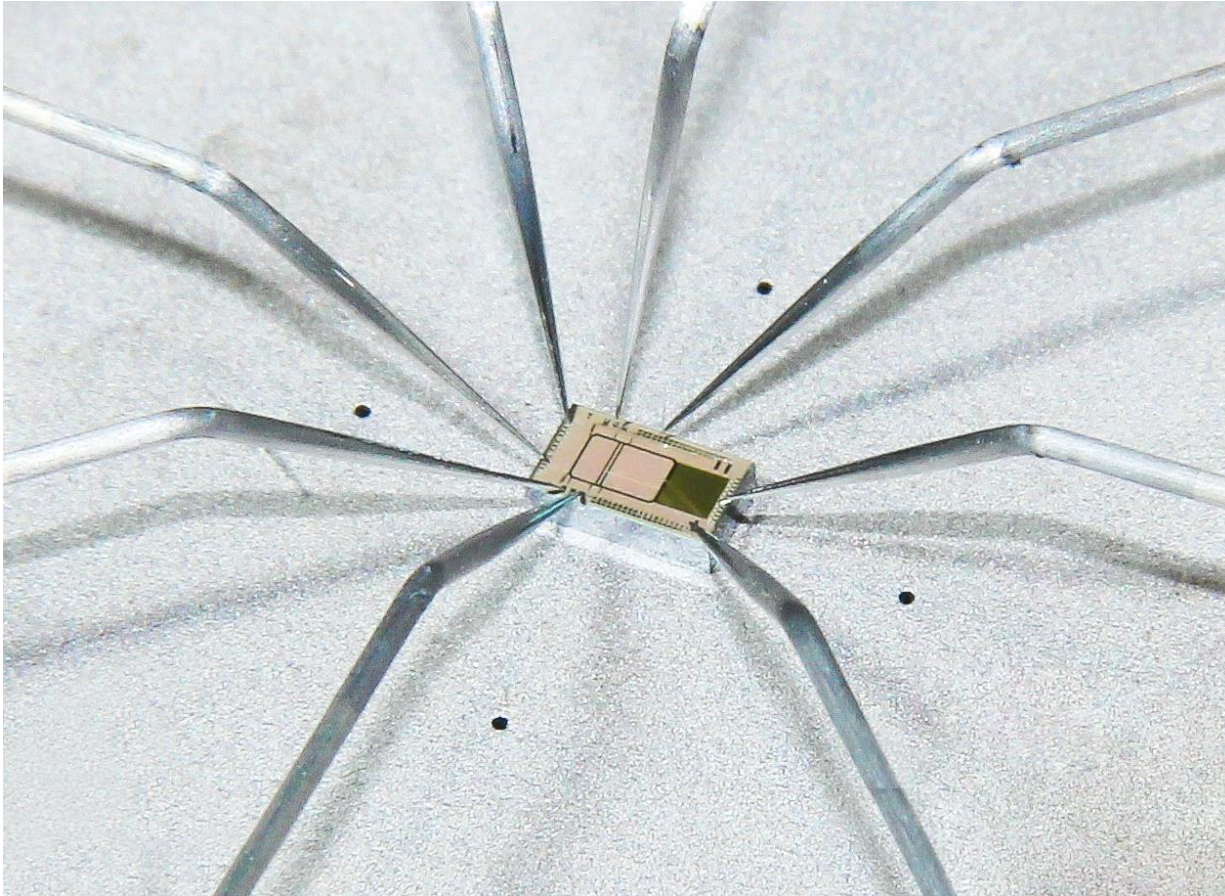
TCAD simulation of the chip



Expected depletion depth $\cong 130 \mu\text{m}$.

Due to the absence of thinning and backplane metallization, **no charge carriers drift velocity saturation**.

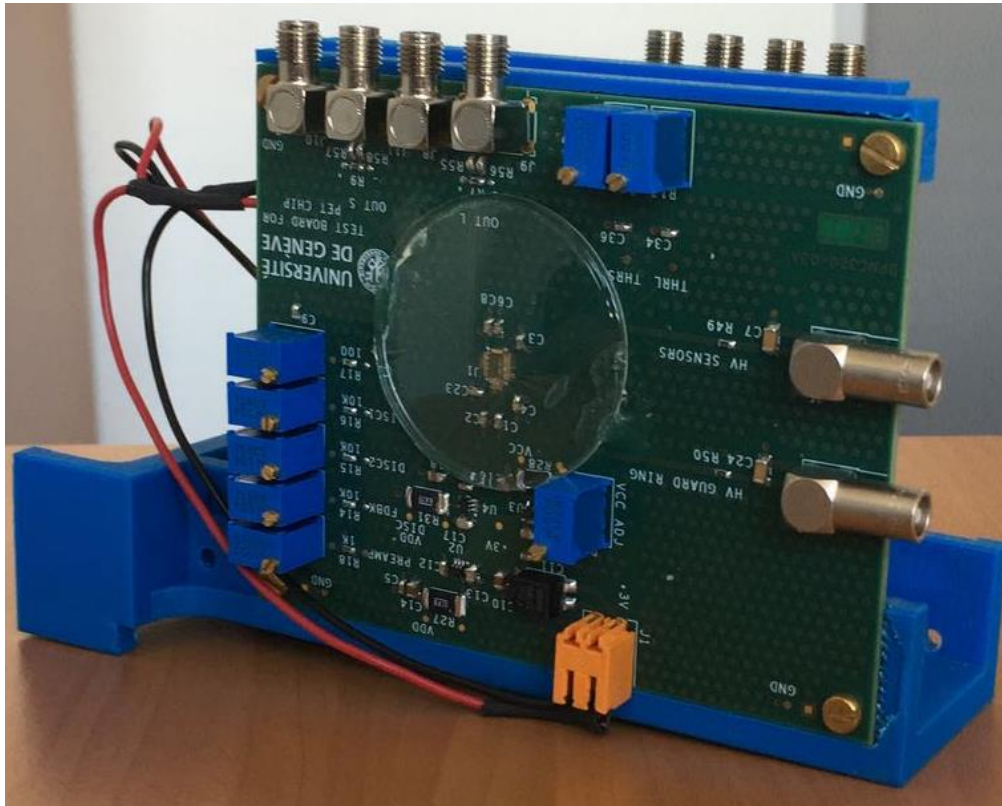
Test on DPNC probe station



Thanks to Mateus for the photo!

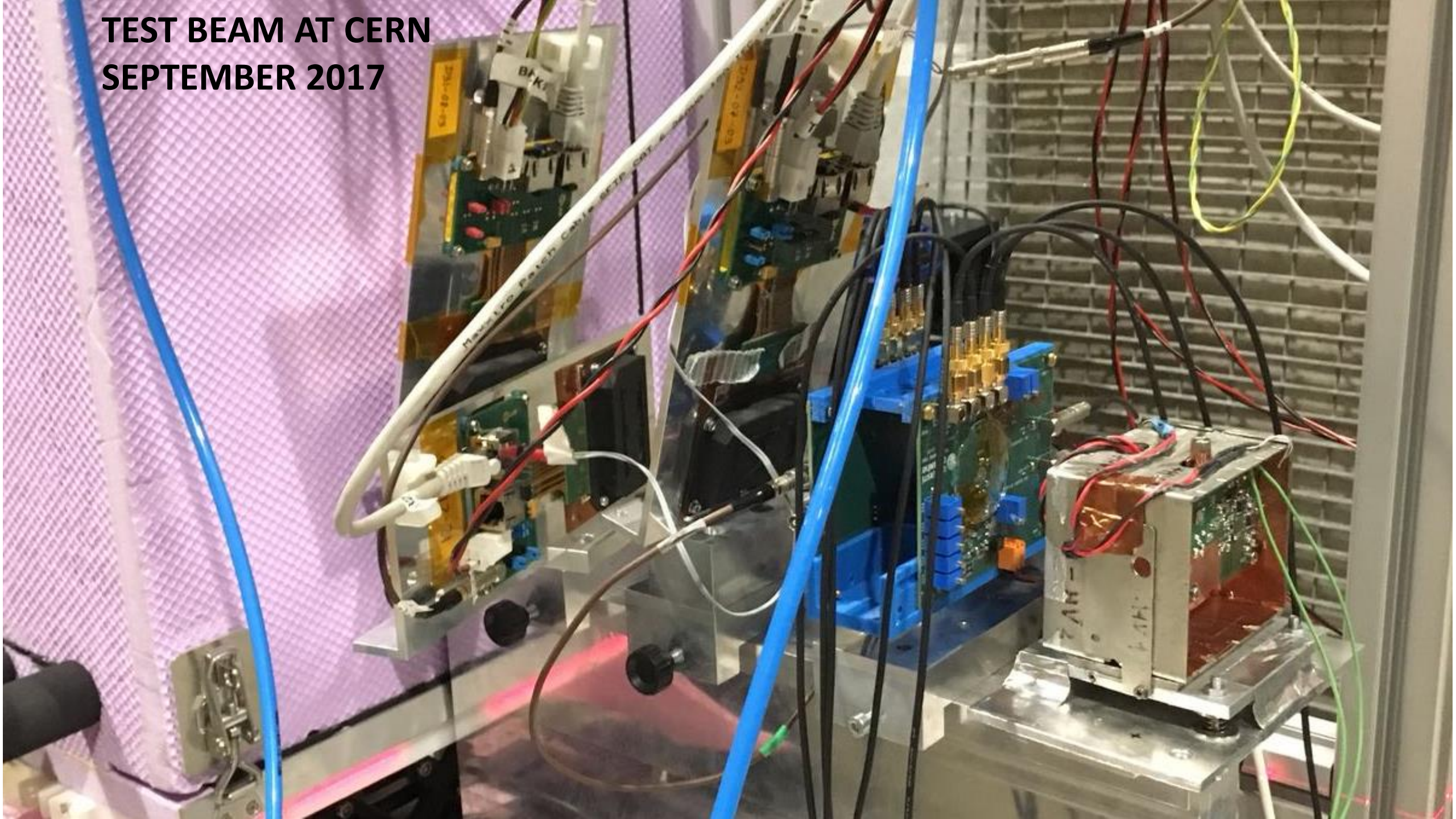
- Breakdown voltage is above 160 V
- Small pixel capacitance 0.8 pF
- Large pixel capacitance 1.2 pF

Test board



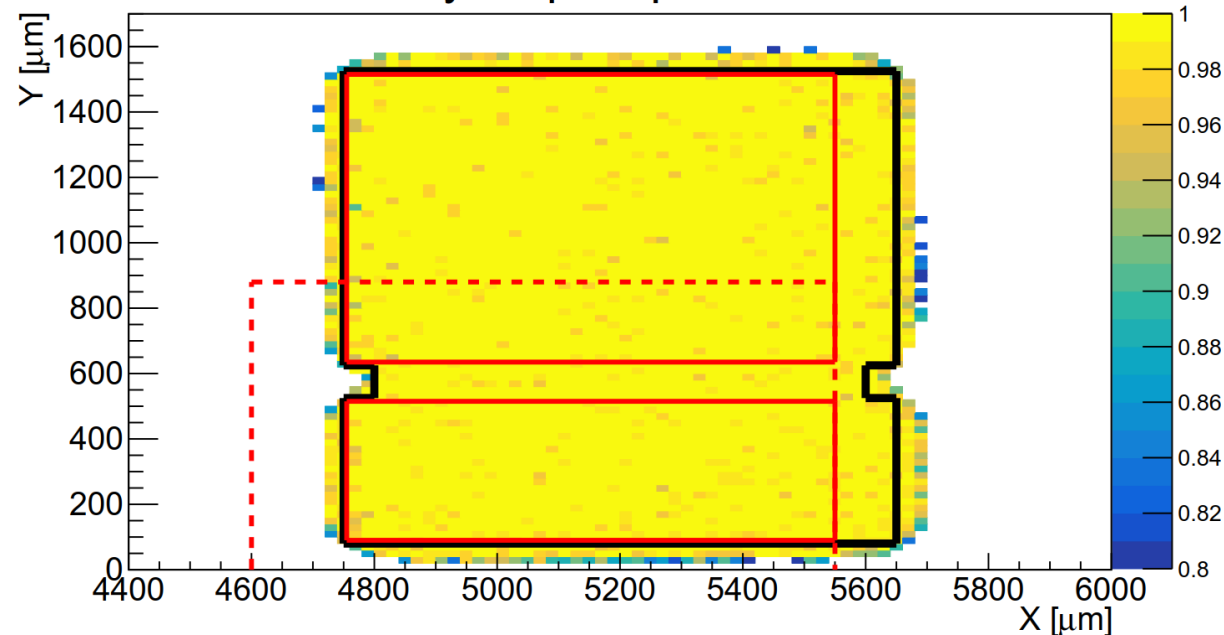
- Produced by the electronic engineering group at DPNC.
- Handles on the same board:
 - Digital pulses with 500 ps rise time.
 - Chip with $30 \frac{mV}{fC}$ gain and $0.1 fC$ noise amplifier.

**TEST BEAM AT CERN
SEPTEMBER 2017**



Test beam results: efficiency

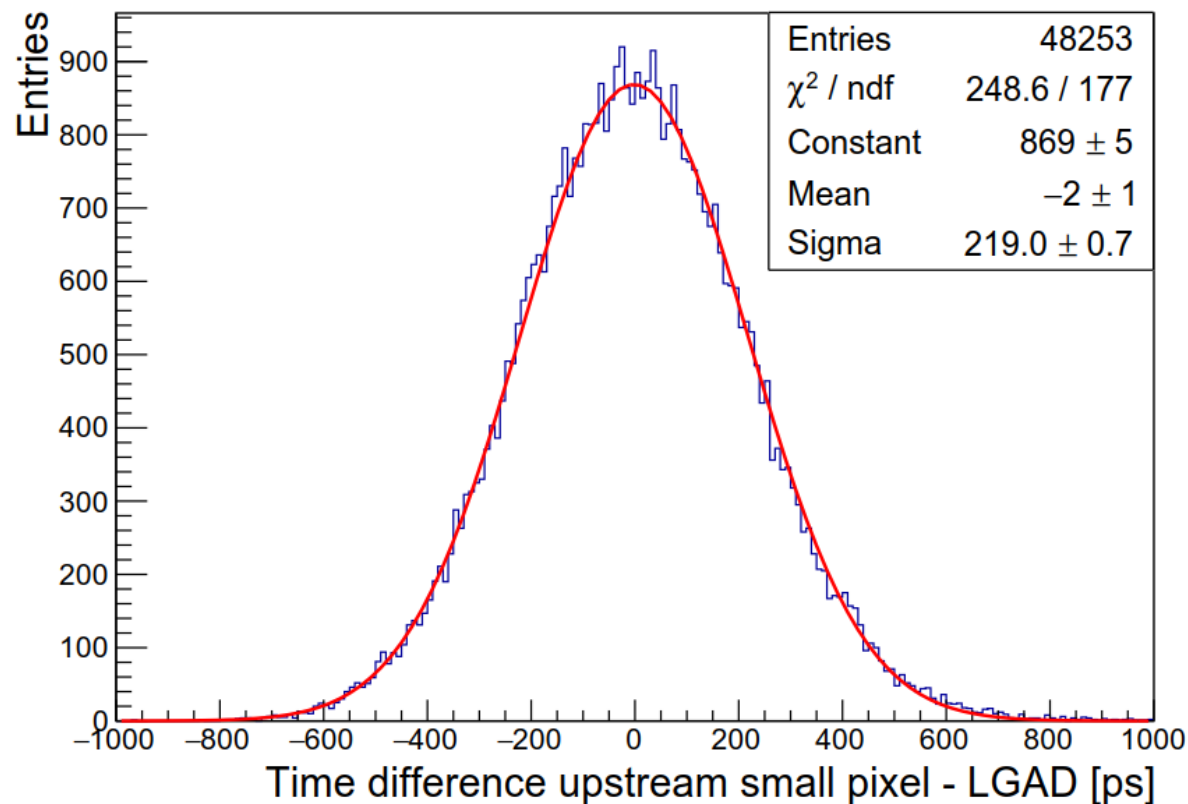
Efficiency Map - Upstream Sensor



- Efficiency 99.8%.
- Amplifier $ENC < 600$ electrons RMS.
- Amplifier power consumption: $< 350 \frac{\mu W}{channel}$, corresponding to $70 \frac{mW}{cm^2}$



Test beam results: time resolution



Time resolution ~ 220 ps RMS

Record for a monolithic pixel detector!

Submitted for publication.

Available on: <http://arxiv.org/abs/1802.01319>

2nd monolithic test chip

“prototype 0”

Prototype 0 layout



- 3×10 matrix, $500 \times 500 \mu m^2$ pixels.
- Preamplifier, discriminator, 20 ps binning TDC, logic, serializer integrated in chip.
- Thinned to $100 \mu m$.
- Full backside processing.
- **High resistivity version will be back from foundry next week. Low resistivity version under test.**

Prototype 0 layout

Observation method: Reflection

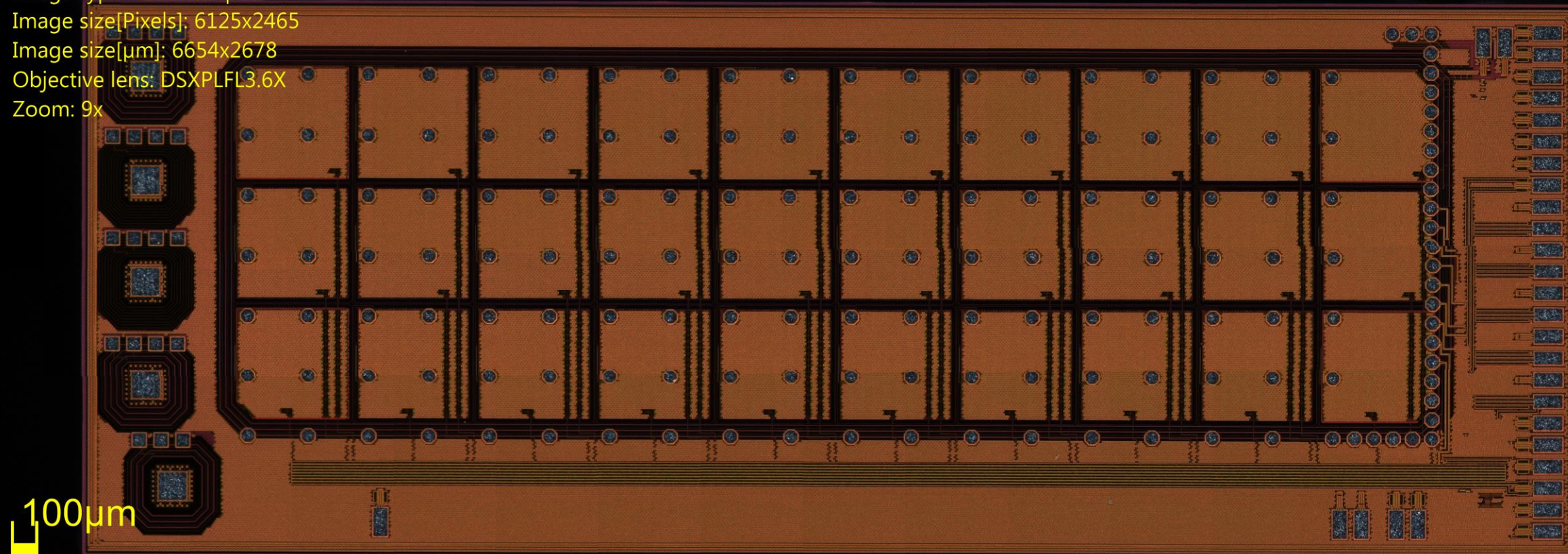
Image type: Color snap

Image size[Pixels]: 6125x2465

Image size[μm]: 6654x2678

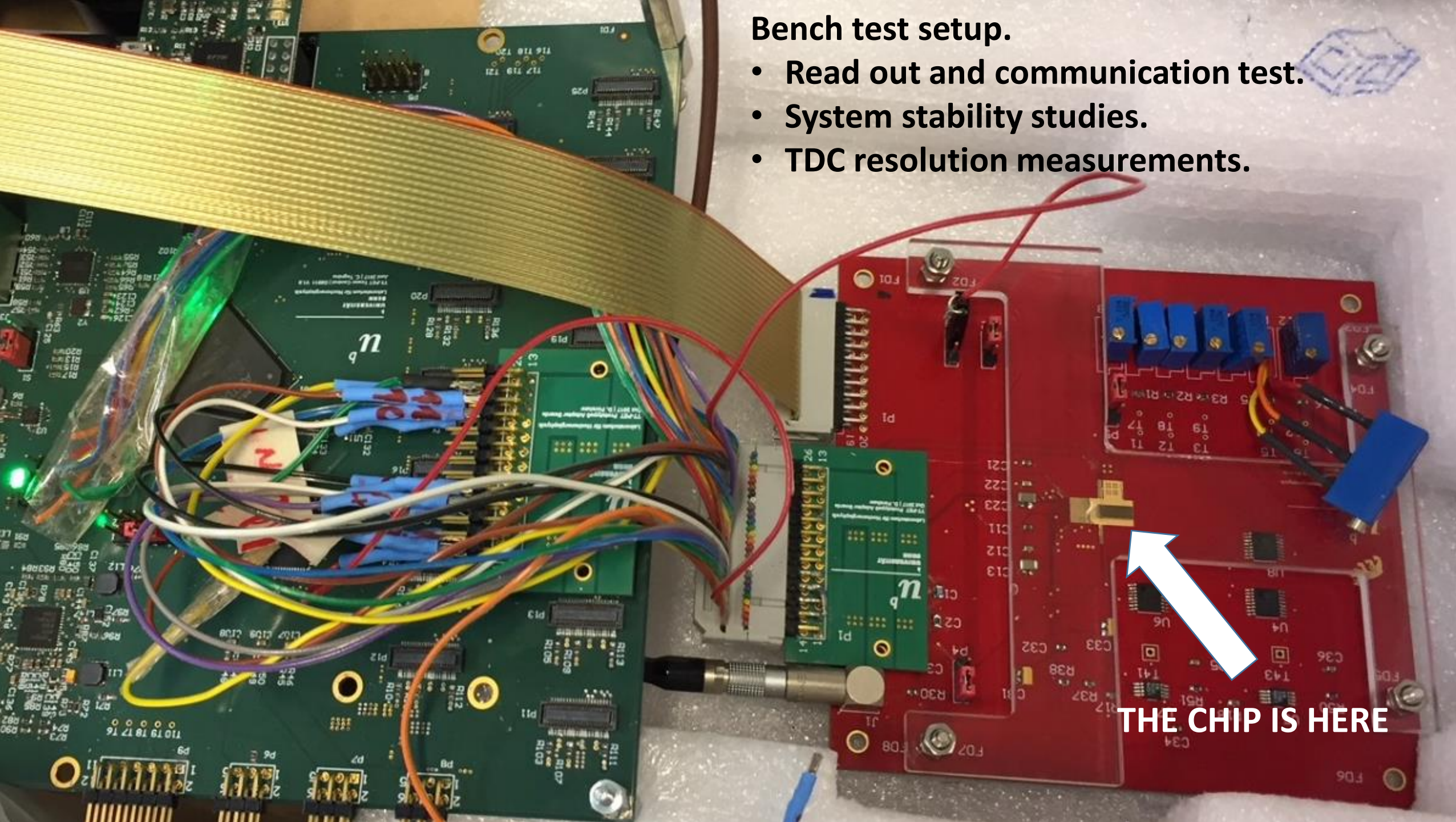
Objective lens: DSXPLFL3.6X

Zoom: 9x

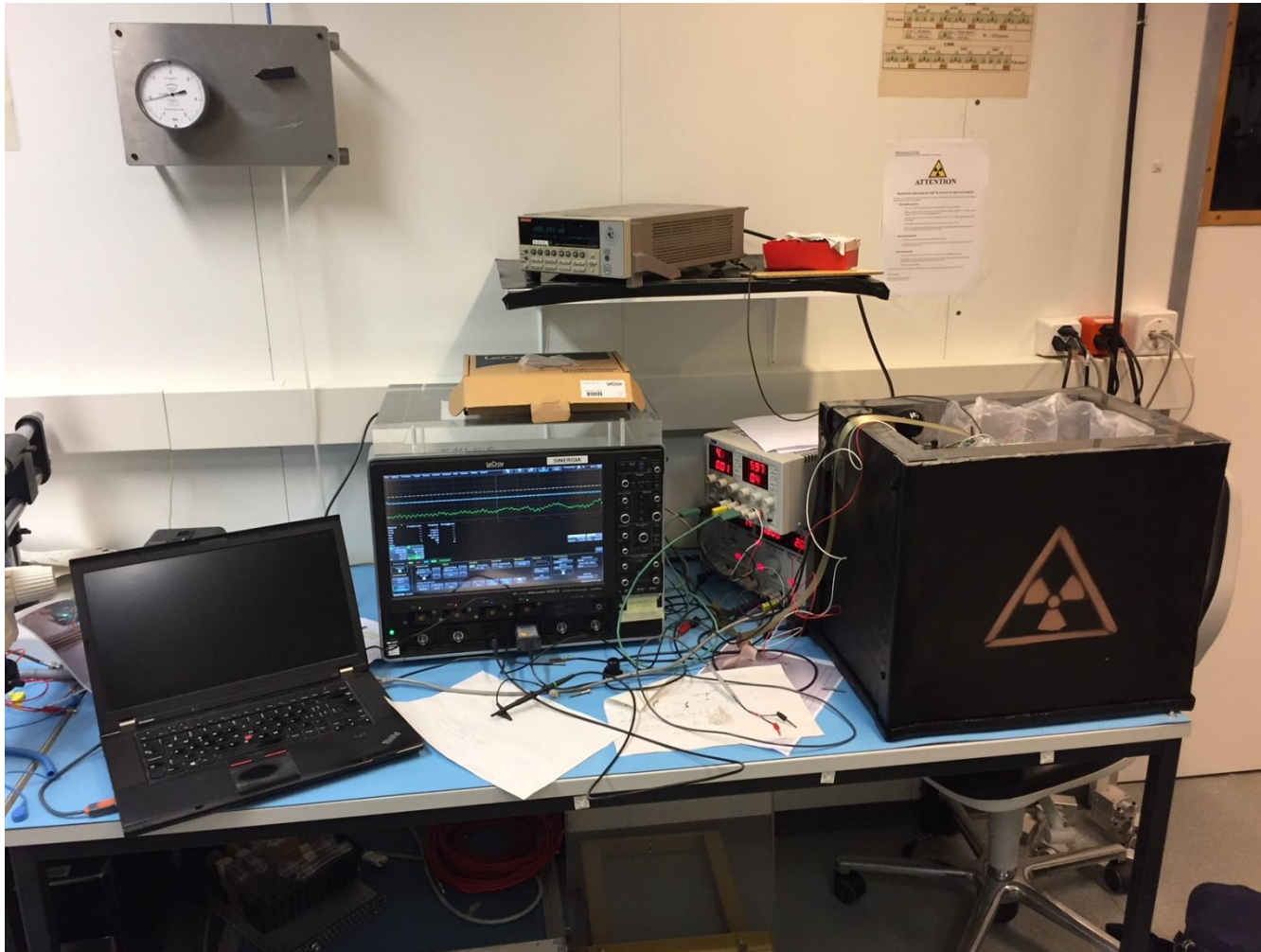


Bench test setup.

- Read out and communication test.
- System stability studies.
- TDC resolution measurements.



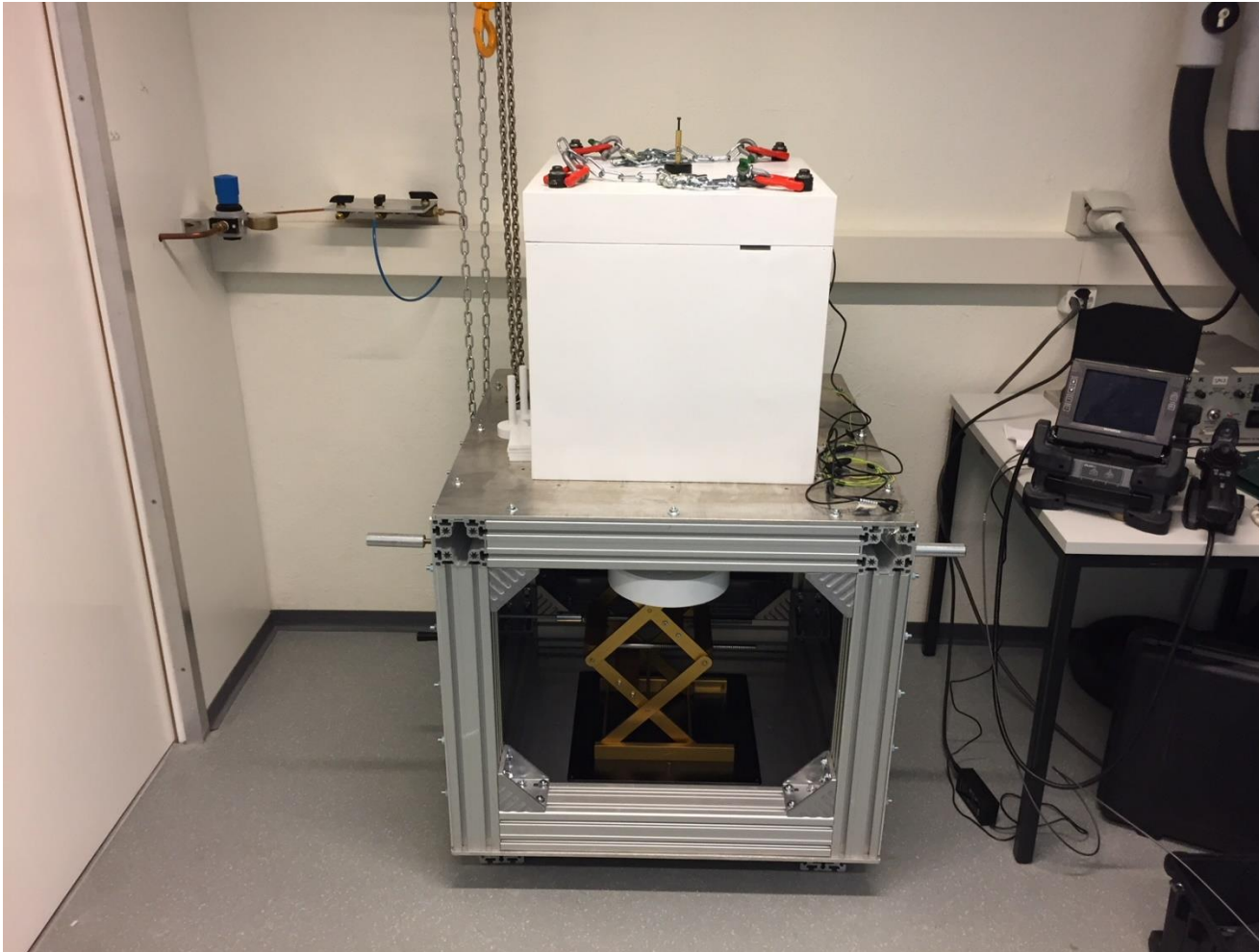
Test setup at DPNC



^{241}Am and ^{90}Sr sources.

- Front end / sensor noise and gain measurement with ^{241}Am and ^{90}Sr sources.
- Performance validation in preparation of the test beam with Minimum Ionizing Particles.

Test setup at DPNC



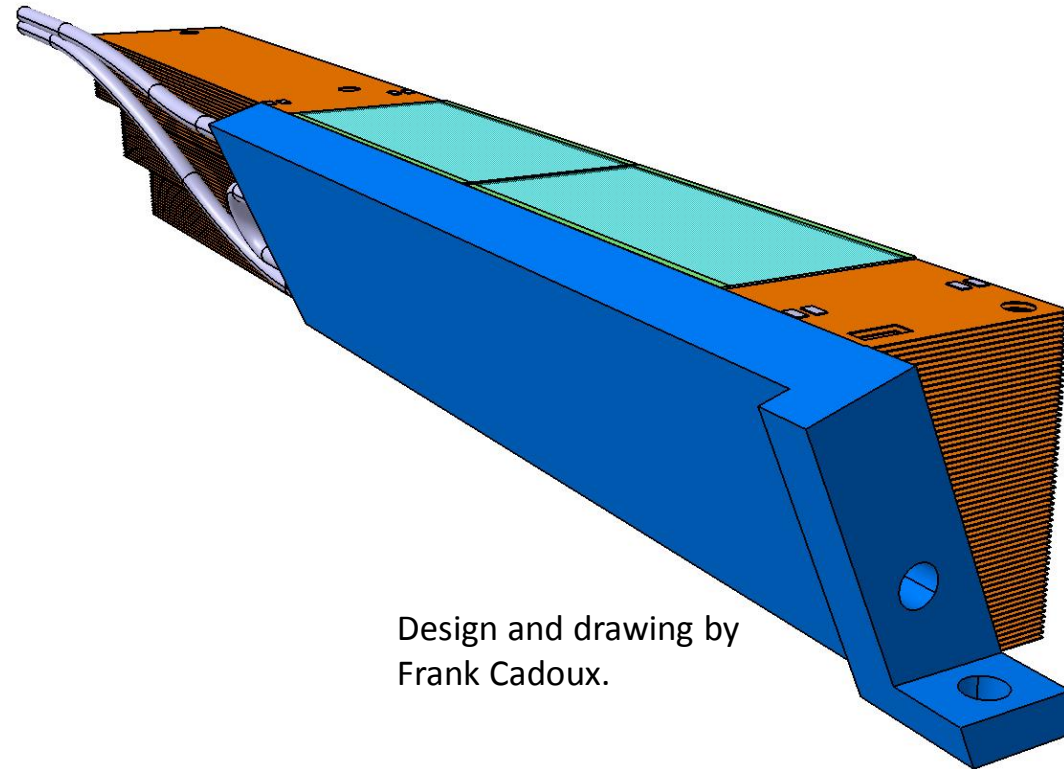
^{22}Na source setup.

- ~ 1 ton of lead.
- Crabbing system for source pick up.
- Sensitivity for 511 keV photons measurement.
- Time of flight to 511 keV photons measurement.

Future steps

Cell assembly test

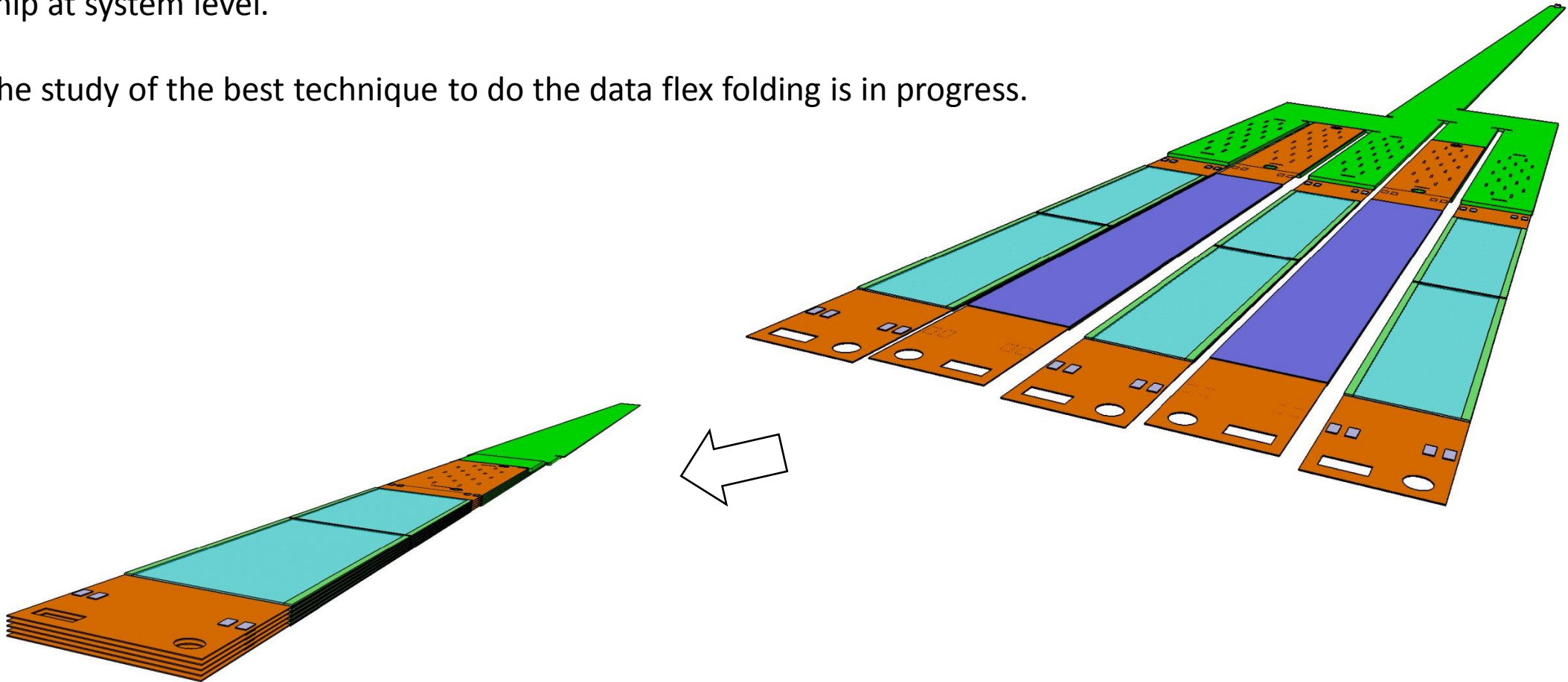
- A thermal mock-up of the sensor will be prepared to test the assembly procedure and the performance of the active cooling.



Design and drawing by
Frank Cadoux.

Cell assembly test

- A prototype of the module flex has been produced in order to study the expected electrical performance of the chip at system level.
- The study of the best technique to do the data flex folding is in progress.



Final assembly

- The final assembly will be done by using the DPNC flip-chip machine.





Chip submission

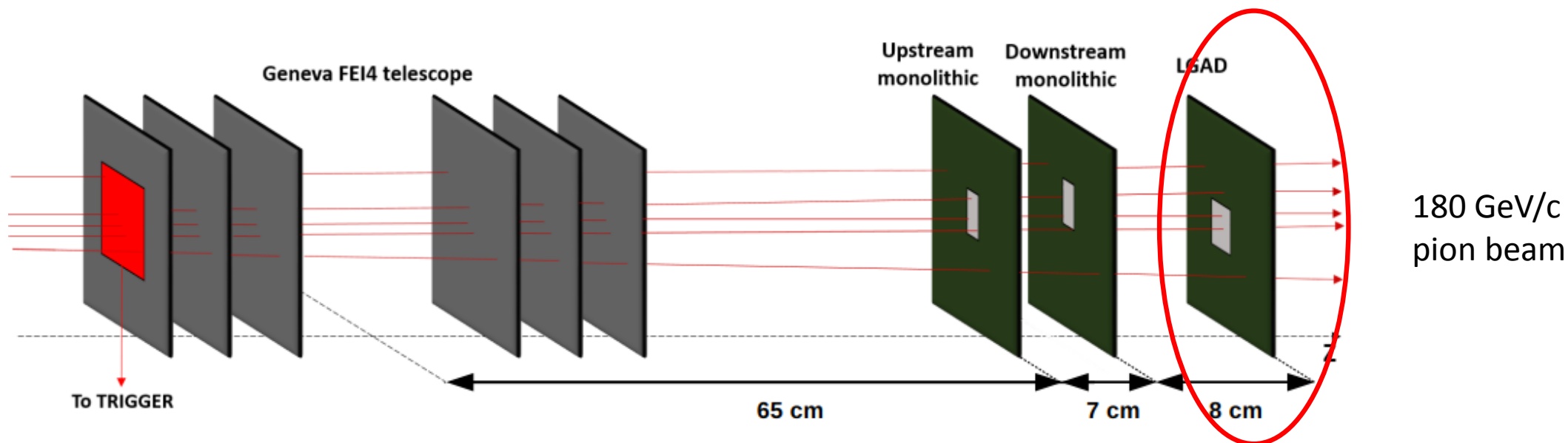
- The design of the final chip will start in May 2018.
- The engineering run is scheduled for September 2018.
- The tower assembly will start in January 2019.

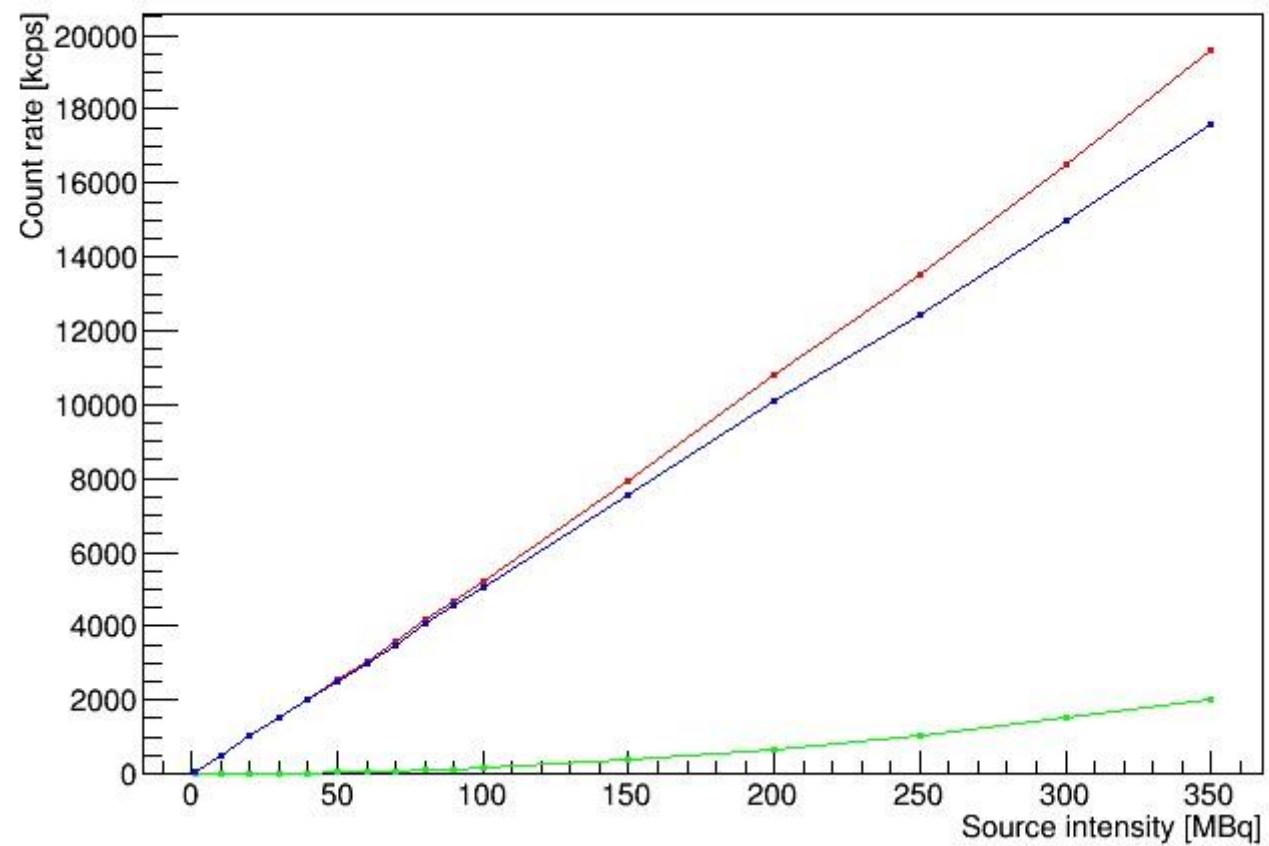
Conclusions

- A **new technique to exploit the timing performance** of the semiconductor sensor has been developed.
- Thanks to this technique, the TT-PET collaboration **obtained the record time resolution** of **106 ps** with silicon sensors and **220 ps** with monolithic silicon pixel detectors.
- The project is very challenging: the assembly of the scanner will **make use of the expertise present in the DPNC** of the University of Geneva.
- The TT-PET scanner will have **unprecedented Time of Flight, space resolution and counting rate capability**, allowing for better study of the metabolic processes.

Backup

Measurements at CERN SPS beam test facility



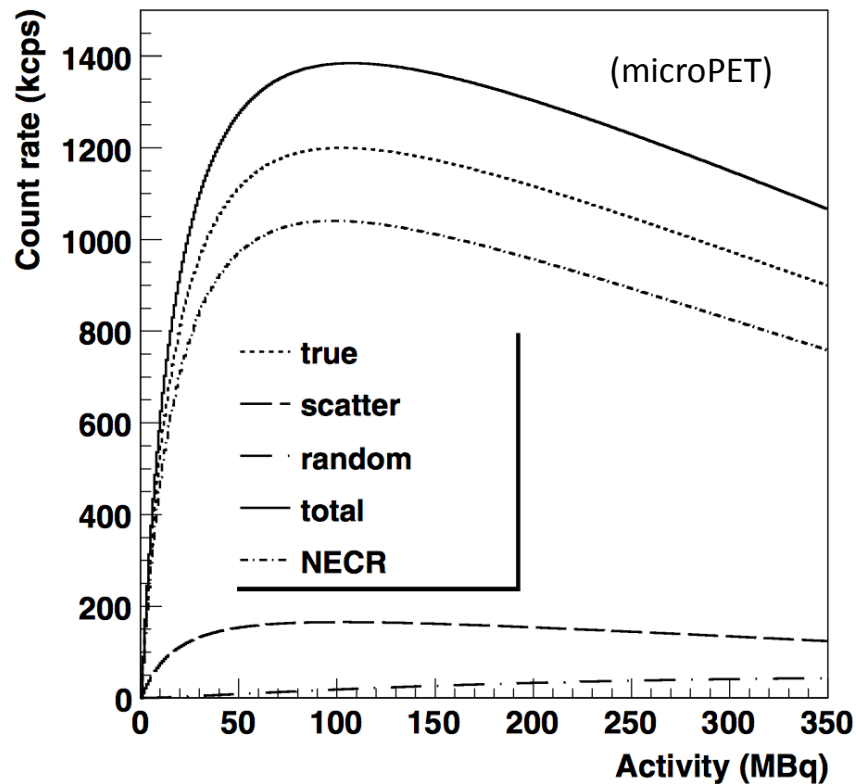




The TT-PET scanner

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Typical performance of a small animal TOF-PET



TT-PET scanner counting rates – Geant4 simulation

