Pixel Detectors
- trends and options for the future

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Outline

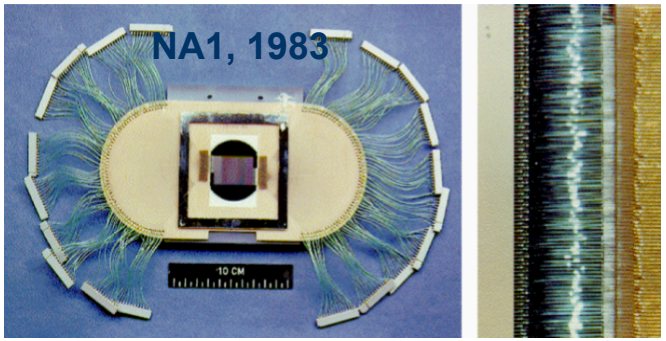
1. Pixels now and for the next 10 years
   - a little review

~~2.~~ Diamond versus Silicon at high fluences

One slide on "the past"

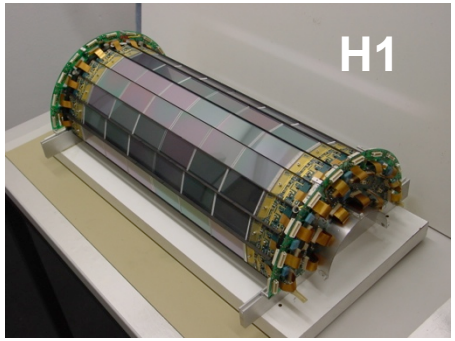
wire chambers

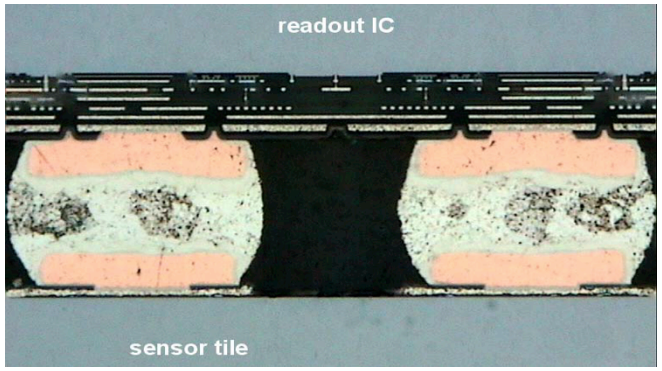
→ electronic recording
of particle tracks



silicon strip detectors

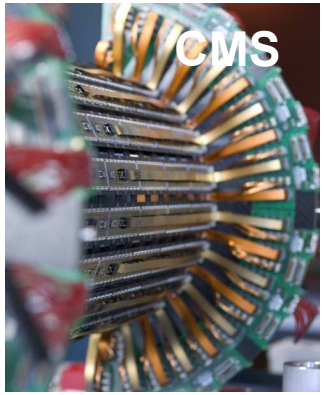
→ measurement of
ps – lifetimes
and decay vertices

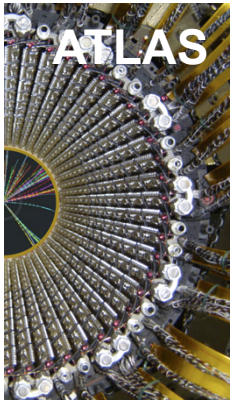




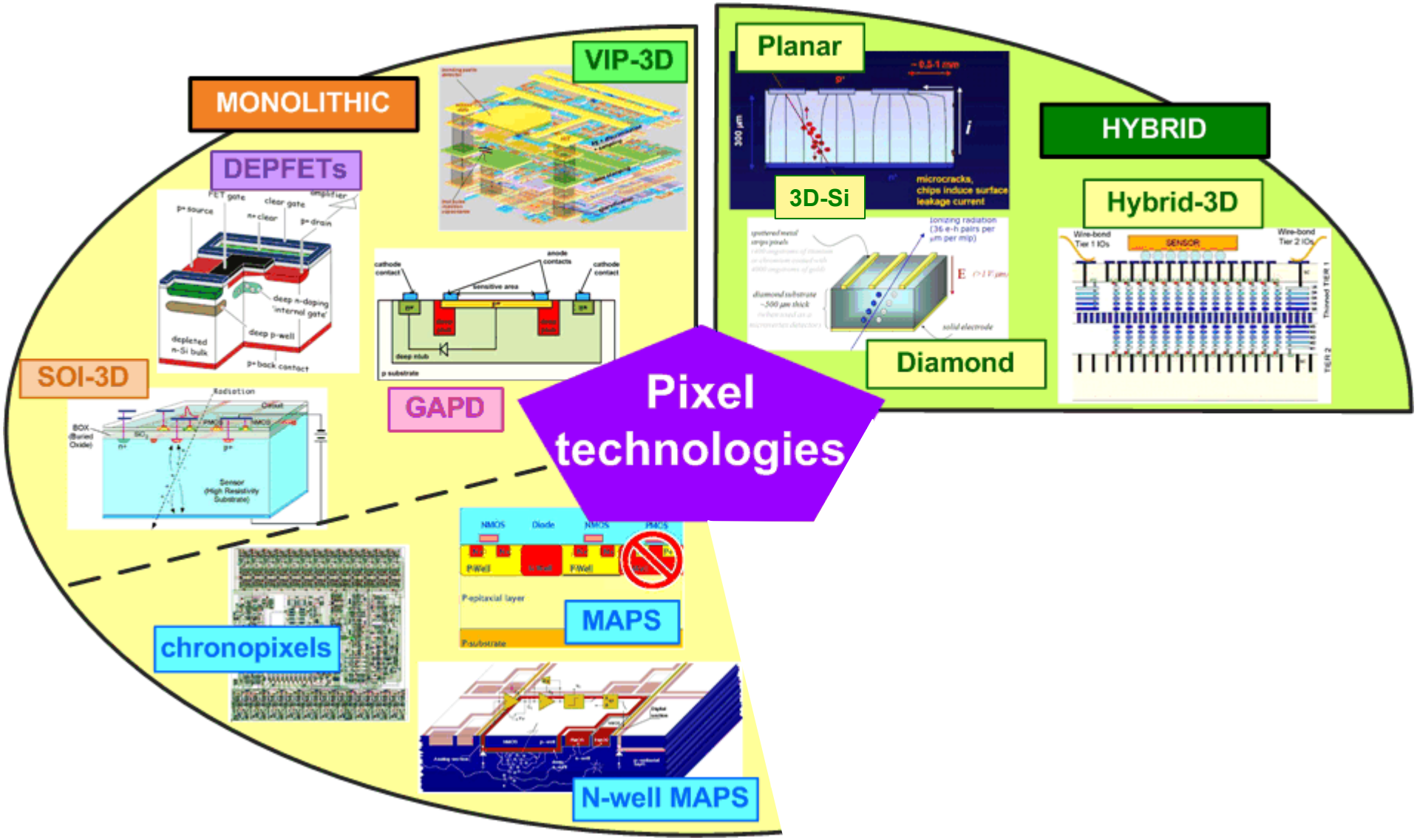
pixel detectors

→ 3-dim point measurement
in high rate environments
like LHC



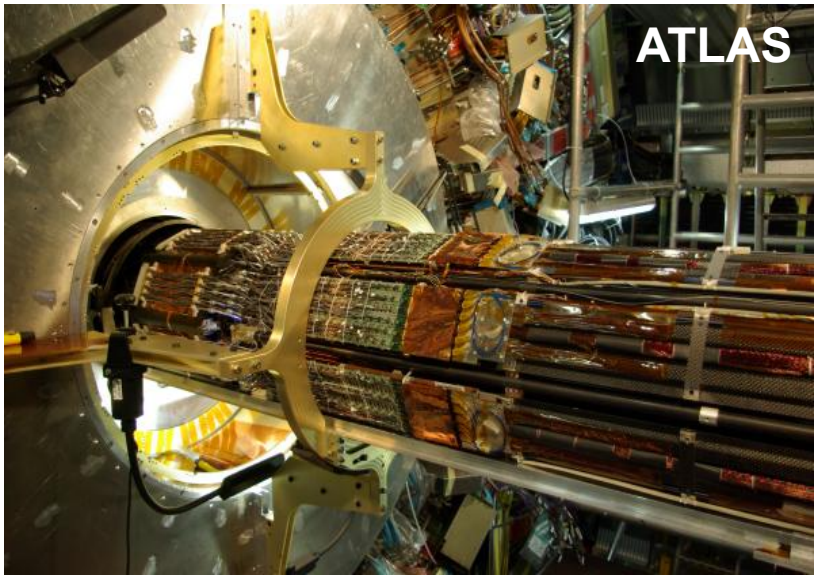


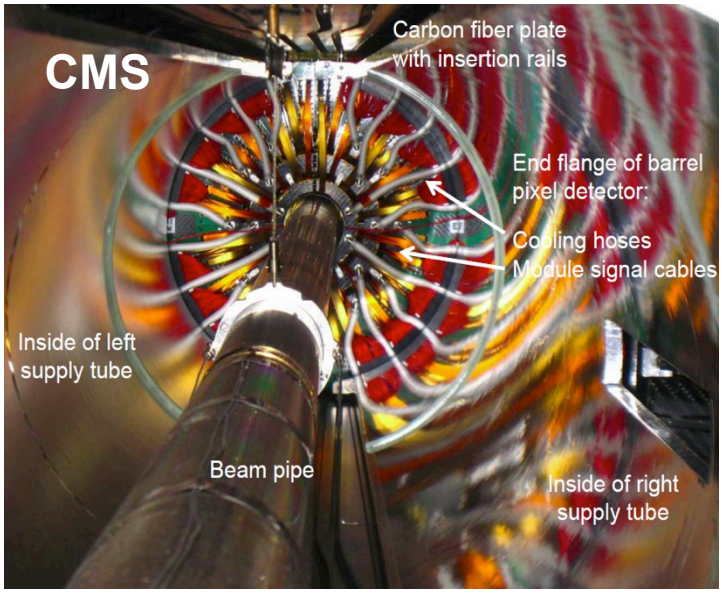
The variety of pixel technologies

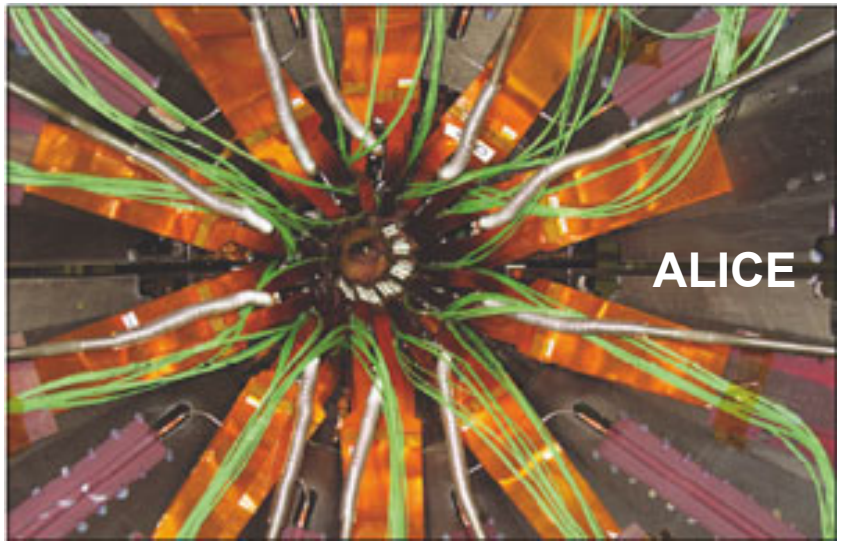


The combination of high resolution, low mass and low power is a substantial challenge

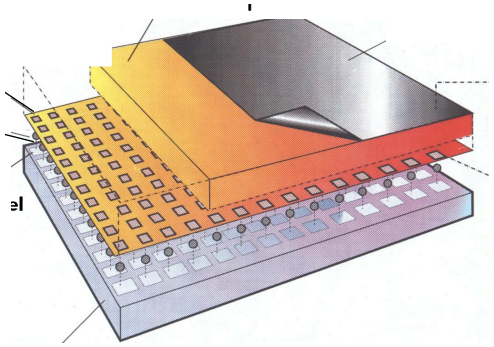
Today's "state of the art" of running detectors

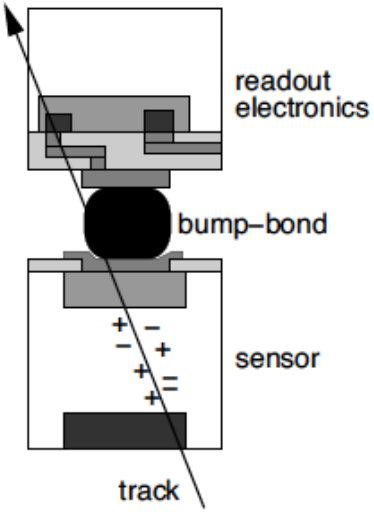






all based on
"Hybrid Pixel Detectors"





Rate and radiation challenges at the innermost pixel layer

Hybrid Pixels

	BX time	Particle Rate	Fluence	Ion. Dose
	ns	kHz/mm^2	n_{eq}/cm^2 per lifetime*	kGy per lifetime*
LHC (10^{34} cm^{-2}s^{-1})	25	1000	1 x 10^{15}	790
sLHC (10^{35} cm^{-2}s^{-1})	25	10000	> 10^{16}	> 5000
SuperBFs (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	100
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	4
RHIC (8x10^{27} cm^{-2}s^{-1})	110	3,8	1.5 x 10^{13}	8

Monolithic Pixels

lower rates
lower radiation
smaller pixels
less material

assumed lifetimes:
LHC, sLHC: 7 years
ILC: 10 years
others: 5 years

An experimentalist's dream

- good S/N
- μm space resolution
- ~ns time resolution
- > 10 MHz / mm^2 rate capability
- radiation hard to 5 MGy
- radiation length per layer < 0.2% x/X_0 (*)
- all in one monolithic pixel "chip"

(*) X_0 = radiation length
= char. length for elmagn. processes
(bremsstrahlung, pair production)

Reality

hybrid pixels

• good S/N	✓ (fully) depleted
• µm space resolution	➢ ~10 µm
• ~ns time resolution	✓ obtained at LHC
• > 10 MHz / mm^2 rate capability	✓ tbd for sLHC
• radiation hard to 5 MGy	✓ tbd for sLHC
• radiation length per layer < 0.2% x/X_0	➢ 3.5%
• all in one monolithic pixel “chip”	➢ no, hybrid

Reality

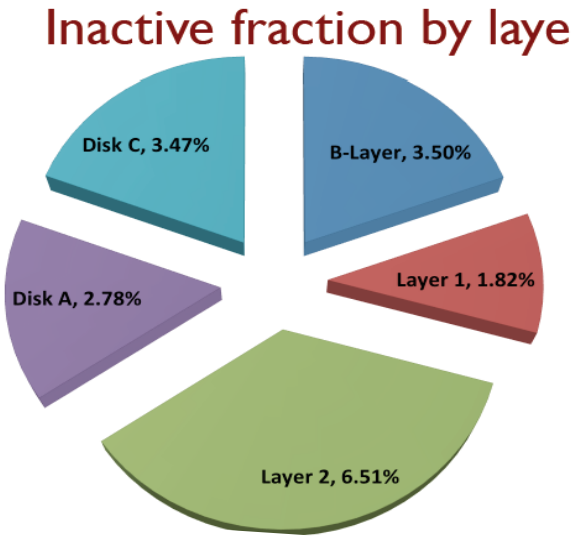
	MAPS/DEPFET
• good S/N	➢ NO / YES
• µm space resolution	✓ 1 µm tough
• ~ns time resolution	➢ slow rolling shutter
• > 10 MHz / mm^2 rate capability	➢ < 0.4 MHz/mm^2
• radiation hard to 5 MGy	➢ < 100 kGy
• radiation length per layer < 0.2% x/X_0	✓ but tough
• all in one monolithic pixel “chip”	○ not quite

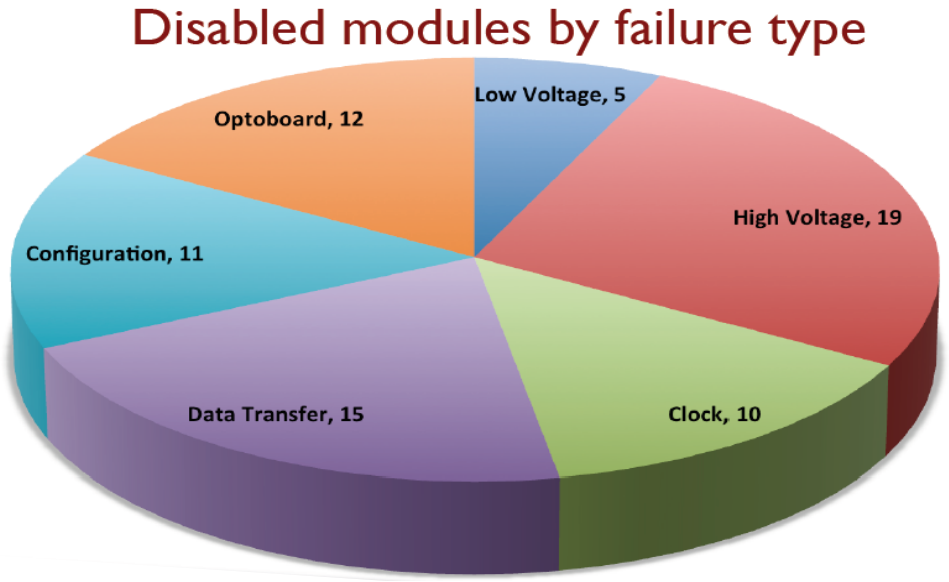
Direction for the “future” = a late outline for the “review”

- Hybrid pixels for sLHC
  - better ICs -> pixel size and bandwidth
  - radiation hard sensors
- (semi)Monolithic Pixels (DEPFET/MAPS)
  - thin
  - towards truly monolithic CMOS
- 3D Integration
  - vias first
  - vias last

ATLAS Pixel Running experience 2010 + 2011

- Pixel data taking efficiency in 2011: 99.8%
- 95.9% of pixel modules active in data taking
  - 72 (out of 1744) modules disabled (4.1%)
    - 2.1% lost before LHC turn on
    - 2.0% lost 2010 + 2011
  - 0.17% front end chips disabled

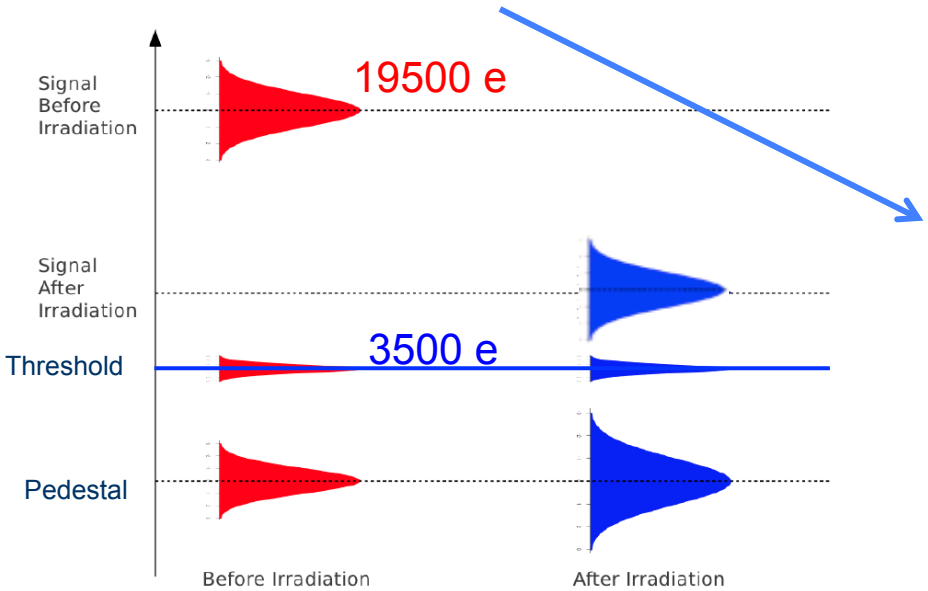


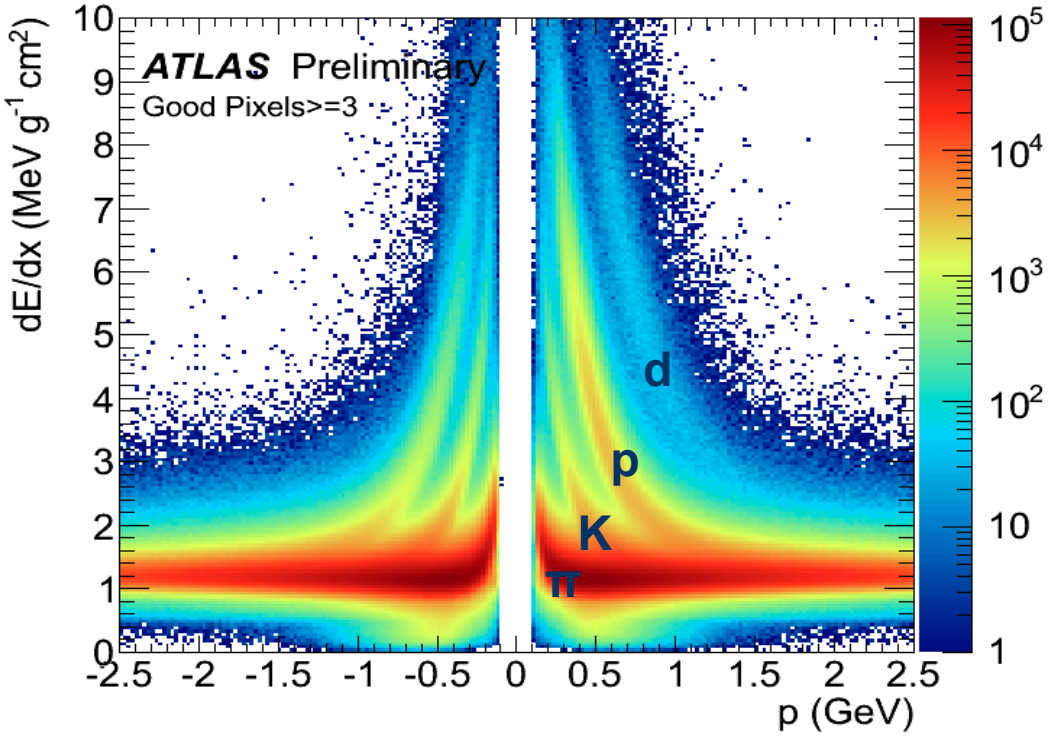


Performance

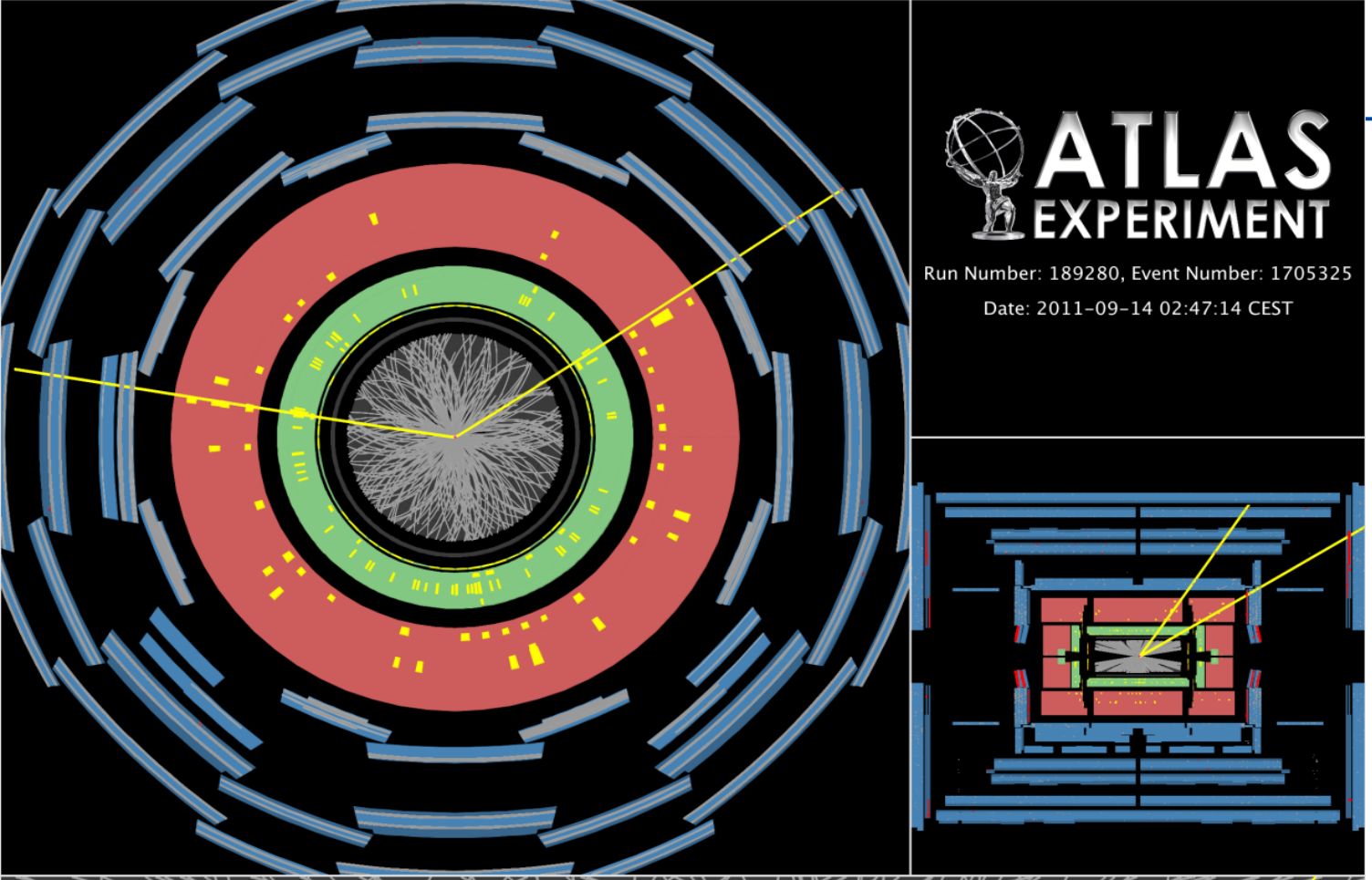
Signal of a high energy particle ≙ 19500 e^-

- Discriminator thresholds = 3500 e, ~40 e spread, ~170 e noise
- 99.8% data taking efficiency
- 95.9% of detector operational
- ca. 10 μm x 100 μm resolution (track angle dependent)
- 12% dE/dx resolution



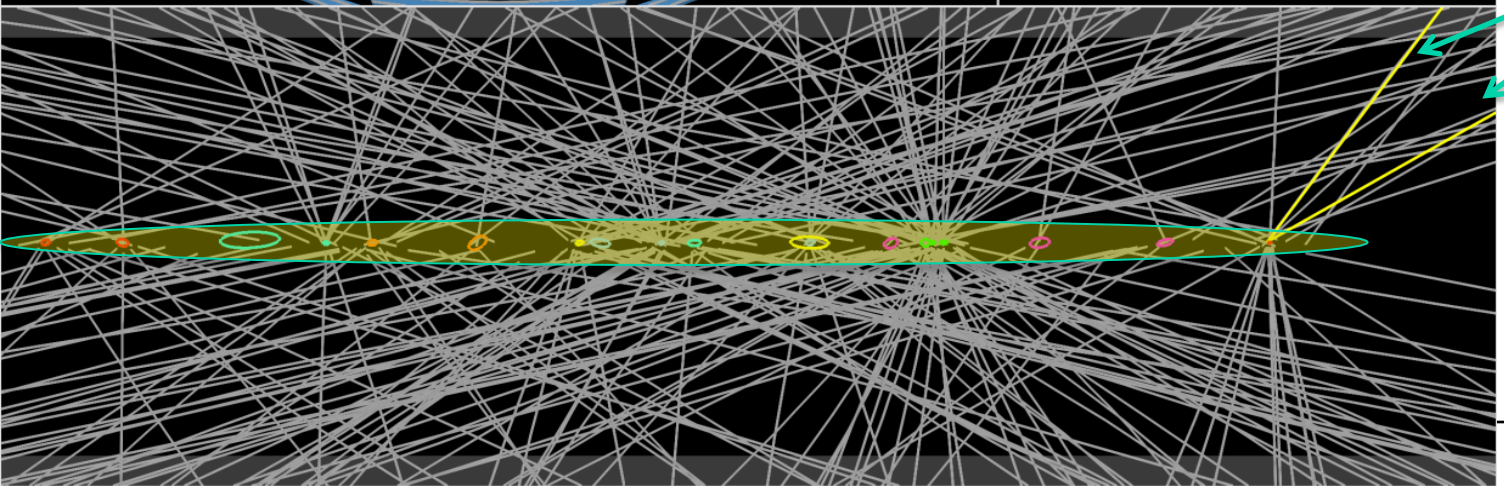


Pile-up



Z → μμ event with 20 interactions

(Typical peak pile-up per bunch crossing: 12)



pp → Z → μμ

Interaction region ~7 cm

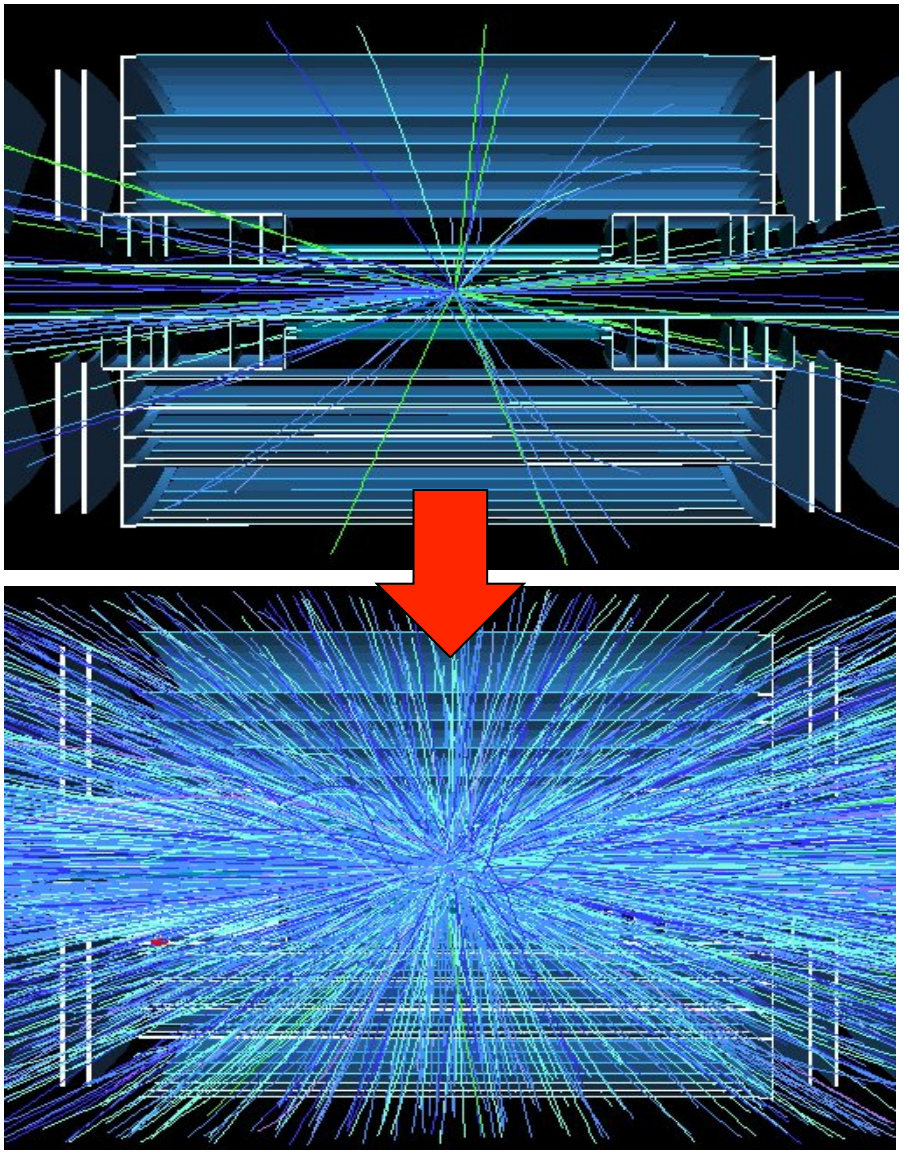
Challenges for the LHC future

Increased luminosity requires

- higher hit-rate capability
- higher segmentation
- higher radiation hardness
- lighter detectors

Radiation hardness required compared to now

- phase 0 (IBL, 2014) ≈ × 5
- phase 1 (2018) ≈ × 5-10
- phase 2 (2022) ≈ × 10-30

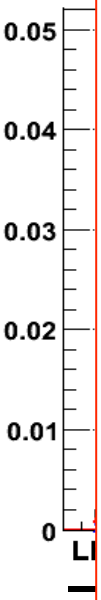


sLHC data rates

Hit inefficiency rises steeply with the hit rate

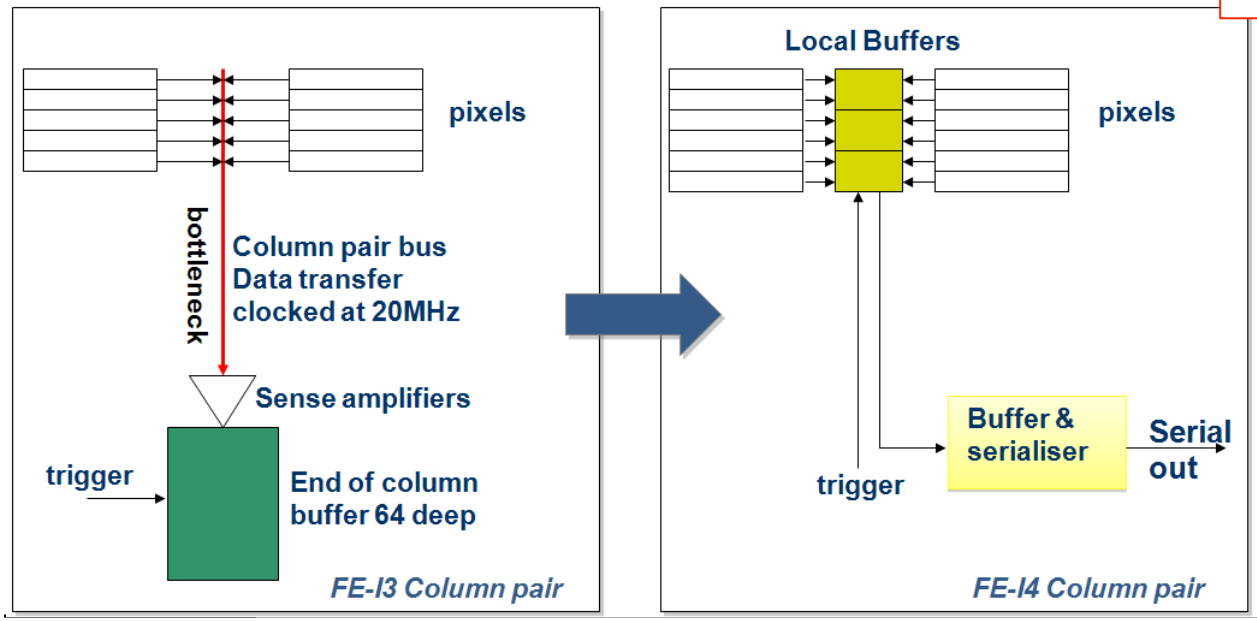
Bottleneck: congestion in (double) column readout

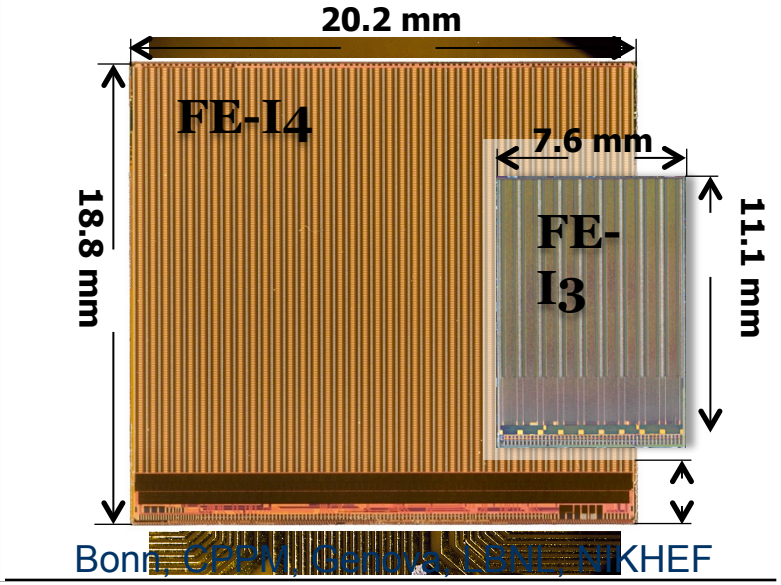
⇒more local in-pixel storage (130 nm !)
>99% of hits are not triggered
⇒ don't move them -> not blocking



- IBM (130 nm)
- 70 Million transistors
- 26880 pixels (50 x 250 μm$^{2)}$
- lower noise than FE-I3
- lower threshold operation
- higher rate compatibility
- radiation hard to >250Mrad

- working horse for future pixel R&D

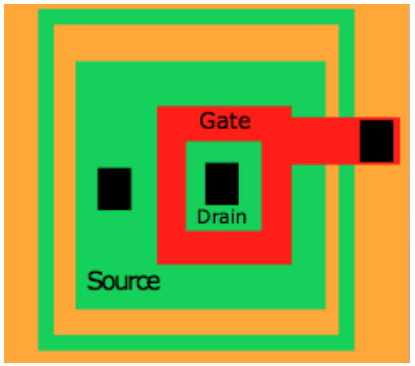




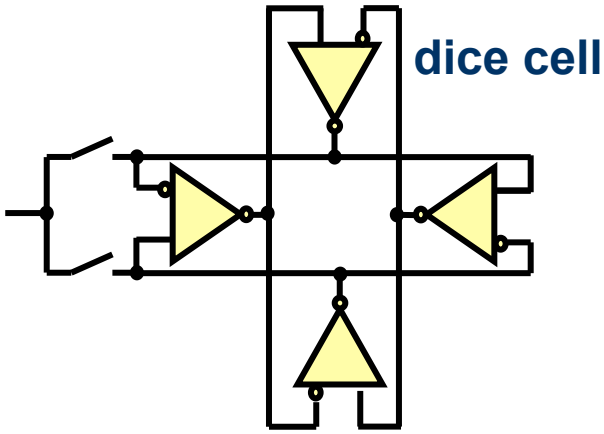
Bonn, CPPM, Geneva, LBNL, NIKHEF

Radiation hardness to sLHC fluences $\gg 10^{15}$ cm^{-2}

- Chips are radhard … provided that …
  - deep submicron technology used (130 nm -> 65 nm)
  - “round” transistors used at critical nodes
  - SEU tolerant digital logic is used



round FET



Radiation hardness to sLHC fluences $\gg 10^{15}$ cm^{-2}

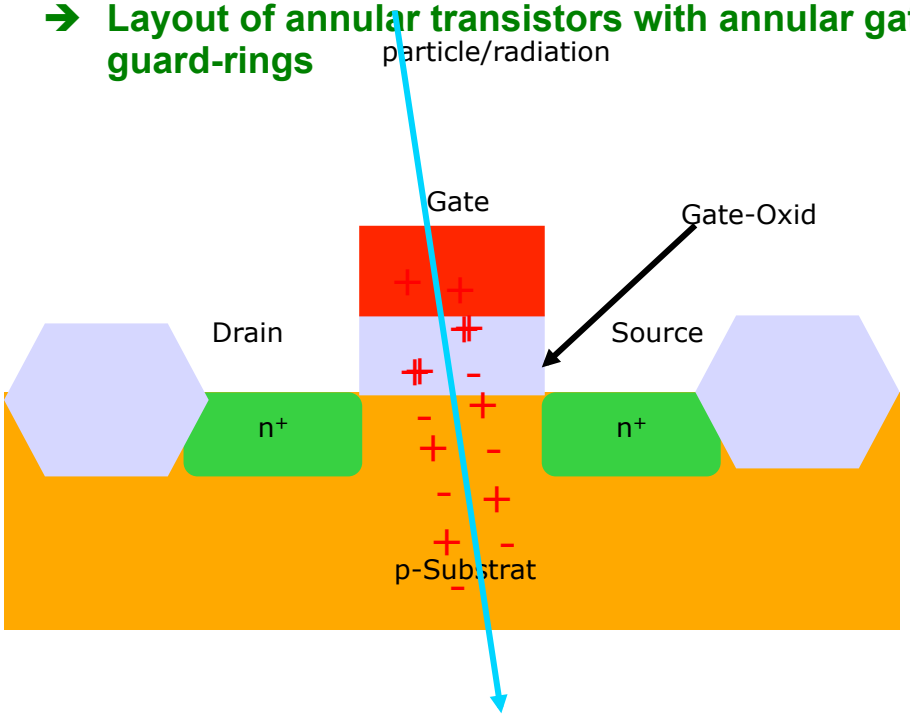
Effects: **generation of positive charges in the SiO_2 and defects in Si - SiO_2 interface**

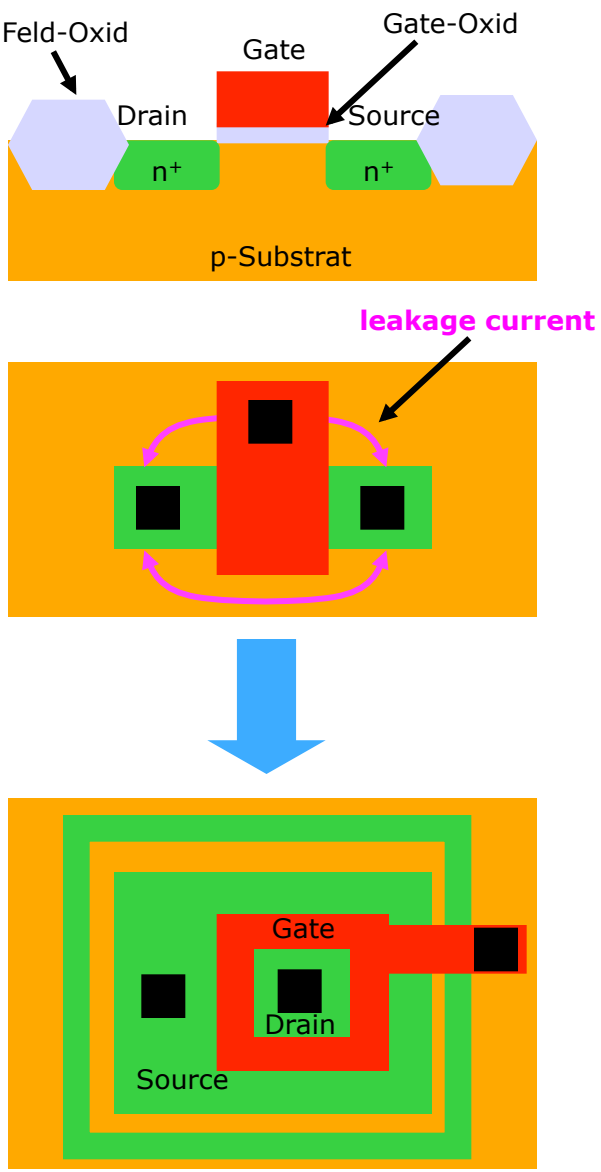
1. Threshold shifts of transistors

➔ **DSM CMOS technologies with small structure sizes (≤ 0,35 µm) and thin gate oxides (d_{ox} < 10 nm) → holes tunnel out**

2. Leakage currents under the field oxide

➔ **Layout of annular transistors with annular gate-electrodes + guard-rings**





Radiation damage to the FE-electronics … and cure

radiation induced bit errors

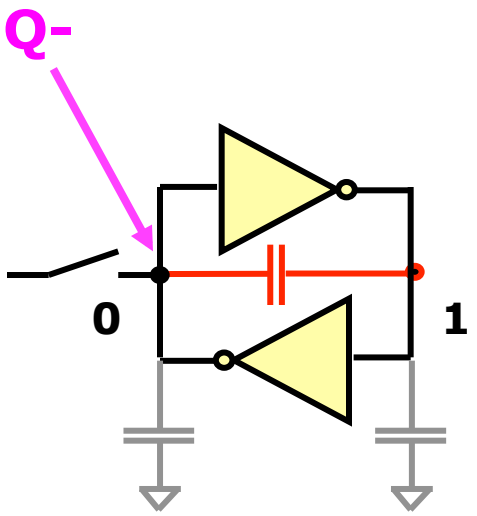
("single event upsets" SEU)

large amounts of charge on circuit nodes
- by nuclear reactions, high track densities -
can cause "bit-flip"

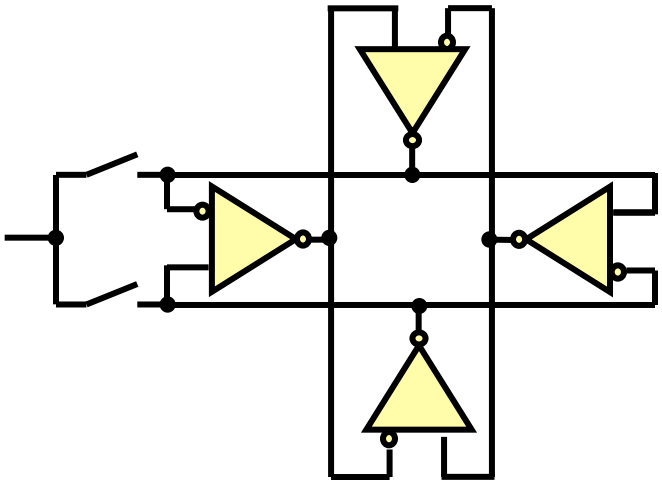
2 examples of error resistant logic cells

➔ **enlarge storage capacitances in SRAM cells:**
$Q_{crit} = V_{threshold} \cdot C$

➔ **storage cells with redundancy (DICE SRAM cell)**

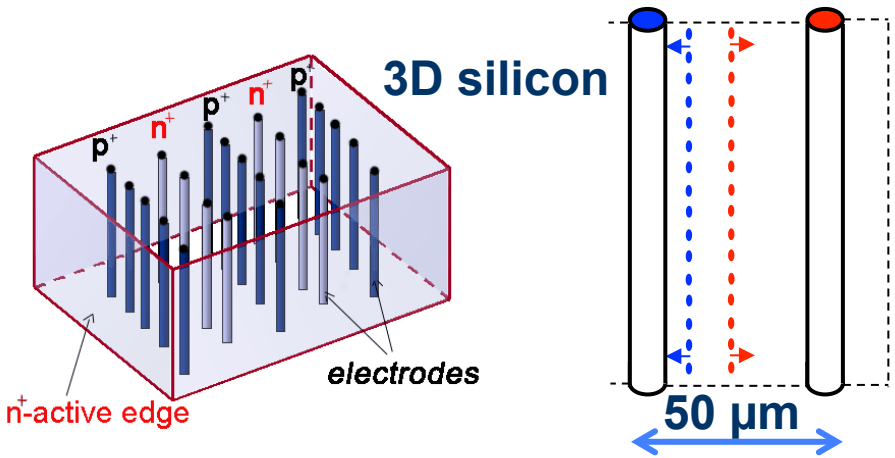


standard SRAM cell

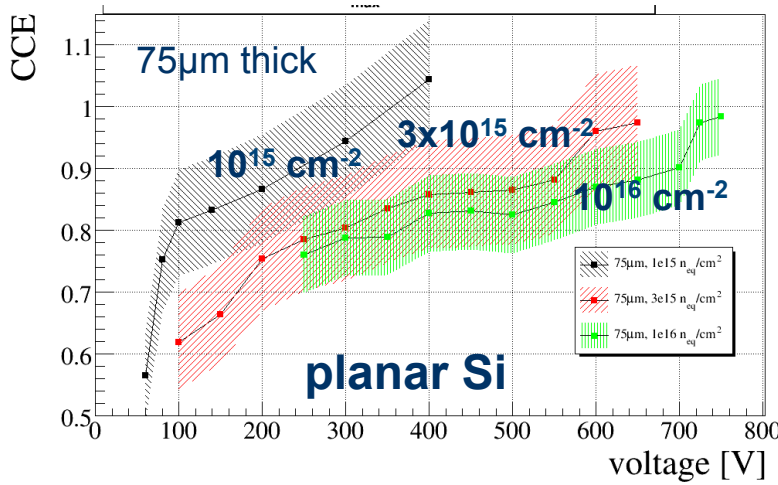

SEU tolerant DICE SRAM cell

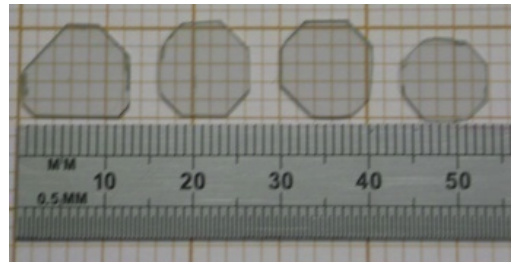
Radiation hardness to sLHC fluences $\gg 10^{15}$ cm^{-2}

- Sensors are not radhard, unless …
  - high voltages are applied (planar Si)
  - special geometries are used (3D-Si)



  - intrinsic radhard materials are used (like diamond)

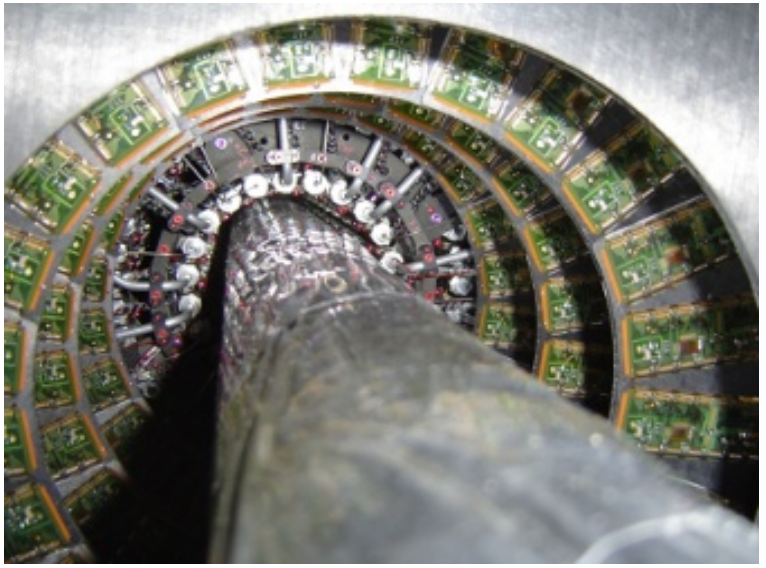


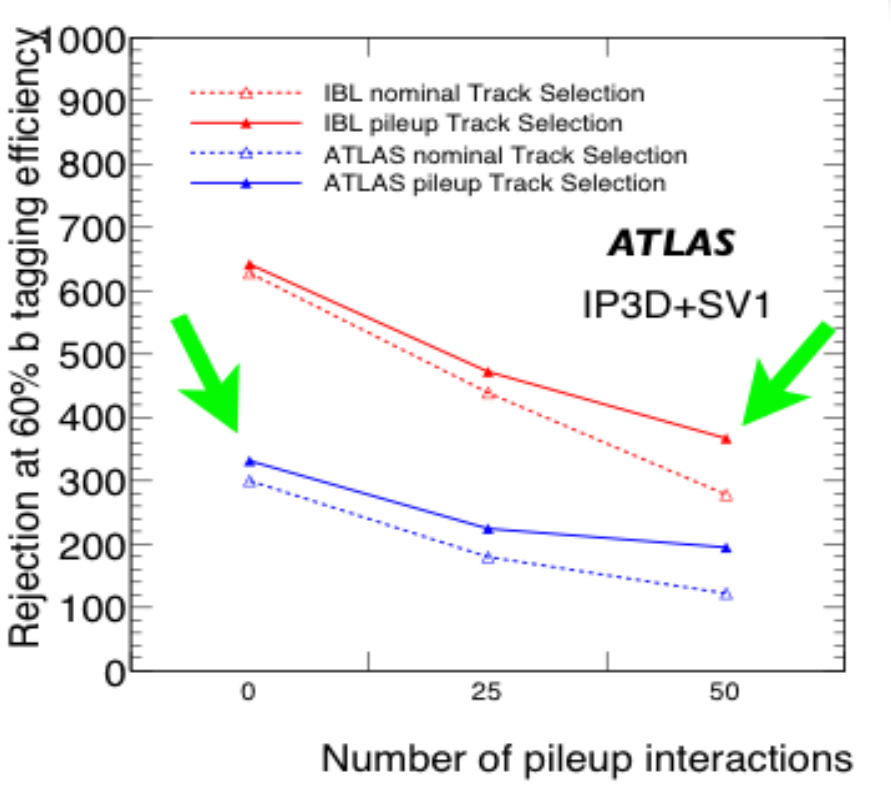


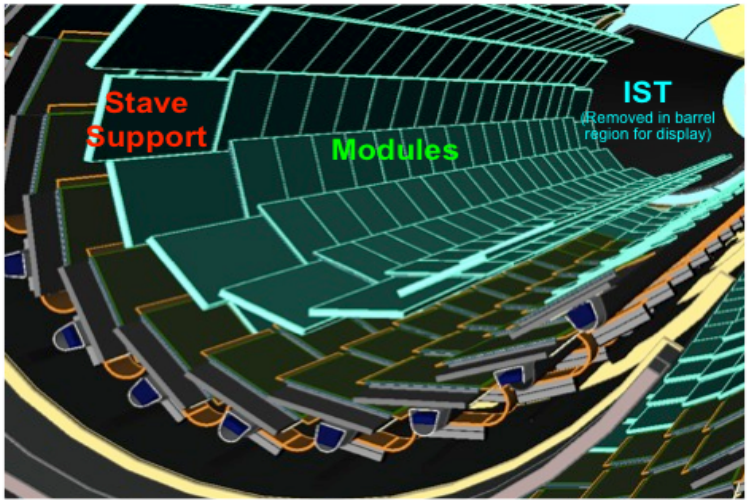
both, 3D-Si and diamond are used as pixel modules in ATLAS IBL/DBM projects

The Insertable B-Layer (2013/14)

- 4th layer
- **closer to IP (5.05 cm → 3.4 cm)**
- **smaller pixels (50 x 250 μm²)**
- **better sensors, better R/O chip**
- more robust tracking
- **better performance**



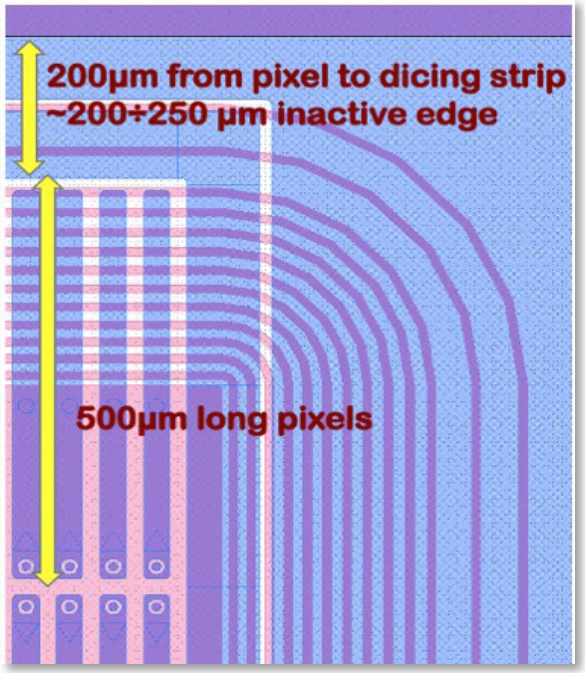




New pixel sensor technologies (IBL and → future)

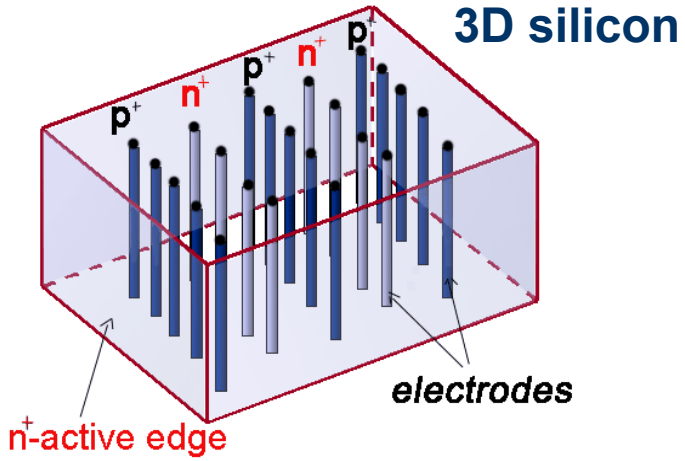
Planar Slim Edge Sensors (CiS)

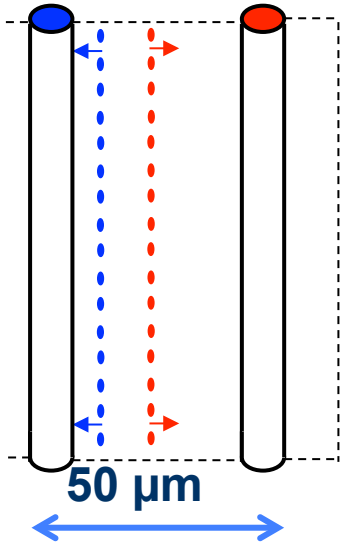
- oxygenated n-in-n silicon
  200 µm thick
- minimize inactive edge to only
  215 µm by shifting guard-ring underneath pixels

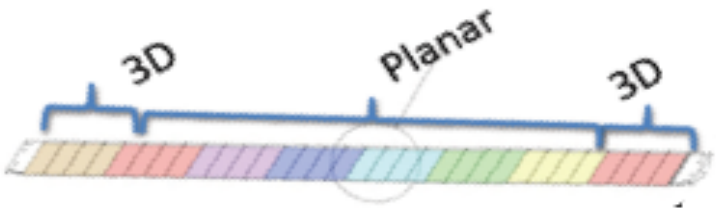


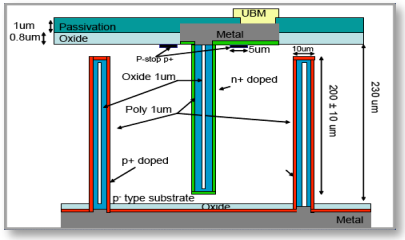
3D Slim Edge Sensors (2 companies: FBK and CNM)

- partial 3D: electrodes etched from both sides
- p-type substrate; 230 µm thick
- 200 µm slim inactive edge



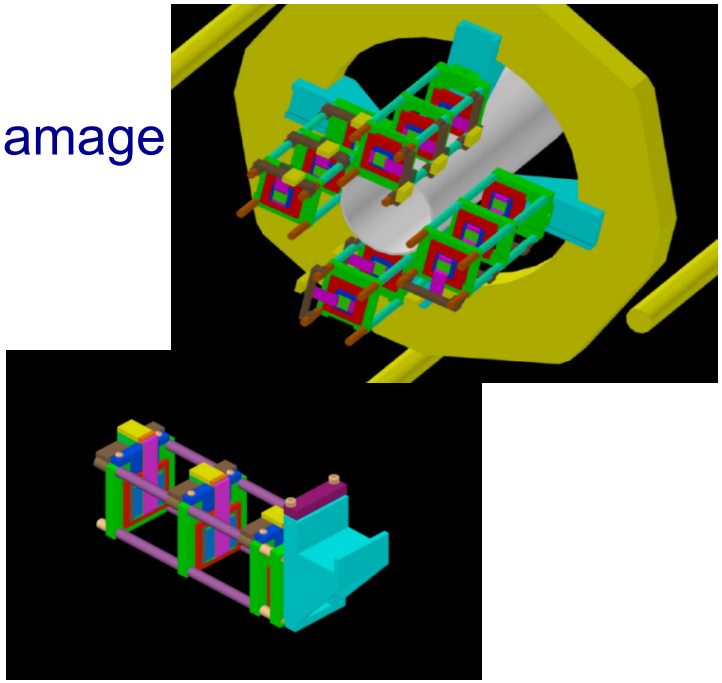


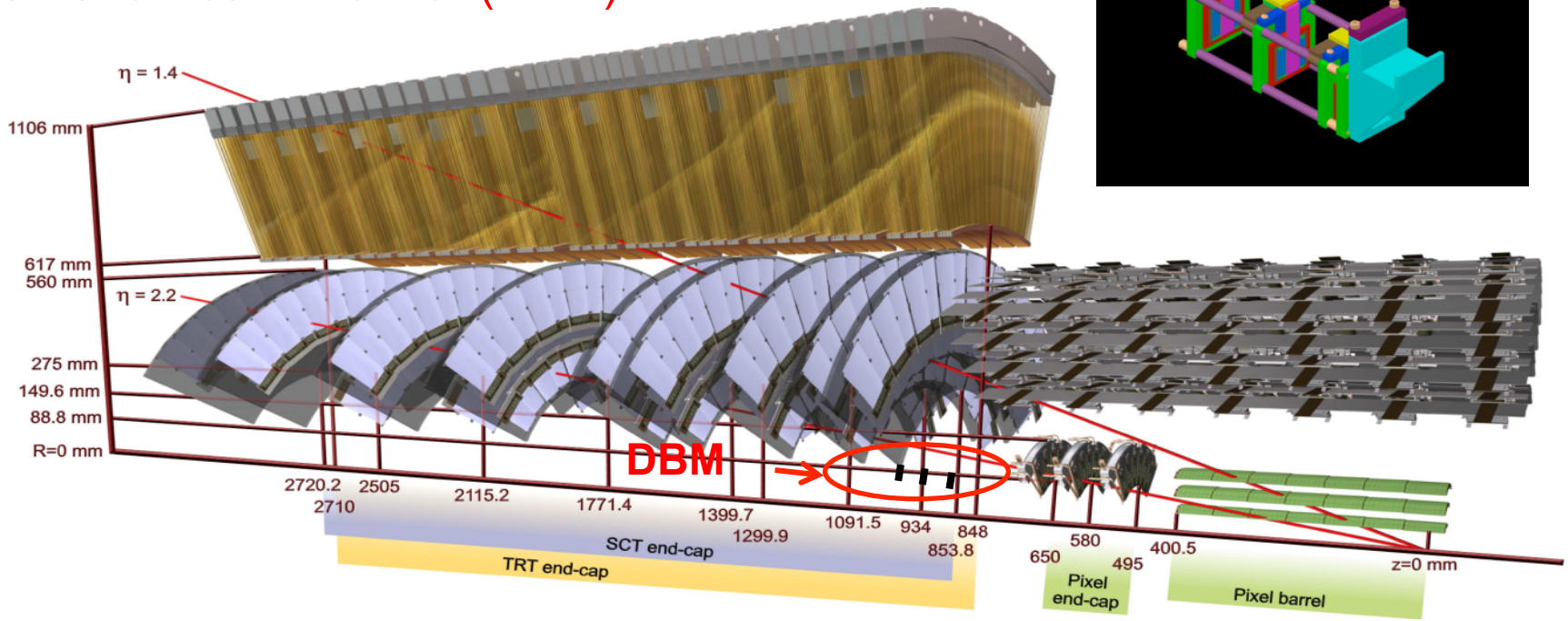




DBM – Diamond Beam Monitor

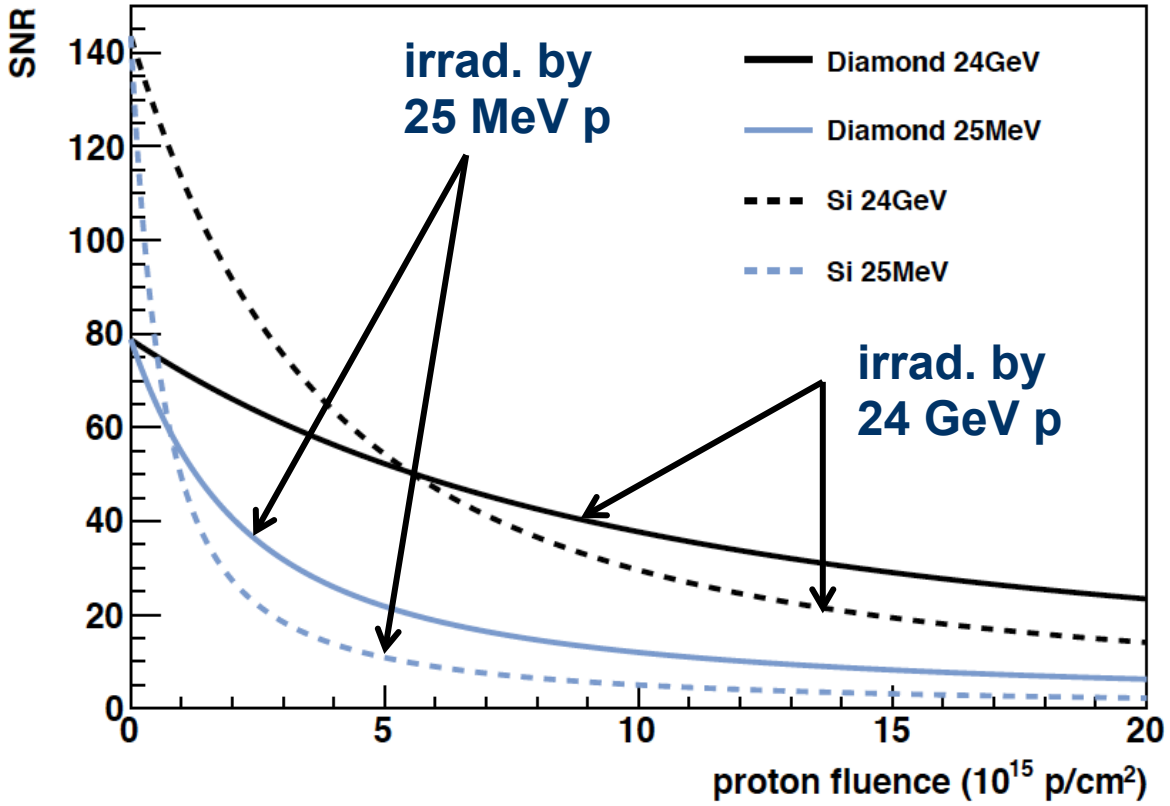
- radiation hard due to
  - 5x larger band gap than Si ⇒ no leakage current
  - strong lattice (x2 stronger than Si) ⇒ less NIEL damage
- low Z
- first pixel use in ATLAS:
  Diamond Beam Monitor (DBM)





Signal to Noise Ratio comparison: diamond vs. planar Si

assumed thickness of sensors: 200 µm



C_D (Si) = 120 fF
C_D (diam.) = 33 fF

——— diamond

- - - - - - silicon

(Semi)- Monolithic Detectors

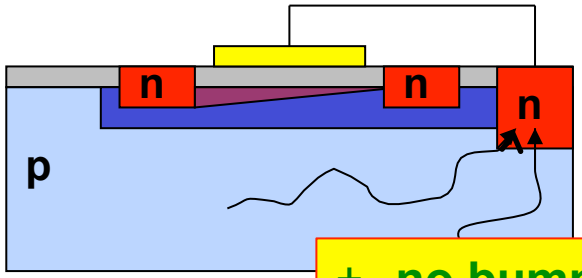
+ **really low mass**
+ **(almost) no interconnection (but need few ASICS with large pitch > 150µm)**
– **slow (frame readout, rolling shutter)**

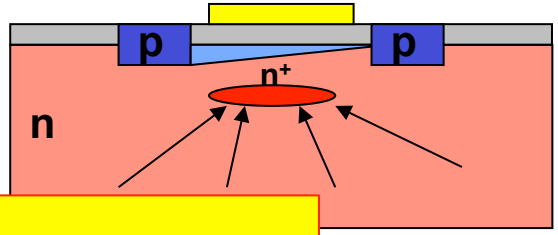
CMOS Sensors (MAPS) -> STAR
DSM CMOS with epi-layer as sensor

+ ‘standard CMOS’ process
+ CMOS circuitry, but limited to NMOS
– small signal, slow collection
– area limited by chip size

DEPFET -> Belle II
FET on fully depleted bulk

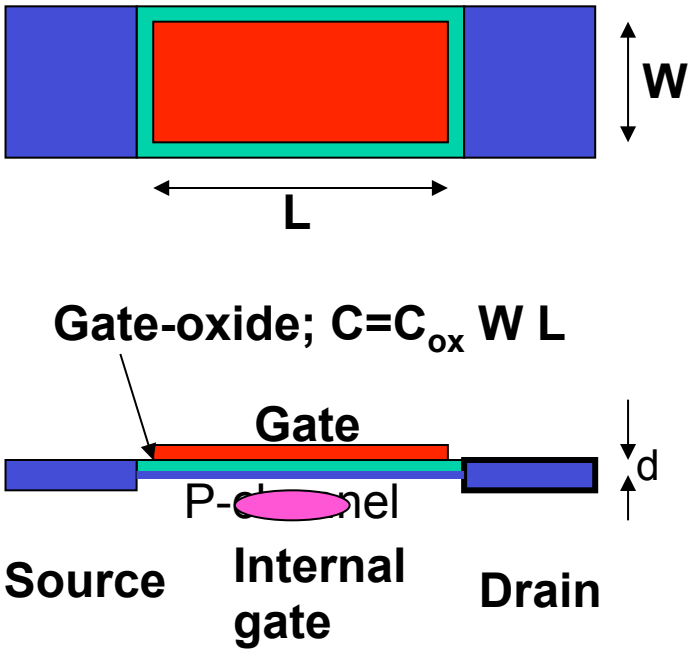
– non standard double-sided process
– simple, one stage amplifier
+ large signal, fast collection
+ wafer size sensors possible





+ **no bump bonding**
+ **very thin (50 µm resp. 75 µm) → ~0.2% x/X_0**
+ **small pixels (20x20 resp. 50x75 μm^2)**
+ **low power → less cooling**
– **radiation hardness**
– **R/O speed**

How does a DEPFET work?



A charge q in the internal gate induces a **mirror charge** αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$ which in turn **changes the transistor current I_d.**

q

FET in saturation:

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right)^2$$

I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
W,L: Gate width and length
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

Conversion factor:

$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha\mu}{L^2}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right) = \alpha\sqrt{2\frac{I_d\mu}{L^3 W C_{ox}}}$$

$$g_m : g_q = \alpha\frac{g_m}{WLC_{ox}} = \alpha\frac{g_m}{C}$$

DEPFET

Each pixel is a p-channel FET on a fully (sidewards) depleted bulk

A deep n-implant creates a potential minimum for electrons under the gate ("internal gate")

Signal electrons accumulate in the internal gate and modulate the transistor current (g_q ~ 400 pA/e^-)

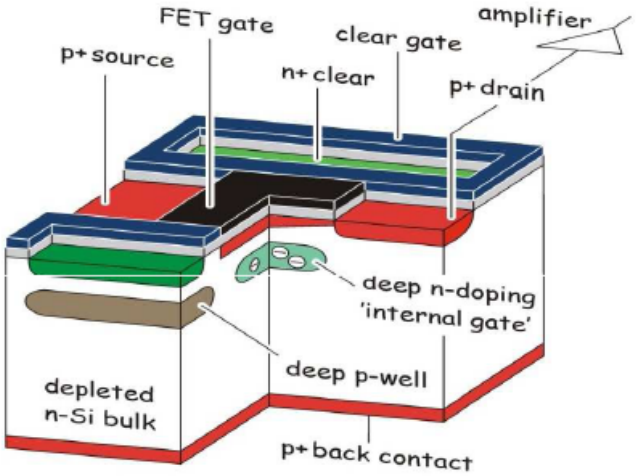
Accumulated charge can be removed by a clear contact

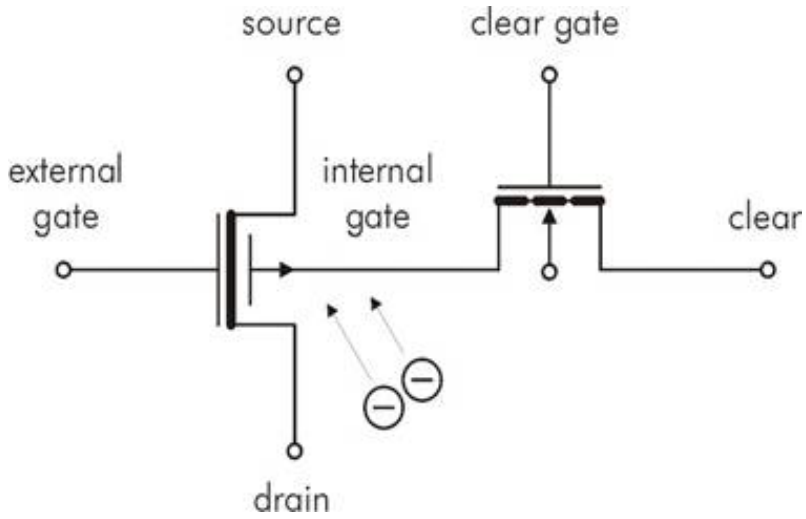
Fully depleted ⇒ large signal, fast signal collection

Low capacitance, internal amplification: => low noise

High S/N even for thin sensors (75 µm)

Rolling shutter mode (col. parallel) for matrix operation
⇒ 20 µs frame readout time
⇒ Low power (only few lines powered)





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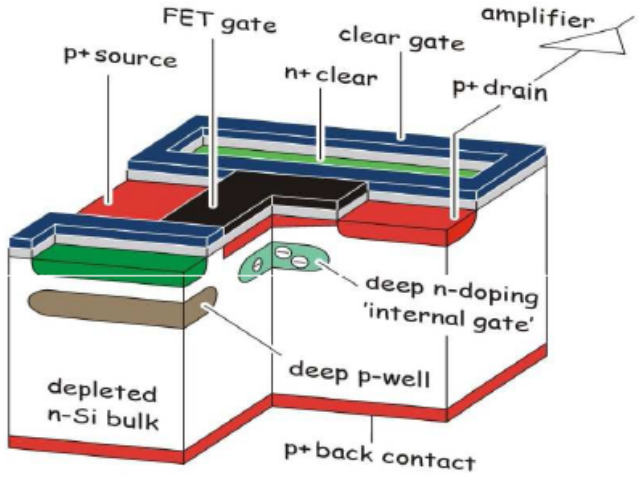
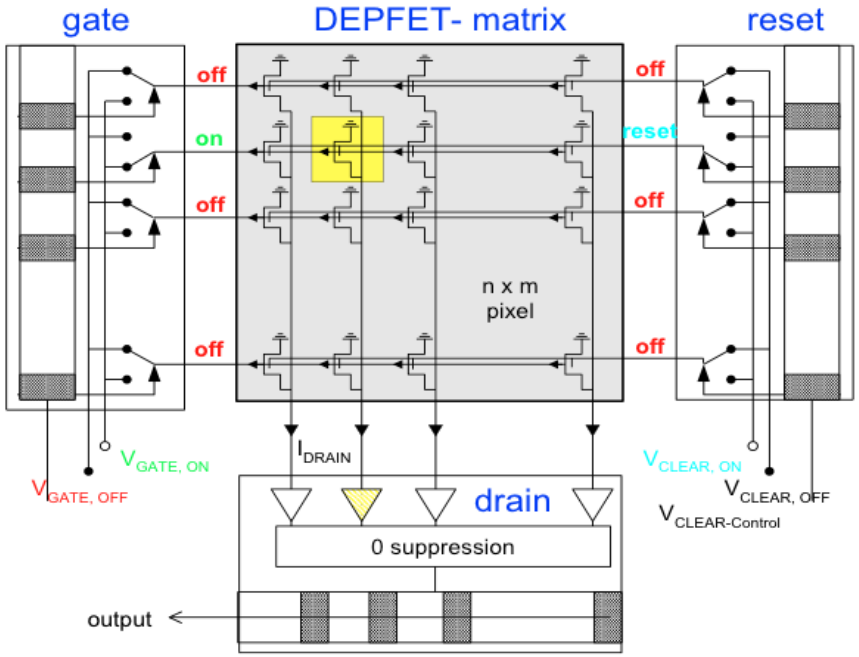
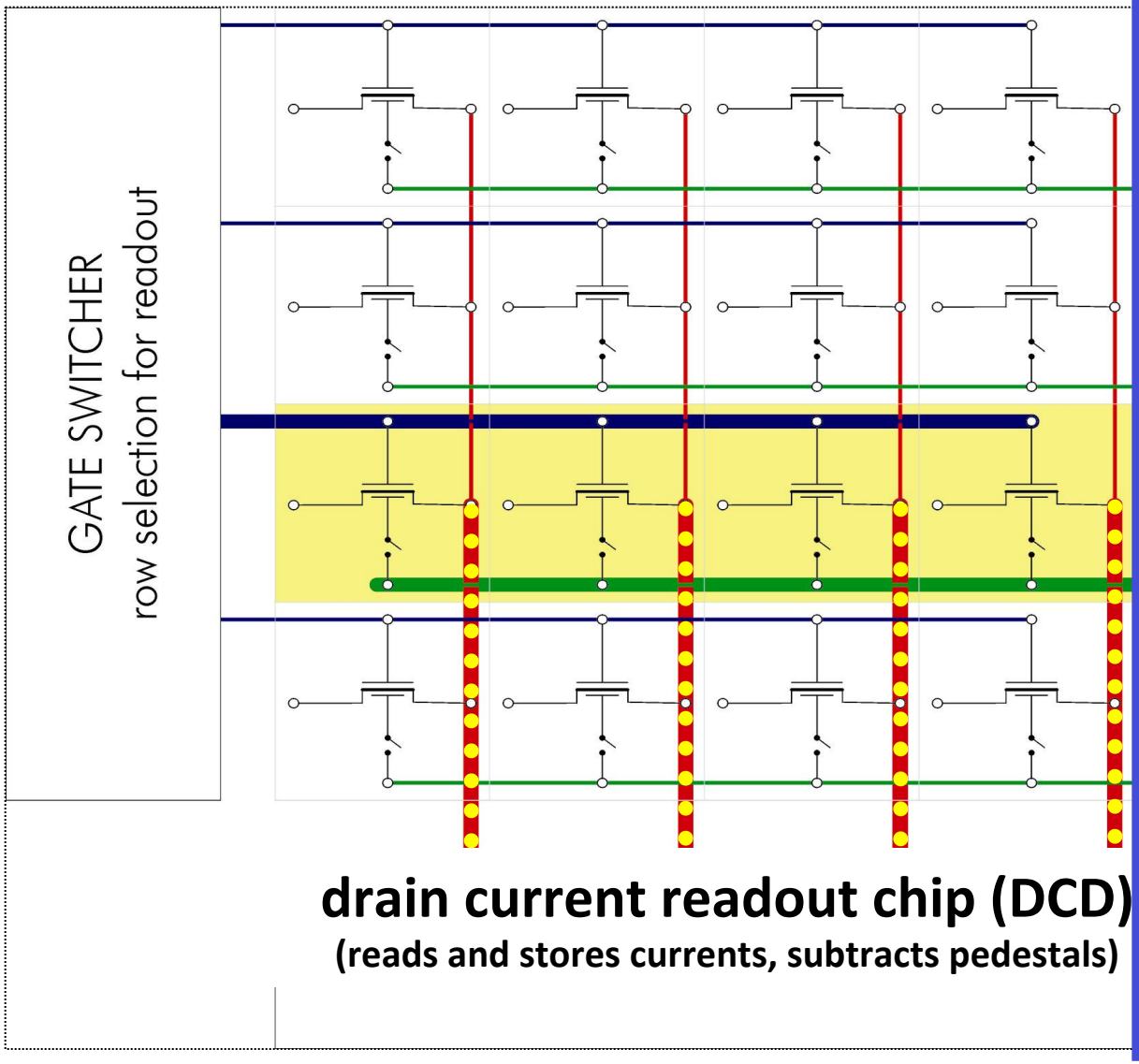




DEPFET pixels: „rolling shutter“ frame R/O



- **1 row active**

  (1) read signal + ped current

  (2) CLEAR

  (3) read pedestal current

  merge currents: (1) – (2)

- **all other rows OFF**

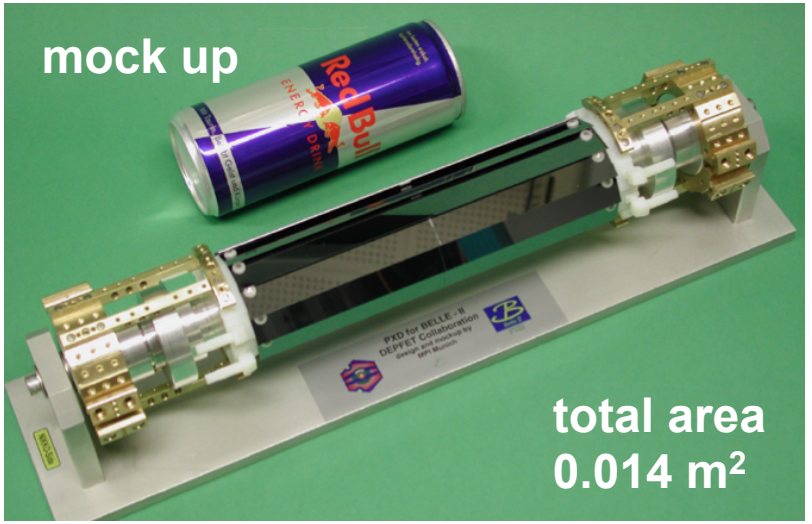
  still active for signals

→ low power !

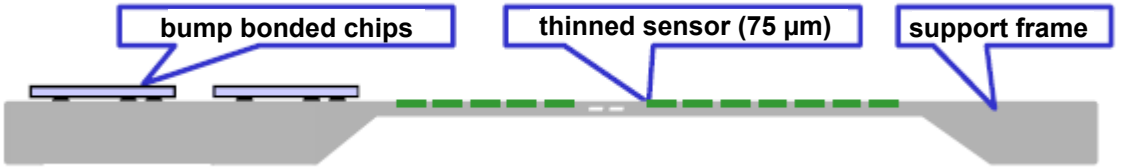
(60 mW/cm²)

DEPFET PXD @ Belle II @ SuperKEKB

2-layer pixel vertex detector (PXD)

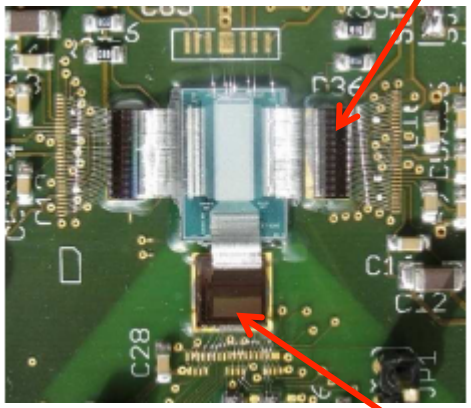


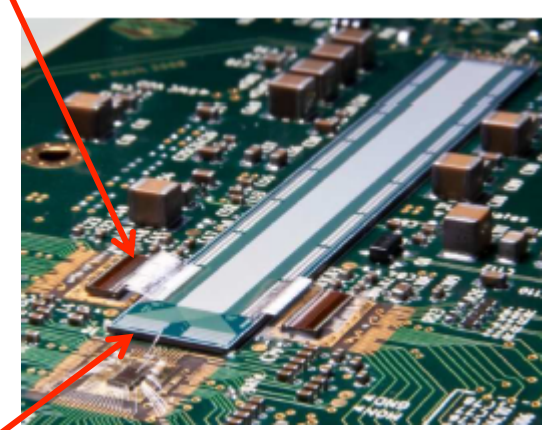
thinned by backside etching, leaving a frame



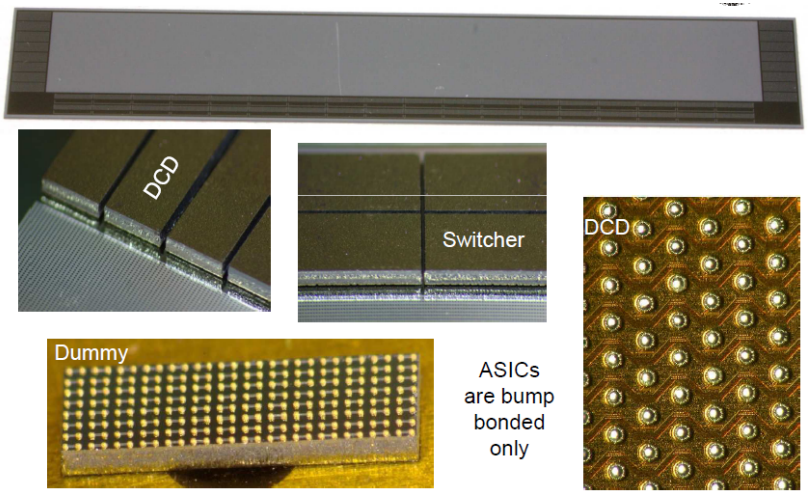
…. on their way to the final module
sensor + switcher + DCD + DHP

ladder control ICs





R/O ICs

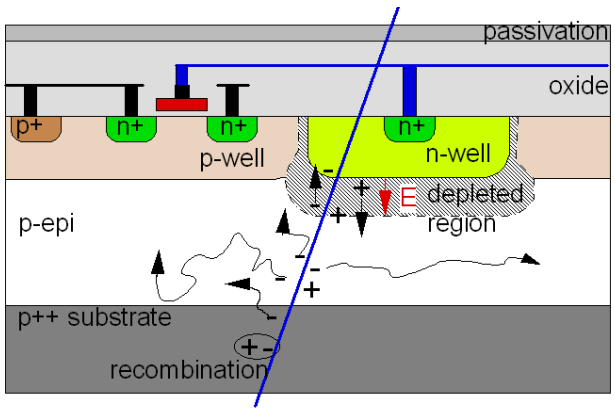


Monolithic Pixel Sensors … an attempt of a sorting (1)

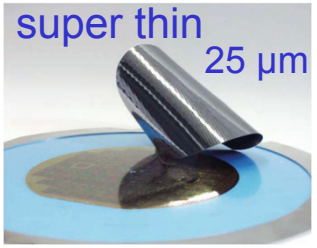
❑ MAPS = Monolithic Active Pixel Sensor

use thick epi-Si layer in some CMOS processes for sensing

→ STAR @ RHIC



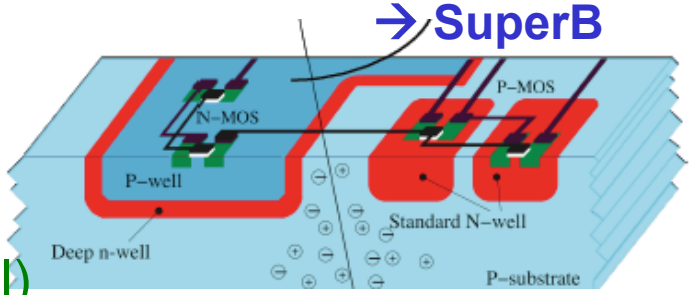
can be made super thin

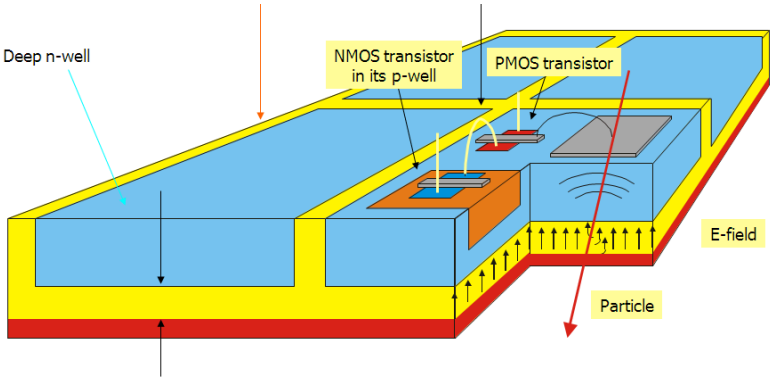


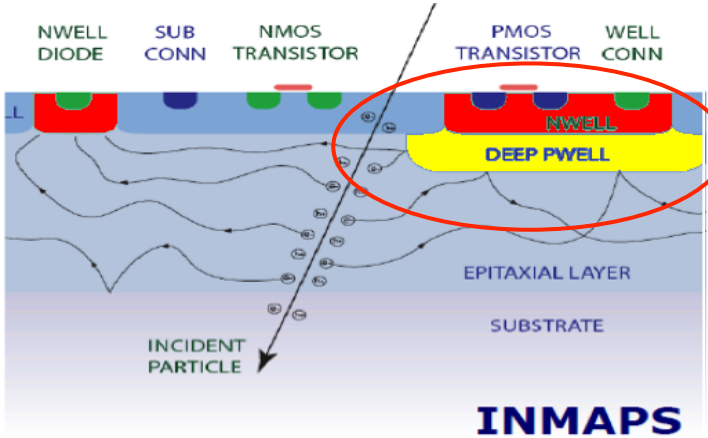
- (1) Q - collection by diffusion (small, slow)
  (2) only nMOST in active area, no pMOST
  (3) not radhard (to LHC standards)

- several developments to improve (1),(2)
  - ➢ large deep n-well, pMOST on the side (65nm)
  - ➢ shield PMOS-nwell by a pwell (quadrupel well)
- developments to improve (1),(2),(3)
  - ➢ higher bulk resistance (-> depletion -> better Q-coll)
  - ➢ HV CMOS (AMS 350 nm -> 180 nm)

→ SuperB







I. Peric

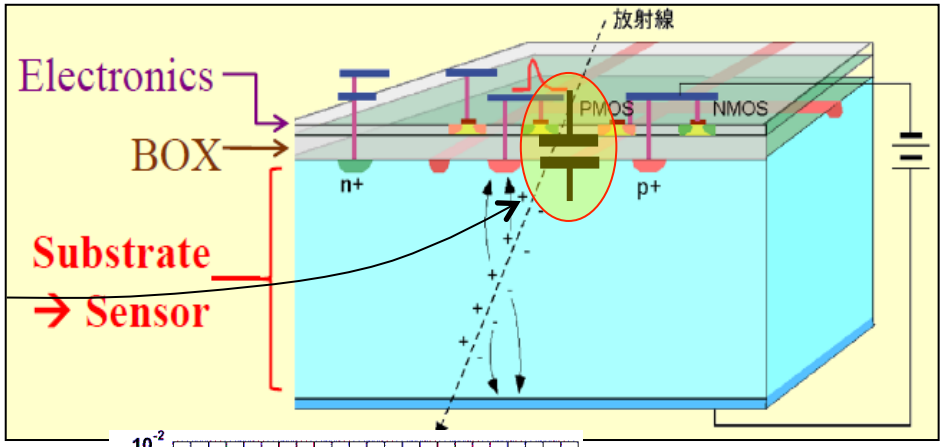
Monolithic Pixel Sensors … an attempt of a sorting (2)

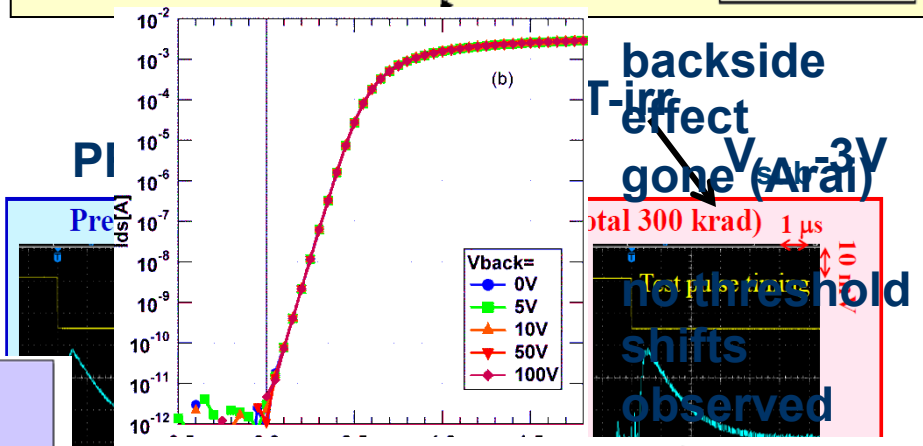
❑ SOI pixels (Silicon On Insulator)

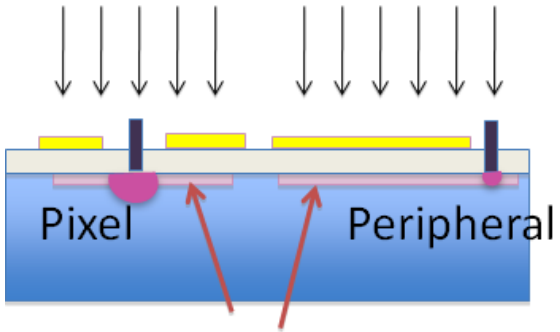
use depleted bulk for Q-collection coupled into CMOS layes separated from bulk by a thick buried oxide (BOX) layer (OKI, Japan)

- backgate effect “BOX is a capacitance”
- on irradiation holes are trapped in BOX

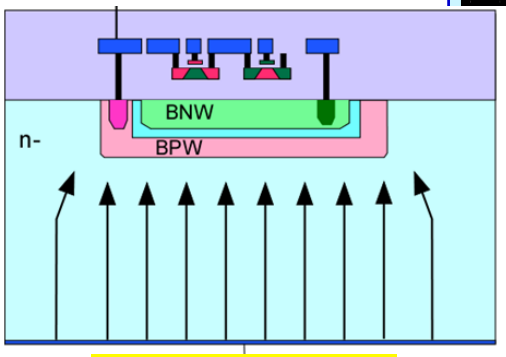
- several attempts to improve this
  - ➢ buried p-wells
  - ➢ nested wells
  - ➢ “double SOI” structures



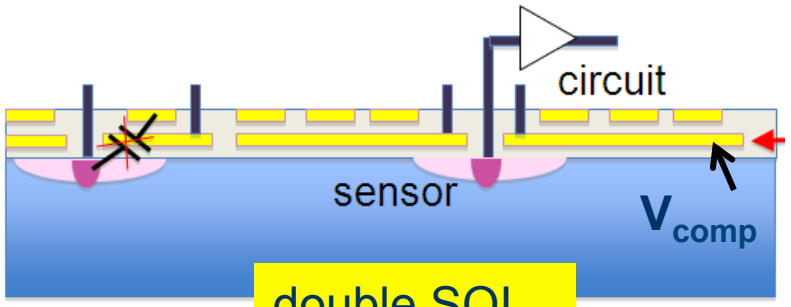




buried p-wells

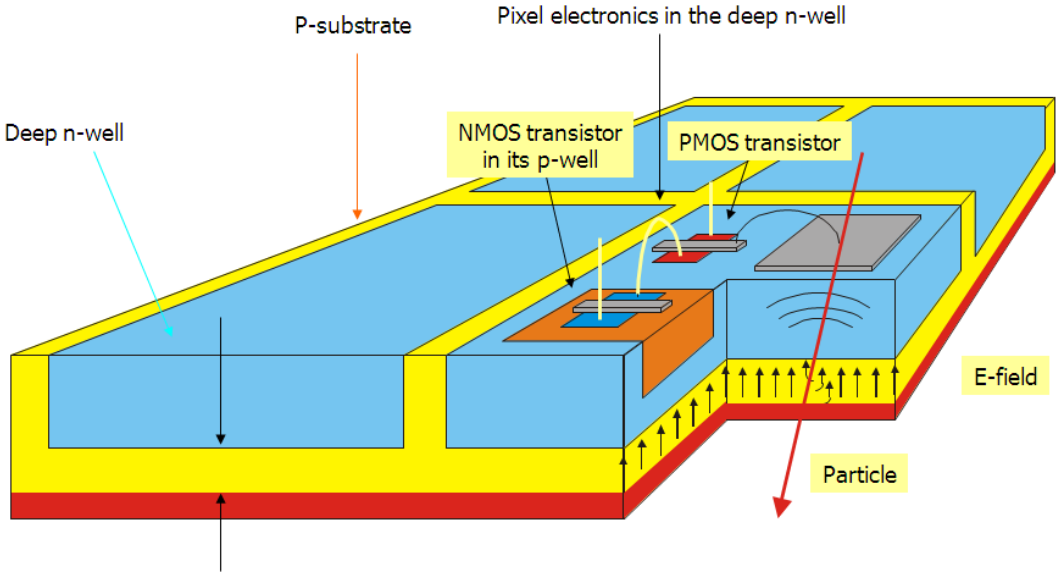


nested wells



double SOI

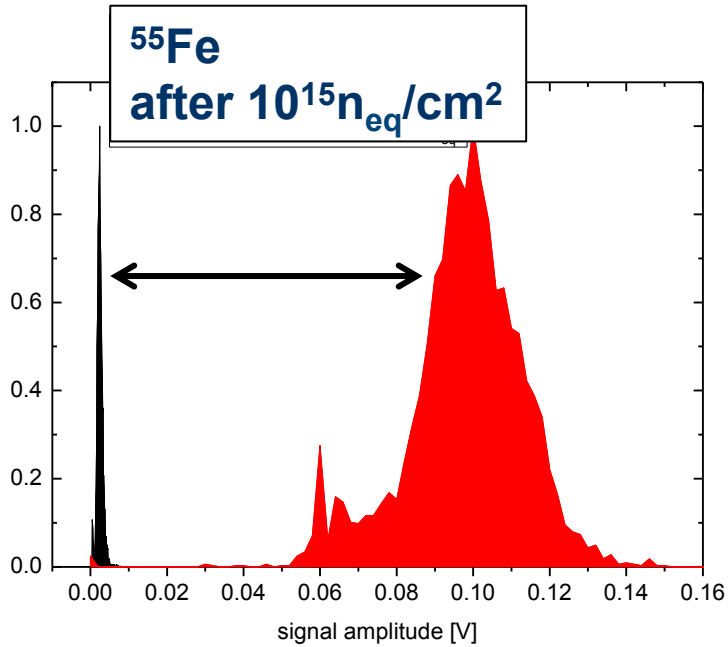
MAPS in HV technology



Ivan Peric, Heidelberg

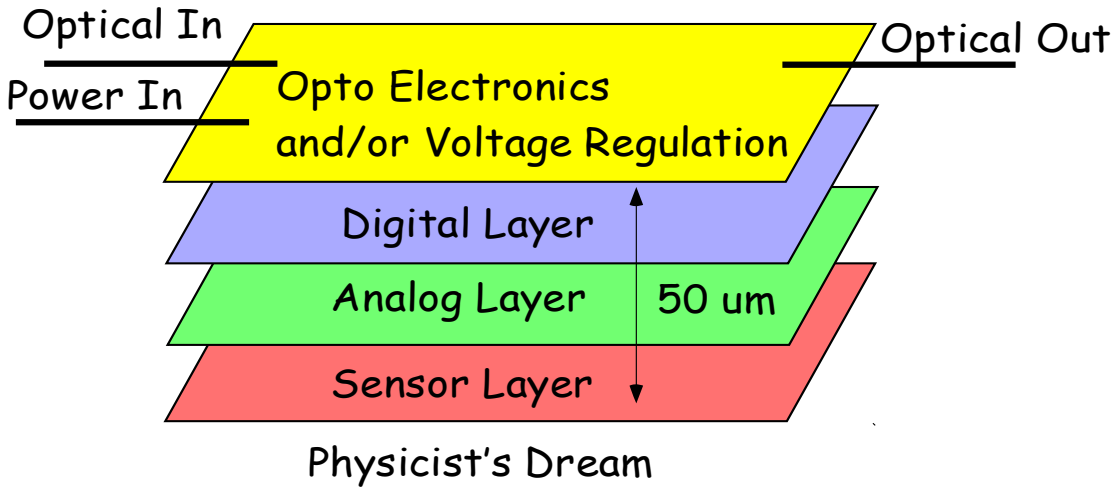
- **all electronics in same deep n-well (triple well), which also collects Q**
- **Q-coll. in depl. volume by drift in E**
- **350 nm AMS -> 180 nm IBM/AMS**

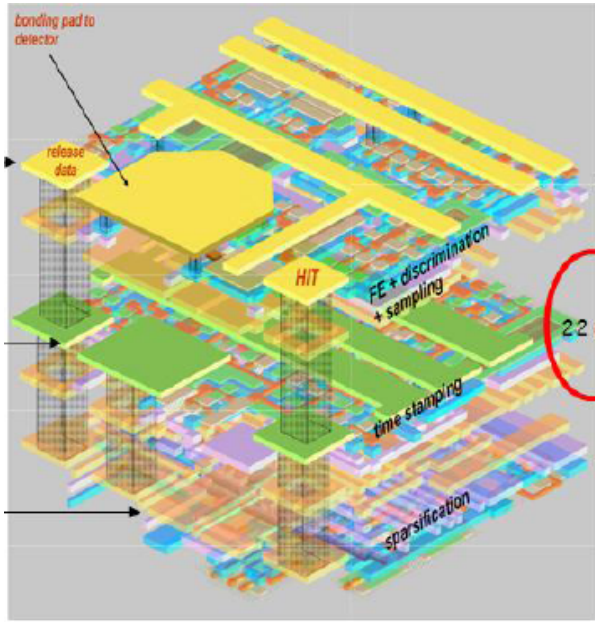
- CMOS in active pixel (but not high density)
- ~full charge collection efficiency
- high S/N (~100)
- small pixels (21x21 μm^2)
- fast
- radiation hard to 10^{15} n_{eq} / cm^2 or 300 Mrad
- ~10 μW / pixel
- rel. large collecting electrode (→ Q dep. bulk effect)
- cap. feedback -> CMOS logic gates -> x-talk



3D integration … a hot topic

"vias first" … various CMOS layers





3D integration promises

- higher granularity
- lower power
- large active over total area ratio
- low mass
- dedicated technology for each functional layer

prototypes with

- **OKI**
- **MIT LL**
- **Tezzaron/ Chartered**

CMOS vias first …

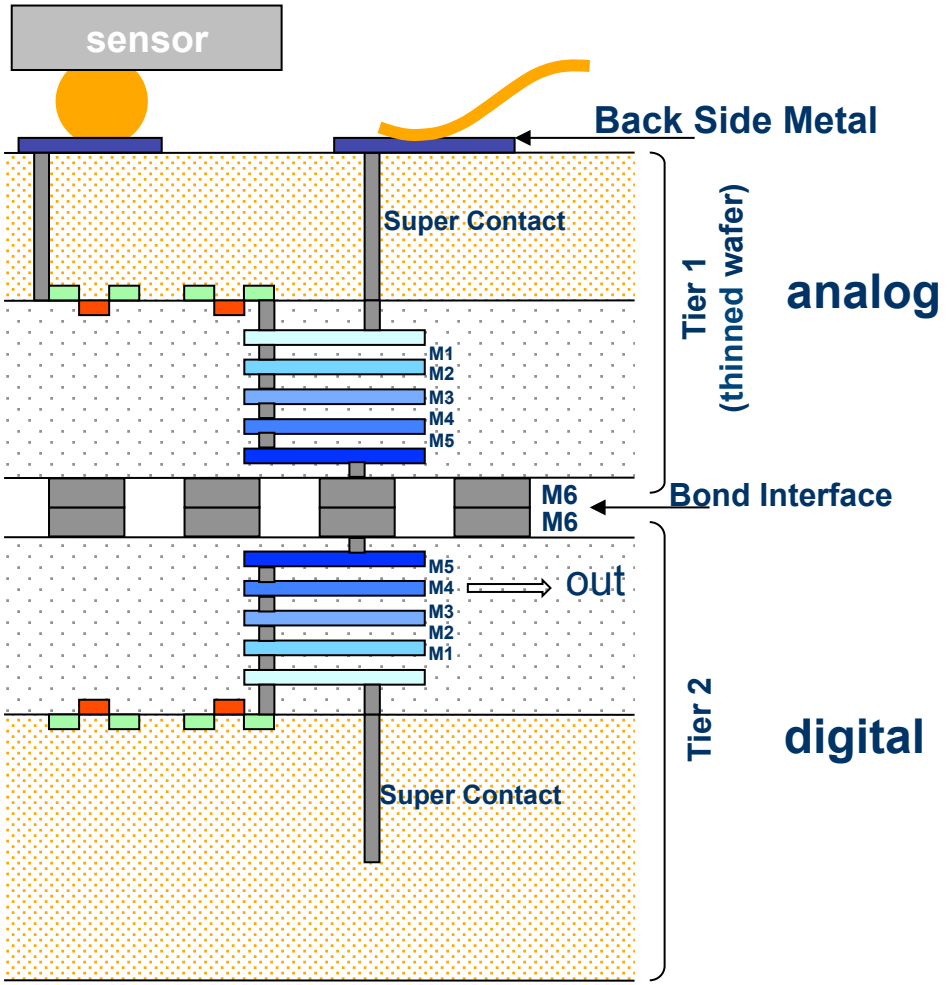
Tezzaron/Chartered 0.13 um Process

Large reticule (25.76 mm x 30.26 mm)

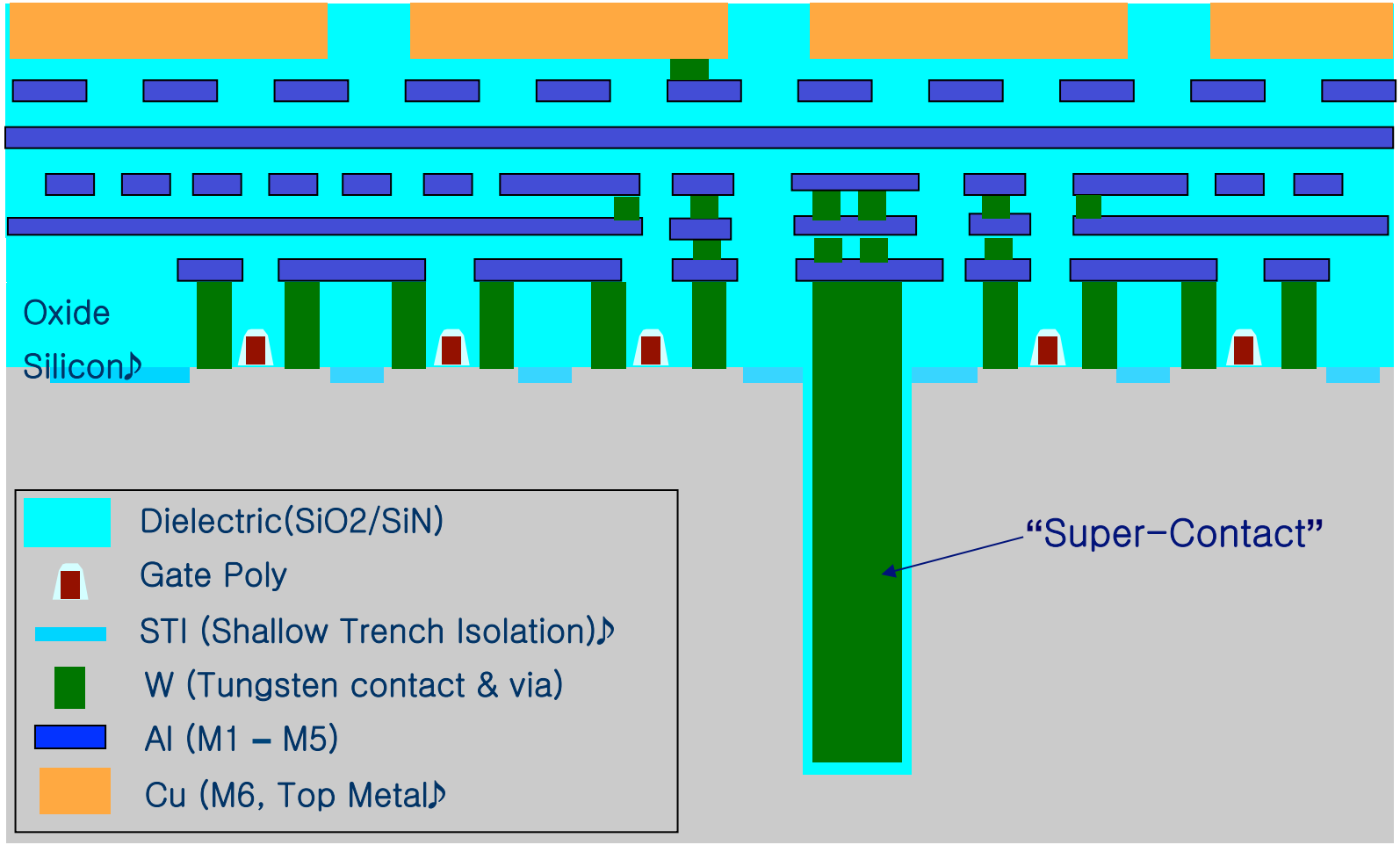
12 inch wafers

vias: 1.6 x 1.6 x 10 μm^3, 3.2 µm pitch

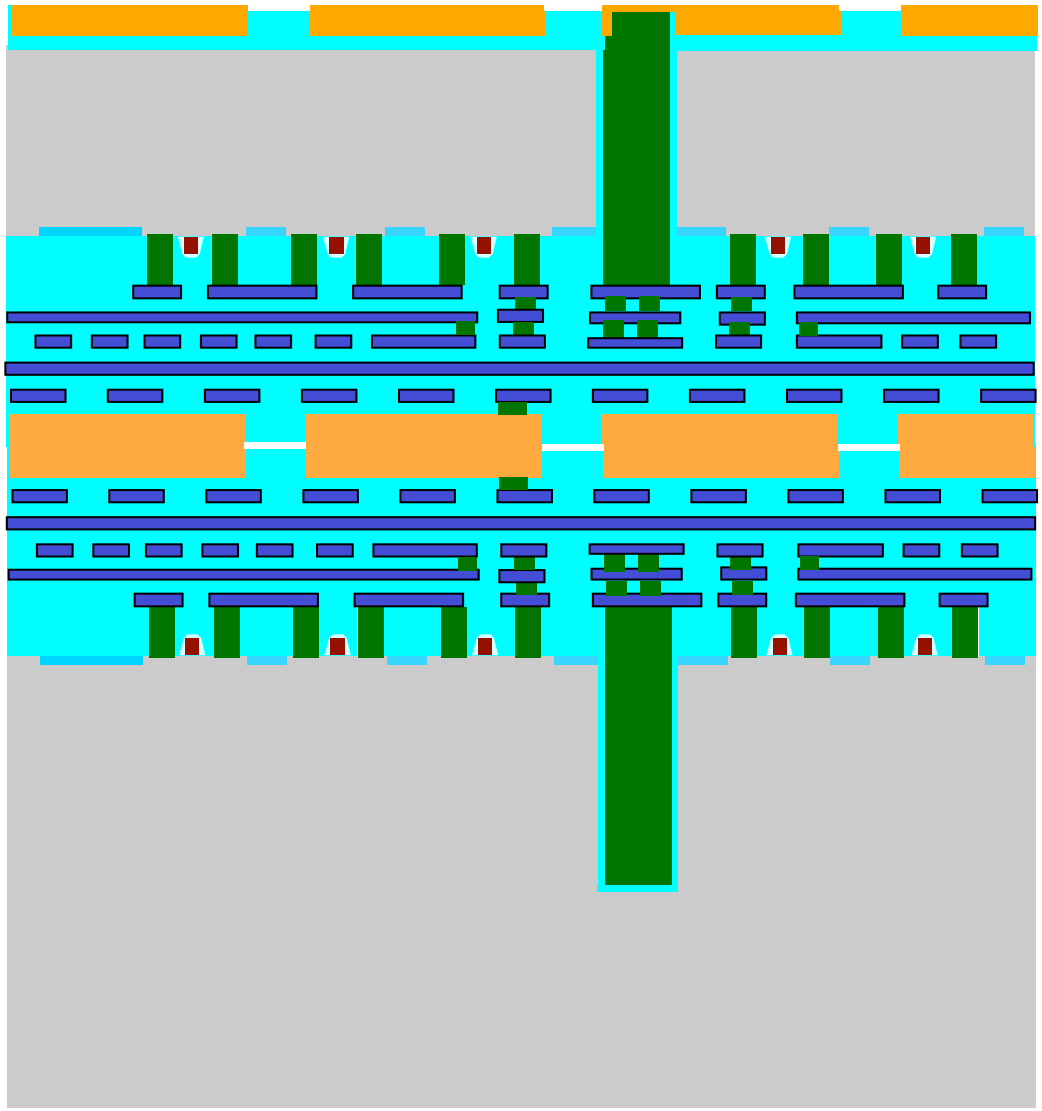
missing bonds: < 0.1 ppm



Wafer-Level Stacking

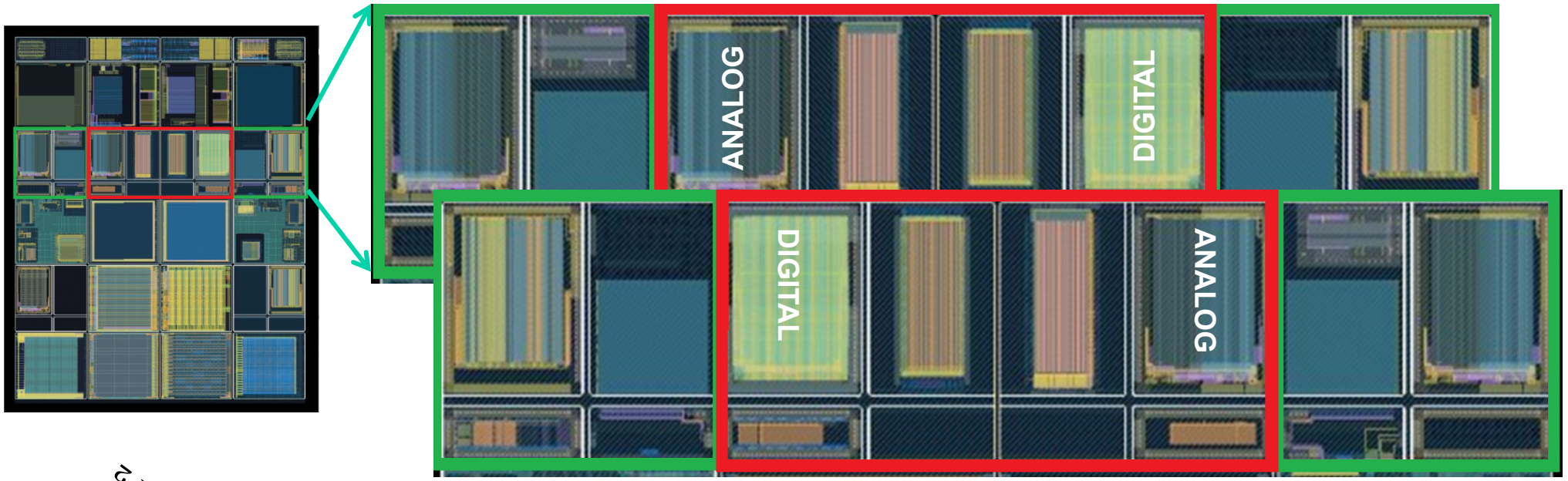


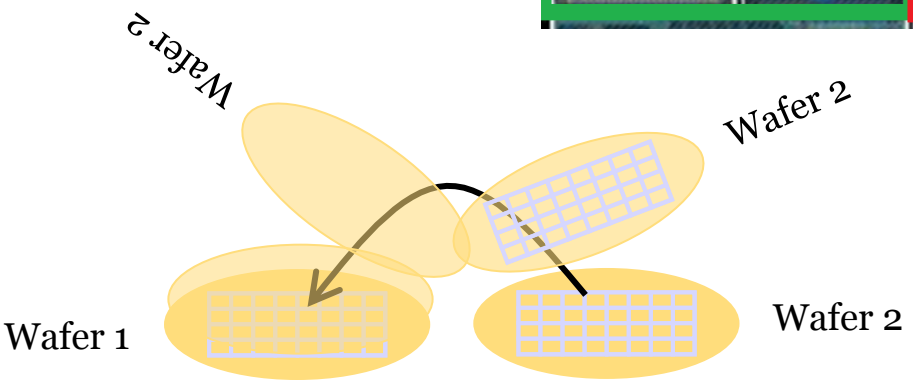
Next, Stack a Second Wafer (thin)

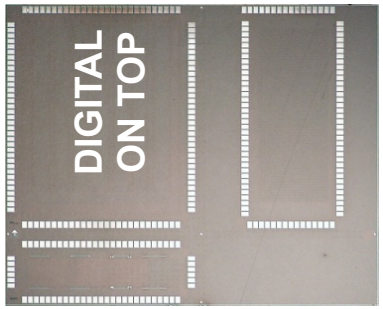


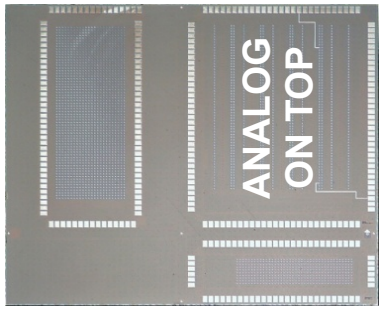
1st HEP 3D MPW

FNAL led (participants from Canada, France, Germany, Italy, Poland, USA).



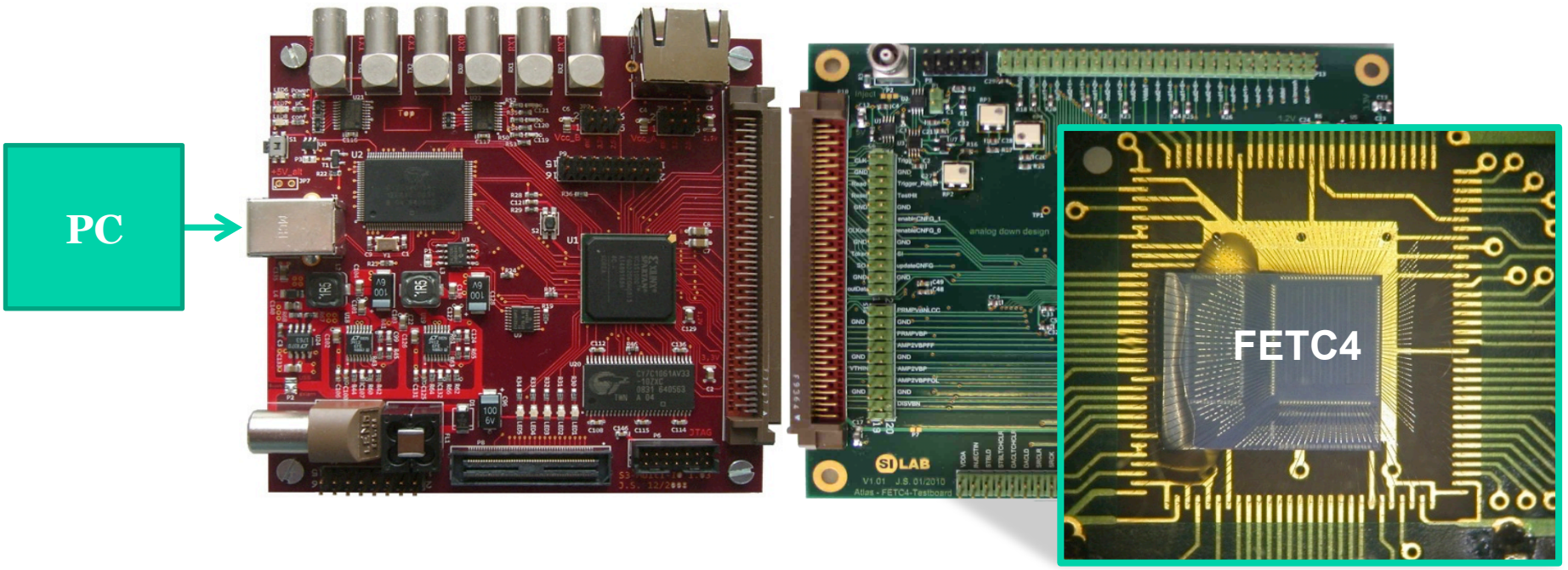






First ATLAS structures …

3D CMOS chip FETC4 bonded and tested.

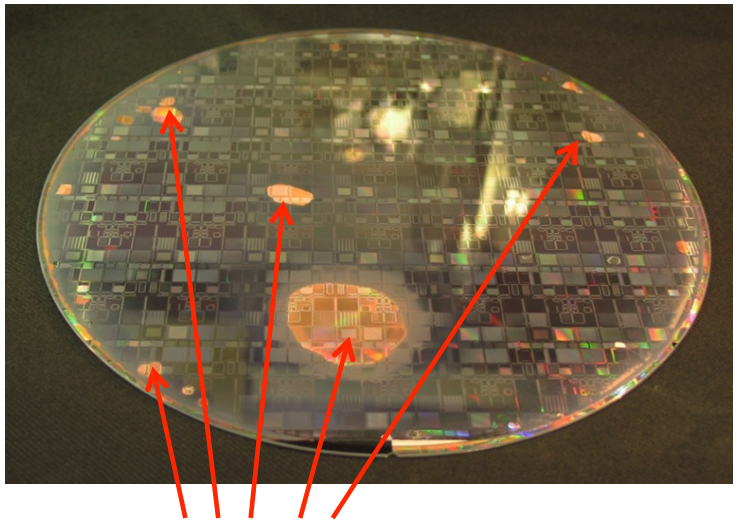


- **still some severe problems**
  - mostly alignment issues
- **analog tier thinned down to 12µm and operated stand alone**
  shows same noise behavior as un-thinned 2D

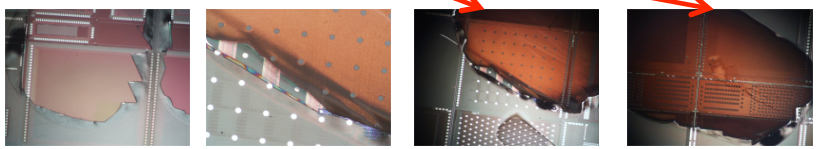
SI LAB
Silizium Labor Bonn

3D IC processing issues

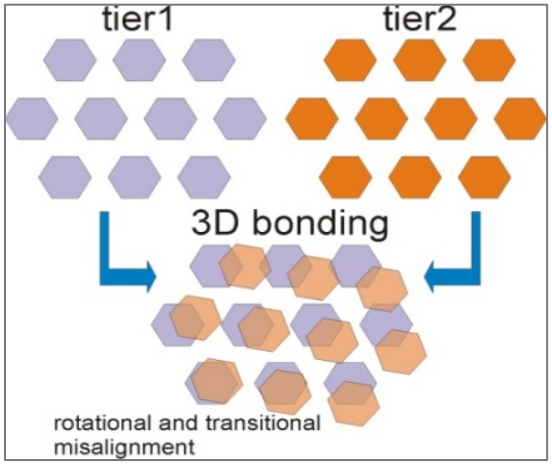
> 30 single wafer produced, only 3 bonded wafer pairs of poor quality have been accepted so far



Damages on the wafer &
Close up photographs



Bad electrical & mechanical connection due to misalignment of the tiers.

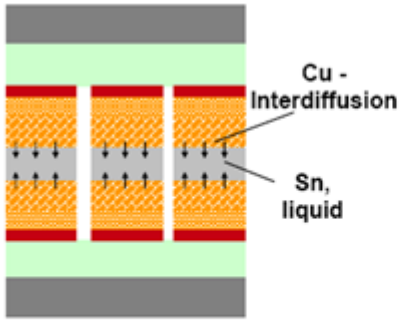


Bad mechanical connection between tiers lead to top tier removal during thinning process

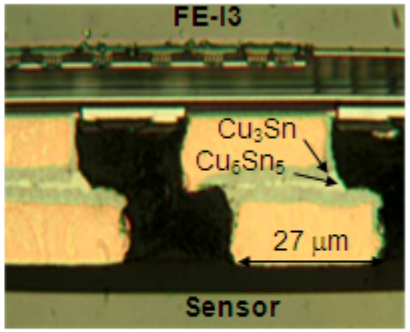
TSV drilled thinned down analog tier (12 µm !!!) works with marginal noise increase.

vias last … post processing

exploit: 3D integration for hybrid pixels, through silicon vias, wafer to wafer connection



Contact under Pressure
and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)



Formation of
Eutectic Alloy;
T_{melt} > 600 °C

Solid Liquid InterDiffusion (SLID)

(FhG EMFT Munich/MPI M)
alternative to bump bonding
but allows stacking of several layers

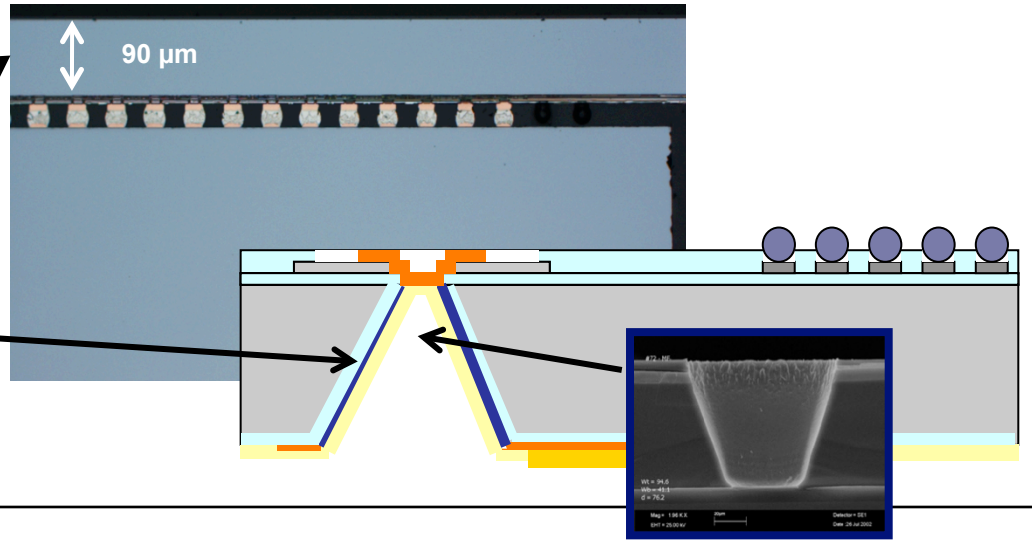
Through Silicon Vias (TSVs)

(FhG IZM Berlin / UBonn)

gain ~ 1% x/X_0 in ATLAS with

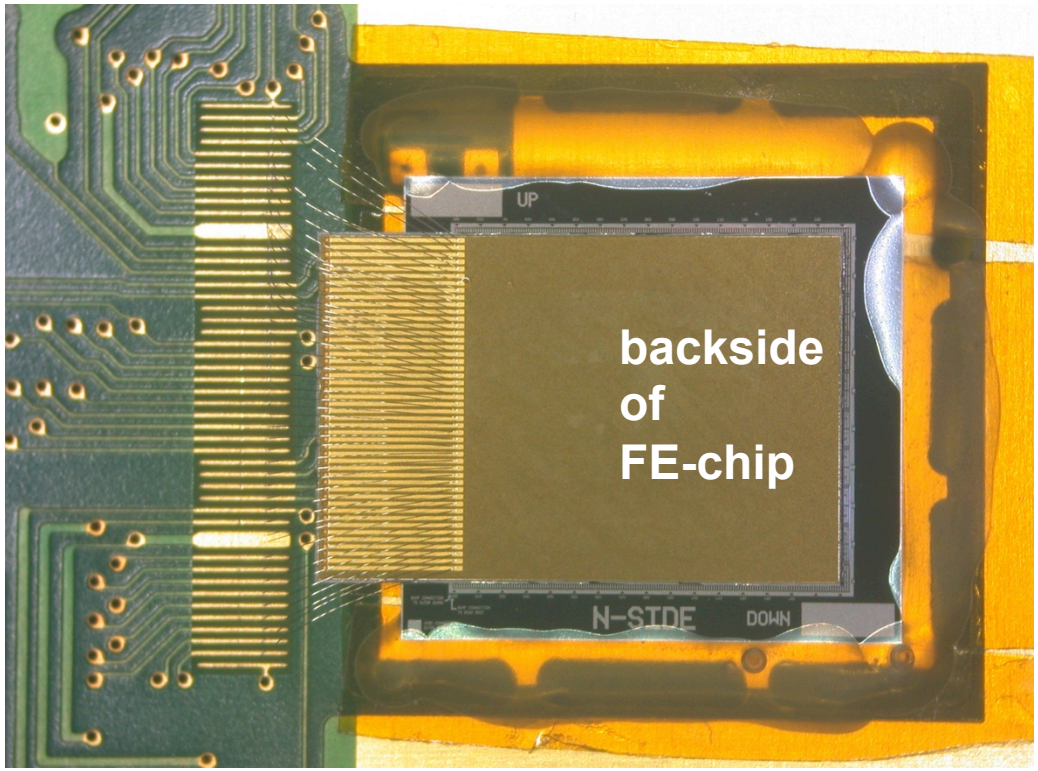
- **90 µm bumped FE-I4 chip**
- **thin Al flex**
- **serial powering**
- **TSV and backside metal routing**

aggressive reduction in material

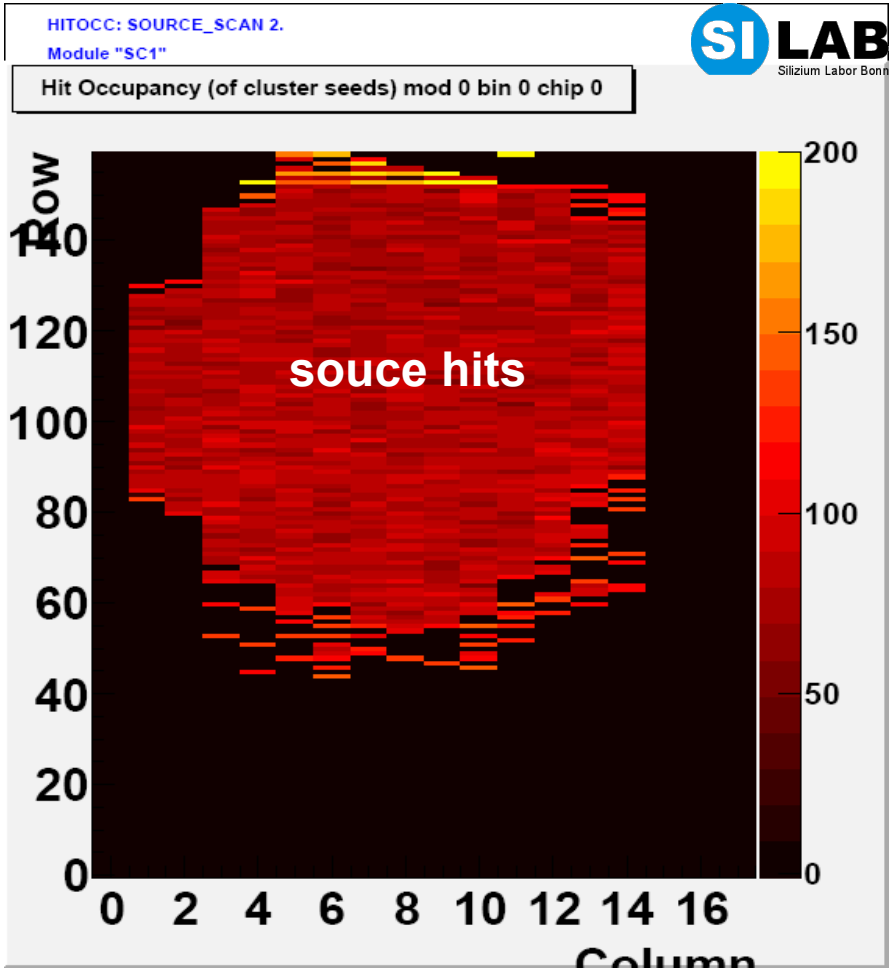


Proof of principle demonstration

ATLAS FE-I3 chip-sensor module operated through TSV and backside re-routing



Source scan with Am-241 source



Conclusions

Looking into the future is always a gamble, but … I am pretty sure that …

- for sLHC
  - only hybrid pixels, possibly with heavy 3D integration (CMOS and post-processing) will manage the environment (irradiation and rates)
  - material will not easily get below 1% x/X_0 per layer
  - … perhaps consider some gaseous advancements

- for (almost all) other applications in HEP
  - thin materials
  - high monolithic integration

  will in my opinion dominate the issue.

  Here CMOS integration and integration of sensor and electronics will be the interesting challenges for the coming years.

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