Development of a 13-inch Hybrid Avalanche Photo-Detector (HAPD) and its Readout System for a Water Cherenkov Detector

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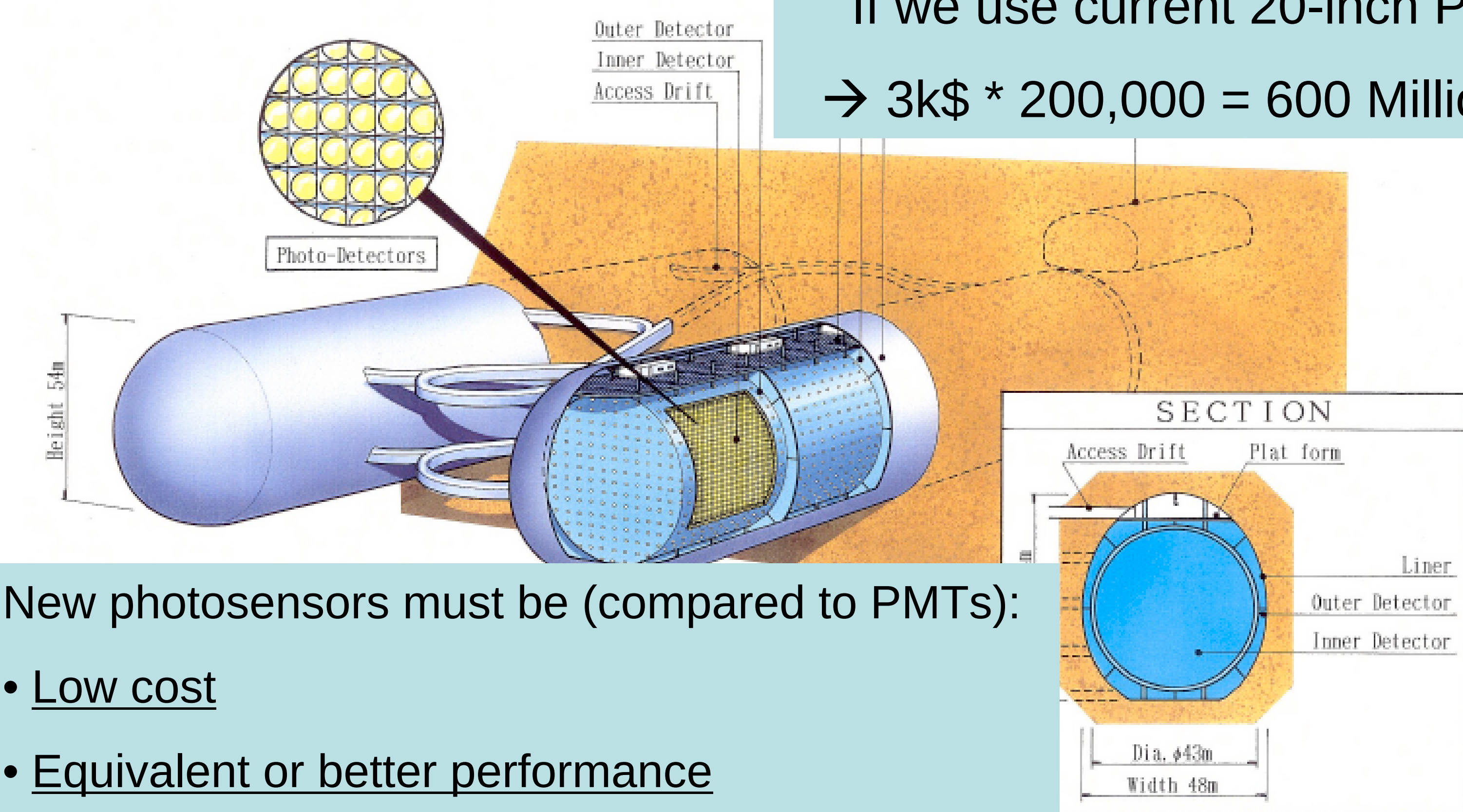
Concept of Hyper Kamiokande (20 times Super K)



If we use current 20-inch PMTs

→ 3k$ * 200,000 = 600 Million $!!

New photosensors must be (compared to PMTs):

- Low cost
- Equivalent or better performance

(Single photon sensitivity, time resolution)

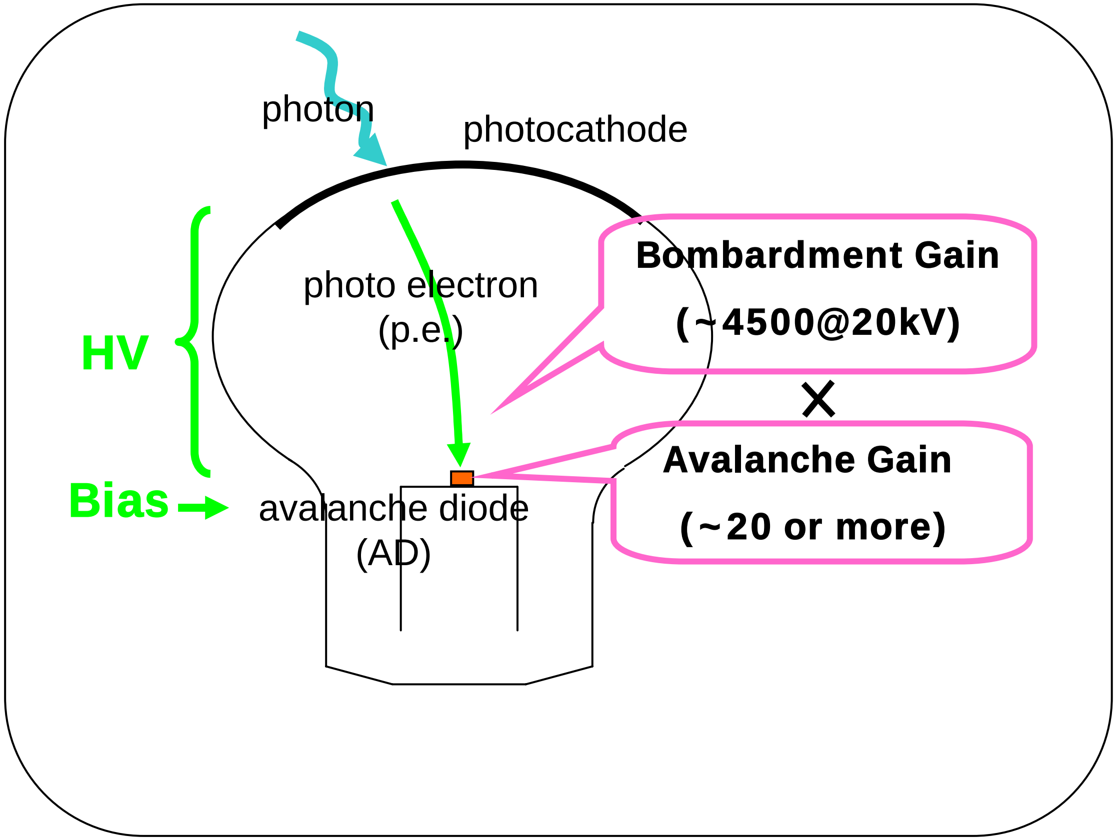
⇨ Our solution to the photosensors:

Hybrid Avalanche Photo-Detector (HAPD) with a large photocathode

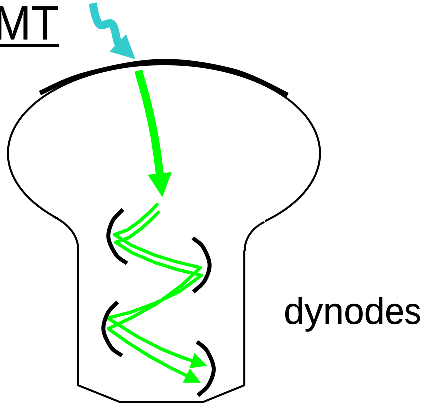
The Principle of HAPD

Main idea of HAPD:

Replace dynodes of PMT with an avalanche diode



cf. PMT



Multiple gain stages in dynodes

The HAPD characteristics

Compared to current PMTs…

☺ Simple structure without dynodes

→ Cost reduction on mass production

☺ Large gain at the first stage of multiplication process

→ Single photon sensitivity

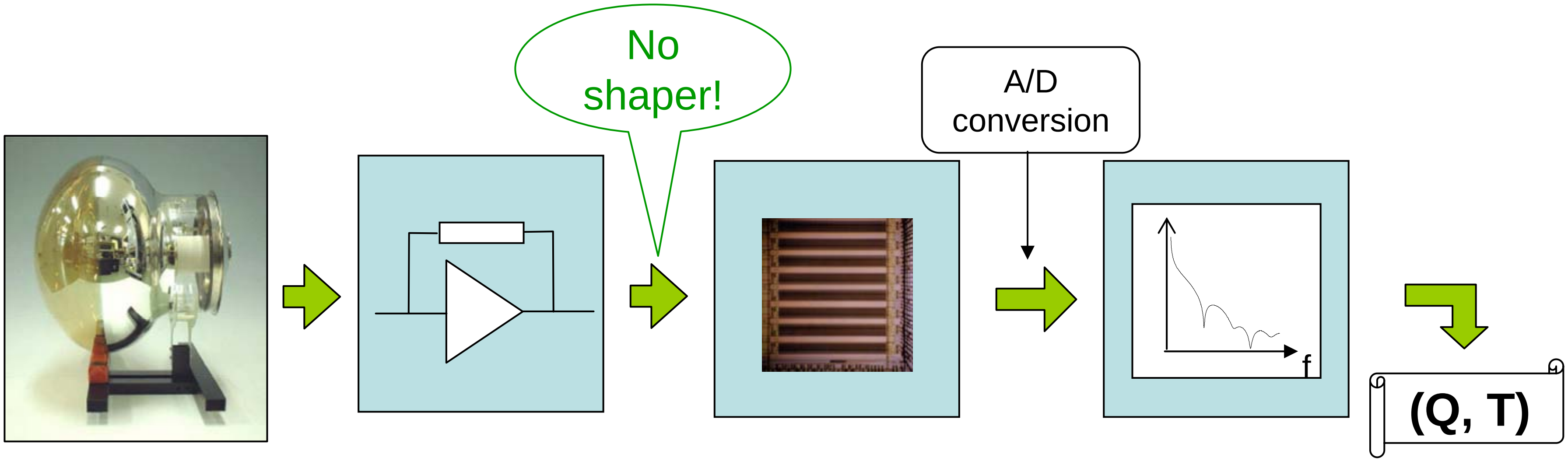
☺ No TTS in dynodes & large HV (~20kV)

→ Good time resolution(σ_t~1ns@1p.e.) ← PMT: 2~3ns

☹ Relatively small gain(~10^5) ← PMT: ~10^7

→ Need a sophisticated readout system

HAPD & Readout System



13-inch HAPD

Pre-amplifier (ASIC)

Waveform sampler (AMC)

Digital Filter (FPGA)

Low noise

Wide bandwidth

Fast sampling

(~1GHz)

Effective noise suppression

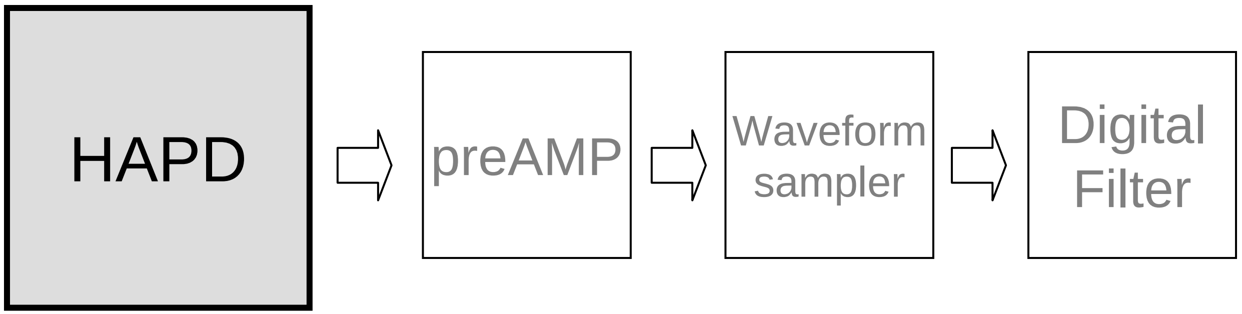
Different from the traditional shaper+ADC+TDC system.

(Digital filter can realize more effective noise suppression!)

Outline

1. **13-inch prototype HAPD**
   - Gain
   - Single photon sensitivity
   - Time resolution
2. **Preamplifier on ASIC**
   - Noise performance
3. **Analog Memory Cell (AMC) as a waveform sampler**
   - Basic functionality
   - Sampling speed
4. **Digital filter on FPGA**
   - Better performance (S/N, σ_t)
   - Lower cost

HAPD

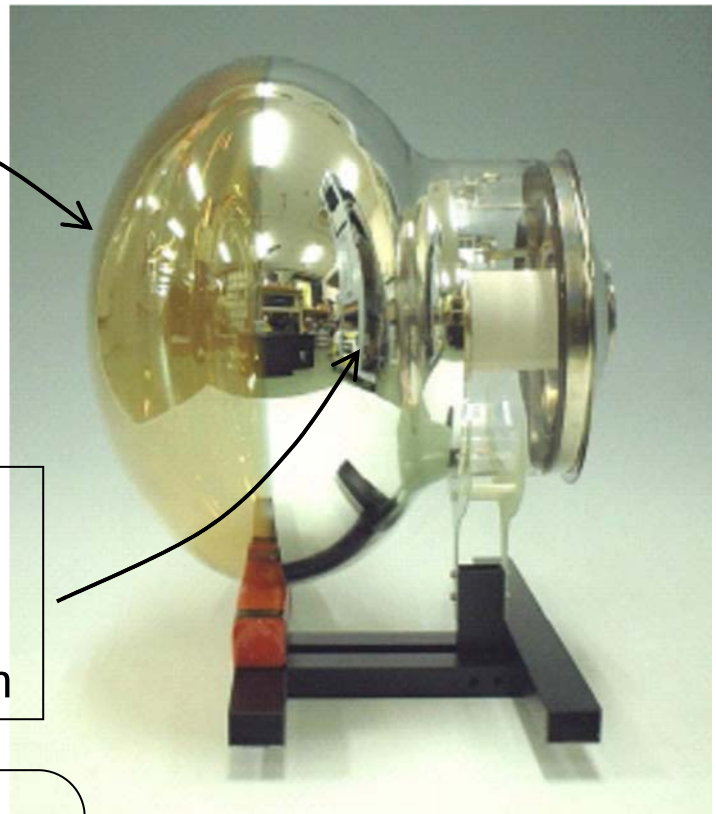


Requirement

- Single photon sensitivity
- Time resolution: (σ_t<1ns)

HAPD Evaluation

13-inch prototype HAPD



Photocathode

- 330mm dia.

(effective area: 240mm dia.)

- Bialkali

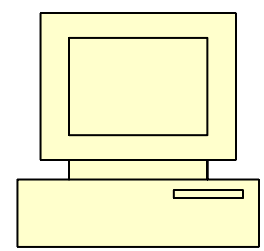
Avalanche Diode

- 5mm dia.
- Front-side illumination

"Positive-HV" mode

- photocathode: GND
- AD: +HV

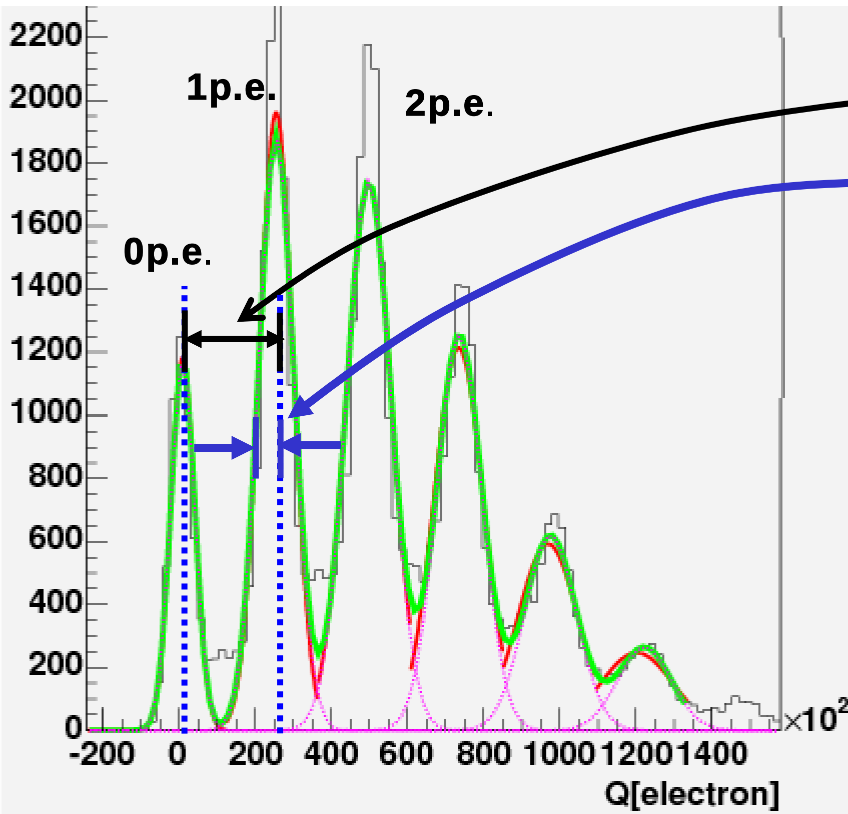
Oscilloscope



Offline filtering

Gain & Single Photon Sensitivity

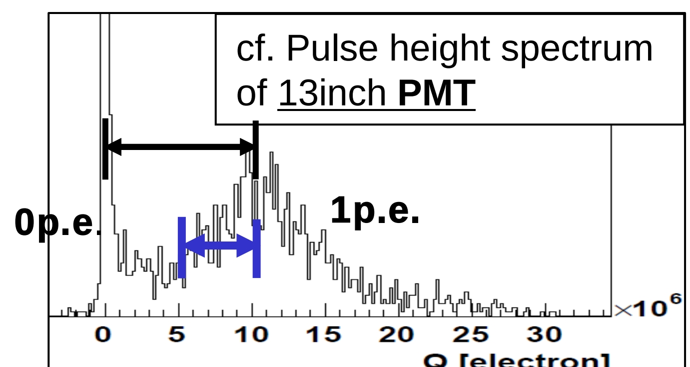
Pulse height spectrum after digital filter



Gain ~ 24,000@12kV

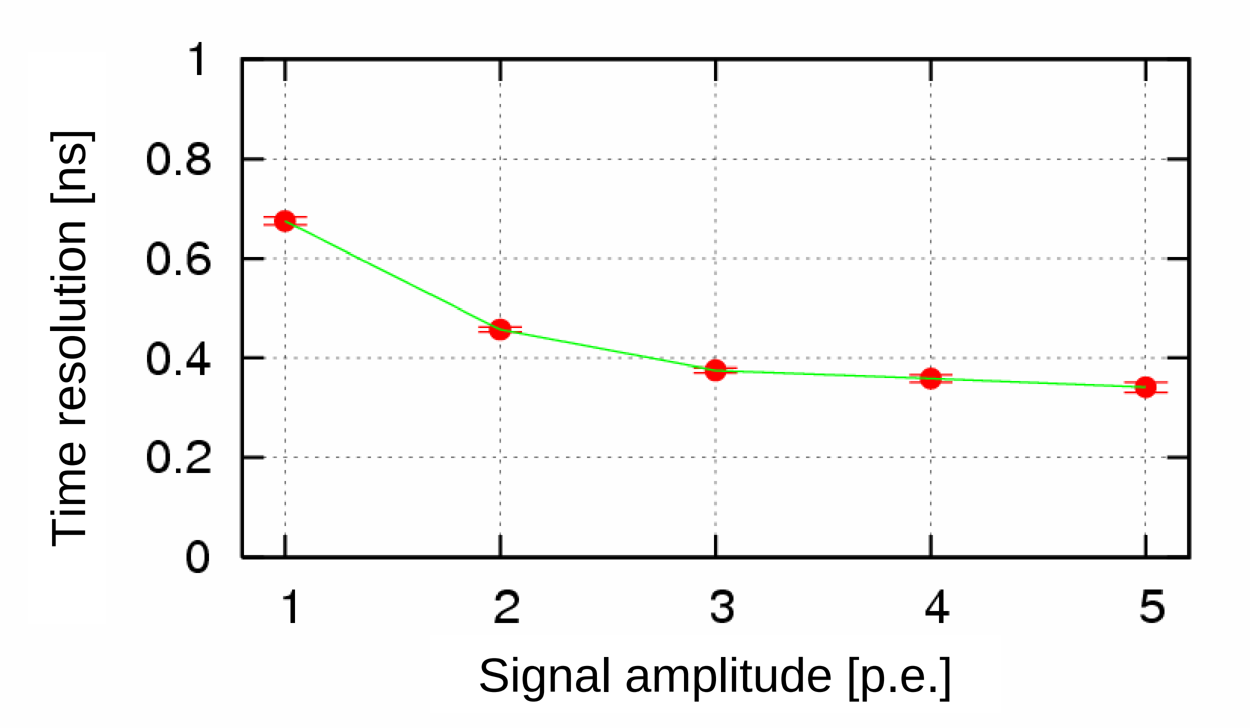
Small gain fluctuation
→ Clear peaks!!

Meet the requirement
(Single Photon Sensitivity)



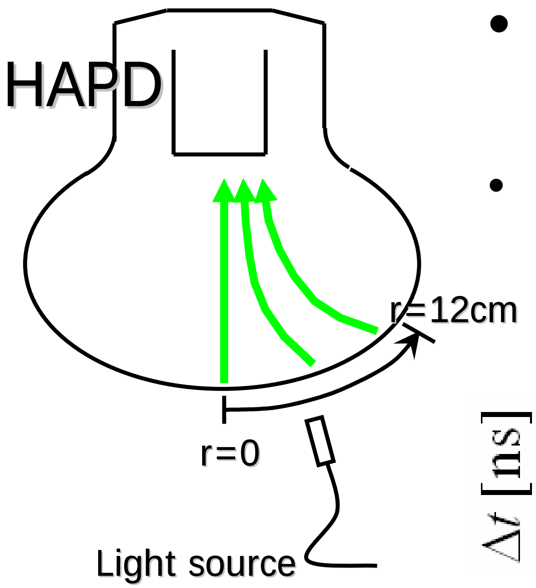
Time Resolution with spot illum.

Light source: spot illumination @ center of the photocathode

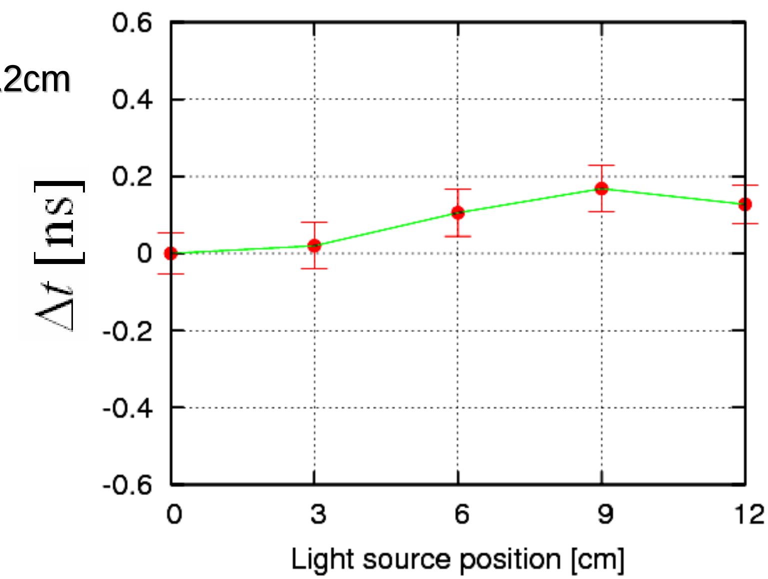


σ_t^{spot}~0.7ns@1p.e.

Transit Time Uniformity



- <u>Transit time</u> vs. position on the photocathode
- Input: ~30p.e.(time resolution: 0.06ns@30p.e.)



Transit time uniformity

$\underline{\sigma_t^u \sim 0.1\text{ns}(<<0.7\text{ns})}$

Time resolution σ_t~<u>0.7ns</u>@1p.e.

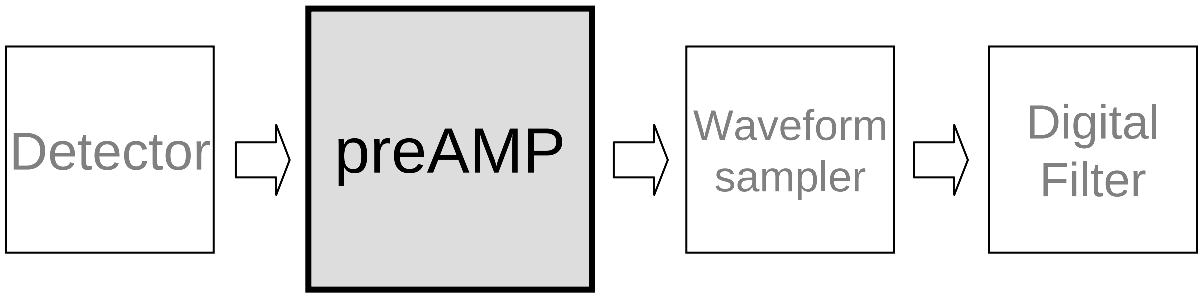
Meet the requirement (σ_t <1ns)

cf. 13inchPMT: σ_t~3ns

HAPD Summary & Future Plans

- Summary
  - Total Gain: ~24,000@HV=12kV
  - Single photon sensitivity: S/N=10@1p.e. ☺
  - Time resolution: σ_t~0.7ns@1p.e. ☺
- Future Plans
  - Tube structure upgrade ⇨
    - Effective area (240mm→300mm)
    - HV insulation (12kV→20kV)
    - Water pressure resistance (2.5atm→7.5atm) ⇨
  - Back-illumination AD
    - Detector capacitance(70pF→30pF)
    - More robust to electron bombardment and alkali pollution

Preamplifier



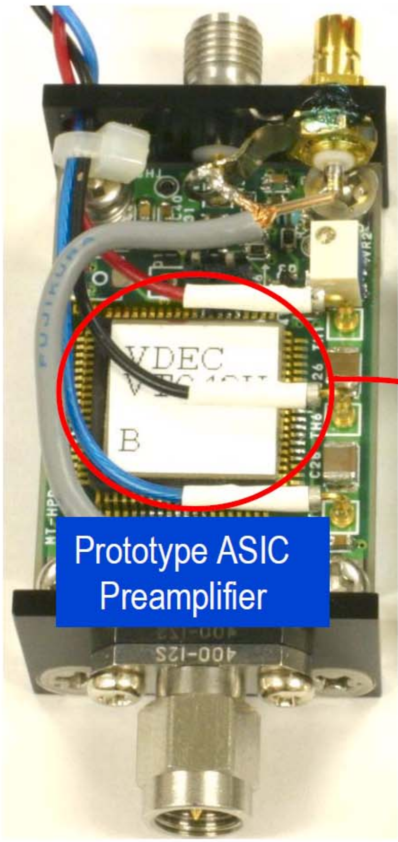
Requirement

- Low noise (ENC: << HAPD gain:10^5)

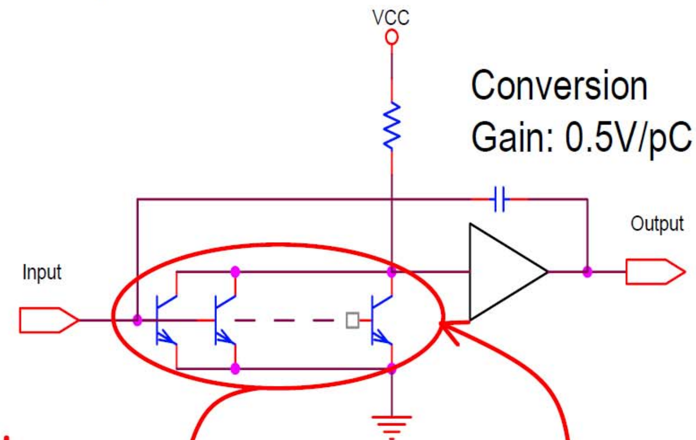
Preamplifier

(version ”ASIC2004”)

Bipolar wide-bandwidth charge amplifier

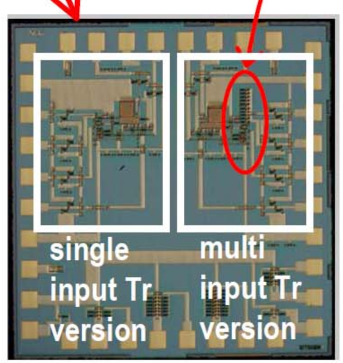


Simplified Circuit Schematics of the ASIC Preamplifier



Conversion Gain: 0.5V/pC

Dynamic Range: ~2V



Multiple Input Transistors:
reduce rbb' for lower noise

$$ENC_s^2 = 4kT \cdot (r_{bb'} + 1/2gm) \cdot Cd^2 \cdot \int W'(t)^2 dt$$

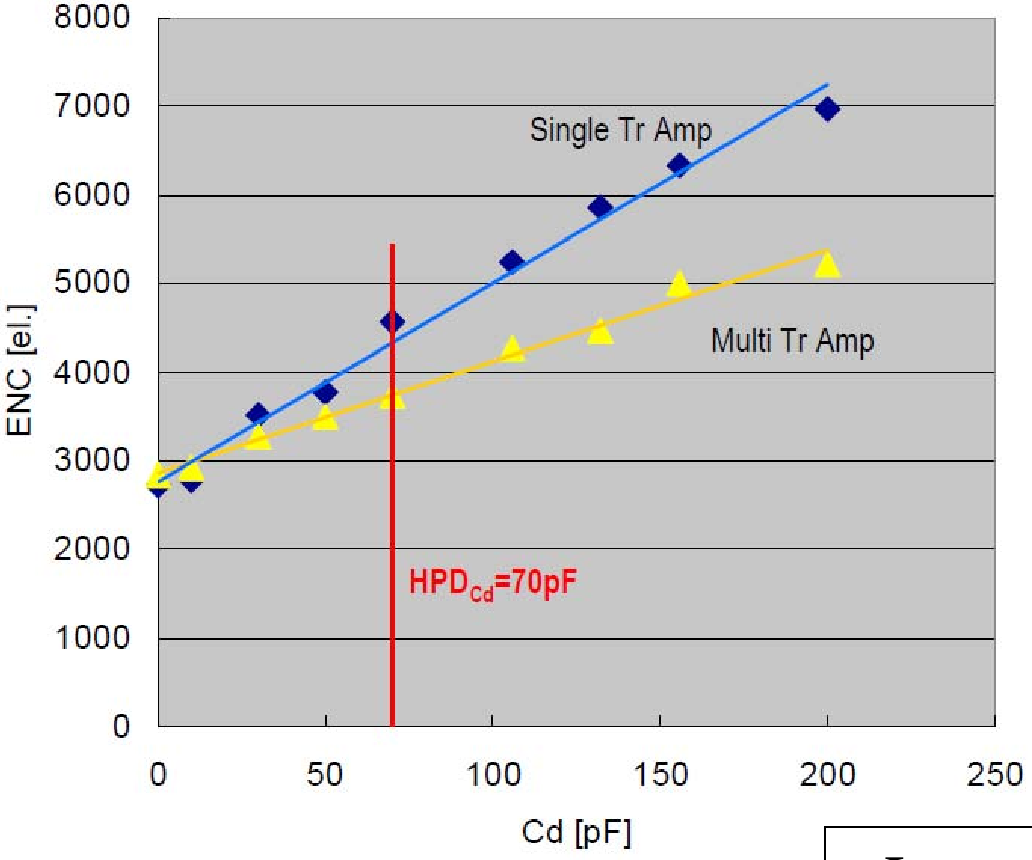
✓High speed

✓Low noise

✓Low power consumption

Equivalent Noise Charge

ENC after filtering:



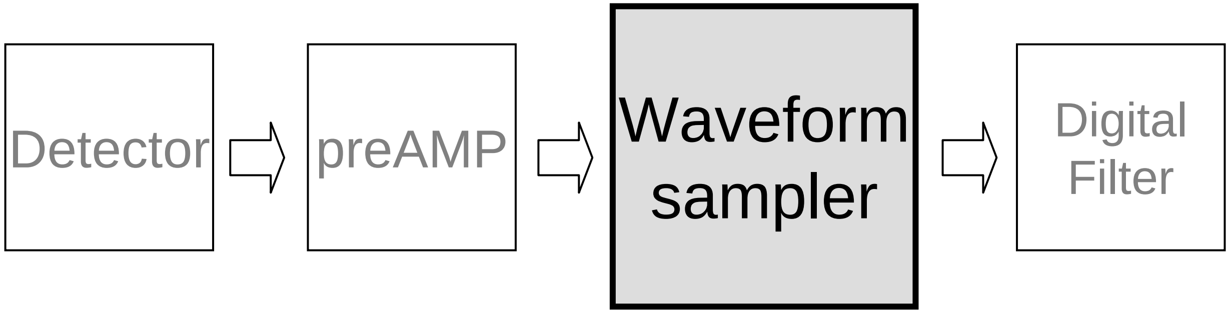
	ENC (Cd at 70pF)
Single Tr Amp	4300 el.
Multi Tr Amp	3800 el.

- Less ENC for Multi Tr. Amp.
- **Meet the requirement (<<10^5 el.)**

Preamplifier Summary

- Summary
  - Multiple input transistor is effective to reduce noise of the preamplifier.
  - ENC=3,800 electrons (<<HAPD gain:10^5) ☺

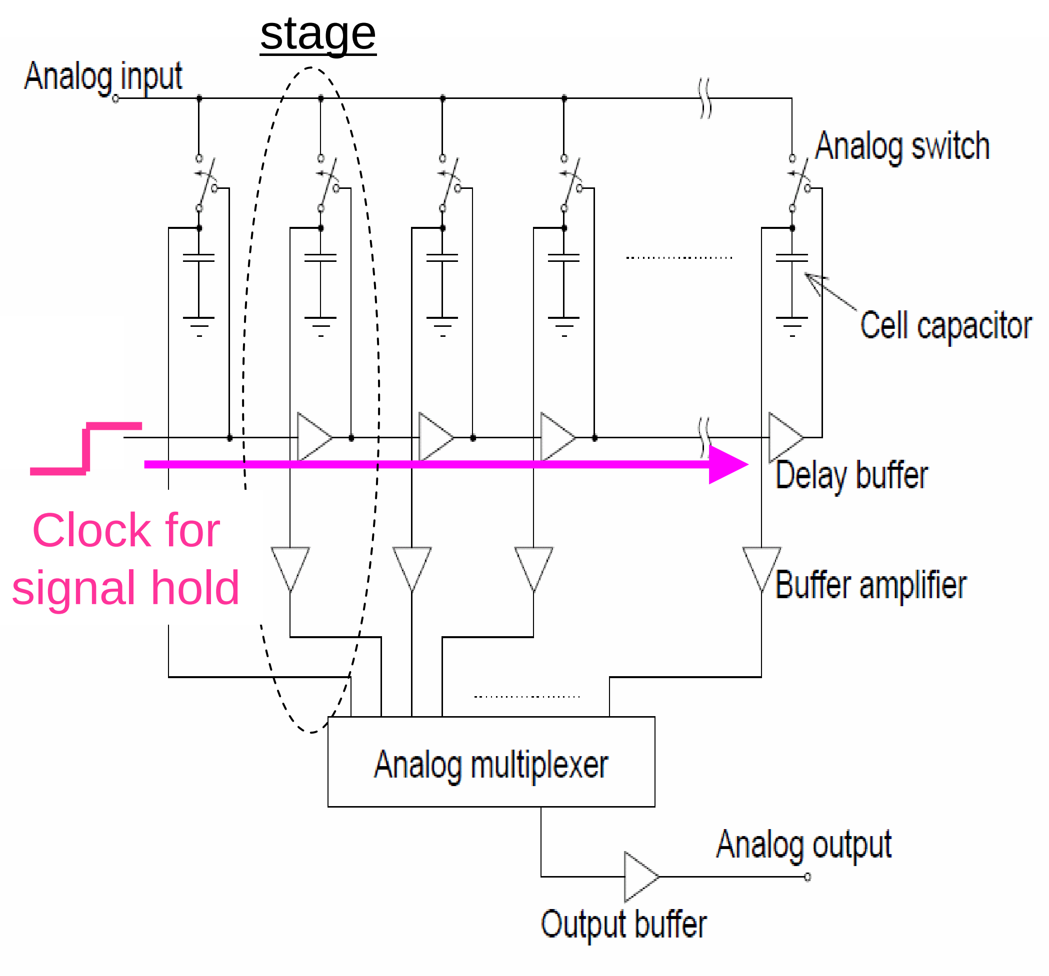
Waveform Sampler (AMC)



<u>Requirement</u>

- Sampling Speed: ~1GHz

Principle of our AMC



Compared to FADC:

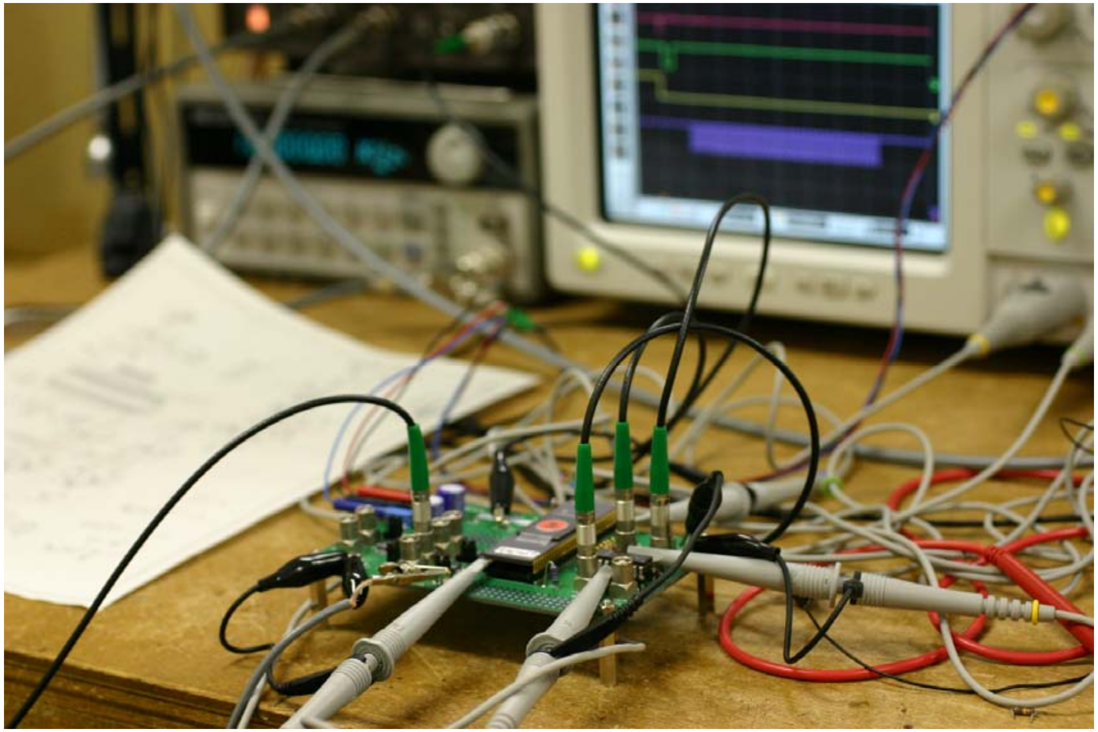
→ low cost, low power !

- A clock for signal hold propagates the delay chain, turning off analog switches one by one to hold the input signal.
- Sampling speed is determined by the delay interval of each stage.

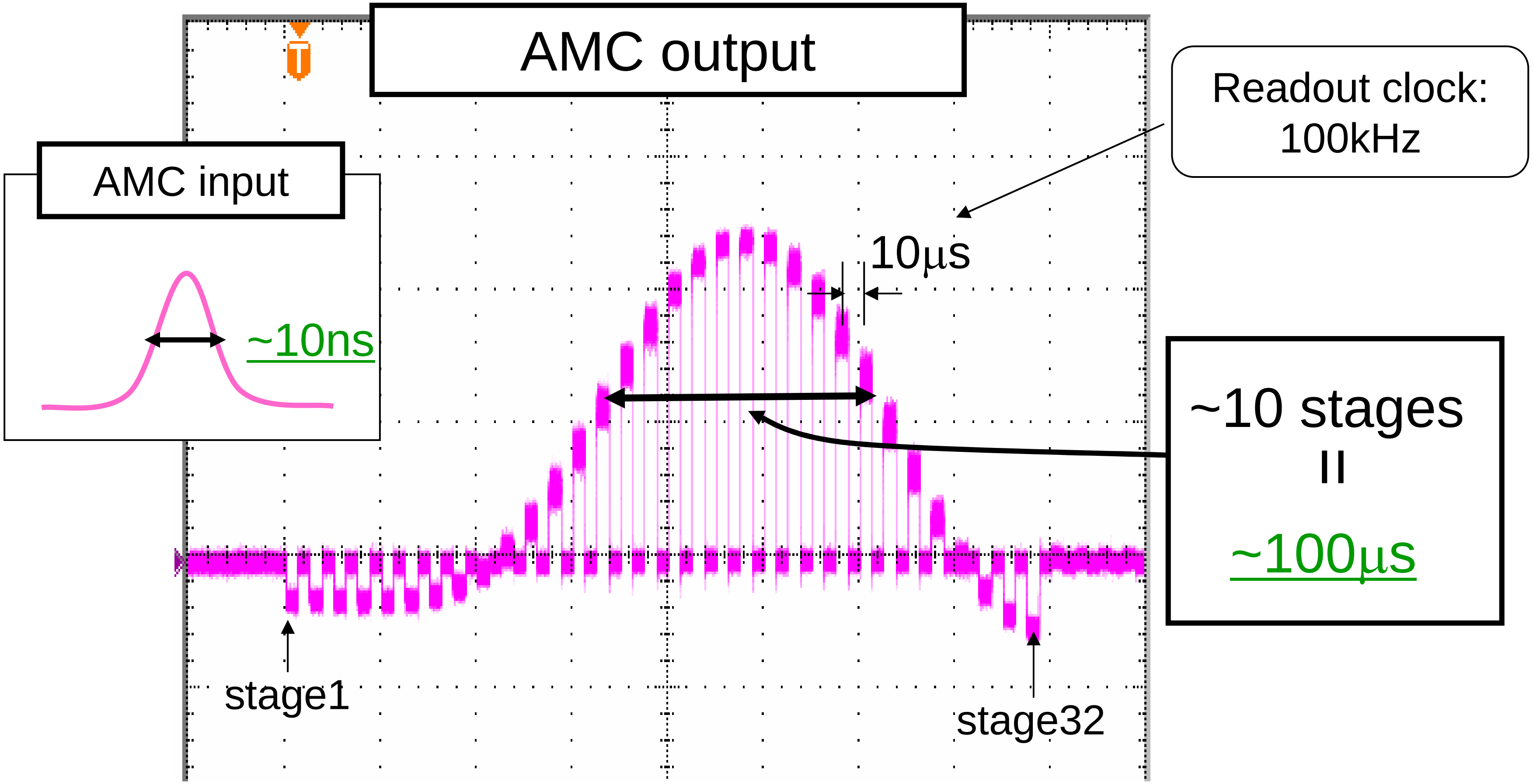
AMC Evaluation

Test version "AMCM64":

64 stages (32 x 2 blocks)

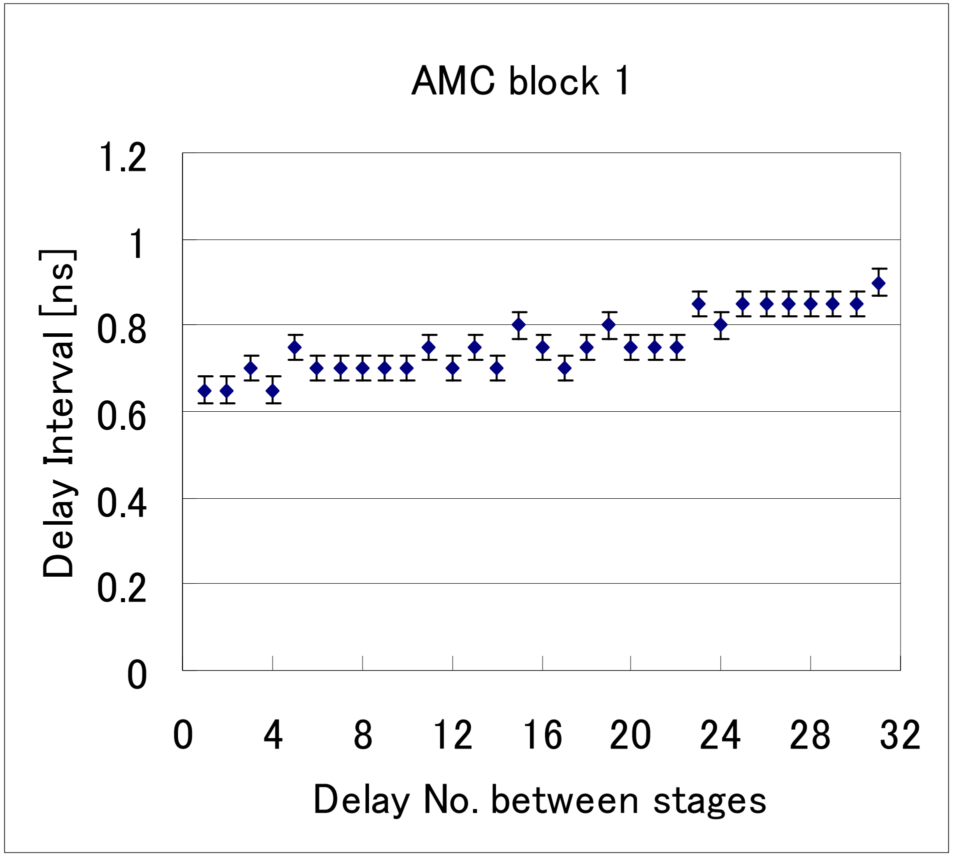


Basic Functionality



Basic functionality is confirmed!

Sampling Speed (Delay Intervals)



Delay intervals: ~1ns

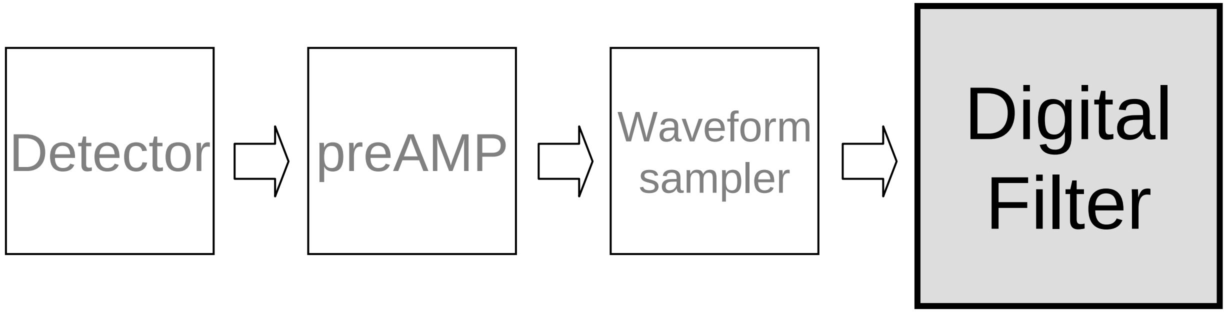
→ **Sampling speed: ~1GHz (Meet the requirement)**

AMC Summary & Future Plans

- Summary (version AMCM64)
  - Basic functionality is confirmed! ☺
  - Sampling speed: ~1GHz ☺
- Future Plans
  - New circuit layout for better performances

    (Ground impedance will be minimized)
  - 64→1024 stages (connect several AMCs in series)

Digital Filter



<u>Requirement</u>

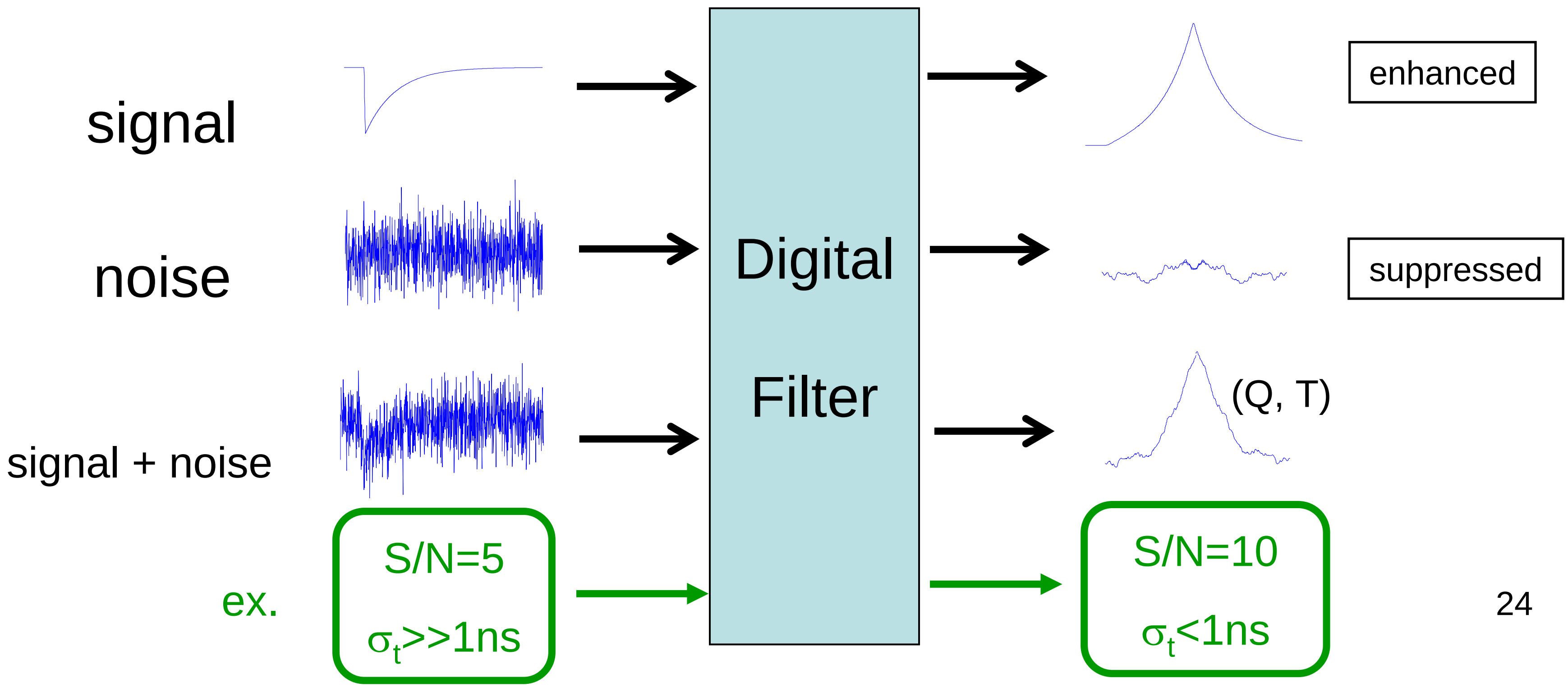
- Better performance (S/N, σ_t)
- Lower cost

Digital Filter

We use “Digital Filter” (instead of analog shaper)

→ better performance in noise suppression

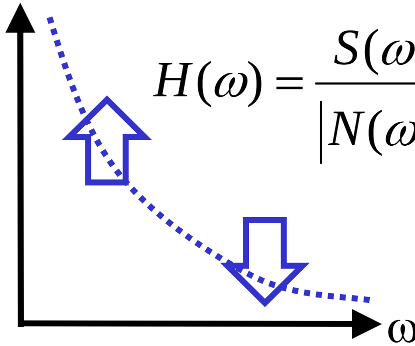
→ better S/N, σ_t



Filter design

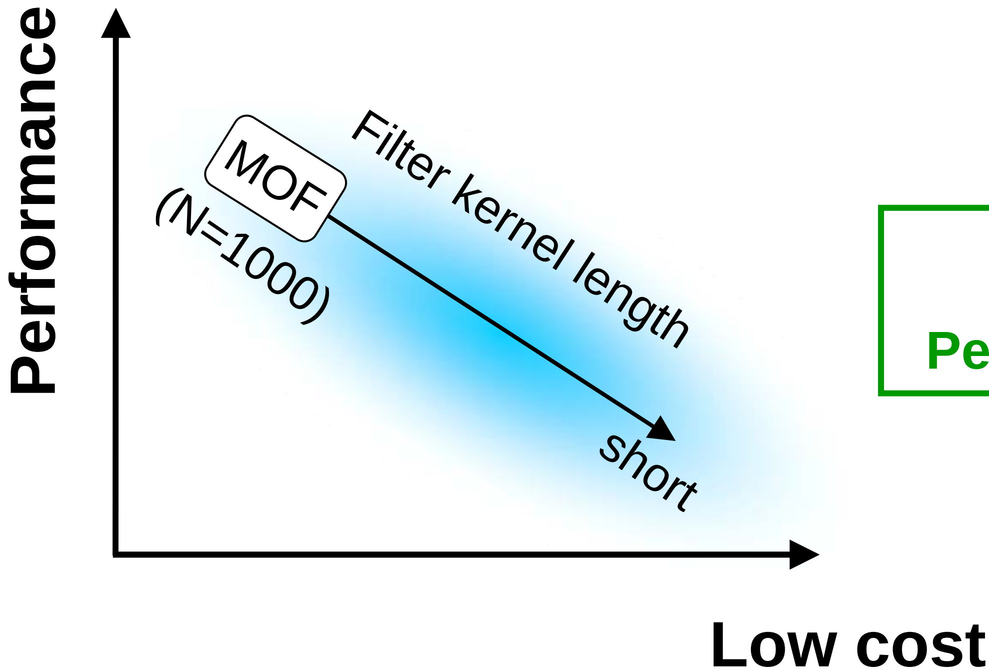
For a given set of S(ω) and N(ω), "Matched Optimal Filter (MOF)" gives the best performance (S/N ratio and σ_t).

MOF response



$$H(\omega) = \frac{S(\omega)^*}{|N(\omega)|^2}$$

A kind of low-pass filter



TRADEOFF

Performance ⇔ Low Cost

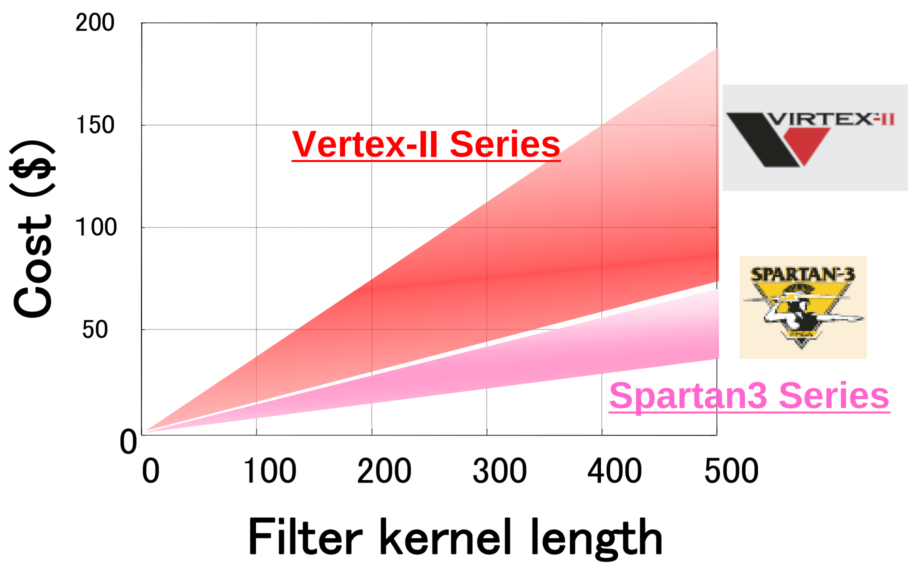
Cost Performance vs. Filter Kernel Length

Software: MATLAB 7.0.4 / Simulink 6.1 / ISE Foundation 7.1i

Hardware: Xilinx Vertex-II xc2v3000 @ SignalMaster-Quad C6713

<Implement option>

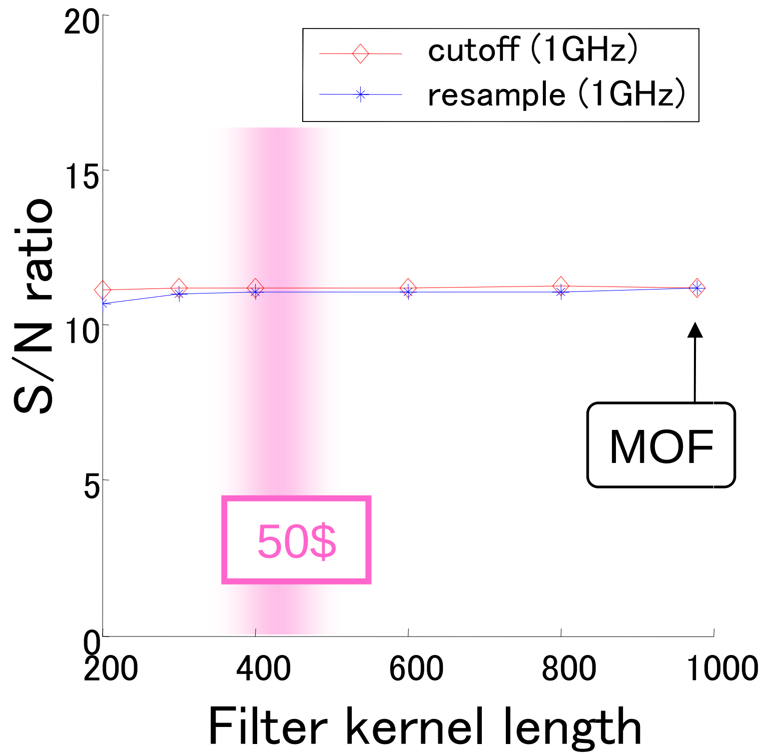
DA-FIR (Distributed-Arithmetic FIR), x11 over sampling, input=10bit, coeff=10bit

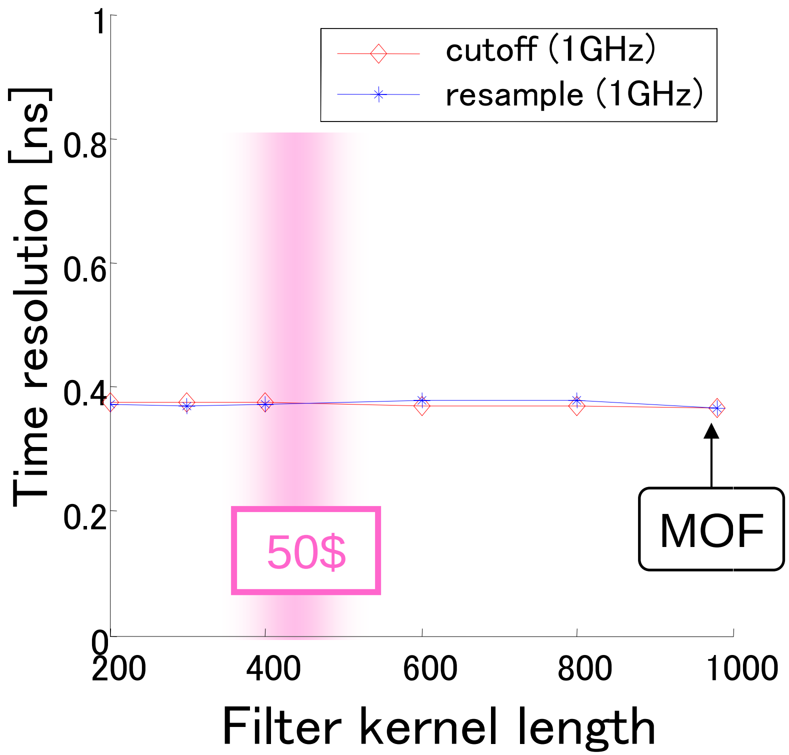


The cost is almost proportional to the filter kernel length

Filter Performance vs. Filter Kernel Length

When S/N ratio at filter input = 5 (equivalent to S/N ratio at filter output of ~10)





Keep MOF's performance and decrease the kernel length to be ~200!

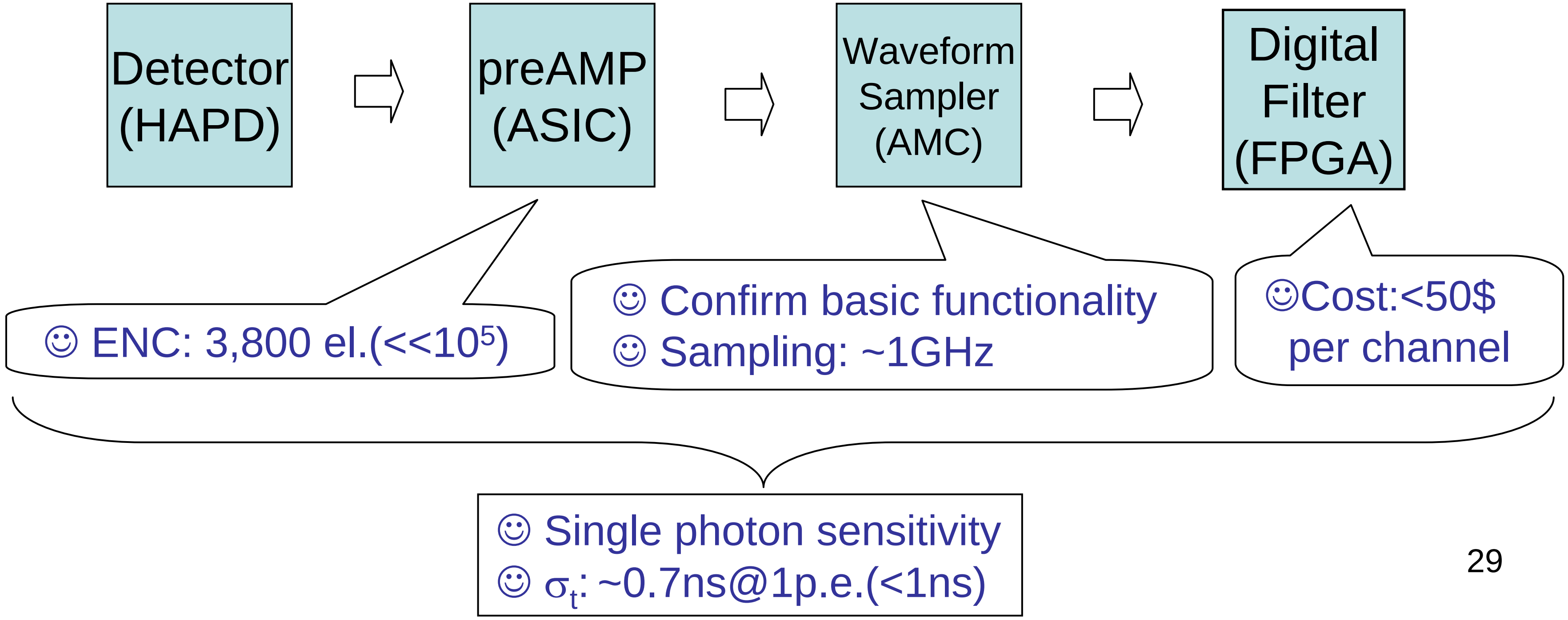
⇒ FPGA cost per channel: < 50$

Digital Filter Summary

- “Matched Optimal Filter (MOF)” gives the best performance.
- However, we found that the shorter filter gives almost same performance.
- Estimated FPGA cost is <50$ per channel. ☺

Summary of this talk

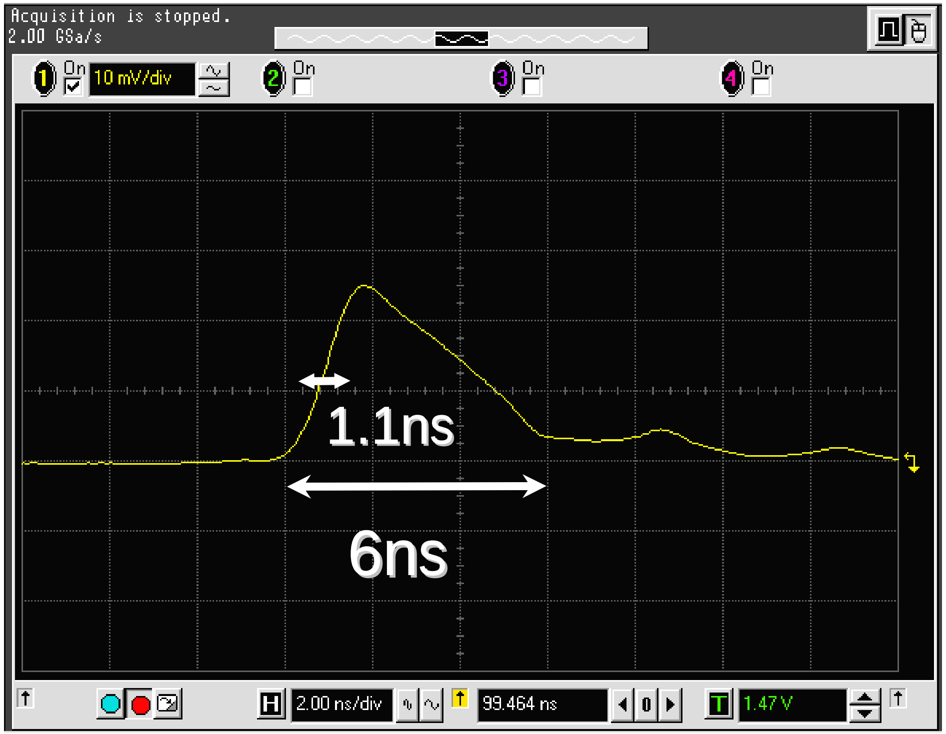
- We have developed a 13-inch prototype HAPD and its readout system.
- Their performances are mostly satisfactory for next generation water Cherenkov detectors:



backup

Detector Only

Raw Signal of the HAPD



10mV/div, 2ns/div

HV, Bias: Max(12kV, 370V)

Input light: ~30p.e.

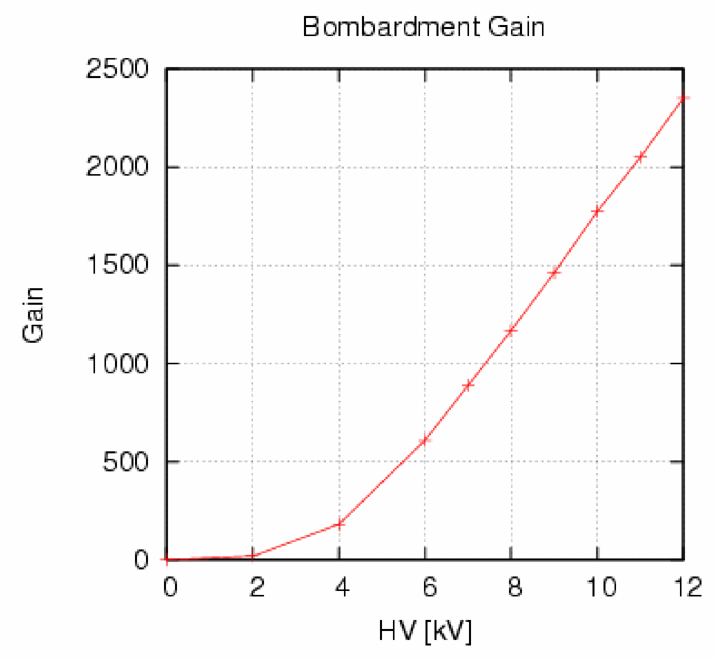
- Fast signal response
  - Rise time ~ 1.1ns
  - Full pulse width ~ 6ns

Detector Only

Bombardment/Avalanche Gain

- Bombardment Gain

Bias=50V(fixed), HV=sweep

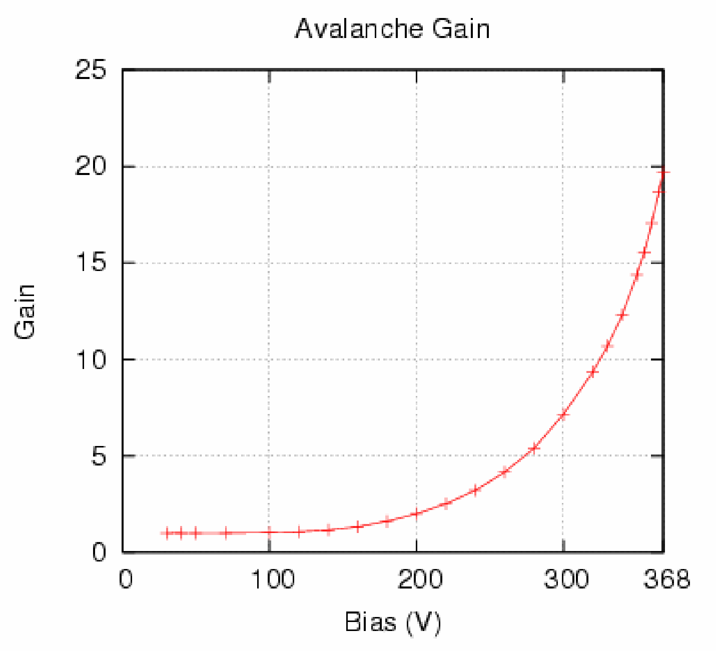


Gain ~2400 @12kV

Gain curve rises >3kV (energy loss in an insensitive layer on AD)

- Avalanche Gain

HV=12kV(fixed), Bias=sweep



Gain ~20 @368V

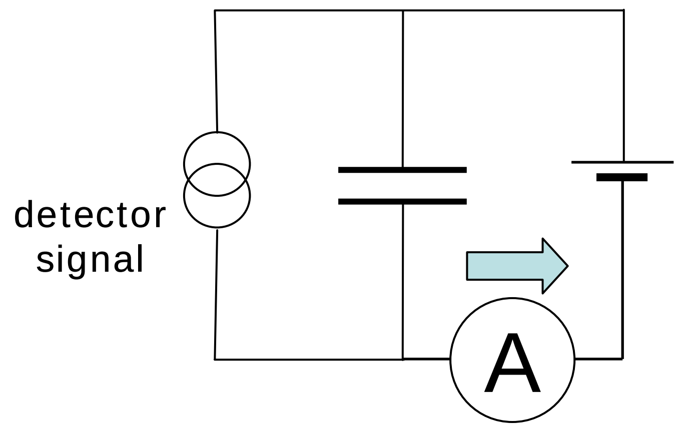
→ <u>Total gain ~50,000</u>

Current mode

Charge loss at preAMP input

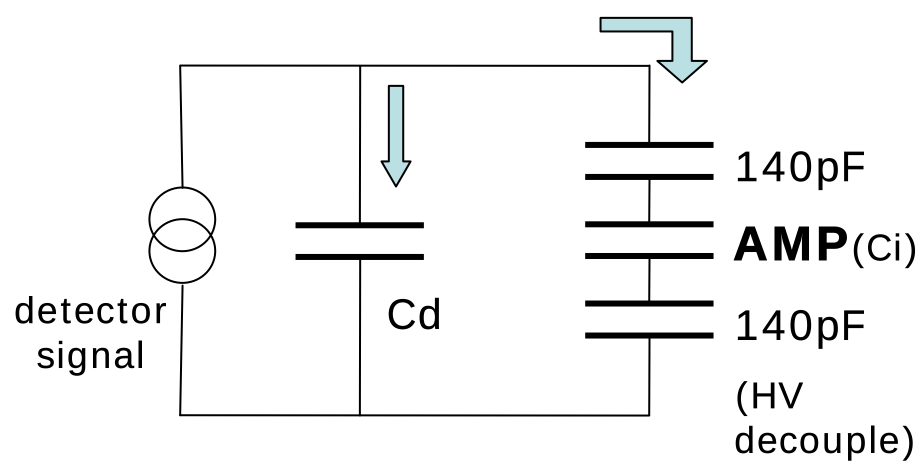
Gain=50,000

(detector only)



Gain=24,000

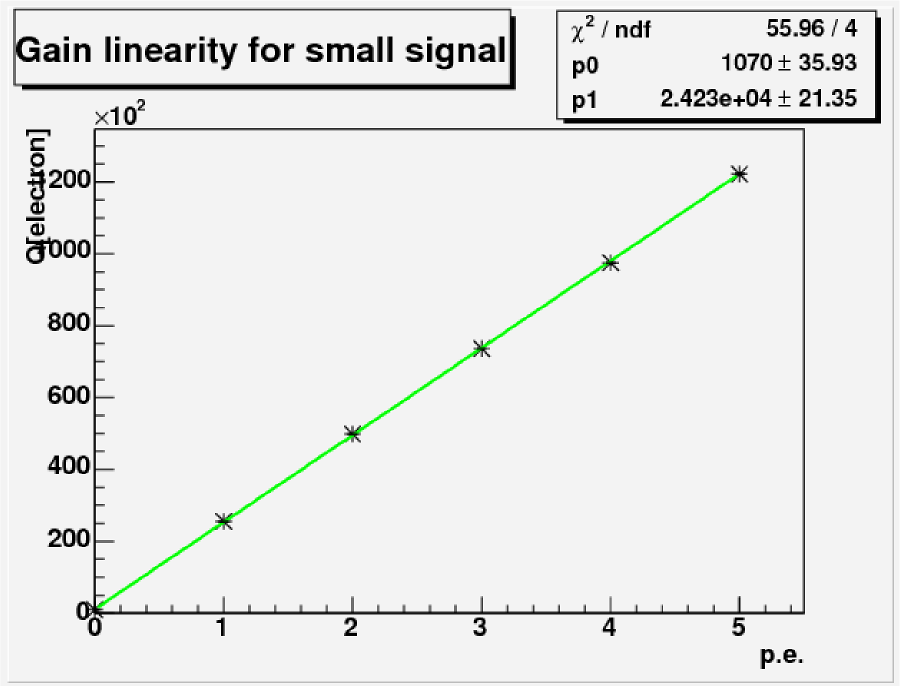
(with preAMP)

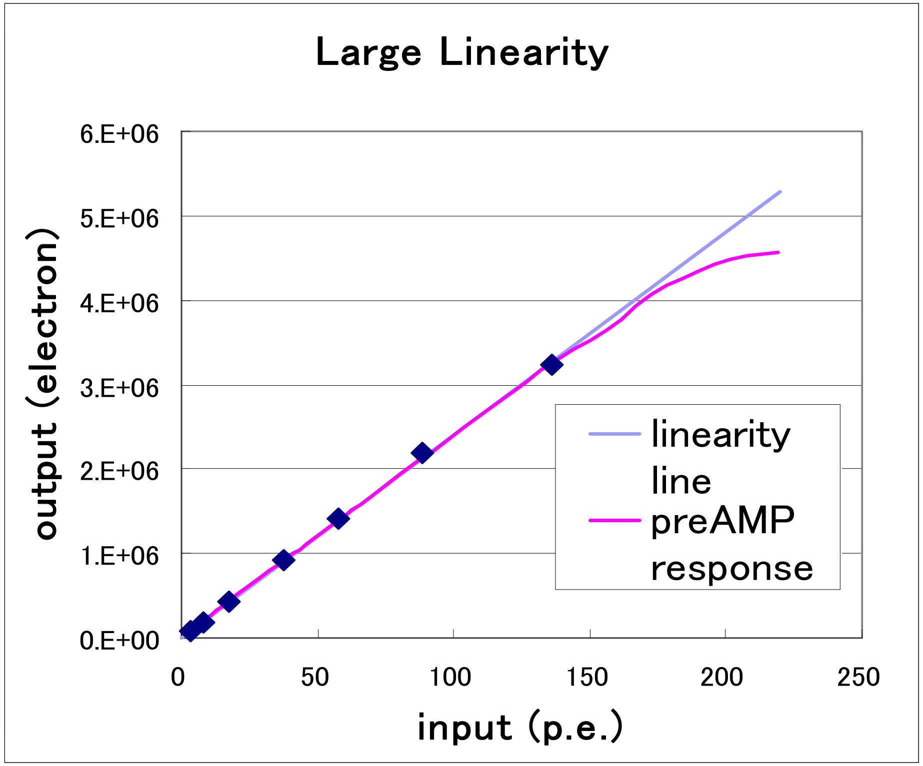


Gain Linearity

Peak positions

in the pulse height spectrum



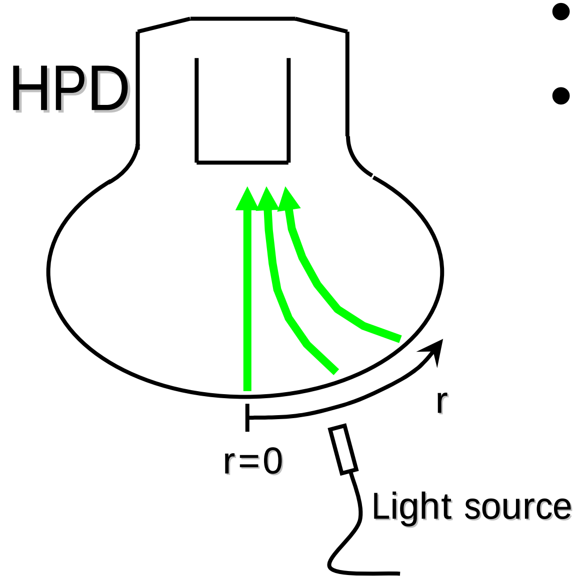


Linearity is good up to 5p.e.

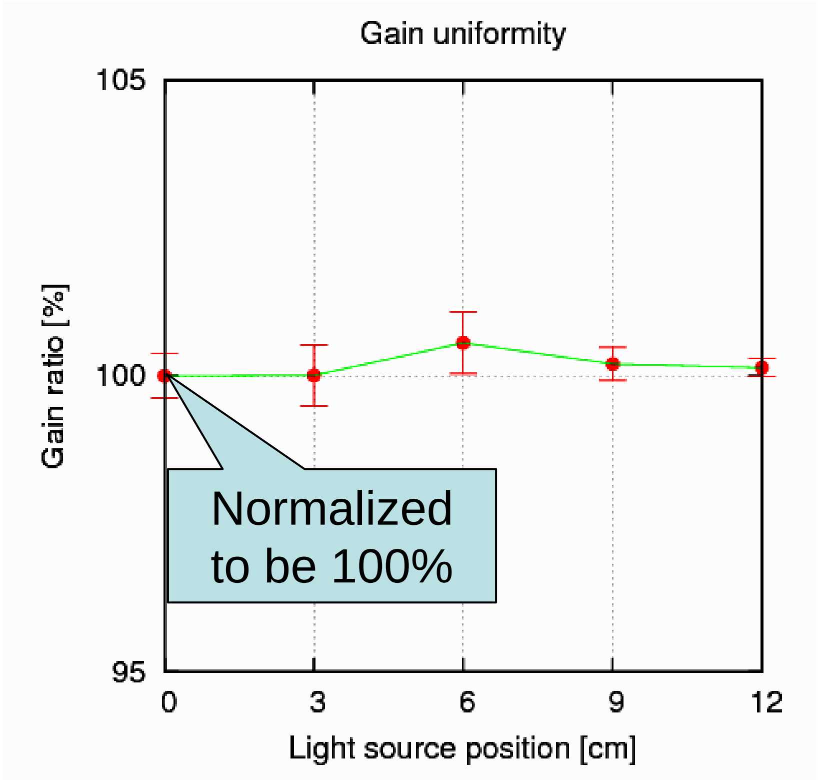
Good linearity up to

~150p.e.(preAMP limit)

Gain Uniformity



- Gain vs. position on the photocathode
- Light input: 1p.e.



Gain Uniformity

within ~2%

Time resolution of 20inchPMT-SK

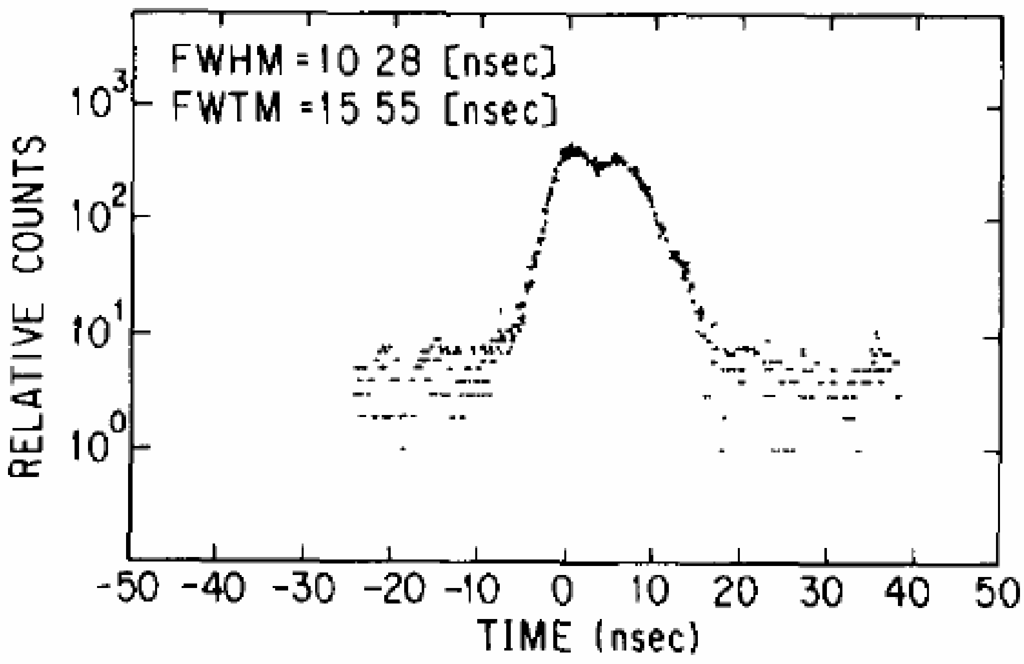
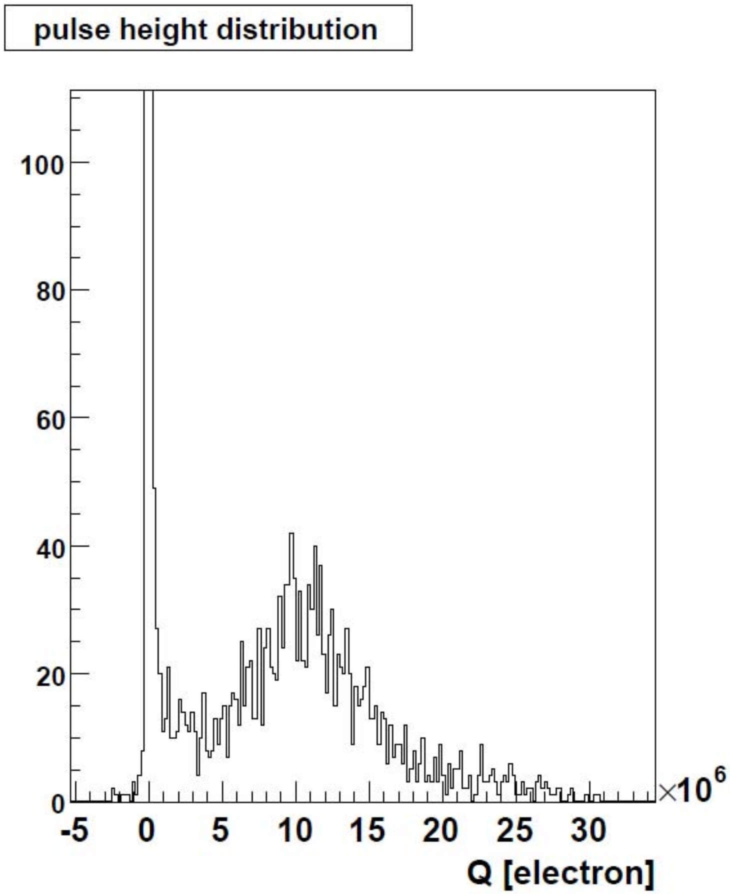


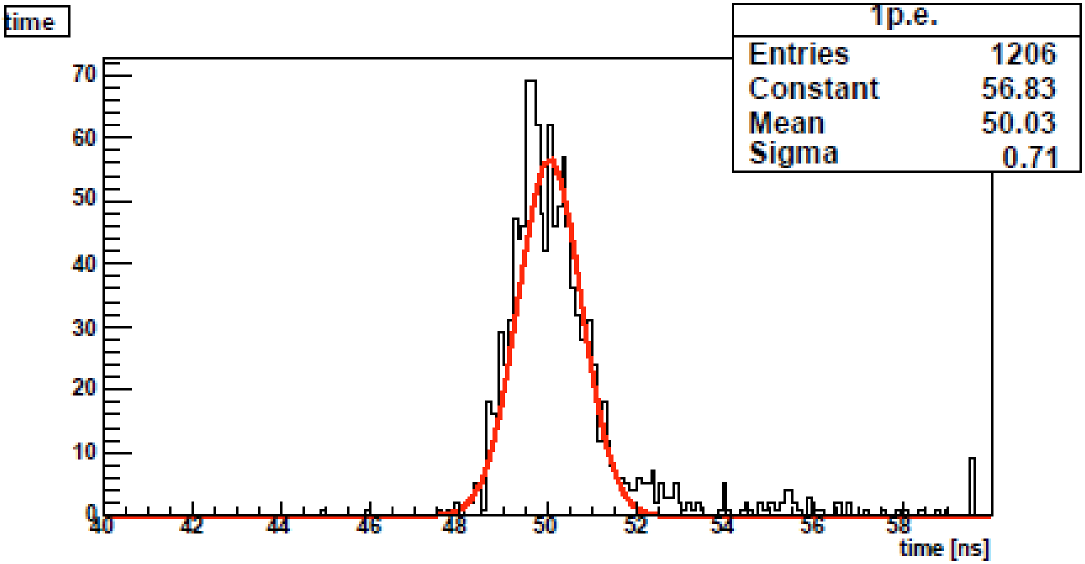
Fig. 4. Single-photoelectron transit time distribution of the present 20 in. PMT.

13-inch PMT (R8055)

No preamplifier, apply digital filter



Gain: ~10^7 @ HV=1.8kV

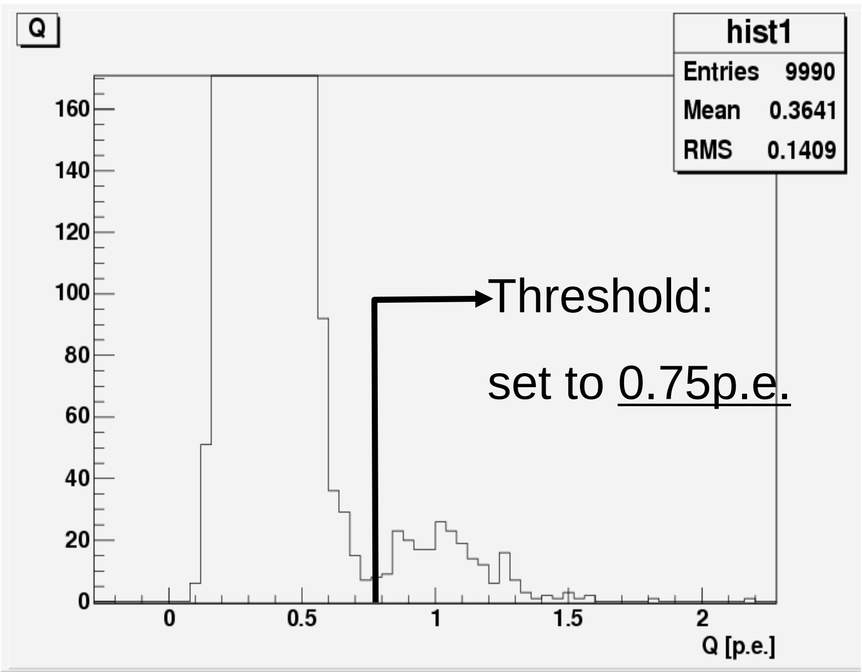


with spot illumination: σ_t ~0.7ns@1p.e.

(cf. T.T.S. by HPK: σ_t~3ns)

Dark Count

- Dominant source: photocathode thermal electrons



HV=15kV, Bias=330V, T=15°C
After 2 hours in the dark

Dark Count: ~100kHz

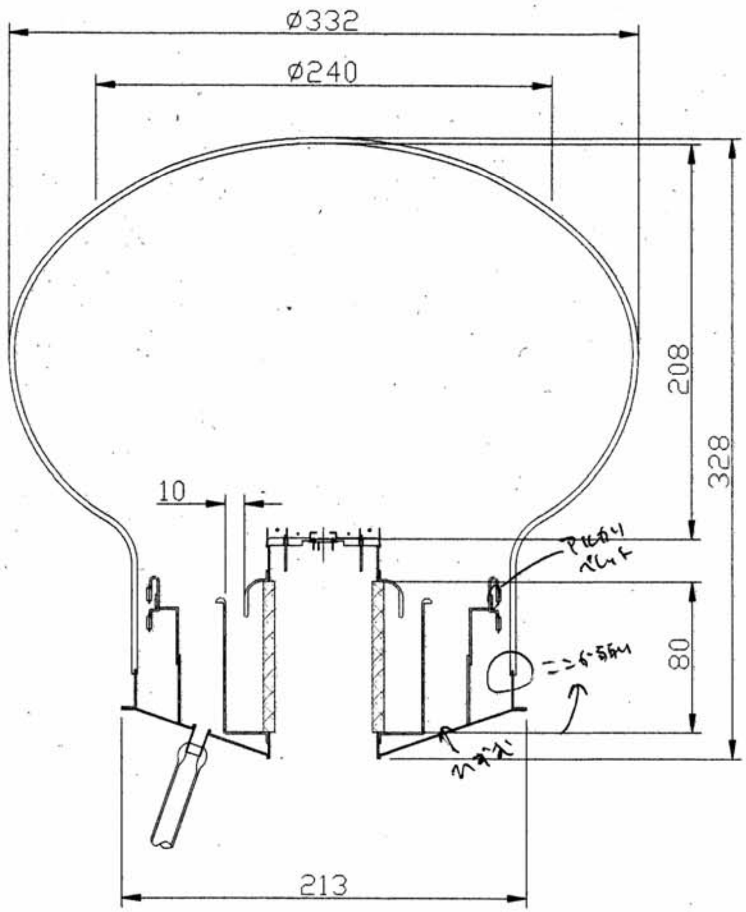
The photocathode activation process is not yet optimized.

→ After the optimization, the dark count is expected to be few kHz.

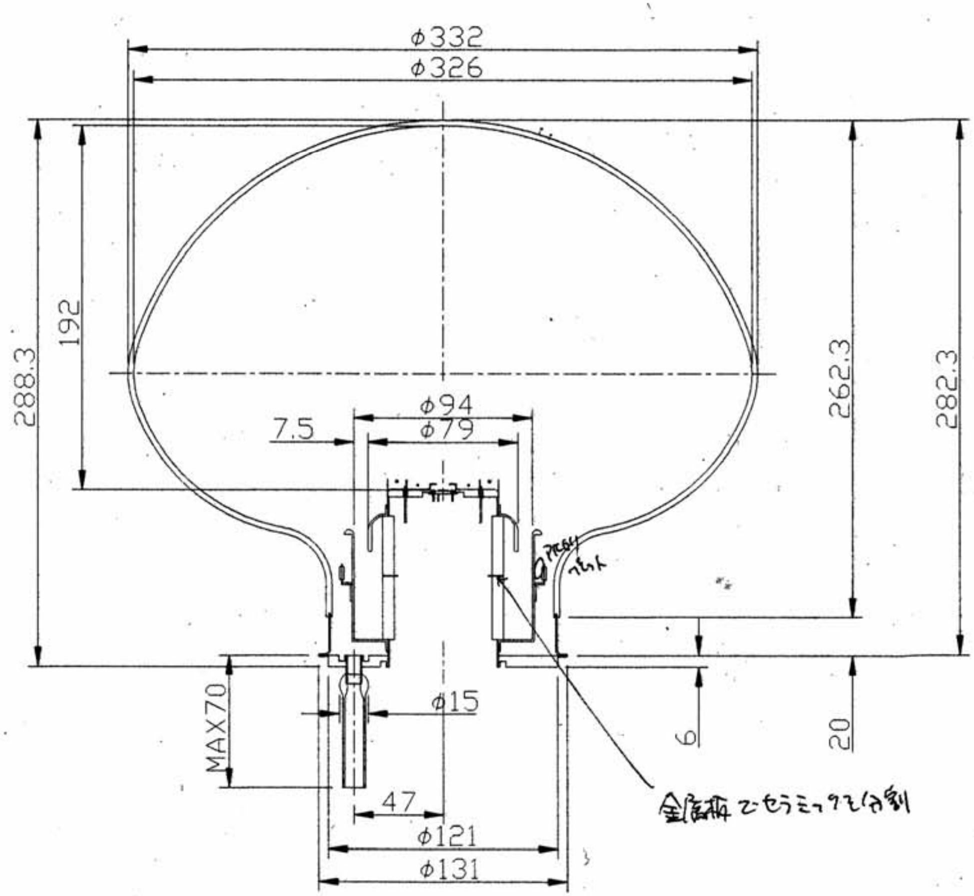
(cf. 20inch PMT-SK:R~10kHz @T=15°C)

16 年度と 17 年度の 13 インチHPD構造比較

平成16年度構造



平成17年度構造

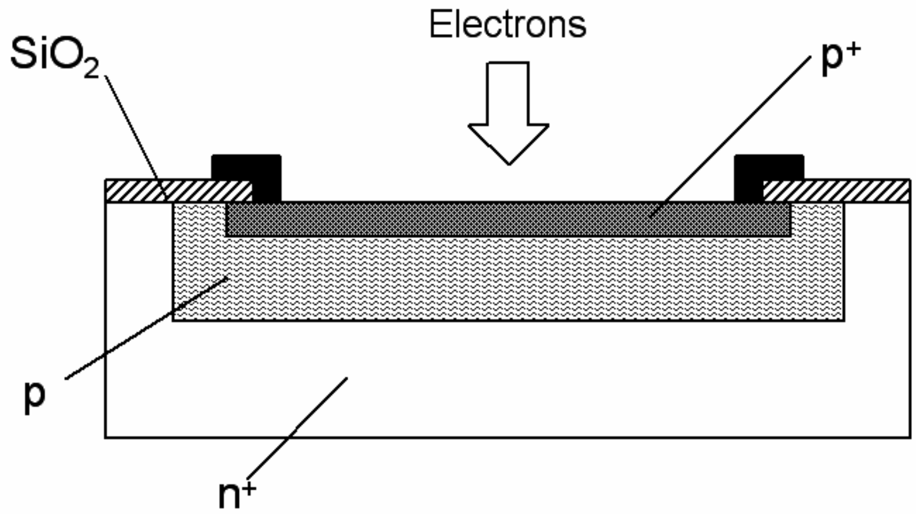


平成17年度構造の特徴

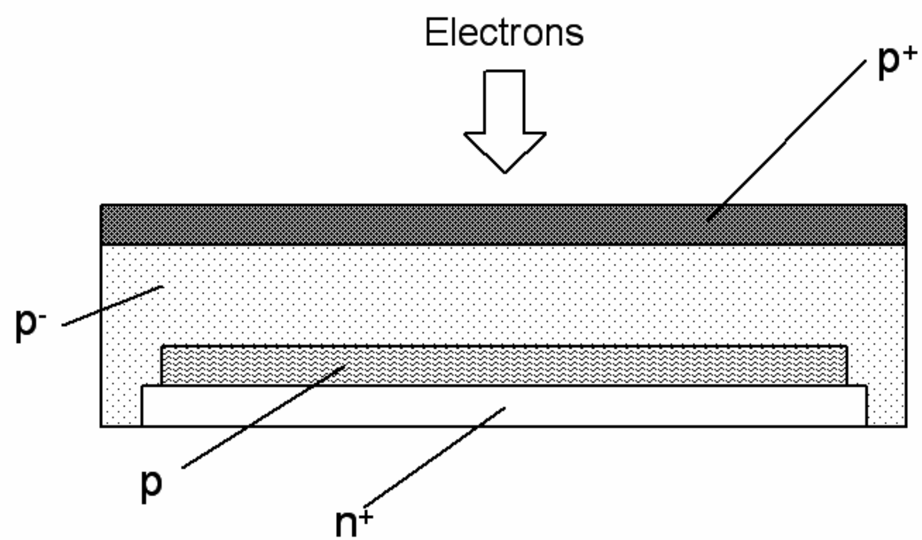
Current version

New version

AD

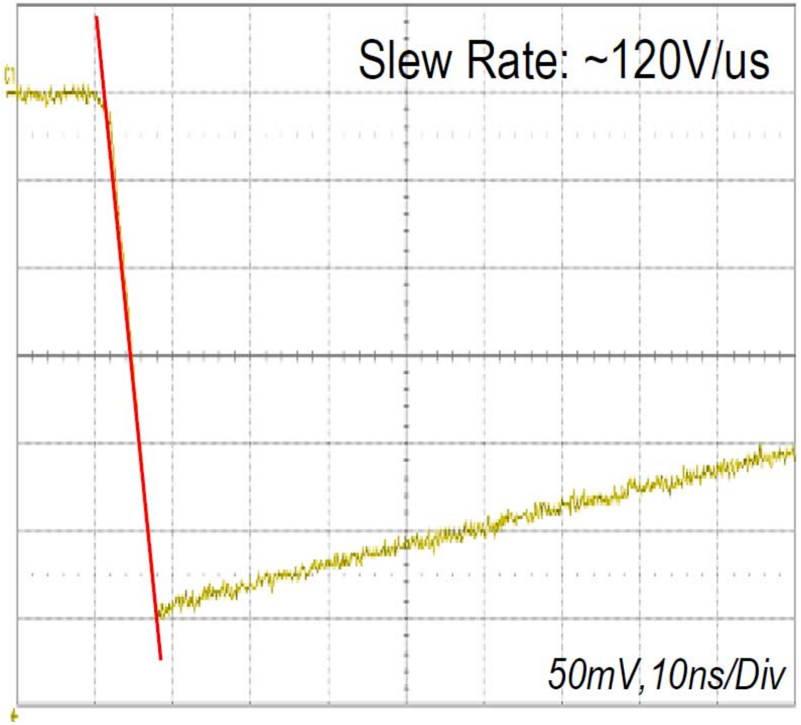


Front-side illumination AD



Back-side illumination AD

Dynamic range

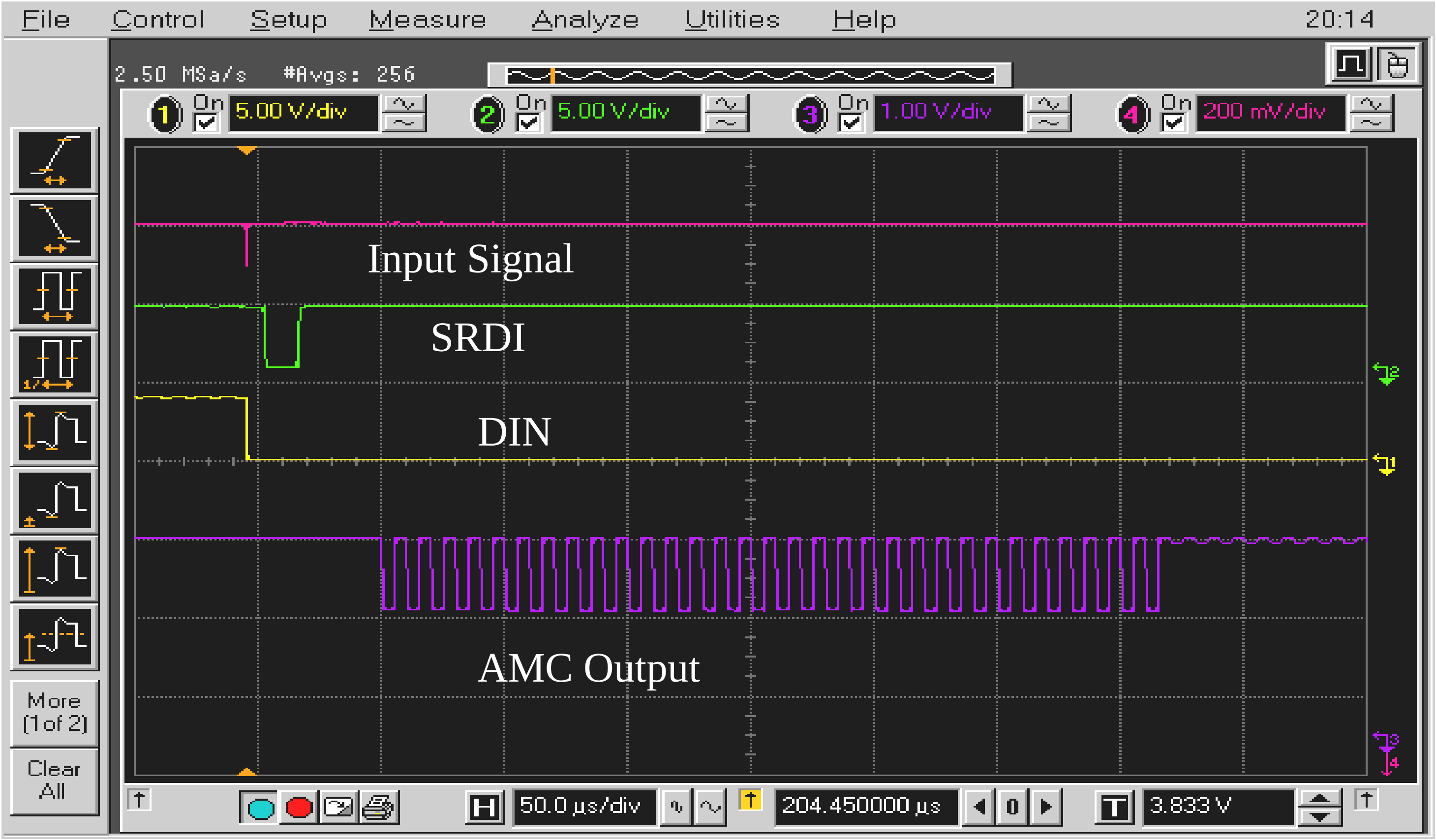


Slew rate (max. ramp-up speed) limits the maximum input photoelectrons.

Dynamic range: **~75p.e.** (raw signal width:5ns, HAPD gain: 10^5)

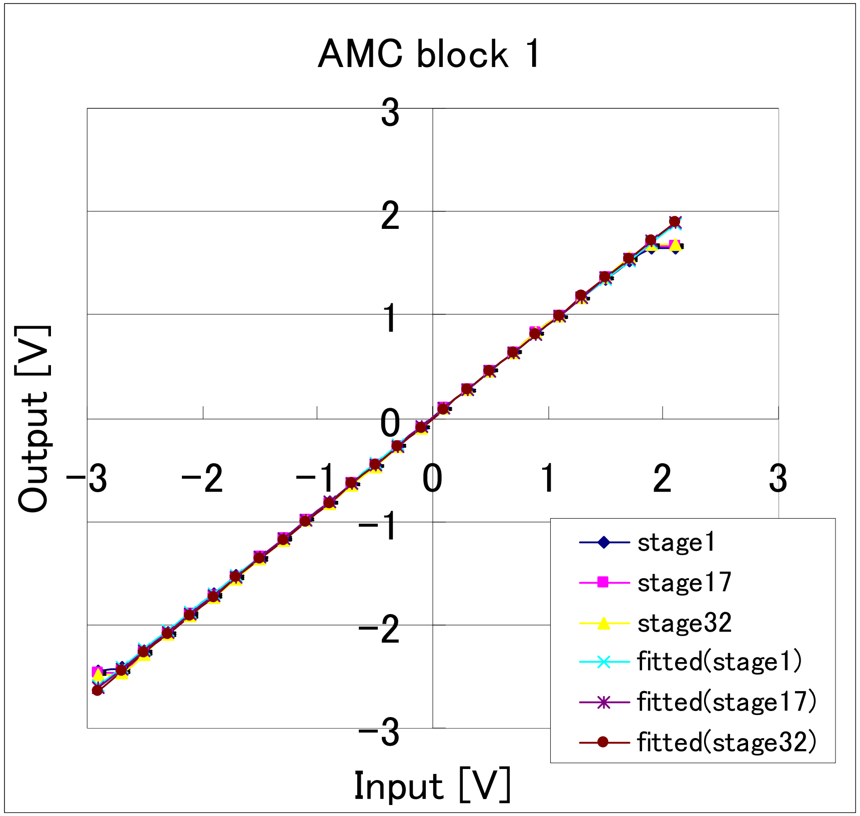
→ Doesn’t meet the requirement (>300p.e.)

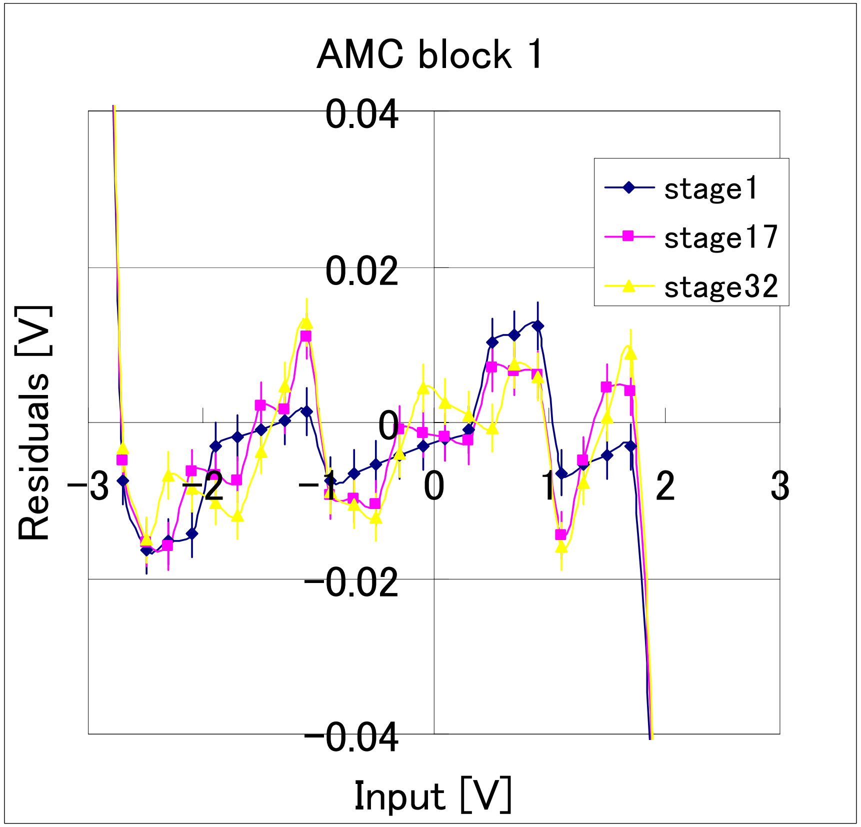
Timing Chart



Readout clock: 100kHz

Resolution of Each Stage

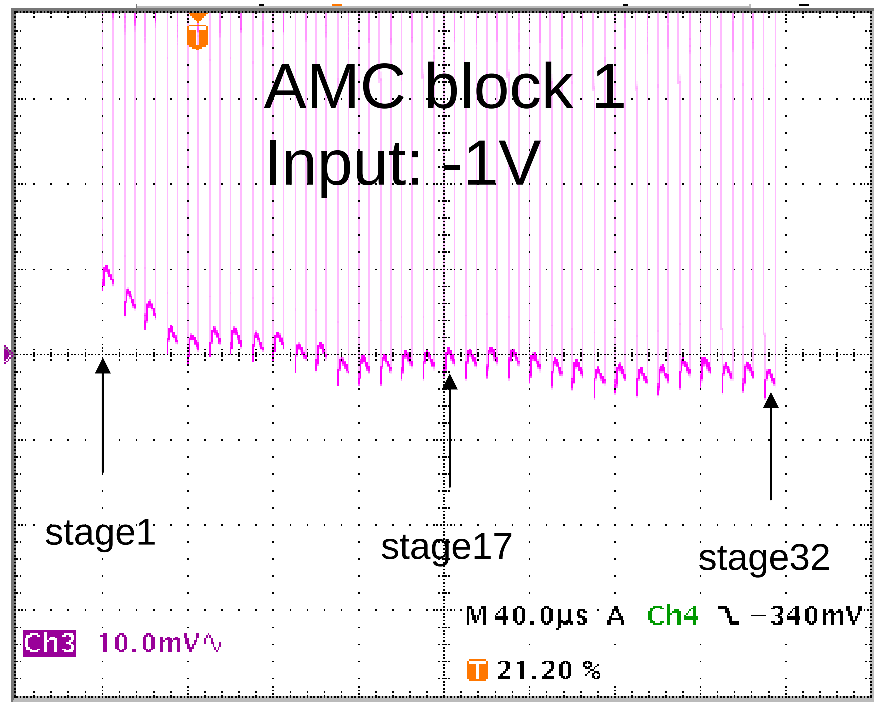


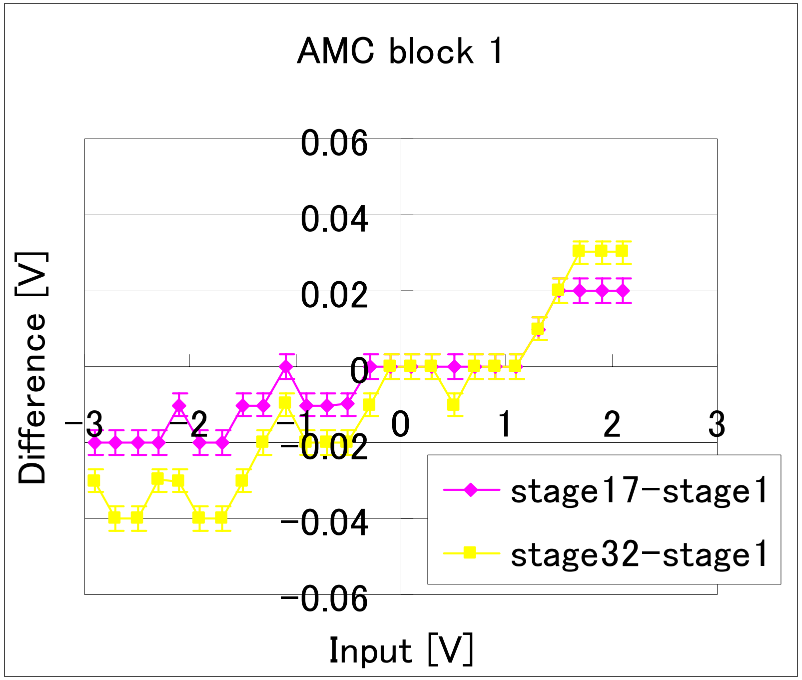


Resolution of each stage: <u>~7bit</u> (at Dynamic range of ~4.5V)

<u>**Doesn't meet the requirement (10bit)**</u>

Stage to Stage Variation of Output Amplitude

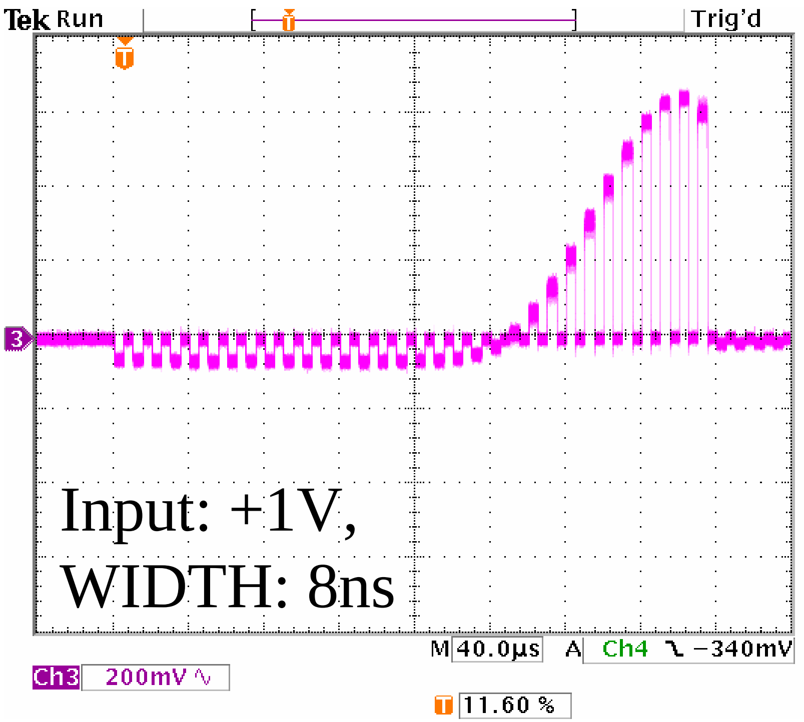


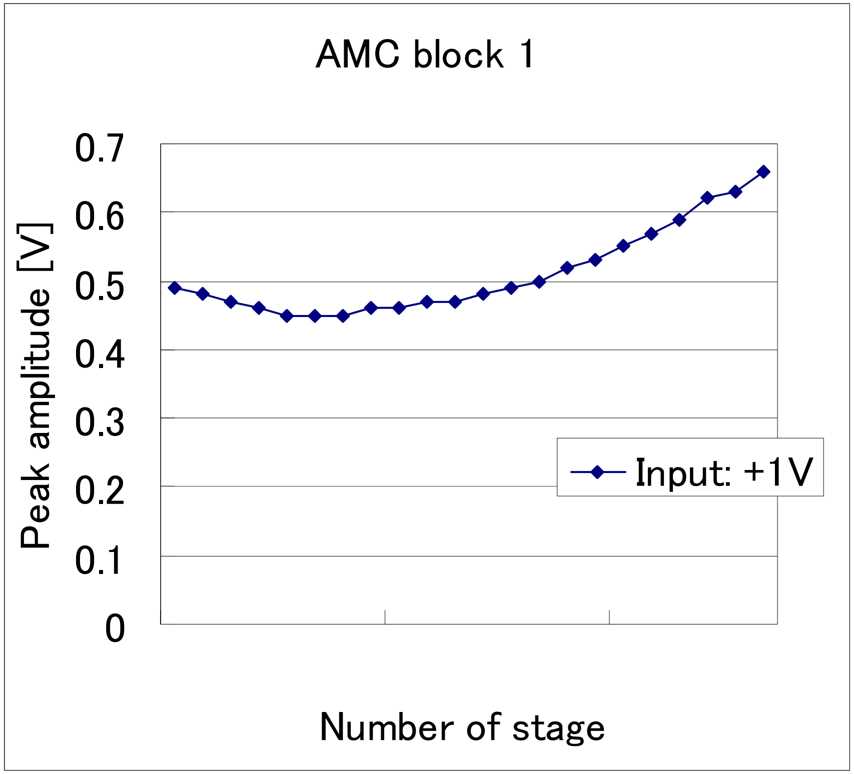


Stage to stage variation ~ 40mV → Resolution of AMC: ~6bit

Doesn’t meet the requirement (10bit)

Pulse Response



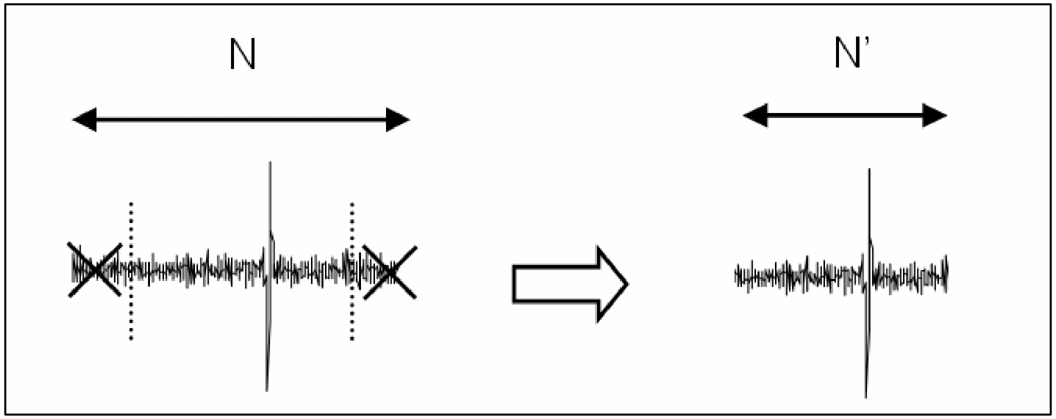


Peak amplitude differs depending on the peak position.

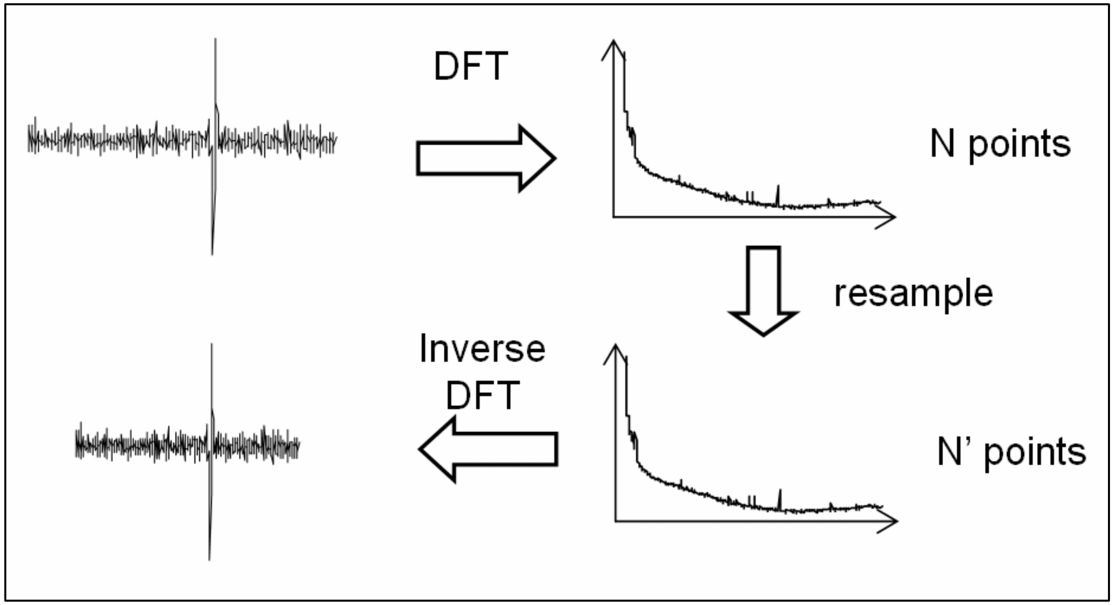
→ Bandwidth of stages is not uniform. (Inappropriate circuit layout?)

Make shorter kernel

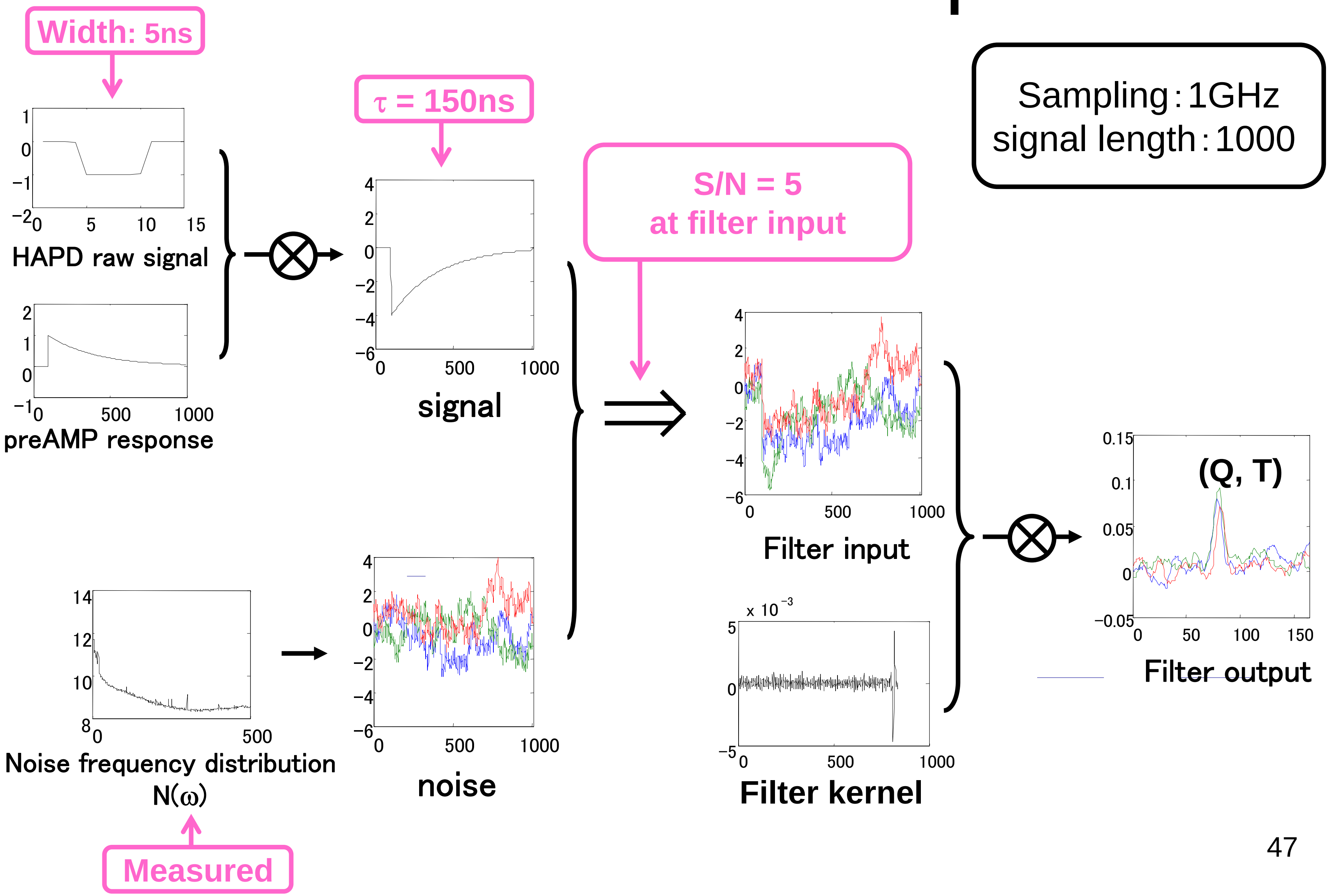
“Cutoff ” method

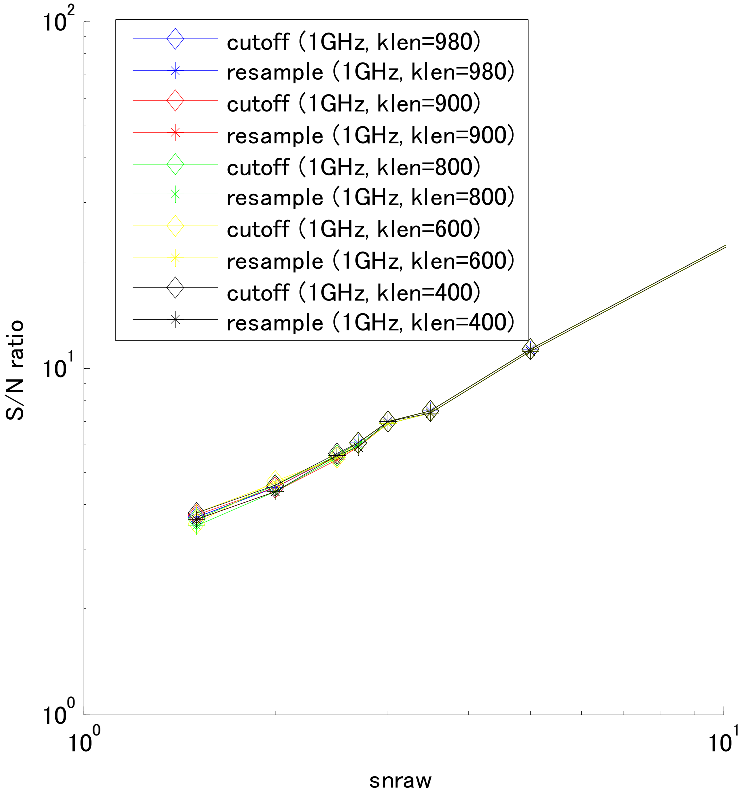


“Resample” method

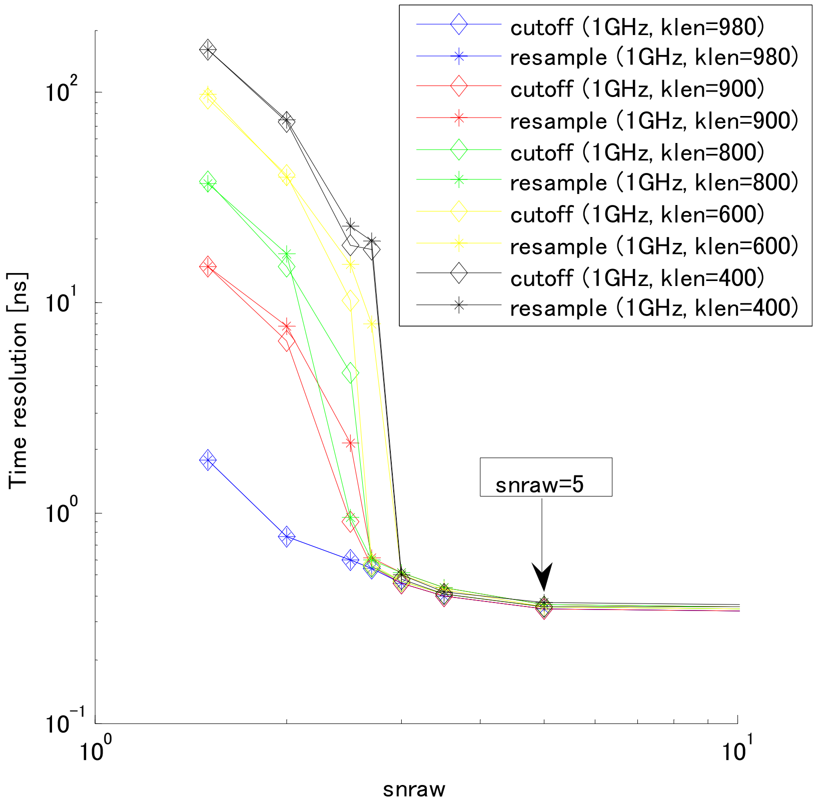


Simulation Setup



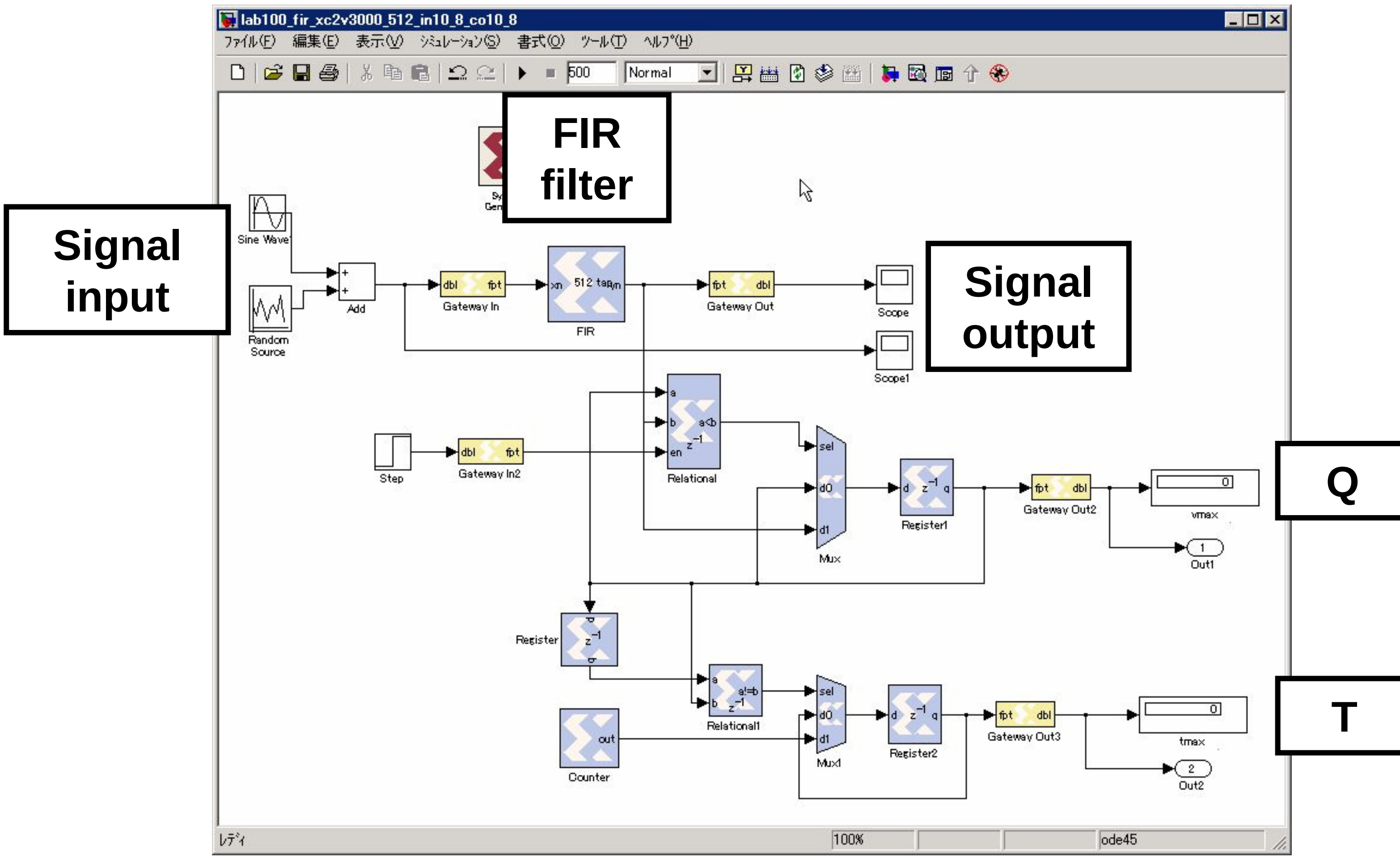


S/N ratio
snraw
cutoff (1GHz, klen=980)
resample (1GHz, klen=980)
cutoff (1GHz, klen=900)
resample (1GHz, klen=900)
cutoff (1GHz, klen=800)
resample (1GHz, klen=800)
cutoff (1GHz, klen=600)
resample (1GHz, klen=600)
cutoff (1GHz, klen=400)
resample (1GHz, klen=400)



Time resolution [ns]
snraw
snraw=5
cutoff (1GHz, klen=980)
resample (1GHz, klen=980)
cutoff (1GHz, klen=900)
resample (1GHz, klen=900)
cutoff (1GHz, klen=800)
resample (1GHz, klen=800)
cutoff (1GHz, klen=600)
resample (1GHz, klen=600)
cutoff (1GHz, klen=400)
resample (1GHz, klen=400)

FPGA Implementation



MATLAB/Simulink + SignalMaster