Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip

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ABSTRACT: The ATLAS Collaboration will upgrade its semiconductor pixel tracking detector with a new Insertable B-layer (IBL) between the existing pixel detector and the vacuum pipe of the Large Hadron Collider. The extreme operating conditions at this location have necessitated the development of new radiation hard pixel sensor technologies and a new front-end readout chip, called the FE-I4. Planar pixel sensors and 3D pixel sensors have been investigated to equip this new pixel layer, and prototype modules using the FE-I4A have been fabricated and characterized in a 120 GeV pion beam at CERN SPS, before and after module irradiation. Beam test results are presented, including charge collection efficiency, tracking efficiency and charge sharing.

KEYWORDS: ATLAS, upgrade, tracker, silicon, pixel, FE-I4, planar sensors, 3D sensors, test beam.

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1. Introduction

The Insertable B-Layer (IBL) is a fourth pixel layer added to the present pixel detector of the ATLAS experiment at the Large Hadron Collider (LHC), between a new vacuum pipe and the current inner pixel layer. The principal motivations of the IBL are to provide increased tracking robustness as the instantaneous luminosity of the LHC increases beyond the design luminosity of $10^{34} \text{cm}^{-2}\text{s}^{-1}$ for the efficient readout of the existing pixel detector, to provide an additional layer for improved pattern recognition as the increasing radiation fluence deteriorates the existing tracker performance, and to provide improved tracking precision and b-tagging performance for physics signals involving b-quark identification. The IBL will be installed in the ATLAS experiment during the LHC shut-down in 2013-14. It is designed to operate at least until a full tracker upgrade planned for high luminosity LHC (HL-LHC) operation foreseen from approximately 2023.

The constraints of the IBL project are stringent, and have influenced the mechanical, sensor and electronics technologies developed for the detector. The small radius of the IBL requires a more radiation hard technology for both the sensors and the front-end electronics, with a required radiation tolerance for fluences of up to $6 \times 10^{15} \text{n}_{eq}/\text{cm}^2$ NIEL and 250 MRad TID. The high occupancy of the individual pixel elements profits from a more efficient front-end readout. The available space does not allow module overlaps in the longitudinal direction (along the beam) and sensors with either an active edge or a slim edge guard ring have been developed to reduce geometrical inefficiencies. Radiation induced displacement damage of silicon sensors causes an increased sensor leakage current ($I_l$), resulting in an increase of noise in the analog front-end, and an increased detector bias voltage ($V_b$) needed for full depletion ($V_d$). Depending on the sensor technology, operating voltages of up to 1000 V are required. Most important, the colling requirements are more stringent. Minimizing the material is very important to optimize the tracking and vertexing performance, and the average radiation length target is 0.015 $X_0$ per layer for perpendicular traversing tracks, as opposed to 0.03 $X_0$ for existing pixel layers. This is achieved using aggressive technology solutions, including a new module based on optimized sensor and front-end chip designs, local support structures (staves) made of recently developed low density, thermally conducting carbon foam, the use of CO$_2$ evaporative cooling which is more efficient in terms of mass flow and pipe size, and electrical power services using aluminum conductors.

Figure shows the new IBL detector. It will consist of 14 staves, located at a mean active geometric radius of 33.4 mm, each loaded with silicon sensors bump-bonded to the newly developed front-end integrated circuit (IC) FE-I4. Figure shows an individual stave. Figure also shows the module design using the FE-I4 IC and either a planar or 3D sensors. The planar sensors will be bump-bonded to 2 ICs, while the 3D sensors will be bump-bonded to a single IC. The ATLAS collaboration intends to build modules using the FE-I4 IC and both planar and 3D sensor technologies for the IBL. This paper describes the development and test of IBL modules using prototype sensors and the FE-I4A prototype IC. Measurements of the module performance have been made before and after irradiation to the fluence levels expected during IBL operation.

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1 The non-ionising energy loss (NIEL) is normally quoted as the equivalent damage of a fluence of 1 MeV neutrons ($\text{n}_{eq}/\text{cm}^2$). This is an important measure of the radiation dose for silicon sensors. The Total Ionising Dose (TID) is a more relevant measure of radiation dose for the front-end electronics.
Section 3 describes the FE-I4A prototype IC, an array of 80 columns by 336 rows of 250 × 50 µm² pixel cells covering an active area of 18.8 × 20 mm². After a discussion of the required FE-I4 specifications, the analog and digital architectures of the IC are described, and test results of the FE-I4A IC are presented.

Section 3 describes the requirements, the resulting operational specifications and the subse-
quent technical designs for both the planar and 3D sensor technologies. Measurements are shown for bare sensors of each type. In Section 4, prototype modules that have been constructed for each sensor type are described, and their performances are evaluated and compared with the specification for each type, before and after irradiation to fluences of up to $6 \times 10^{15} \text{neq/cm}^2$.

Finally, the performance of individual prototype modules in a test beam is assessed before and after irradiation in Section 5 and Section 6 provides some conclusions.

2. The FE-I4 Front-End Readout Chip

2.1 Requirements and Specifications for the FE-I4 chip

The present 3-layer ATLAS pixel detector is based on 16-chip modules using the $7.6 \times 10.8 \text{mm}^2$, 2880 pixel FE-I3 readout IC [2], with a pixel granularity $400 \times 50 \mu \text{m}^2$ in a 250 nm feature size bulk CMOS process. The limitations of the FE-I3, in particular its radiation hardness for the fluences expected at the IBL radius and its ability to cope with high hit rates, make the FE-I3 unusable at the IBL radius for the expected LHC luminosities of up to $3 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$. The new FE-I4 IC has been developed with a pixel size of $250 \times 50 \mu \text{m}^2$ in a 130 nm feature size bulk CMOS process, in view of future ATLAS high luminosity pixel applications, and is well matched to the IBL requirements. Using a smaller feature size presents advantages. Firstly, the increased digital circuitry density means that more complexity can be implemented despite the smaller available pixel area, leading to the chip’s ability to cope with much higher hit rates. Secondly, the 130 nm feature size is advantageous in terms of TID hardness, the chip being rated for 250 MRad and therefore able to cope with the IBL environment [6].

The main innovation of the FE-I4 IC is a pixel matrix organization that is radically different from previous pixel hybrid readout IC’s based on a column drain architecture with peripheral data storage and peripheral trigger logic. The local data storage is at the pixel level inside the array until triggering and subsequent propagation of the trigger inside the pixel array. This organization overcomes the efficiency limitation of the FE-I3 architecture. Demonstrations using physics based simulations have shown that the FE-I4 readout will remain efficient up to luminosities of $3 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ at the IBL radius [7, 8].

The 130 nm CMOS process core transistors have a gate-oxide thickness of about 2 nm. The trapping of positive charges in the gate oxide is therefore reduced compared with previous generation processes (250 nm processes typically have a 5 nm gate-oxide thickness), and threshold shifts after irradiation as well as radiation induced leakage current paths are better controlled [8]. The use of specific hardening techniques (e.g. enclosed layout transistors) is no longer necessary for all digital and even for most analog transistors. Guard rings are used for sensitive analog transistors, and minimal sized transistors are in general avoided. However, it is noted that processes with smaller feature sizes are not intrinsically more Single Event Effect (SEE) hard, and the resistance of the design in particular to Single Event Upset (SEU) needs to be assessed (see Section 2.3).

Hybrid pixel readout IC’s are based on analog sections interleaved with digital sections. In the FE-I4 IC, the digital sections are based on standard synthesized cells. This allows to use the full power of available industry tools developed for digital logic synthesis and verification, and not to rely on custom cells developed for our specific application. Digital logic is synthesized from a
high level description language. The digital logic library therefore has at first sight the drawback of
directly coupling the local digital and analog substrates. This would normally be a major concern
for sensitive analog sections that require a noise-free substrate. This problem is avoided in the FE-
I4 by providing a deep n-well option that then allows the isolation of the digital cell local substrate
from the global one, and leads to reduced noise coupling to the analog parts.

The FE-I4 IC consists of an array of 26,880 pixels, 80 in the z-direction (beam direction) by
336 in the azimuthal rφ direction (referring to the ATLAS detector coordinates). The pixel size is
250×50 μm². The rφ granularity was chosen to match the established bump-bonding pitch used
to build existing pixel modules. The pixel length is then chosen to have sufficient area to embed
the more complex digital section, taking into account power routing constraints. The FE-I4 IC is
18.8×20 mm², with 2 mm in the rφ direction devoted to the IC periphery. The IC is the largest so
far designed for High Energy Physics applications. Going to the large FE-I4 size is beneficial in
many respects. It enhances the active over total area ratio, and allows integrated module and stave
concepts. As a consequence, it reduces the inert material and therefore the IBL material budget,
resulting in a significant enhancement in physics performance, for example the b-tagging efficiency
versus light jet rejection factor [1]. A large FE-I4 IC also reduces the bump-bonding cost which
scales as the number of manipulated IC’s (not important for the IBL but an important parameter
for large area detectors such as the outer pixel layers at a future HL-LHC). Such a large IC can
only be designed if a solid power distribution can be established, and a satisfying yield model can
be achieved. The former point is addressed by the powerful features of the CMOS process used,
with 8 metal layers among which 2 are made of thick aluminium (also good to provide effective
shielding). The latter point is addressed by an active yield enhancing policy as will be outlined in
Section 2.2.3. Table 1 shows the main specifications of the FE-I4.

2.2 Design of the FE-I4A chip

Figure 3 shows the layout of the first full scale prototype, the FE-I4A, submitted in Summer 2010.
It is the basic element of all IBL prototype modules tested during 2011. Figure 4 gives an insight
into the IC organization. Each pixel consists of an independent analog section with continuous
reset, amplifying the collected charge from the bump-bonded sensor. In the analog section, hits
are discriminated at the level of a tunable comparator with an adjustable threshold, and charge is
translated to Time over Threshold (TOT) with a proportionality factor that the user can tune by
changing the return to baseline behavior of the pixel (see section 2.2.1). The 26,880 pixel array is
organized in columns of analog pixels, each pair of analog columns tied to a shared digital double-
column unit centred between them. Inside the double-column, 4 analog pixels communicate to a
single so-called “4-pixel digital region” (4-PDR). Details of the architecture and the 4-PDR benefits
will be described in Section 2.2.2. Communication is organized inside the digital double-column
and coordinated with peripheral logic. Section 2.2.3 will describe how communication to the FE is
established and how the data output is organized, as well as give an insight into the major peripheral
blocks. Finally, Section 2.3 will give a few test results.

2.2.1 Analog front-end of the FE-I4A chip

The analog front-end of the FE-I4A is implemented as a 2-stage amplifier optimized for low power,
low noise and fast rise time, followed by a discriminator. A schematic of the analog section is
Table 1. FE-I4 main specifications.

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
<th>Unit (note)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of pixels</td>
<td>80×336 = 26,880</td>
<td>(column × row)</td>
</tr>
<tr>
<td>Pixel unit size</td>
<td>250×50</td>
<td>µm² (direction z × rφ)</td>
</tr>
<tr>
<td>Last bump to physical edge on bottom</td>
<td>≤ 2.0</td>
<td>mm</td>
</tr>
<tr>
<td>Nominal analog supply voltage</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>Nominal digital supply voltage</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>Nominal analog current</td>
<td>12</td>
<td>µA</td>
</tr>
<tr>
<td>Nominal digital current</td>
<td>6</td>
<td>µA</td>
</tr>
<tr>
<td>DC leakage current tolerance per pixel</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>Normal pixel input capacitance range</td>
<td>0-500</td>
<td>fF</td>
</tr>
<tr>
<td>Edge pixel input capacitance range</td>
<td>0-750</td>
<td>fF</td>
</tr>
<tr>
<td>Hit trigger association resolution</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>Single channel ENC</td>
<td>&lt; 300</td>
<td>e⁻</td>
</tr>
<tr>
<td>In-time threshold within 20ns (400fF)²</td>
<td>≤ 4000</td>
<td>e⁻ (at discriminator output)</td>
</tr>
<tr>
<td>Tuned threshold dispersion</td>
<td>&lt;100</td>
<td>e⁻</td>
</tr>
<tr>
<td>Charge → Digital coding method</td>
<td>TOT</td>
<td>(on 4 bits)</td>
</tr>
<tr>
<td>Radiation tolerance (specs met at dose)</td>
<td>250</td>
<td>MRad</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>-40 to +60</td>
<td>°C</td>
</tr>
<tr>
<td>Readout initiation</td>
<td>Trigger</td>
<td></td>
</tr>
<tr>
<td>Maximum number of consecutive triggers</td>
<td>16</td>
<td>(internal multiplication)</td>
</tr>
<tr>
<td>Minimal time between external triggers</td>
<td>125</td>
<td>ns</td>
</tr>
<tr>
<td>Maximum trigger latency</td>
<td>6.4</td>
<td>µs</td>
</tr>
<tr>
<td>Maximum sustained trigger rate</td>
<td>200</td>
<td>kHz</td>
</tr>
<tr>
<td>I/O signals</td>
<td>custom LVDS</td>
<td></td>
</tr>
<tr>
<td>Nominal clock input frequency</td>
<td>40</td>
<td>MHz</td>
</tr>
<tr>
<td>(design includes 20% frequency margin)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal serial command input rate</td>
<td>40</td>
<td>Mb/s</td>
</tr>
<tr>
<td>Output data encoding</td>
<td>8-10</td>
<td>bits</td>
</tr>
<tr>
<td>Nominal data output rate</td>
<td>160 (up to 320)</td>
<td>Mb/s</td>
</tr>
</tbody>
</table>

**Figure 3.** Picture of the FE-I4A IC (with as incrustation the to scale FE-I3 for comparison).
Figure 4. Sketch of the organization of FE-I4A IC.

shown in Fig. 5: it comprises approximately $3/5$th of the total pixel size.

The first stage of amplification consists of a regulated cascode with triple-well NMOS input. The preamplifier uses a continuous current-source reset that gives an approximately linear signal TOT. It contains an active slow differential pair, tying the first stage input to its output, that is used to compensate radiation induced leakage current coming from the sensor and to provide DC leakage current tolerance above 100 nA. The second stage is AC coupled to the first stage, and implemented as a folded cascode with PMOS input. This AC coupling has the advantage of decoupling the second stage from potential leakage current related DC shifts, and of reducing the pixel-to-pixel threshold mismatch. It also gives an extra gain factor coming from the ratio of the second stage feedback capacitance to the coupling capacitance ($\approx 6$ in the actual FE-I4A design). This allows to increase the first stage feedback capacitance with beneficial consequences on charge collection efficiency, signal rise time and power consumption, but with no degradation of the signal amplitude at the discriminator input [3]. Finally, the discriminator has a classic two stage architecture.
For test purposes and calibration, a test charge can be injected at the pre-amplifier input through a set of 2 injection capacitors. Hits can also be injected after the discriminator to test the digital part of the pixel. In total, 13 bits are stored locally in each pixel for tuning of operation: 2 bits for the control of the injection switches, 4 bits for the local tuning of the feedback current of the first stage (they control the return to baseline of the first stage output, hence the charge to TOT conversion factor), 5 bits for the local tuning of the discriminator threshold, 1 bit for switching on the MonHit output (leakage current output) and the HitOR output (global OR of all pixel hits), and the last bit used for masking off the pixel.

2.2.2 Digital organization of the FE-I4A chip

A critical innovation of the FE-I4 IC is its digital architecture, which allows to accept much higher hit rates than was possible with the FE-I3. With a smaller feature size, the trigger can be propagated inside the array and the hits stored locally at pixel level until triggering or erasing. For each analog pixel there exist 5 buffer memories where TOT information can be stored during the trigger latency. Studies have shown that an organization with 4 analog pixels tied to a single 4-Pixel Digital Region (PDR) as shown in Fig. 6 is a very efficient implementation [3].

In this structure, 4 independently working analog pixels share a common digital block. The outputs of the 4 discriminators are fed to 4 separate hit processing units (in purple in Fig. 6) that provide Time-Stamping and compute the TOT. An extra level of digital discrimination can also be programmed, to distinguish large and small recorded charges. When one (or more) of the four hit processing units detects a “large” hit, the unit books one of the central latency counters (in green). Regardless of which of the four pixels has initiated the booking of the latency counter, four TOT memories for the four pixels will be associated to the event, thanks to a fixed geographical association (the 1st latency counter corresponds to 4 1st TOT buffer memories, the 2nd latency counter to 2 2nd TOT memories, and so on).

This architecture presents several advantages. First, it makes good use of the fact that the pixels inside the 4-PDR are in geographic proximity, by sharing some resources. Resource sharing is efficient to record hits, as real hits are clustered. Second, it is advantageous in terms of lowering the power used, as the un-triggered hits are not transferred to the periphery, and some logic.
inside the 4-PDR is common to several hits at a time. Third, it is efficient in terms of time-walk compensation, as one can use the digital discriminator to associate a small hit (below digital discriminator threshold) with a large hit (above digital discriminator threshold) occurring in previous bunch-crossing, by simple geographical association. Finally, it also improves the active fraction of the FE-I4A as the memory is located at the level of the pixels, not in the periphery.

2.2.3 Periphery of the FE-I4A chip

The periphery schematic of the FE-I4A is shown in Fig. 6. It contains blocks that fulfill the following operations: communication and operational tuning of the IC; organization of the data read back and fast data output serialization. Finally some blocks are implemented to provide extra testing capabilities (e.g. redundant memories, low speed multi-purpose multiplexer), or as prototype blocks for the future production IC (e.g. powering section).

Two LVDS inputs are required to communicate to the FE-I4A: the clock (nominally 40 MHz); and the command input Data-In (40 Mb/s). In the FE-I4 command decoder, the command stream is decoded into local pixel configuration, global configuration and trigger commands. It is based on the module control chip of the existing ATLAS pixel detector. No separate module control chip is needed for the IBL, further reducing the IBL mass. The pixel configuration is sent to the pixels for storage in the 13 local register bits of the pixel. The global configuration is stored in SEU-hardened configuration registers using Dual Interlock storage CEII (DICE) latches and triplication logic. The 32 16-bit deep registers are used for global tuning of the operation of the chip. In the bias generator section, based on an internal current reference, DACs convert the stored configuration values to voltages and currents needed to tune the various sections of the IC. The decoded trigger is propagated to the pixels and to the “End of Chip Logic” block where the readout is initiated.

When a trigger confirms a hit (the coincidence of a trigger with a latency counter reaching its latency value inside a 4-PDR), data stored in the 4-PDR TOT buffers are sent to the periphery and associated to the bunch-crossing corresponding to the specific trigger. In the double-column,
the 4-PDR address as well as the 4 TOTs are propagated to the End of Chip logic (the transmitted
signals are Hamming coded for yield enhancement). The data are then re-formatted (for band-width
reduction and to facilitate the following data processing steps) and stored in a FIFO to be sent out.
In addition to stored pixel data, read back information from pixel and global registers, as well as
some diagnostic information (error messages), can be included. The data is then 8b10b-encoded
in the Data Output Block and serialized at 160 Mb/s. Fast serialization is made possible by
use of a high speed clock provided by a Phase Lock Loop clock generator [13]. The custom LVDS
receiver and transmitter have been described elsewhere [14].

In addition, a few structures are used for test purposes, for example the IOMux-based redundant
configuration memories that also provide diagnostic access to various signals and the prototype
powering section (Shunt-LDO [15,16] and DC-DC converters [17]).

During implementation, design strategies have been followed to SEU-harden the FE-I4A: the
test of 2 flavors of DICE latches for the in-pixel memories; DICE-cells with interleaved layout
and triplication logic for the global configuration; and triplication of counters and logic in the
End of Chip Logic block. The yield enhancement for such a large IC has also been an important
consideration: the use of Hamming coding with a minimal number of gates for the data transfer
in the array; triplication and majority voting for the peripheral Command Decoder; redundant
(and user selectable) configuration shift registers in each double-column; triple redundant read
token passing inside the double-column and at the level of the End of Digital Column logic; the
use of lithography friendly bus widening and bus spacing; and using multi-via digital cells when
synthesizing the design.

2.3 Test results on bare FE-I4A

2.3.1 The USBpix system

Most of the testing of both the bare FE-I4 chips and the subsequent pixel modules has been made
with a portable USB data acquisition system called USBpix [18]. USBpix is a modular test system,
developed for lab measurements with FE-I3 and FE-I4 chips. It consists of a Multi-IO board that
provides a USB interface with a micro controller, a FPGA and 2 MB of on-board memory. The
Multi-IO board is connected to an adapter card that is specific to the choice of FE-I3 or FE-I4 chip
to be tested. The adapter card provides all signals to the chip using LVDS transmitters or CMOS
level shifters. The FE-I4 adapter card allows to either route all power and signal lines via a flat
cable to the chip, or to connect power lines and signal lines separately in which case the signals are
routed via an RJ45 connector to the chip.

2.3.2 Characterization of bare FE-I4A chips

The analog pixel, the 4-PDR implementation, the communication and programming, and the data
output logic path, have all been successfully characterized for the prototype FE-I4A IC.

The two main contributions to the FE-I4A analog power consumption are the biasing of the
pre-amplifier and of the discriminator. The digital power is the sum of a static contribution and a
contribution that is proportional to the hit rate. Typical values for operation are approximately 16
\( \mu \text{W/pixel} \) for the analog power and 7 \( \mu \text{W/pixel} \) for the digital part, giving a total power consump-
tion of approximately 160 mW/cm\(^2\).
The measured noise value depends on the operational parameters. For typical operation, a bare IC shows a noise in the range 110-120 ENC for a 3000 e\(^{-}\) threshold. After tuning, the IC shows a threshold dispersion of order 30-40 e\(^{-}\), well within specification. Calibrations of the FE-I4A require source measurements and are therefore difficult to make. The calibration results quoted in units of electron ENC therefore have an intrinsic 10-20 % normalisation uncertainty.

As expected, the 130 nm technology used for the IC design is very radiation tolerant. Three fully powered bare ICs have been exposed to TID doses of respectively 6, 75 and 200 MRad in an 800 MeV proton beam at the Los Alamos Laboratory. Over this range of irradiations, the measured threshold dispersion was almost unchanged, and the noise increased by 15-25 % in comparison to pre-irradiation values.

FE-I4A wafers have been tested in collaboration laboratories. The selection criteria included the analog and digital power taken by the ICs in different configuration states, global configuration scans, local pixel configuration scans, the analog and digital pixel maps, and the threshold and noise pixel maps. The criteria retained were sufficient for the purpose of building high quality prototype modules in the first phase of prototyping. With this custom testing, the wafer yield (on a sample of 21 wafers) reached on average close to 70%. Nevertheless, to enhance the failure mode coverage of the test primitives, the future wafer probe test list will address more points, for example enhanced coverage of failure mechanisms in the 4-PDR, cross-talk assessment, current probing as a function of activity and the testing of stuck at bits in the synthesized peripheral digital blocks through scan chain probing.

The command decoder, the configuration register section and the DACs have been extensively characterized and only minor tuning was needed in the IBL production IC iteration (FE-I4B). The data output path, the data readout organization in the end of chip logic (EOCHL) block, the 8b10b encoder making use of the PLL-based generated high frequency clock and the LVDS transmission at 160 Mb/s have all been successfully characterized. For the FE-I4B IC iteration, new functionalities have been added to the EOCHL based on DAQ requirements, including increasing the bunch crossing and trigger counters, and the implementation of a user-defined event size limit. Based on test results, a specific flavour of the FE-I4A pixel implementation was selected and the modifications brought to the periphery were of limited scope to ensure robustness of the FE-I4B production IC.

The results, together with pre- and post-irradiated test results when bump-bonded to both planar and 3D sensors (see Sections 4.2 and 4.3), indicate that the FE-I4 IC is a very solid component for future IBL module developments.

3. The IBL Sensor Design and Performance

As noted in Section 1, the main challenge for the IBL sensor is to retain adequate detection efficiency following fluences up to \(6 \times 10^{15} \text{ n}_{\text{eq}} / \text{cm}^2\) (the current ATLAS pixel sensor, APS, is specified for a fluence of \(10^{15} \text{ n}_{\text{eq}} / \text{cm}^2\)). Several promising new sensor technologies have been developed, for example advanced silicon designs [19, 20, 21, 22], p-CVD diamond sensors [23] and pixelised gas detector concepts (GOSSIP) [24]). Because of the tight IBL construction schedule, n\(^{+}\)-in-n planar and double-sided 3D silicon pixel sensor technologies driven by the ATLAS Upgrade Pla-
The prototype IBL sensor design is based on established prototype designs using the FE-I3 IC, but it is modified to match the FE-I4 geometry, to minimize the radial envelope of the IBL and to minimize the material thickness of the IBL layer. To match the FE-I4 geometry, the pixel size is $50 \mu m \times 250 \mu m$. The pixel matrix is enlarged to 336 rows $\times$ 80 columns so that the area of an FE-I4 IC covers nearly six times the area of an FE-I3 IC. The high fabrication yield of planar sensors has allowed the adoption of Multi Chip Sensor modules (MCS) having 2 FE-I4 ICs. For 3D sensors, yield limitations mandate the use of Single Chip Sensor modules (SCS). The small radial space between the beam pipe and the current b-layer prevents the use of shingled modules to ensure hermiticity. Due to this constraint, a flat arrangement of the modules on the staves is foreseen for the IBL. To guarantee a sufficient hermeticity of the detector layer, the inactive sensor edge must be minimized in the z-direction along the stave.

An additional change concerns the position of bump pads to access the bias-grid ring (DGRID) and the outer guard implantation which takes up all edge leakage currents (DGUARD). These bumps are routed via the read-out chip and should normally be DC-connected to GND to be able to channel leakage currents. In the FE-I4 design, these bump pads are placed within the second and second last column (DGRID) and within the third and third last column (DGUARD). The FE-I4 planar design is compared with that of the existing pixel sensor in Fig. 7. For 3D sensors, no bias grid mechanism exists and DGRID is generally not used. There are, however, guard fences which can be connected to GND via the DGUARD or DGRID.

Regardless of technology, the following sensor requirements follow from the operational conditions.

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3Within the FE-I4A, the two bumps are shorted together while for the FE-I4B, they will be separately accessible.
• An inactive edge width $< 450 \mu m$ for 2-chip sensors (MCS) and $< 225 \mu m$ for 1-chip sensors (SCS) is required. This value translates into a geometric efficiency of 97.8% (without taking into account any necessary gaps) and is deemed to be the upper tolerable limit for geometric inefficiencies.

• A sensor thickness between 150 and $250 \mu m$ is required. The current APS sensor thickness of $250 \mu m$ is a conservative upper limit. Thinner sensors would reduce the material budget and for planar sensors would also yield more charge at a fixed bias voltage after irradiation.

• A power dissipation $< 200 \text{mW/cm}^2$ at $V_b = 1000 \text{V}$ bias voltage is specified. This specification limits the sensor power dissipation to approximately that dissipated by the FE-I4. The specification is used as input for cooling design and thermal runaway calculations.

• The maximum leakage current is specified to be $< 100 \text{nA/pixel}$. This is the maximum pixel current allowed by the FE-I4 compensation specification.

• The sensor operating temperature should be $< −15^\circ$ at $< 200 \text{mW/cm}^2$. This maximum temperature is specified to engineer the cooling system.

• The hit efficiency is specified to be $> 97\%$ after a benchmark fluence of $5 \times 10^{15} \text{n}_{eq}/\text{cm}^2$ at a maximum $V_b < 1000 \text{V}$. This hit inefficiency specification is chosen to limit the degraded performance after irradiation. The limit does not include geometric inefficiencies.

The IBL will consist of a combination of $n^+\text{-in-}n$ MCS modules using planar sensors and 3D $n^+\text{-in-p}$ SCS modules using 3D sensors. Specific details of the two designs are discussed in the following sub-sections. However, both planar and 3D prototypes discussed in this paper are of the SCS type.

3.1 The planar sensor design

The baseline IBL planar sensor is an electron-collecting $n^+\text{-in-}n$ silicon sensor design fabricated by CiS\textsuperscript{4}. The $200 \mu m$ thick lowly n-doped substrate contains a highly n$^+$-doped implantation on the front side and a highly p$^+$-doped implantation on the back side. It is based on the current APS design [27] also fabricated by CiS.

The p$^+$ implantation is made as a single large high voltage pad opposite the pixel matrix, that is surrounded by 13 guard ring implantations with a total width of approximately 350 $\mu m$. The purpose of the guard rings is to provide a controlled potential drop from the high voltage pad to the grounded cutting edge. The guard ring scheme is adopted from the original APS design that used 16 guard rings and was optimised during previous studies [28] to find the combination of number of guard rings and dicing street position that allows the most slim edge while still allowing safe depletion before irradiation\textsuperscript{5}.

\textsuperscript{4}CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Konrad-Zuse-Strasse 14, 99099 Erfurt, Germany

\textsuperscript{5}$n^+\text{-in-}n$ sensors deplete from the p$^+$-implant and must be operated fully depleted before type inversion to ensure inter-pixel isolation.
The n⁺ implantation is segmented into a matrix of 80 columns and 336 rows of mostly 250×50 μm² pixels surrounded by an inactive edge region. The inter-pixel isolation is adapted from the APS sensor and follows the moderated p-spray concept [29]. The outermost columns contain long pixels that are extended to 500 μm length and overlap about 250 μm with the guard ring structure. Due to the non-vertical inhomogeneous electric field, not all of the overlap region is efficient/active. Before type inversion [30], the inactive edge width is below 250 μm rather than 450 μm without overlap. After type inversion, the hit efficiency drops below 50%, defining the start of the inactive region, even closer to the cutting edge because the depletion zone grows from the n⁺ pixel implant.

Figure 8. Comparison of the edge region of the current ATLAS Pixel (APS) design (upper) and the IBL planar sensor design (lower).

To ease characterization and to avoid a floating potential on pixels having an open bump connection, a punch-through network (bias grid) following the APS design was implemented even though this is known to lead to reduced charge collection efficiency in the bias-dot region after irradiation. The bias dots are always located at the opposite side of a pixel cell with respect to the contact bump (see Fig. 7). The bias grid is connected to an approximately 90 μm wide bias grid ring which surrounds the pixel matrix. Outside the bias ring, a homogenous n⁺-implantation (designated as the outer guard, edge implant or DGUARD) extends to the dicing streets and ensures that the sensor surface outside the pixel matrix and the cutting edges share the same potential.

Each pixel, the bias grid and the outer guard are connected to the FE-I4 read-out chip via bump-bonds. As already noted, there are two bumps each for the bias grid (DGRID) and outer guard (DGUARD).

The prototype wafer mask contained two versions of FE-I4 sensors, the slim-edge design described above and a conservative design where the edge pixels were only 250 μm long without any overlap between pixel and guard rings. Both designs behaved identically except for the edge efficiency where the conservative design showed the expected 450 μm inactive edge. It is the slim-edge design that is described in this paper.

The production used n-doped FZ silicon wafers with <111> crystal orientation and 2-5 kΩ cm bulk resistivity which were thinned to thicknesses of 250, 225, 200, 175 and 150 μm. All wafers were diffusion oxygenated for 24 hours at 1150°C after thinning, as for the current APS production.
The remaining production steps are as for the APS sensor: thermal oxide deposition, n⁺-implantation, tempering, p⁺-implantation, tempering, nitride deposition, p-spray implantation, tempering, nitride openings, oxide openings, aluminium deposition and patterning, and passivation deposition.

The production of 5 different thicknesses aimed at obtaining experience of the production yield without the use of support wafers; thin sensors are preferred because they can be operated at lower bias voltage and because of the reduced detector material. After irradiation, they also tend to give more collected charge for the same bias voltage. The production yield was stable down to the 175 μm batch. However, the bump-bonding vendor required at least 200 μm thick 4” wafers to be able to apply Under-Bump Metallisation (UBM)⁶ without the need for an additional support wafer. A 200 μm sensor thickness was therefore proposed for the IBL production. No yield difference was measured between the slim-edge and conservative designs and so the slim-edge design was selected as the baseline geometry.

The floor plan of the IBL prototype production includes one MCS and two SCS sensors for each of the slim-edge and conservative designs in the central part of the wafer. In addition, several FE-I3 compatible sensors, diodes and dedicated test structures are included in the periphery of the wafer.

### 3.2 The 3D Sensor Design

The 3D sensor fabrication uses a combination of two well established industrial technologies: MEMS (Micro-Electro-Mechanical Systems) and VLSI. The micromachining used in MEMS is applied to etch deep and very narrow apertures within the silicon wafer using the so-called Bosch process [32] followed by a high temperature thermal diffusion process to drive dopants in to form the n⁺ and p⁺ electrodes. Two etching options have been considered for the prototype 3D sensors: Full3D with active edges and double-side 3D with slim fences. For the first option, etching is performed from the front side, with the use of a support wafer and at the same time implementing active edge electrodes, but this requires extra steps to attach and remove the support wafer. In the second option, etching is made from both sides (n⁺ columns from the front side, p⁺ columns from the back side) without the presence of a support wafer.

For the prototype 3D sensors reported here, the double-side option with slim fence was chose since all the technological steps were reliable and well established. It should be noted that all of the remaining processing steps after the electrode etching and doping are identical to those of a planar silicon sensor. In particular, both the 3D and planar sensors have the same handling and hybridization requirements.

The 3D silicon sensors use 4” FZ p-type high resistivity wafers having specifications normally used for fabrication of high resistivity p-type silicon sensors. The wafers were supplied by TOP-

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⁶UBM is a post-processing galvanic application of a sandwich of metals to make the aluminium bump-bonding pads solderable. The choice of UBM depends on the bump-bonding process (Pb/Sn, Ag/Sn, Indium reflow, Indium stud bumps).
SIL to two manufacturers in the 3D Pixel Collaboration: CNM-CSIC and FBK. Figure show details of the 3D layout for the CNM (a) and and FBK (b) sensors.

The main difference between the two sensor versions regards the column depth: in CNM sensors, columns do not traverse the substrate but stop at a short distance from the surface of the opposite side, whereas FBK sensors have traversing columns. Another difference concerns the isolation implantation between the $n^+$ columns at the surface: p-stops are implanted on the front side of CNM sensors while FBK sensors use p-spray implantations on both sides. The slim edge guard ring design in CNM sensors is made using the combination of a $n^+$ 3D guard ring that is grounded, and fences that are at the bias voltage from the ohmic side. In FBK sensors, the slim edge fence consists of several rows of ohmic columns that effectively stop the lateral depletion region from reaching the cut line, thus significantly increasing the shielding of the active area from edge effects.

The core of the prototype wafer layout is common for both CNM and FBK sensors, and contains 8 single chip sensors adapted for the FE-I4A IC, 9 single chip sensors compatible with the currently installed Atlas FE-I3 IC, and 3 pixel sensors compatible with the CMS-LHC experiment front-end readout IC. At the wafer periphery, test structures that are foundry specific are added to monitor the process parameters and to perform electrical tests.

### Table 2. 3D sensor specifications.

<table>
<thead>
<tr>
<th>Item</th>
<th>Sensor Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tile type</td>
<td>single</td>
</tr>
<tr>
<td>Number of $n^+$ columns per 250 $\mu$m pixel</td>
<td>2 (so-called 2E layout)</td>
</tr>
<tr>
<td>Sensor thickness</td>
<td>$230 \pm 20 \mu$m</td>
</tr>
<tr>
<td>$n^+$-$p^+$ columns overlap</td>
<td>$&gt; 200 \mu$m</td>
</tr>
<tr>
<td>Sensor active area</td>
<td>$18860 \mu m \times 20560 \mu m$ (including scribe line)</td>
</tr>
<tr>
<td>Dead region in Z</td>
<td>$&lt; 200 \mu m$ guard fence $\pm 25 \mu m$ cut residual</td>
</tr>
<tr>
<td>Wafer bow after processing</td>
<td>$&lt; 60 \mu m$</td>
</tr>
<tr>
<td>Front-back alignment</td>
<td>$&lt; 5 \mu m$</td>
</tr>
</tbody>
</table>

### 3.3 Measurements of fabricated sensors

The main measurements used for production quality assurance (QA) are $I - V_b$ and $C - V_b$ curves, measured for all batches after production and after dicing. Only the final measurement is relevant to the overall production yield and QA acceptance.

For planar sensors, the $I - V_b$ curve measures the sensor leakage current via the bias grid by placing the sensor with the n-side onto a metal chuck and applying high voltage to the p-side HV pads. The metal chuck connects the n-implanted cutting edge and a punch-through is formed between the outer guard and bias grid ring. The $C - V_b$ curve measures the depletion voltage $V_d$.
by sensing the plateau in capacitance that is reached after the bulk is fully depleted. To ensure safe
depletion, a breakdown voltage $V_{bk} > (V_d + 30)\, V$ is required for accepted devices.

For both 3D manufacturers, $I - V_b$ measurements are made on each sensor at the wafer scale
using probe stations, using a removable temporary metal (FBK) or measuring the guard ring current
(CNM). Working 3D sensors were required to satisfy the following electrical specifications at room
temperature (20-24 $^\circ$ C):

- $V_d \leq 20\, V$ and $V_b \geq V_d + 10\, V$ (by construction $V_b$ and $V_d$ are much lower than for planar
  sensors);
- Leakage current $I(V_b) < 2 \, \mu A$ per tile and $I(V_b)/I(V_b - 5\, V) < 2$;
- Guard-ring current before bump-bonding $I_{guard}(V_b) < 200\, nA$ per tile;
- Breakdown voltage $V_{bk} > 25\, V$.

After processing the accepted 3D FE-I4A SCS-type sensors also satisfied the geometrical speci-
fications of Table 5.
For the planar IBL qualification production, successive measurements have been made on all batches after production, after UBM application and after dicing. Figure 10 displays I−Vb measurements from 4 wafers of 200µm thick sensors after the UBM and dicing steps. Only a few sensors exhibit early breakdown; the depletion voltage was measured to be Vd < 40 V and hence a requirement Vbk > 70 V was applied. The production yield including UBM and dicing post-processing was approximately 90%.

The temporary metal selection method used by FBK allows a measurement of I−Vb at the column level in each sensor. A temporary metal line is deposited after the completion of the process, as in Fig. 11 (a). Probing pads, on the left hand side of the figure and placed outside the active region to avoid surface damage, are used to measure the I−Vb at column level. This operation is made automatically on pixels corresponding to the 80 FE-I4A columns by using a dedicated probe card. Each I−Vb measurement therefore tests the performance of 336 pixels, allowing a fine definition of potential defects. After this operation is completed and I−Vb curves obtained, the temporary metal is removed. An example of the measurement is shown in Fig. 11 (b) where I−Vb measurements from all 80 columns are added together to provide an I−Vb measurement of the full sensor for the FBK 111 and FBK 112 modules. I−Vb measurements after bump-bonding show only a small increase of the sensor leakage current, and confirm the measurement method.

The guard ring I−Vb measurement used by CNM is sensitive to defects on the sensor edges, that used have been shown to be indicative of the bulk sensor behaviour. A photograph of the guard ring probing pad is visible in Fig. 12 (a). The guard ring current is not a measurement of the full sensor current but should provide a reproducible selection test based on Vbk. Tests performed before and after bump-bonding support this measurement method, as can be seen in Fig. 12 (b).
Figure 11. (a) FBK temporary metal used for sensor selection on wafer. Details are visible for two columns. On the left the metal line termination on probing pads outside the active region to avoid surface damage. (b) $I - V_b$ measurements of the FBK 111 and FBK 112 modules, before and after bump-bonding but before irradiation. The on-wafer curve corresponds to the sum of the 80 columns $I - V_b$ characteristics of 336 pixels joined together by an aluminium strip. Each measurement is recorded twice to check reproducibility.

where $I - V_b$ measurements have been recorded before and after bump-bonding. The difference in leakage current is due to the reduced volume probed through the guard ring pad.

Further $I - V_b$ measurements of FBK and CNM sensors after bump-bonding are discussed in Section 4.2.

Figure 12. (a) Corner picture of one of the CNM 3D sensors showing the guard ring surrounding the pixel active area and guard ring probing pad. (b) Guard ring leakage current measured as a function of the bias voltage for 3 CNM 3D sensors before bump-bonding. The full sensor current is also shown after bump-bonding to the FE-I4 readout electronics.

4. The IBL Module

As already discussed in Section 3, prototype FE-I4A compatible sensors have been fabricated by CiS (planar sensors) and by FBK and CNM (3D slim edge sensors). The planar sensors are of two
types: MCS sensors as foreseen for the final IBL planar modules, and smaller SCS sensors foreseen for the final 3D modules. All of the prototype modules described in this paper, either planar or 3D silicon, are of the SCS type, with a single FE-I4A IC bump-bonded to the sensor.

The focus of this section is to provide test characterizations of the SCS modules constructed, both pre-irradiation and post-irradiation, and to compare the data with that obtained using the individual sensors. As noted previously, $I - V_b$ and $C - V_b$ measurements are made, and in addition TOT measurements of the collected charge, for a given threshold setting\(^{10}\). Unless explicitly stated, all un-irradiated pixel modules were characterized at room temperature (20 – 24°C), while irradiated modules were characterized at −15°C.

Data from irradiated modules result from irradiations at KIT\(^{11}\) with a 25 MeV proton beam or with neutrons at the TRIGA reactor\(^{12}\). The particle fluences were scaled to 1 MeV equivalent neutrons per square centimeter ($n_{eq}/cm^2$) with hardness factors of 1.85 and 0.88 for 25 MeV protons and reactor neutrons, respectively. The uncertainty in the irradiation fluences is smaller than 10%. The modules irradiated at KIT were unpowered and maintained at a temperature of −25°C. At the TRIGA reactor, the modules were irradiated unpowered at the ambient temperature of 45 – 50°C. After irradiation, all irradiated modules were stored at < 0°C, but were annealed at 60°C for two hours before the first measurements, effectively destroying the previous irradiation history.

Two planar modules and one module from each 3D manufacturer were retained for comparison with irradiated samples as both the test-bench and test-beam levels. Unfortunately, for logistic reasons, there are no consistent measurements of $I - V_b$ and $C - V_b$ at the sensor stage, and the pre- and post-irradiation stages, for individual modules. The modules used, together with the level of irradiation, are shown in Table 3.

### 4.1 Assembly of the IBL module

An IBL prototype module consists of a sensor integrated to an FE-I4A via flip-chip bump-bonding, connecting each pixel on the sensor side to its dedicated FE-I4A pixel pre-amplifier input. Bump-bonding requires a low defect rate (nominally $< 10^{-4}$), with a bump density of order 8000 per cm$^2$ and a bump pitch in the $r\phi$ direction of 50 $\mu$m. The principal bump-bonding provider for this prototyping phase has been IZM\(^{13}\). IZM also provided a large fraction of the bump-bonding for the FE-I3 based modules of the current ATLAS pixel detector.

A complication is that the FE-I4A IC is thinned to reduce the IBL material budget. The procedure for thin IC bump-bonding needed specific development and has been subject to R&D development. After wafer level thinning, a glass handling wafer is temporarily glued to the FE-I4A wafer backside. Once bumps are formed on the FE front side, the FE are diced, and flip-chipping to sensor tiles is carried out. The carrier chip is then detached from the assembly by laser exposure. With this method, FE-I4A ICs have been thinned to 150 $\mu$m and 100 $\mu$m, and successfully flip-chipped. Working with thin ICs also brings constraints to all subsequent steps in the module assembly, for example the module manipulation and wire-bonding steps. As noted

\(^{10}\) Since no reliable TOT charge calibration exists, uncalibrated TOT spectra, as well as the peak (most probable value or MPV) are presented in this paper, in units of the 25 ns bunch crossing clock (BC)

\(^{11}\) Karlsruhe Institute of Technology, Karlsruhe, Germany

\(^{12}\) TRIGA reactor, Jozef Stefan Institute, Ljubljana, Slovenia

\(^{13}\) Fraunhofer IZM-Berlin, Gustav-Meyer-Allee 25, 13355 Berlin
Table 3. Sensors characterized following irradiation at the KIT 25 MeV proton beam or the TRIGA reactor neutron source (see text). The quoted fluences are normalised to the equivalent damage of 1 MeV neutrons. Also listed are non-irradiated modules used for comparison. In particular, PPS L1 is characterized before and after irradiation. Those modules used in the test beam are noted.

<table>
<thead>
<tr>
<th>Sample ID</th>
<th>Type</th>
<th>Irradiation Facility</th>
<th>Dose</th>
<th>Test beam</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPS 31</td>
<td>PPS Slim Edge 250 µm</td>
<td>n/a</td>
<td>un-irradiated</td>
<td>Test beam</td>
</tr>
<tr>
<td>PPS 40</td>
<td>PPS Slim Edge 200 µm</td>
<td>n/a</td>
<td>un-irradiated</td>
<td>Test beam</td>
</tr>
<tr>
<td>PPS 51</td>
<td>PPS Slim Edge 200 µm</td>
<td>KIT (p)</td>
<td>6 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>PPS 60</td>
<td>PPS Slim Edge 200 µm</td>
<td>KIT (p)</td>
<td>6 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>PPS 61</td>
<td>PPS Slim Edge 200 µm</td>
<td>KIT (p)</td>
<td>6 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>PPS 91</td>
<td>PPS Slim Edge 200 µm</td>
<td>n/a</td>
<td>un-irradiated</td>
<td>TRIGA (n)</td>
</tr>
<tr>
<td>PPS L1</td>
<td>PPS Slim Edge 250 µm</td>
<td>n/a</td>
<td>un-irradiated</td>
<td>Test beam</td>
</tr>
<tr>
<td>PPS L2</td>
<td>PPS Slim Edge 250 µm</td>
<td>TRIGA (n)</td>
<td>3.7 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>PPS L4</td>
<td>PPS Slim Edge 200 µm</td>
<td>TRIGA (n)</td>
<td>5 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>CNM 34</td>
<td>CNM IBL design</td>
<td>KIT (p)</td>
<td>5 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>CNM 36</td>
<td>CNM IBL design</td>
<td>KIT (p)</td>
<td>6 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>CNM 55</td>
<td>CNM IBL design</td>
<td>n/a</td>
<td>un-irradiated</td>
<td>TRIGA (n)</td>
</tr>
<tr>
<td>CNM 81</td>
<td>CNM IBL design</td>
<td>TRIGA (n)</td>
<td>5 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>CNM 82</td>
<td>CNM IBL design</td>
<td>TRIGA (n)</td>
<td>5 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>CNM 97</td>
<td>CNM IBL design</td>
<td>KIT (p)</td>
<td>5 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>CNM 100</td>
<td>CNM IBL design</td>
<td>TRIGA (n)</td>
<td>2 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>CNM 101</td>
<td>CNM IBL design</td>
<td>n/a</td>
<td>un-irradiated</td>
<td>Test beam</td>
</tr>
<tr>
<td>FBK 13</td>
<td>FBK IBL design</td>
<td>n/a</td>
<td>un-irradiated</td>
<td>Test beam</td>
</tr>
<tr>
<td>FBK 87</td>
<td>FBK IBL design</td>
<td>KIT (p)</td>
<td>5 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>FBK 90</td>
<td>FBK IBL design</td>
<td>KIT (p)</td>
<td>2 × 10^{15} n_{eq}/cm^{2}</td>
<td>Test beam</td>
</tr>
<tr>
<td>FBK 111</td>
<td>FBK IBL design</td>
<td>n/a</td>
<td>un-irradiated</td>
<td>Test beam</td>
</tr>
<tr>
<td>FBK 112</td>
<td>FBK IBL design</td>
<td>n/a</td>
<td>un-irradiated</td>
<td>Test beam</td>
</tr>
</tbody>
</table>

in Section 3, the sensors are also thin (nominally 200 µm for planar sensors and 230 µm for 3D sensors).

Contrary to the present FE-I3 based module, there is no need of providing an additional steering IC for FE-I4 based modules: the FE-I4A needs only 2 LVDS inputs (40 MHz clock and 40 Mb/s command) and streams out data on one LVDS transmitter pair at 160 Mb/s.

4.2 Pre-irradiation module performance

The performance of unirradiated planar sensors is well understood, and therefore details of only two assemblies (PPS L1 and PPS 91) are shown as a reference for comparison to irradiated behaviour. In particular, the PPS L1 module has been measured before and after irradiation. Figure 13 displays the expected diode-like $I - V_{b}$ curve with a plateau extending much beyond the working point of approximately 70 V followed by a (in this case) rather slow breakdown. The beam-spot of a collimated $^{90}$Sr source is clearly visible within the hitmap of all events having a single-pixel cluster. Using the $^{90}$Sr source, Fig. 14 shows the measured TOT charge and the ENC noise as a function of $V_{b}$ for PPS 91 after tuning to a mean threshold of approximately 1600 e⁻. Evidently
PPS 91 depletes below 30 V since the noise is as expected from isolated pixels after depletion. The threshold behaviour is very stable.

Figure 13. (a) I − V_b measurement of the PPS L1 sensor and module successively before the UBM process, after the slim-edge dicing of the sensor, and after bump-bonding. The increased leakage current after bump-bonding can be attributed to the increased temperature, due to the FE-I4A IC. (b) Hit map of a strongly collimated 90\(^{\text{Sr}}\) source on the PPS 91 module. Only hits with a cluster size of 1 pixel were selected for the hit map to avoid hits with stronger electron scattering that would make the beam spot less clear.

Figure 14. Measured MPV of the TOT spectrum in units of the 25 ns bunch crossing, collected using a 90\(^{\text{Sr}}\) source (a) and the ENC (b) measured as a function of the bias voltage for the PPS 91 module. The tuning was made at V_b = −80 V, aiming for a mean 1600 e\(^{-}\) threshold and a TOT measurement of 5 bunch crossing for a 10000 e\(^{-}\) signal.

The qualification of 3D modules was made on 32 bump-bonded sensors from the CNM and FBK prototype batches. I − V_b measurements are shown for the full qualification set in Fig. [15], for modules using FBK (a) and CNM (b) sensors. Clearly visible are the break-down points which for most assemblies are greater than 30 V, reaching, in the case of CNM assemblies values greater than 100V. The lower values of V_bk for FBK sensors are due to the p-spray, that is designed to yield much large V bk values following irradiation.

As with the planar modules, 241\(^{\text{Am}}\) and 90\(^{\text{Sr}}\) radioactive sources have been used to test the
Figure 15. Measurement of the leakage current as a function of the bias voltage for modules using (a) FBK sensors and (b) CNM sensors. In each case the measurements are for a module temperature of 20°C.

Figure 16. The MPV of the TOT spectrum measured for FBK and CNM 3D modules after bump-bonding but before irradiation, using a $^{90}$Sr source. The data are shown in units of the 25 ns bunch crossing clock as a function of $V_b$.

4.3 Post-irradiation module performance

The post-irradiation performance of planar modules was generally satisfactory, with stable operation at a module temperature of $-15\degree$C. Threshold tunings as low as 1000 e$^-$ were possible, with
only a modest noise increase. While neutron-irradiated modules were in all cases well-behaved, proton-irradiated modules suffered from a significant fraction of digitally unresponsive pixels. This effect was also measured in test beam data and was later found to result from the non-optimized value for an internal DAC (Amp2Vbpf) which had to be significantly increased to account for surface charge effects generated by the ionizing dose during proton irradiation.

Measurements from four irradiated planar modules (PPS L4, PPS 51, PPS 60 and PPS 61, see Table 3) are shown in this section. \( I - V_b \) measurements are shown in Fig. 17 for PPS 51 and PPS 61 samples: both show a dominantly ohmic behaviour as normally seen after heavy irradiation. The measurements of PPS 51 and PPS 61 were controlled using a Pt-1000 temperature sensor on the module. Taking into account the active area of approximately 3.44 cm\(^2\), the power dissipation (leakage current) satisfied the specified value of 200 mW/cm\(^2\) (200 \( \mu \)A/cm\(^2\) at \( V_b = 1000 \text{ V} \)). Test-beam data for PPS61 are shown in Section 5.2. Following irradiation, no module breakdowns have been observed.

**Figure 17.** \( I - V_b \) curves after irradiation of the PPS 51 and PPS 61 modules measured at a sensor temperature of \(-15^\circ\text{C}\).

Figure 18 (a) shows the MPV of the TOT for PPS L4 as a function of the bias voltage, using data collected with a \(^{90}\text{Sr}\) source. The measured increase of collected charge towards higher \( V_b \) is expected after irradiation from the increased depletion voltage and at the highest voltages from charge multiplication. A comparison to the tuning value of 7 TOT at 10000 e\(^-\) suggests that the collected charge is of the order 8000-9000 e\(^-\). At the same time the threshold tuning is stable at a low values. Figure 18 (b) shows the ENC as a function of \( V_b \) for the PPS L4 module. With increasing \( V_b \), the ENC increases slightly, in particular for very low thresholds. The noise figure of about 150 ENC for a threshold setting of 1600 e\(^-\) is of the same order as before irradiation.

As an example for proton-irradiated assemblies, Figures 19 (a) and (b) show the threshold and ENC noise distribution for each channel of the PPS 60 module, with a mean threshold tuned to
Figure 18. (a) MPV of the TOT spectrum for 1-hit clusters in the PPS L4 module, measured as a function of the bias voltage using a $^{90}\text{Sr}$ source. (b) ENC noise as a function of the bias voltage for PPS L4 at several threshold values.

1000 $e^{-}$. Figures 19 (c) and (d) show the projections of each measurement. The measured noise is very low, with a mean value of 134 ENC. The noise increase in some columns is an artifact of the increased leakage current due to the corresponding FE-I4A injector switches.

$I - V_b$ measurements as a function of bias voltage following irradiation to a fluence ($5 \times 10^{15} \text{n}_{eq}/\text{cm}^2$) are shown in Fig. 20 for FBK 87 (a) and CNM 36 (b) modules, measured at different sensor temperatures. Fig. 20 (c) shows a compilation of the leakage current as a function of the fluence and operating temperature for the CNM module. These values grow linearly with the bias voltage and indicate that no breakdown or thermal runaway occurs at the temperatures considered.

Figure 21 shows a compilation of the MPV TOT measurement in units of the 25 ns bunch crossing clock for three different CNM modules (CNM 101, CNM 100 and CNM 36), as measured using a $^{90}\text{Sr}$ source with an external electron trigger. For a bias voltage of $V_b \approx 200$ V and an operating temperature of -15°C, signal efficiencies of 82% and 60% are measured after respectively $2 \times 10^{15} \text{n}_{eq}/\text{cm}^2$ and $5 \times 10^{15} \text{n}_{eq}/\text{cm}^2$.

Figure 22 (a) shows the threshold setting as a function of the bias voltage for both FBK and CNM modules, before and after irradiation. Figure 22 (b) shows the effect of irradiation on the measured noise for these modules as a function of the irradiation. In each case, the performance remains satisfactory.

5. Test Beam Measurements of the IBL Module

Detailed test beam studies of both non-irradiated and irradiated modules are essential to understand the module performance. These studies allow a direct comparison with bench-top ENC noise and TOT data, and as well allow both an understanding and an optimization of the module operating parameters. Several IBL prototype modules have been characterized using 120 GeV/c pions at the CERN SPS H6 and H8 beam lines in respectively June and September 2011. More extensive test beam campaigns are underway.
Figure 19. (a) Channel-by-channel threshold measurement for the PPS 60 module, with (c) the histogram of all channels. (b) The measured noise distribution of each channel, for the threshold values quoted, and (d) the histogram of the measured noise for all channels.

5.1 Test beam setup

Three modules, together with a non-irradiated FE-I4A reference module, were normally included in the test beam at any given time. For a part of the run period, measurements were possible with the modules mounted within the bore of the 1.6 T superconducting Morpurgo dipole magnet, simulating the ATLAS solenoid field direction. However, because of limited beam time, only a few measurements were made using the magnetic field. Most measurements use perpendicular incident tracks, but some measurements were also made using non-perpendicular incidence tracks to replicate features of the IBL geometry.

The modules under test were mounted normally with respect to the incoming beam using mechanical holders so that the long pixel direction (corresponding to the $z$ direction in the IBL) was horizontal. Small, well-defined tilt angles around that horizontal axis, referred to as tilts in the $\phi$ direction (see Fig. 1), were achieved by mounting the modules on wedges machined to the desired angle. Rotations around the vertical axis, corresponding to different pseudo-rapidity values ($\eta$), were made using specially designed spacers allowing rotations in the range $0.88 \leq \eta \leq 4.74$ (Fig. 23).
Figure 20. $I - V_b$ measurements shown at different module temperatures, after irradiation to a fluence of $5 \times 10^{15} \text{n}_{eq} \text{cm}^{-2}$, for (a) the FBK 87 module and (b) the CNM 36 module. c) The measured leakage current as a function of the fluence for different module temperatures. The bias voltage at maximum fluence was $V_b = 160 \text{V}$.

Figure 21. MPV TOT signal for the CNM 36, CNM 100 and CNM 101 modules irradiated at different fluences, compared to a non-irradiated sample from the same batch. The measurements were made using a $^{90}\text{Sr}$ source and an external electron trigger.

The three test modules were placed in an insulated thermally controlled box together with
Figure 22. Threshold (a) and noise (b) of FBK and CNM modules, measured as a function of the bias voltage before and after irradiation. The operating temperature of the modules is -15°C.

Figure 23. (a) Photograph of the High-eta setup. (b) The high-η set-up.

do the reference plane. For some measurements, the modules were also mounted with the long pixel direction in the vertical, such that the magnetic field of the dipole pointed in the same direction as in IBL (see Fig. 23). To test the modules under IBL operating conditions, they were cooled in the insulated box to a sensor temperature of approximately -15°C.

Beam particle trajectories were reconstructed using the high resolution EUDET telescope [35], consisting of six planes instrumented with Mimosa26 active pixel sensors with a pitch of 18.5 μm. Each plane consists of 1152 × 576 pixels covering an active area of 21.2 × 10.6 mm². A coincidence of four scintillators was employed for triggering resulting in an effective sensitive area of 2 × 1 cm². The track position uncertainty when interpolated to the test modules was estimated to be 3 μm.

The Mimosa26 sensors employ a continuous rolling shutter for readout. For every trigger signal the telescope planes integrate hits for 115 μs, while the test modules are sensitive for only 400 ns. Tracks passing through the telescope during the sensitive time of the modules (in-time tracks) were selected by requiring at least one hit in another module and the reference plane.

The telescope planes are read by a custom-made VME system controlled by a single board PC.
for each telescope arm (see Fig. 23). Each of the PCs sends a separate ethernet data stream to a run control PC. The test modules are read using the USBpix system (see Section 2.3.1) connected to the EUDET telescope trigger interface [36].

5.2 IBL modules measured in the test beam

Several PPS slim edge design modules with different sensor thickness, as well as 3D sensors from both CNM and FBK, were studied in the test beam. The devices used are indicated in Table 5.

<table>
<thead>
<tr>
<th>Sample ID</th>
<th>HV(V)</th>
<th>Magnetic Field</th>
<th>Tilt Angle (°)</th>
<th>Threshold (e⁻)</th>
<th>Hit Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPS 31</td>
<td>−150</td>
<td>off</td>
<td>0</td>
<td>xx.x</td>
<td>99.9</td>
</tr>
<tr>
<td>PPS 60</td>
<td>−940</td>
<td>off</td>
<td>15</td>
<td>xx.x</td>
<td>99.9</td>
</tr>
<tr>
<td>PPS 61</td>
<td>−550</td>
<td>off</td>
<td>15</td>
<td>xx.x</td>
<td>96.9</td>
</tr>
<tr>
<td>PPS L2</td>
<td>−1000</td>
<td>off</td>
<td>15</td>
<td>93.7</td>
<td>86.7</td>
</tr>
<tr>
<td>PPS L4</td>
<td>−400</td>
<td>off</td>
<td>15</td>
<td>95.7</td>
<td>99.0</td>
</tr>
<tr>
<td>CNM 55</td>
<td>−20</td>
<td>on</td>
<td>0</td>
<td>xx.x</td>
<td>99.5</td>
</tr>
<tr>
<td>CNM 34</td>
<td>−140</td>
<td>on</td>
<td>0</td>
<td>99.6</td>
<td>97.5</td>
</tr>
<tr>
<td>CNM 81</td>
<td>−150</td>
<td>off</td>
<td>0</td>
<td>xx.x</td>
<td>96.5</td>
</tr>
<tr>
<td>CNM 97</td>
<td>−140</td>
<td>off</td>
<td>15</td>
<td>97.4</td>
<td>99.8</td>
</tr>
<tr>
<td>FBK 13</td>
<td>−150</td>
<td>off</td>
<td>15</td>
<td>xx.x</td>
<td>98.2</td>
</tr>
<tr>
<td>FBK 90</td>
<td>−150</td>
<td>off</td>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FBK 87</td>
<td>−160</td>
<td>off</td>
<td>15</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The FE-I4A front-end IC is rated to be radiation hard until TID values of approximately 250 MRad but due to the low proton beam energy, devices at KIT were irradiated to an estimated TID of 750 MRad. For the reasons described in Section 4.3, this led to some dead and noisy pixel cells that were subsequently masked and excluded from all analyses. Most of the dead pixels could be subsequently recovered following reconfiguration of the FE-I4A IC.

5.2.1 Charge collection

The front-end chip provides a digital TOT measurement in units of the 25 ns LHC bunch crossing rate and with a 4-bit resolution. The TOT to charge calibration was unreliable in this period and was therefore not used. The raw TOT distributions of four representative samples for a 15° incident azimuthal beam angle are shown on Fig. 24. The distributions cannot be directly compared directly because the sensors were irradiated differently and had different thicknesses and thresholds.
Figure 24. The raw TOT spectra for (a) PPS 61 (threshold setting 1400 e⁻), (b) CNM 97 (threshold setting 2950 e⁻), (c) PPS L4 (threshold setting 1600 e⁻) and (d) FBK 87 (threshold setting 2450 e⁻) modules, with no magnetic field and with a 15° incident beam angle. The distributions are shown in units of the 25 ns bunch crossing clock.

5.2.2 Hit efficiency

The hit efficiency is a key performance parameter for pixel sensors. It is particularly important for sensors which have to survive such a large radiation dose as in the IBL.

The overall hit efficiency is measured using tracks reconstructed with the telescope and interpolated to the test modules to search for a matching hit. The number of tracks with a matching hit is divided by the total number of tracks passing through the sensor. To remove fake tracks that would bias the efficiency measurement of a particular test module, a matching hit in at least one other test module is required, as described above.

As already noted, the large TID dose received by the front-end IC led to some noisy or dead pixel cells and to assess the intrinsic effect of radiation dose on the sensor behavior, tracks pointing to very noisy or dead pixels and surrounding pixels were excluded for the efficiency measurement.

The tracking efficiency measurements for all samples and all operating conditions are summarized in Table 4. As expected the measured efficiency for the un-irradiated PPS sample is nearly 100%. The un-irradiated 3D sensor has a slightly reduced efficiency due to the tracks that pass through the empty electrodes where the charge is not collected. Full efficiency is recovered for tilted tracks [37].

The efficiency measured with the magnetic field on and off are comparable for the 3D samples confirming that the effect of magnetic field is negligible on 3D sensors [37]. All irradiated sensors
show very good behavior with efficiencies larger than 95% in all cases at bias voltage of Table 4. For the irradiated planar sensors, the efficiency increases with increased bias voltage. This is a well-known behavior as the depletion region increases with bias voltage, increasing the collected charge and therefore the hit efficiency.

5.2.3 Cell efficiency

The in-depth behavior of the sensor and the relative loss of efficiency after irradiation are better assessed by looking at the efficiency distribution inside the pixel cells. To improve the statistics and assuming that they behave similarly, all cells have been added together. Fig. 25 shows the two dimension efficiency maps for the PPS 61 sample at $-1000 \text{ V}$ and $-600 \text{ V}$ for $15^\circ$ track.
inclination, for the CNM 34 sample at normal incidence and for the CNM 97 sample using $15^\circ$ track inclination. The lithography sketches are also shown. Two cells are actually plotted: a central cell (dashed line) surrounded by two half cells in both the vertical and horizontal directions.

The PPS bias grid and dots, and solder bumps can be seen on the left and right of the lithography sketch. Efficiency loss occurs at the edge of cell. At $V_b = -1000$ V the effect is mainly visible on the bias side of the cell. When the bias voltage decreases, the effect shows up on the solder bump side as well. The loss is primarily due to charge sharing between cells. When charge sharing occurs, less charge is collected by the readout cell, reducing the probability to exceed the electronics threshold. The effect is more pronounced for highly irradiated samples and for lower bias voltage. In addition, some charge is lost and trapped in the bias grid and dots, further decreasing the collected charge and therefore the efficiency.

The n-type readout electrodes (red) and p-type bias electrodes (blue) are shown on the 3D lithography sketch. The CNM 34 data are for magnetic field off and normal incidence. The loss of efficiency for tracks passing through the electrodes is clearly visible since the electrodes are empty and do not produce charge. More efficiency loss occurs near the bias electrodes as the electric field is smaller than near the readout electrodes. The CNM 97 data are for inclined tracks. The efficiency loss is less noticeable as the tracks pass through some of the wafer bulk and not entirely through the electrodes. The effect of charge sharing is in this case more evident on the shorter side because of the track inclination.

### 5.2.4 Edge efficiency

The size of the inactive area of the sensors can be estimated by measuring the hit efficiency of the edge pixels. Two dimensional efficiency maps and their one-dimensional projection onto the long pixel direction are built for edge pixels. Figure 26 shows the photo-lithography sketch of the edge pixels for both PPS and CNM-3D sensors, and the corresponding one dimension efficiency projections. Projections are fitted with s-curve functions.

For PPS sensors, the inactive length is measured from the fixed dicing street. For PPS L2 at full depletion, the inactive region is estimated to be $215 \, \mu m$ at 50% efficiency (fit shown on Fig. 26).
The 3D edge design has a 200 µm guard ring extending over the edge pixels. The active area extends to about 20 µm over the edge pixel making the inactive area of the order of 180 µm at 50% efficiency. The reduced efficiency in some columns results from a lack of full depletion at $V_b = -140$ V.

Overall, PPS and 3D sensors show similar inactive regions.

![Graphs showing cluster size distributions for PPS and 3D sensors](image)

**Figure 27.** Comparison of the cluster size distributions for (a) the PPS 61 module and (b) the FBK 87 module, with no magnetic field and at 15° beam incident angle. The threshold settings for the PPS 61 and FBK 87 modules are respectively 1400 e$^-$ and 2450 e$^-$.

### 5.2.5 Charge sharing

The charge sharing between cells is another important parameter of pixel detectors. Large charge sharing between neighbouring pixels leads to better tracking resolution as the hit position is better determined. However if charge sharing occurs, less charge is available to the hit cells, decreasing the probability to pass the electronics threshold, therefore degrading the hit efficiency. This can be a major concern for highly irradiated samples as the total available charge is reduced.

Charge sharing between cells is directly related to the size of the reconstructed clusters. Cluster size distributions for a PPS and a 3D sensor, for 15° beam incident angle are shown on Fig. 27. In the absence of magnetic field, PPS and 3D modules show similar behavior. The results of Table 3 indicate that charge sharing is not a concern, for bias voltages as noted there.

### 5.2.6 Spatial resolution

Spatial resolution is another key parameter of pixel detectors. For multi-hit clusters the analog information of the deposited charge can be used to improve the determination of the track position in the sensor. We estimate the spatial resolution of PPS and 3D samples from residual distributions of all-hit clusters in the short pixel direction, where the track position is interpolated from the telescope and the cluster position is calculated using simple charge weighting between cells. Distributions fits for some representatives PPS and 3D samples, for 15° beam incident angle are shown on Fig. 28.
Figure 28. (a) Residual distribution of the PPS L4 module for all-hit clusters in the short pixel direction, for 15° beam incident angle and for a threshold setting of 1600 e−. (b) Residual distribution for the CNM 81 module at the same incident angle and a threshold setting of 1500 e−. The widths of the 2 distributions are similar.

5.3 Measurements at small incidence angle

In the IBL, largest eta sensors are positioned at $\eta = 2.9$ which corresponds to a very small track incident angle $\theta = 6^\circ$. The behavior of Planar and 3D sensors has been measured for 80° beam incident angle with respect to normal incidence. Given the sensor thickness and the pixel length, tracks at that angle can traverse up to seven cells in the z-direction. The cluster size has a direct implication on the measured track precision and can be affected by two factors:

- Threshold effects. The charge produced in the cluster edge cells may not be sufficient to pass the electronic threshold setting and to register a hit;
- Depletion voltage. Following a large radiation dose, the sensors may be required to operate at a bias voltage for which the sensor is not fully depleted, therefore reducing the collected charge and hence not registering a hit in one or more cells. Depending on the depletion depth, cells traversed close to the sensor surface may not be recorded.

Fig. 29 compares the cluster size distribution for two CNM modules, mounted back-to-back: the un-irradiated CNM 55 module and the irradiated CNM 34 module. As expected, due to a combination of the threshold effect and the reduced charge collection after irradiation, the cluster size distribution is broader and with lower mean value for the irradiated module. This will affect and possibly deteriorate the track hit accuracy. Because of the electrode orientation, this effect is much less important for modules using 3D sensors.

After irradiation, type inversion occurs in planar sensors and the devices may operate at under-depleted bias voltages. Depending on the depletion depth, cells located close to the sensor surface may not be recorded (no or less charge to pass the electronic threshold). As a consequence, recorded clusters may be smaller than actual clusters, leading to a degradation of the tracking resolution. The cluster size distribution of an irradiated sample operated at two bias voltages is shown on Fig. 30.
Figure 29. (a) Cluster size distribution for the unirradiated CNM 34 module for tracks at 80° incident track angle with respect to normal incidence. The bias voltage was $V_b = -30$ V and the nominal threshold setting was $*** \text{e}^-$.
(b) Similar data for the CNM 55 module, following proton irradiation to a fluence of $5 \times 10^{13} \text{n}_{\text{eq}}/\text{cm}^2$. The data are collected with $V_b = -160$ V and a threshold setting of $*** \text{e}^-$.

Figure 30. Cluster size distribution for PPS xx at bias voltages of (a) $V_b = 600$V and (b) $V_b = 1000$V, at high eta.

6. Conclusions
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References


[29] J. Wuenstefeld, *Characterisation of Ionisation-Induced Surface Effects for the Optimisation of Silicon Detectors for Particle Physics Applications*, UniDo-PH-E4-01-06.


I. Tsurin\textsuperscript{24}, D. Tsybychev\textsuperscript{44}, Y. Unno\textsuperscript{23}, L. Vacavant\textsuperscript{28}, B. Verlaat\textsuperscript{32}, E. Vianello\textsuperscript{48}, E. Vigeolas\textsuperscript{28}, S. von Kleist\textsuperscript{15}, V. Vrba\textsuperscript{59}, R. Vuillermet\textsuperscript{13}, R. Wang\textsuperscript{31}, S. Watts\textsuperscript{27}, M. Weber\textsuperscript{9}, M. Weber\textsuperscript{16}, P. Weigell\textsuperscript{30}, J. Weingarten\textsuperscript{19}, S. Welch\textsuperscript{13}, S. Wenig\textsuperscript{13}, N. Wermes\textsuperscript{11}, A. Wiese\textsuperscript{42}, T. Wittig\textsuperscript{15}, T. Yildizkaya\textsuperscript{1}, C. Zeitnitz\textsuperscript{51}, M. Ziolkowski\textsuperscript{42}, V. Zivkovic\textsuperscript{32}, A. Zoccoli\textsuperscript{10(a),10(b)}, N. Zorzi\textsuperscript{48}, L. Zwalinski\textsuperscript{13},

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