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CRIAD2:

a 0.7μm 13-bit

Low Power ADC

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1. Introduction

The aim of this project was to make available a low power and low cost ADC for the silicon tracker of the AMS (Alpha Magnetic Spectrometer) experiment to be flown on the International Space Station Alpha. AMS is designed to measure the amount of antimatter nuclei present in cosmic rays to a much higher precision than has been possible to date. The best commercial ADC candidate was the CLC949 from Comlinear, but it seemed to be a little too high in power consumption and also in cost. Since the University of Geneva took part in the CRIAD[1] design within the framework of the RD2 program at CERN, we decided to try to increase the specifications of this particular ADC. The main improvements were to add two bits to the maximum of the resolution, change the polarity of the input range, adapt the digital inputs and outputs to the standard 3V TTL and improve the comparator design in order to reach 10Msamples/s. The CRIAD2 has been fabricated and tested.
This project was initiated by M. Bourquin and developed with the help of F. Anghinolfi for the coordination and the test, N. Produit for the specifications and the test, D. La Marra for the digital part of the design and the layout assembly, V. Valence and P. Deval for the comparator, the layout assembly and other analog parts of the design, and P. Béné for the tests. The project was supported in part by the *Fonds national suisse de la recherche scientifique*.
The process is the standard CMOS 0.7μm technology from IMEC[2] for analog applications. The analog parts are made in full custom whereas the digital parts are made in standard cells.

2. Description

The CRIAD2 0.7μm is a multi-range linear ADC with 4 ranges defined as 0 to 64mV, 64 to 128mV, 128 to 512mV, 512mV to 2.048 V. In each range the resolution is defined by an 8-bits linear conversion performed between two references, the upper one being the high end of the range, the lower one being ground (0 V). The commutation of ranges is automatic with the signal amplitude. The functional diagram is sketched in Figure 1.

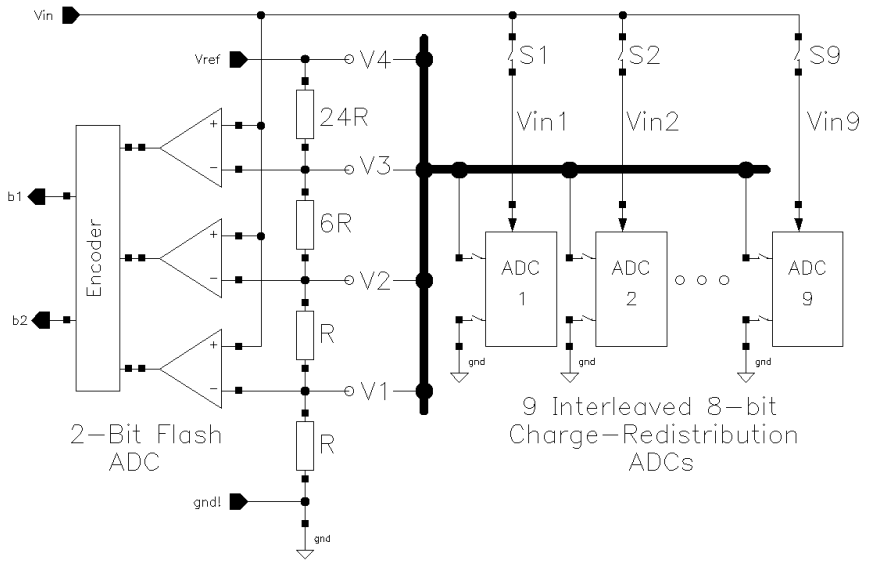


Figure 1: Functional diagram of the CRIAD2 0.7μm 13-bit Low Power ADC

The resolution obtained by this architecture is as high as 0.25mV in the first low range, then 0.5mV, 2mV and 8mV.

[1] *"A Low Power Piece-wise Linear Analog to Digital Converter for use in Particle Tracking" V. Valencic, F. Anghinolfi, P. Deval, R. Bonino, D. La Marra, and H. Kambara, IEEE Trans. on Nuclear Science, Aug. 1995, Vol42, no4, p. 772-776.*

[2] *IMEC Kapeldreef 75 B-3001 Leuven*

Due to the overlap between the ranges, not all the codes are used within the ranges (except the first one).

The aim of the CRIAD2 0.7μm is to provide a very low power ADC chip with a dynamic range as large as 13 bits. The output is encoded onto 10 bits, the two higher bits being for the range order, the 8 following bits being the result of the linear conversion within the range. The conversion rate is specified as 5 Msamples/sec, but the design is done to reach 10 Msamples/sec in nominal conditions.

3. Test System

To test the CRIAD2, we have used a CAMAC crate connected to a PC through a Kinetic 3920/2925 interface.
The CAMAC board is a four-layer circuit including a good ground plane. It contains:

- 4 separately adjustable power supplies:
  - +3V analog
  - +3V digital
  - -2V analog
  - -2V digital
  - Separate GND for analog part of CRIAD2.
- 1 voltage reference (+ 2.048V)
- 1 oscillator.
  - A crystal 10MHz-oscillator gives clock for the board. This frequency is divided by two for ADC and FIFO. To run at 10MHz with ADC, replace the oscillator by a 20MHz one.
- 1 FIFO
  - 10 bits width, 8K depth. Used to memorize the output of the ADC. The FIFO is then read by CAMAC.
- 1 circuit for CAMAC communication.

The start of conversion is given by CAMAC or by an external NIM pulse. Others functions can be given only by CAMAC (reset FIFO, reset ADC, ADC in standby mode and so on). The signal to convert is produced by an external generator.

4. Analysis of Conversion Characteristics

An analog signal from a sinusoidal voltage source is injected to the ADC running at 5 Msamples/s. The FIFO is filled and then the 8192 data values are transmitted to the computer through CAMAC.
Each 10 bit data word is treated in the following way: the 10 output bits are converted to a 13 bit equivalent word in multiplying the 8 lower bits by 1, 2, 8 or 32 depending on the value of the 2 most significant bits. So the final range is from 0 to 8192 but with varying resolution.
Figure 2 top left shows the output codes succession for a full scale sinusoid sampled at 5 MHz, with 4.5μA biasing current for the ADC. At this picture scale the varying resolution is not obvious but can be seen under magnification. The top right plot is the resulting function from a χ^2 minimization of the function:

$$\chi^2 = \sum_{n=1,8192} \left(y(n) - a*\sin(n-b)+c\right)^2 \Big/ \sigma(n)^2$$

where:
a, b and c are unknown.
n is the data index.
y are the data points.
$\sigma = {}^{1}\!/\!_{\sqrt{12}}$, ${}^{2}\!/\!_{\sqrt{12}}$, ${}^{8}\!/\!_{\sqrt{12}}$ or ${}^{32}\!/\!_{\sqrt{12}}$ .according to the range of the data points.
The lower left plot is the pull of the data: i.e.:

$$pull(n) = \left(y(n) - a*\sin(n-b)+c\right) \Big/ \sigma(n) .$$

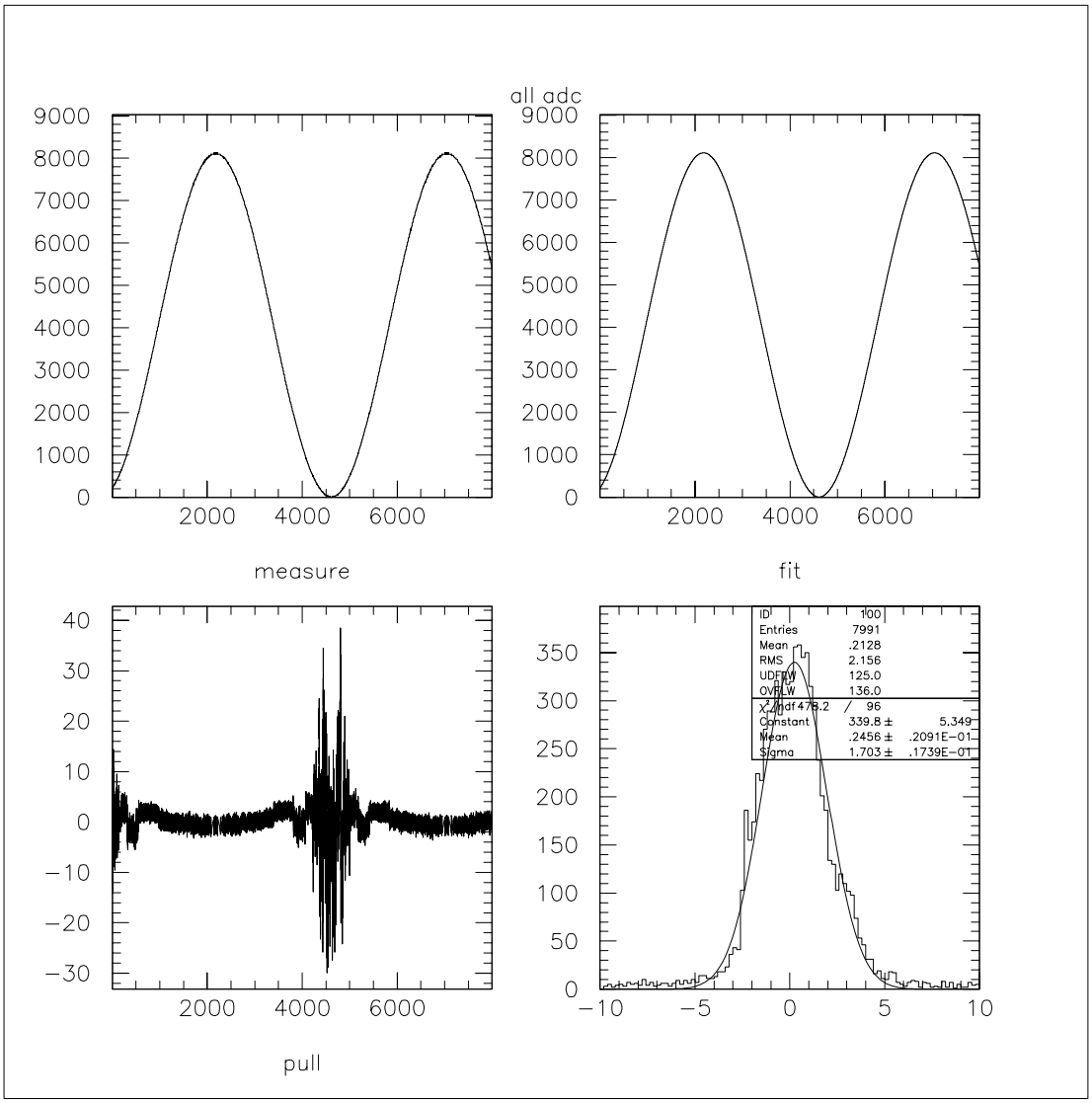


Figure 2: Response of CRIAD2 to a sinusoidal voltage

It indicates some small non-linearity and some problems at the range change. We also see that the lower range is not perfect. The lower right plot shows the distribution of the pull. Mathematically the pull must be distributed as a gaussian of mean 0 and width 1. The width is 1.7 indicating some non-linearity and some non-gaussian tails. Tails are coming mainly from noise in the lower range.

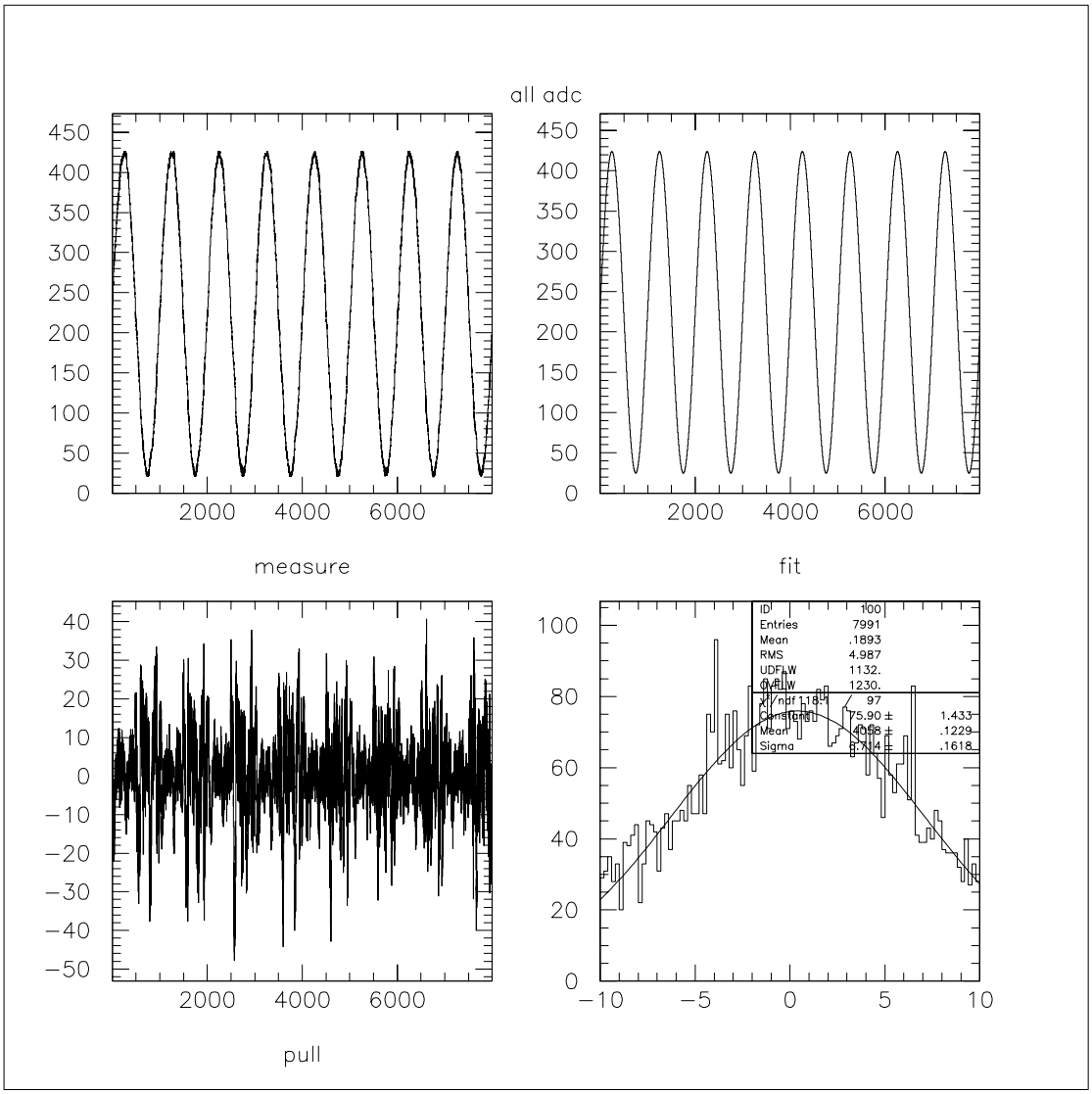


Figure 3: Same as Figure 2, but for a signal covering the two lowest ranges only.

To study the lower range, the same analysis was repeated but with a sinusoidal signal that covers only the two lowest ranges (see figure 3). We see that the pull distribution is the sum of two gaussian curves and corresponds to the two ranges. The pull for the lowest range is 6 indicating a noise level of 1.5 mV. We think that the actual test board is not suited to do a fine analysis of signal at the mV level. Such a noise can come from the function generator or from card induced ambient noise. So this study is inconclusive for the behavior of the lowest range and more careful card design must be accomplish to measure the performance of the ADC there.
According to those measurements we can see that the CRIAD2 is not perfect in the lower range and has some problems in the range switching regions but it can be used as an acceptable 12 bit ADC.

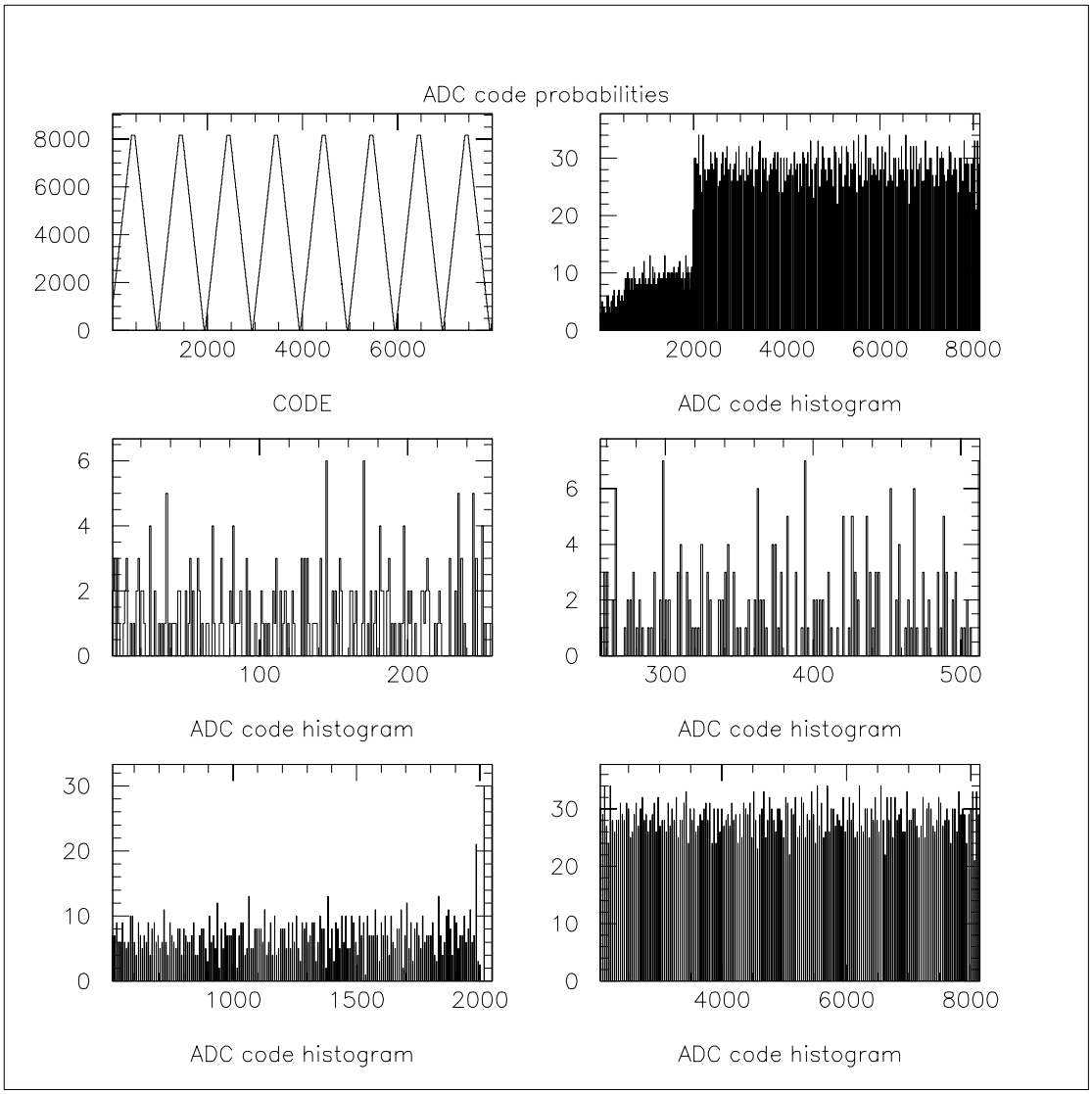


Figure 4: Response of CRIAD2 to a triangular analog signal.

As a further test, a triangular analog signal is injected into the ADC running at 5 Msamples/s. Care is taken that the triangle covers all the range and overflows a little above and below the maximal range. Such a signal should populate all the ADC codes with the same probability except the code 0 and the maximum code which are the most probable. Because of the range mechanism not all the codes exist in the CRIAD2 so that the probability goes to 0 for some codes and some other codes have higher probability accordingly. The measured probability shows the expected shape as seen in figure 4.

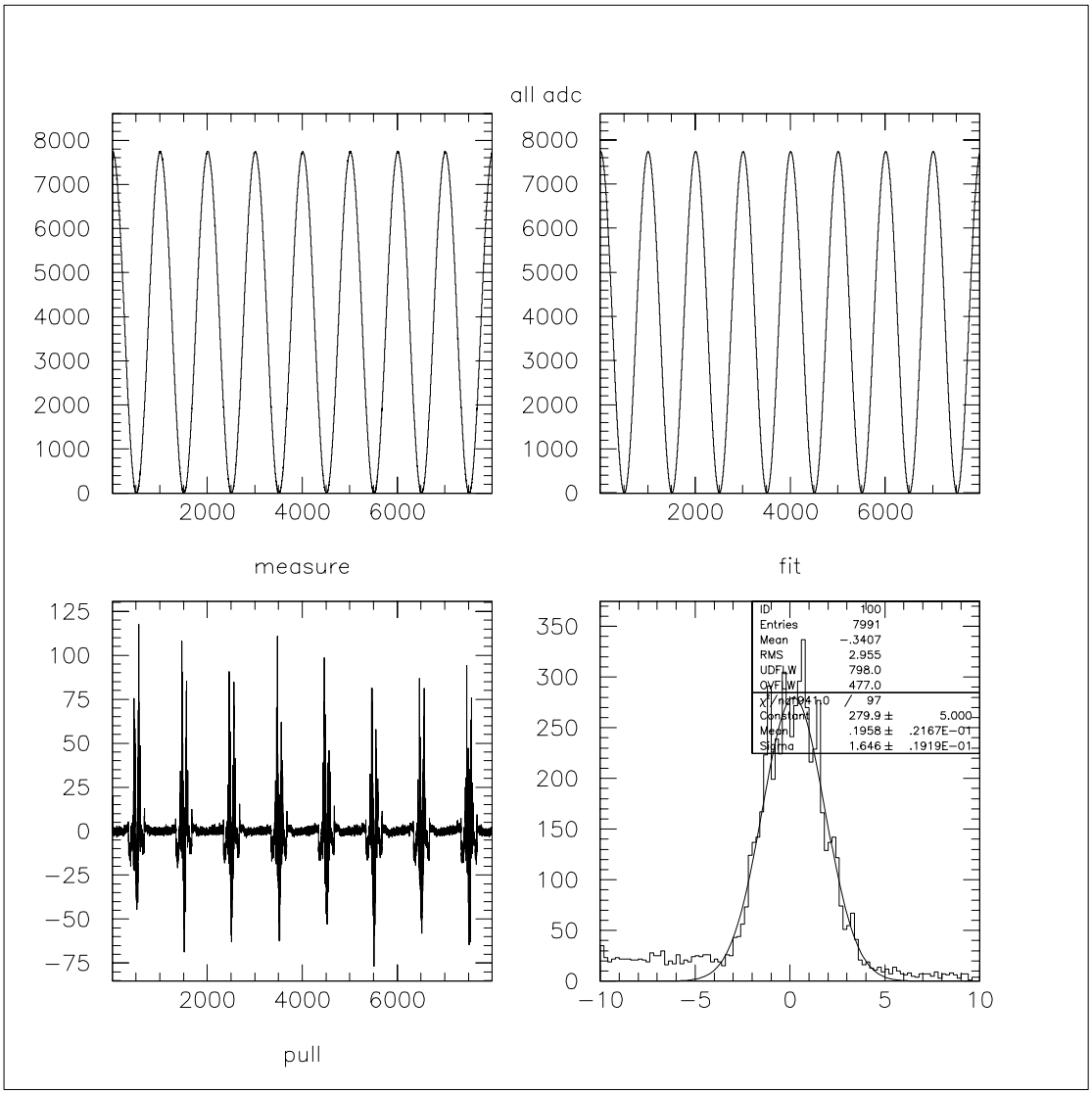


Figure 5: Same as figure 2, but with the CRIAD2 running at 10Msamples/s.

Figure 5 is the same measurement as figure 2 but with an ADC sampling at 10Msamples/s. The ADC shows the same behavior as observed at 5Msamples/s.

5. Pin List

Pin Number	Name	Pin Number	Name
1	VDDD	21	N.C.
2	VSSD	22	N.C.
3	VDDD	23	N.C.
4	VSSD	24	N.C.
5	NVI	25	N.C.
6	RESETb	26	N.C.
7	CLOCK	27	N.C.
8	OEb	28	N.C.
9	B1	29	N.C.
10	B2	30	DIS_OC
11	B3	31	IB
12	B4	32	VSSA
13	B5	33	N.C.
14	B6	34	VDDA
15	B7	35	N.C.
16	B8	36	N.C.
17	B9	37	VIN
18	VSS	38	VREF
19	B10	39	VSS
20	D_GND	40	A_GND

6. Pin Description

VDDD	Two connections to the nominal +3V digital supply voltage. Both must be connected.
VDDA	Connection to the nominal +3V analog supply voltage.
VSSD	Two connections to the nominal -2V digital supply voltage. Both must be connected
VSSA	Connection to the nominal -2V analog supply voltage.
VSS	Cavity and capot. Must be connected to VSSA or VSSD by jumper.
D_GND	Connection to the digital ground.
A_GND	Connection to the analog ground.
CLOCK	Nominal 5MHz Clock input
RESETb	This is an active low input which if asserted, it will provide a synchronous reset of all the internal storage elements. Must be asserted during at least two clock periods.
NVI	Non Valid Input, this is an active high input, which if asserted, it will provide the auto-zero function (automatic offset compensation). During the auto-zero function the digital conversion of the analog input is not performed.
OEb	This is an active low input, which if asserted, it will provide that data outputs (B1 to B10) are activated. If not asserted the outputs are in high impedance state.
B1-B10	This set of ten bits is the digital conversion of the analog input. B1 is the MSB (Most significant bit) and B10 is the LSB (Last significant bit).
VIN	This is the analog input which will be converted. The analog range is 0 V to +2.048 V.
VREF	Voltage reference input. Must be connected to the +2.048V.
DIS_OC	Disconnect Offset Compensation. This active high input which if asserted, it will disable the internal auto-zero system. When set, NVI input is inactive.
IB	Input Bias. 330KΩ resistor to VSSA and decoupling capacitor to VSSA (1nF).

7. Power Consumption & Speed Limit

At 5MHz sampling rate the power consumption was measured as:
Analog components: 5.5mW
Digital power: 4.7mW
Reference ladder: 7.3mW

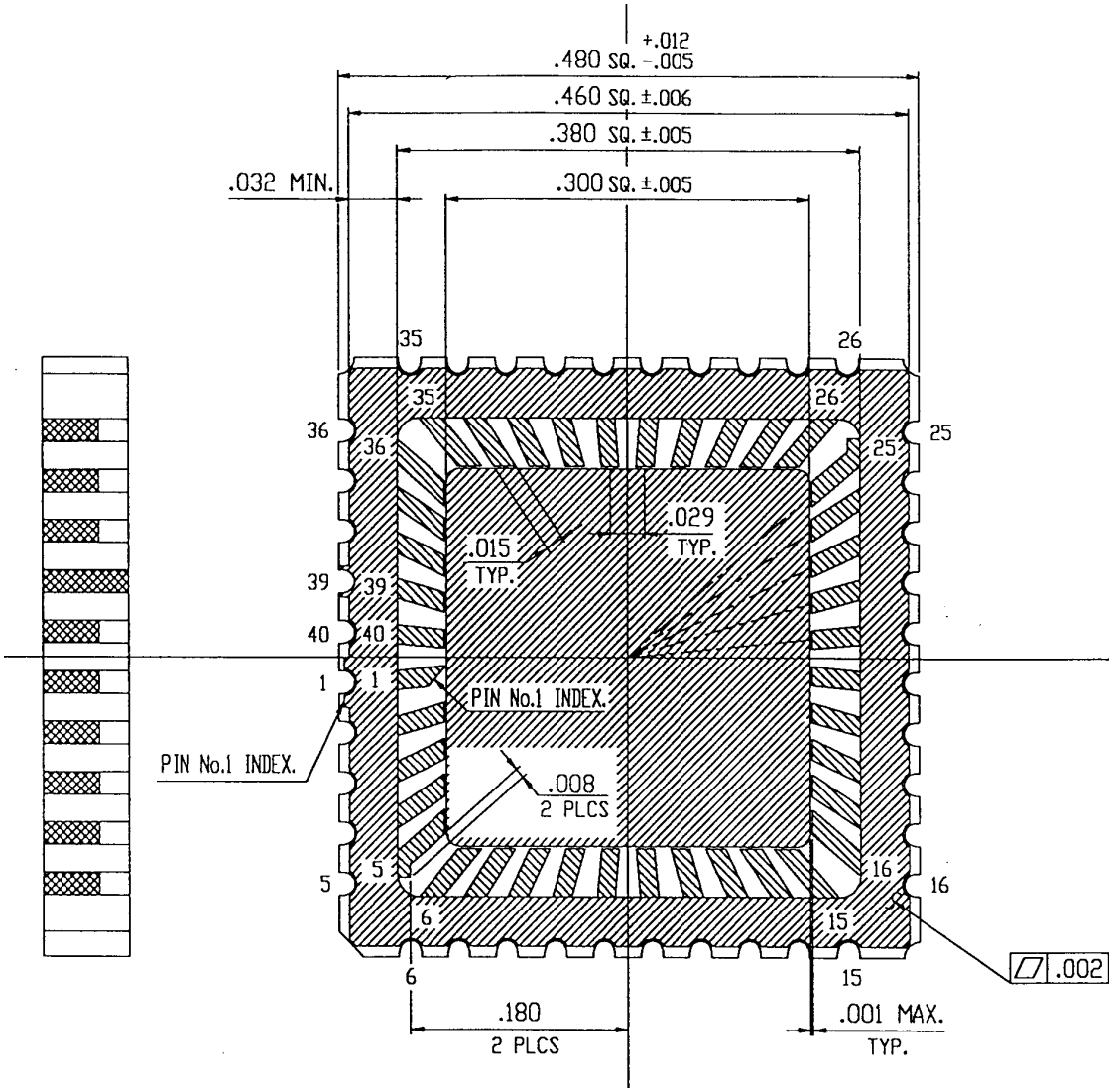
Total power at 5MHz: 17.5mW

At 10MHz sampling rate the power consumption was measured as:
Analog components: 12mW
Digital power: 8mW
Reference ladder: 7.3mW

Total power at 10MHz: 27.3 mW

The present version of the chip runs up to 13 MHz sampling rate (specification was 5MHz, design target was 10MHz). An increase in speed is possible provided there are some optimization done in the digital part of the design.

8. Package Diagram



9. Conclusions

The CRIAD2 is performing to specification in every aspect we can study with the present test bench. Another test bench should be build if one wanted to characterize the design also in the lowest range.
For the silicon tracker of the AMS experiment, the final ADC choice was the COMLINEAR CLC949 which has a slightly better noise performance and was already available at the time of the decision. Nevertheless, the excellent characteristics of the CRIAD2, in particular its smaller power consumption, make it a very good candidate for such applications.