

Attachment CIO8Fm0 with trigger function

and 2BPp - 5HVswitch in ECH 135L

HV-System in ½ - 19" / 3U

Note

The information in this manual is subject to change without notice. We take no responsibility for any error in the document. We reserve the right to make changes in the product design without reservation and without notification to the users.

Document: **cio_relay_timestamp_att** Version: 1.20 Date: **30. May 2006 15:32**

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1.1 Attachment to the summary of CAN data frame accesses via the Front-end-address identifier (cio8_multi_channel_can.pdf 4.4)

Following list describes the accesses of the DCP made for one CIOFFm0_24 module.

Access	EXT_INSTR	DATA_DIR	DATA_ID								read / write / active	DATA-Bytes	Page
			Bit										
	ID1	ID0	7	6	5	4	3	2	1	0			
No DATA_ID	x	x	0	x	x	x	x	x	x	x			
Single access CHANNEL:	1/0	1/0	1	0	S1	S0	M3	M2	M1	M0			
Set time stamp	1	1/0	1	0	1	0	M3	M2	M1	M0	r/w/ a	2/5/ 5(2)	5
Start sequence of time stamped relay switches from buffer	1	1/0	1	0	1	0	M3	M2	M1	M0	r/w/ a	2/5/ 5(2)	5
Group access MODULE:	1/0	1/0	1	1	G3	G2	G1	G0	R1	R0			
Set trigger time	1	1/0	1	1	0	0	0	1	0	0	r/w	3	9
Log-on Front-end device in superior layer	0	1	1	1	0	1	1	0	0	0	a	2	10
Log-off superior layer at Front-end device	0	0	1	1	0	1	1	0	0	0	w	2	10
S _i : Single access													
G _i : Group access													
M _i 0 to 15: Channel 0 to 15													
R _i : reserved													

1.2 Description of data information per DATA_ID in DCP

1.2.1 Single Access

1.2.1.1 Set time stamp (extended single write- / read-write access / active call-back)

The hardware has internal RAM of 1 Kbytes. For handling of all data we need ca. 300 bytes that mean it remain approximately 700 bytes. We suggest you a buffer for different times to switch the relays. The buffer will divided in 3 parts:

-1 byte for the time stamp, witch will mark the call back at the arriving of the time

-2 time bytes as a 16 bit word with a resolution of 1ms (range is 2 ms to 65.535 ms) and

- 1 byte to mask the 5 relays on the Eurocard HV-PS module (0 = relay is closed; 1 = relay is open).

You can load the buffer with 154 different time stamps with an according relay mask for the 4 connected HV-PS modules (channel no. 0, 2, 4, ... , 14) and start then with a single access (start time stamp from buffer). You will get a CAN message with higher priority to control your program if does the different time will be arrived. Than you can reload the next time stamps and so you will get times greater than 65s. A relay mask which would make a short cut of the High Voltage will be rejected by the firmware.

device class 4

read-write access

Byte	ID		DATA_ID	DATA_0		
	ID1	ID0		7	...	0
Data	1	1	0xa0 + M _x	LSB		MSB
Description		read	Channel M _x of 0,2,4, ... 14	time stamp 0 to 254		

Controller (DLC = 2):
Read time stamp and
relay mask at the corresponding
channel

↓ Response module (DLC = 5)

Byte	ID		DATA_ID	DATA_3			DATA_2			DATA_1			DATA_0						
Bit	ID1	ID0		7	...	0	7	...	0	7	...	0	7	...	4	3	2	1	0
Data	1	0	0xa0 + M _x	MSB		LSB	MSB					LSB			R5	R4	R3	R2	R1
Description		write	Channel M _x of 0,2,4, ... 14	time stamp			time						relay mask						

write access (Controller [DLC = 5]: Write time stamp and relay mask at the corresponding channel)

Byte	ID		DATA_ID	DATA_3			DATA_2			DATA_1			DATA_0						
Bit	ID1	ID0		7	...	0	7	...	0	7	...	0	7	...	4	3	2	1	0
Data	1	0	0xa0 + M _x	MSB		LSB	MSB					LSB			R5	R4	R3	R2	R1
Description		write	Channel M _x of 0,2,4, ... 14	time stamp			time			relay mask									

active call back end of time stamp (Module [DLC = 5]: Module send end of time stamp with high priority [ID9=0])

Byte	ID			DATA_ID	DATA_3			DATA_2			DATA_1			DATA_0						
Bit	ID9	ID1	ID0		7	...	0	7	...	0	7	...	0	7	...	4	3	2	1	0
Data	0	1	0	0xa0 + M _x	LSB		MSB	MSB					LSB			R5	R4	R3	R2	R1
Description			active	Channel M _x of 0,2,4, ... 14	time stamp			time						relay mask						

The time stamp will be set on 000 in the buffer in this moment.

DATA_3 time stamp: is a number of 1 to 254, if this number 0 the running of buffer pointer will be stop, the last relay mask will be keep

DATA_2 and 1 time: is a 16 bit word with a resolution of 1ms (max. 65.535 ms)
minimal time is 2 ms (relay transfer time)

DATA_0 relay mask for five relays (see schematic on page 6)
bx = 0 relay is closed / bx = 1 relay is open

active call back end of buffer (Module [DLC = 2]: Module send end of buffer with high priority [ID9=0])

Byte	ID			DATA_ID	DATA_0							
Bit	ID9	ID1	ID0		7	6	5	4	3	2	1	0
Data	0	1	0	0xa0 + M _x	1	1	1	1	1	1	1	1
Description			active	Channel M _x of 0,2,4, ... 14	End of buffer, buffer pointer will be set to the first time stamp							

1.2.1.2 Start sequence of time stamped relay switches from buffer (extended write access)

device class 4

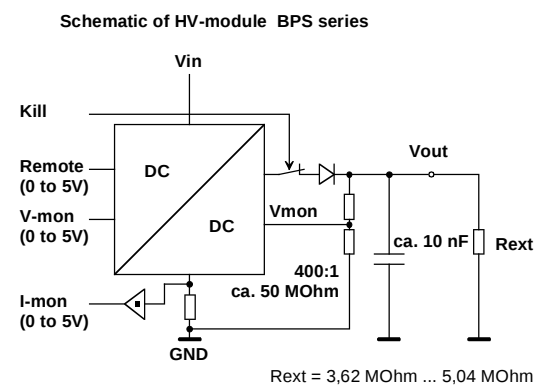
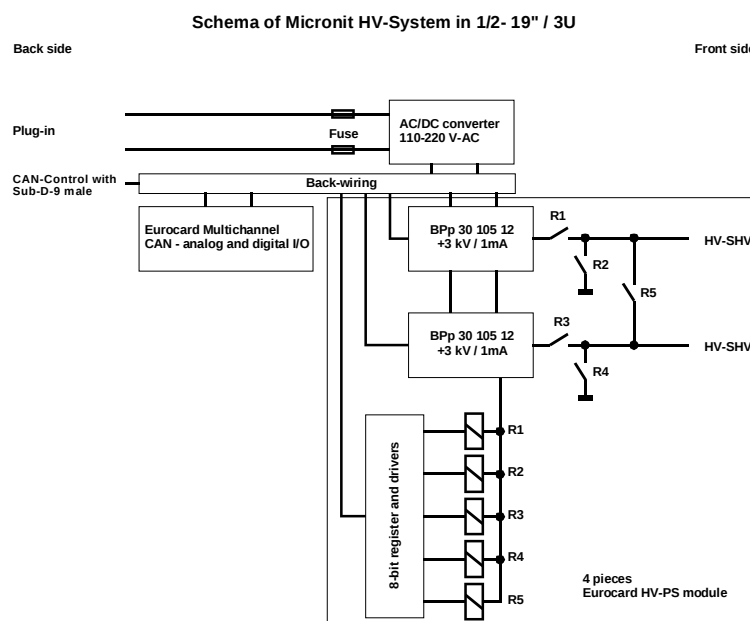
write

Byte	ID		DATA_ID
Bit	ID1	ID0	
Data	1	0	0xb0 + M _x
Description		write	Channel M _x of 0,2,4, ... 14

Controller (DLC = 1):

Start running of time stamps from buffer on according channel

The running of time stamps will be continue up to the first time stamp with the number 0. If the buffer pointer reaches the last buffer address it will begin with the first address again.



1.2.2 Group access

1.2.2.1 Set trigger time (extended group write- / read-write access)

Read-write

Byte	Identifier		DATA_ID	Controller (DLC = 1): Read actual trigger time
Bit	ID1	ID0		
Data	1	1	0xc4	
Description		read		

↓ Response module (DLC = 8)

Byte	Identifier		DATA_ID	DATA_1			DATA_0		
Bit	ID1	ID0		7	...	0	7	...	0
Data	1	0	0xc4	MSB					LSB
Description		write		tt = unsigned 16-bit data word $t_{\text{TRIGGER}} = (tt - 1) * 4 \mu\text{s}$ $3 \leq tt \leq 65536 \Rightarrow 8\mu\text{s} \leq t_{\text{TRIGGER}} \leq 262,14 \text{ ms}$					

This time will be start with the **single access “start time stamps from buffer”**. The start signal is the rising edge from the TTL-signal on the connector “Trigger-out”.

Write (Controller [DLC = 3]: Write new trigger time)

Byte	Identifier		DATA_ID								DATA_1			DATA_0		
Bit	ID1	ID0	7	6	5	4	3	2	1	0	7	...	0	7	...	0
Data	1	0	1	1	0	0	0	1	0	0	MSB					LSB
Description		write									tt = unsigned 16-bit data word $t_{\text{TRIGGER}} = (tt - 1) * 4 \mu\text{s}$ $3 \leq tt \leq 65536 \Rightarrow 8\mu\text{s} \leq t_{\text{TRIGGER}} \leq 262,14 \text{ ms}$					

1.2.2.2 Log-on Front-end device at superior layer (group active access)

After POWER ON the Front-end device will give this group access cyclically on the bus (ca. 1 sec). If a controller of superior layer identifies this access then it is able to register this as a Front-end device and is able to address it with FE_ADR. (see also description of the 11 bit identifier)

DATA_ID=0xD8

all Devices

DATA_1 equal to DATA_0 of general status

DATA_0 information device class of module

DATA_1	DATA_0
see general status	device class

SN. 457xxx device class = 4 8 channel CIO with relay control

SN. 457xxx device class = 5 16 / 8 channel CIO 8V / 8I

SN. 457xxx device class = 8 16 / 8 channel CIO V/I mux normal

1.2.2.3 Log-on/off superior layer at Front-end device (group write access)

After the successful registration the Front-end device will not send further 'Log-on' accesses as long as: it receives accesses from the external CAN Bus in periods shorter than one minute or until the superior controller will send a 'Log-off' access to the Front-end device.

all Devices

DATA_ID=0xD8

DATA_0=1 superior layer send "Log-on" at Front-end device to registration

DATA_0=0 superior layer send "Log-off" to Front-end device