Low–power high dynamic range front–end electronics for the AMS Silicon Tracker

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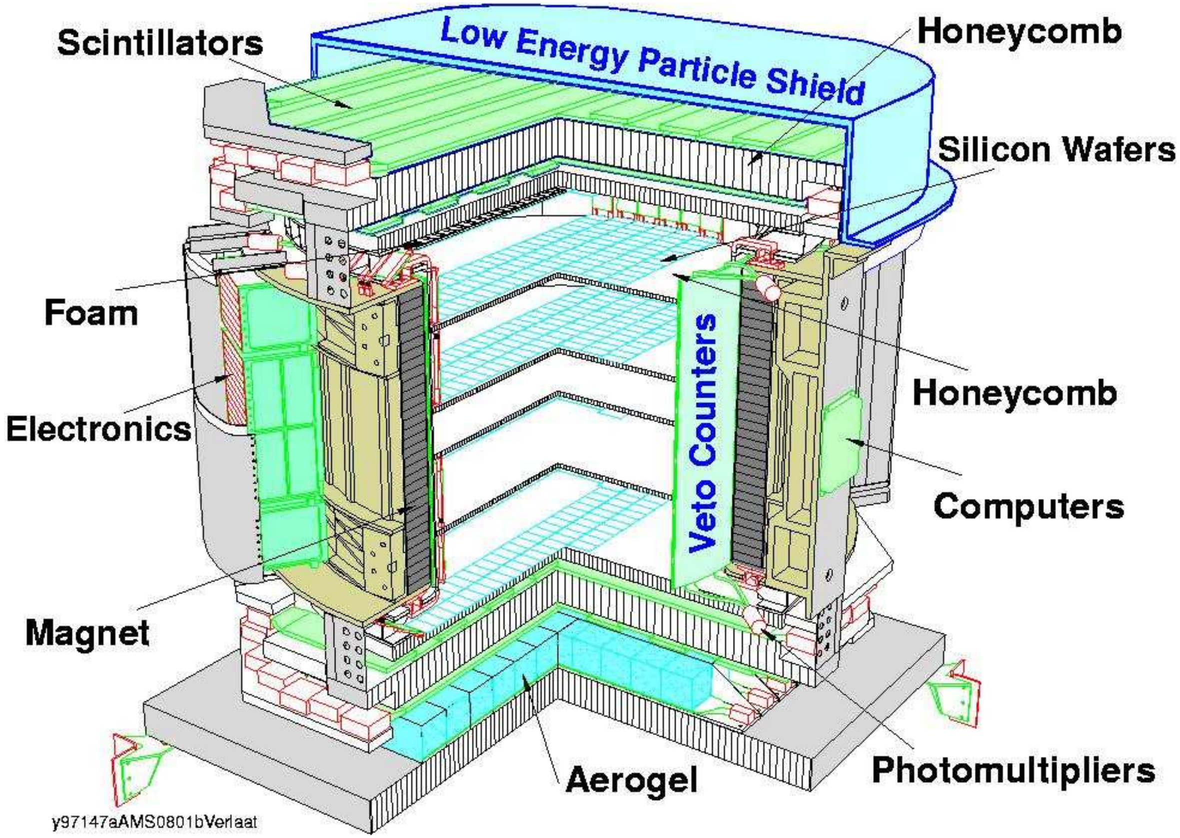
- Introduction to the experiment
- The experience with the VA_hdr.64
- New developments and preliminary results
- Conclusions

The AMS experiment:
a particle physics experiment in space



B field = 0.14 T

TOF → velocity

Tracker → Rigidity (p/|Z|)

→ charge id

Areogel → e/p discrim.

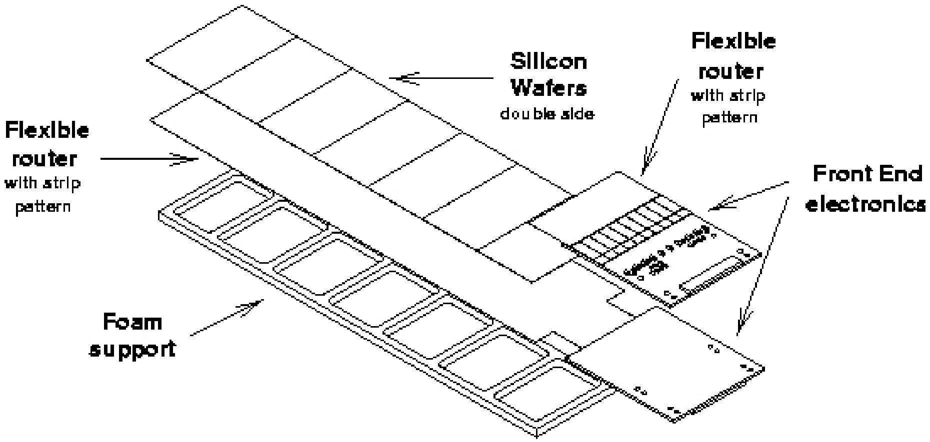
Veto → transverse particles

Detector requirements

- Track reconstruction with ~10μm accuracy
  - ➔ S/N for MIPs greater then 10
- dE/dx measurements for $|Z| \leq 10$
  - ➔ high dynamic range, 3.6 – 360 fC
- Avoid passive material in the acceptance
  - ➔ electronics at the end of the ladder, C_{det} ~ 60 pF
- Continuos shaping (random trigger)
- Negligible dead time at 1kHz trigger rate

Silicon Tracker numbers ...

- Double side, 300 μm thick, silicon microstrip detector
- Readout pitch = 110 μm (strip pitch = 27.5 μm) on p^+ side
- Readout pitch = 208 μm (strip pitch = 26 μm) on *n* side
- 57 ladders, for a total of 720 detectors (2.1 m^2)
- 912 VA_hdr.64 chips, for a total of 58368 readout channels



System limitation
(the detector operate in space)

- Tight schedule (4 years to project and build the detector)
- 1 kWatt power limit for the whole experiment
  - ➔ max 1mW per front–end channel
- operation in vacuum
  - ➔ no convection for heat dissipation
  - ➔ materials choice
- Severe mechanical stress at launch
  - ➔ robust (space qualified) assembly

On orbit constraints

- Single event latch–up
  - ➔ protected power lines
- Single event upset
- Modest radiation level (1kRad/year)
- No access to the detector or its electronics
  - ➔ reliability
  - ➔ avoid single point failure

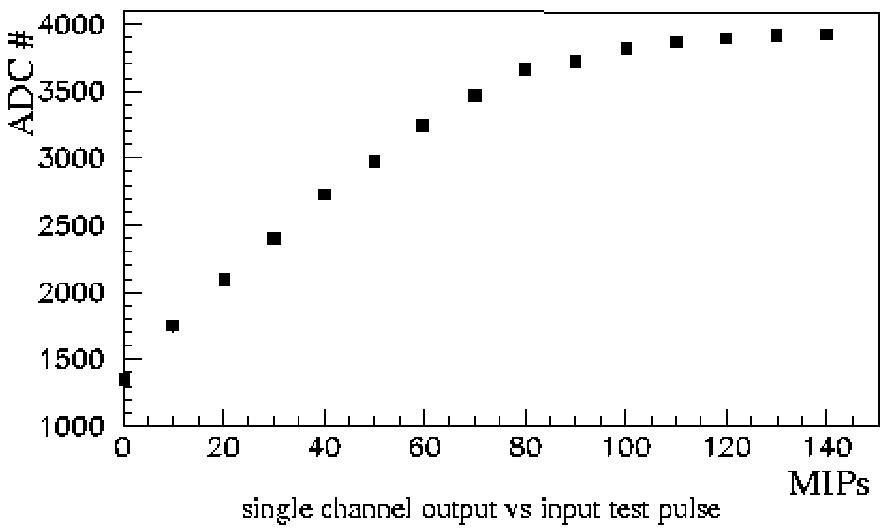
Solution for the front–end: VA_hdr.64

- Direct development from a well known chip (the VA from IDEas, Oslo)
- AMS 1.2 μm technology
- Measured:
  - ➔ Power consumption: 0.7 mW/channel
  - ➔ ENC = (350 + C_{det} ∗ 4/pF) e^- at 6 μs shaping
- Expected latch –up rate < 10^{-3}/day/chip

  (ions test done in Dubna)

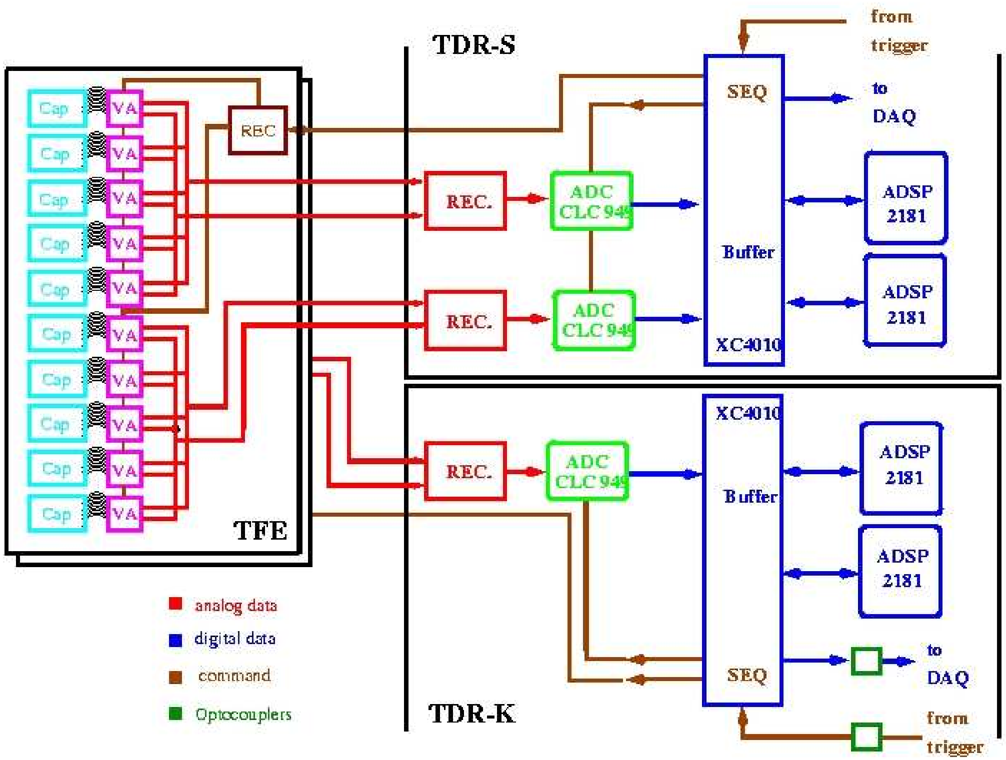
VA_hdr.64

- 64 Charge ampli, CR−RC shaper, S&H plus analog multip.
- +/− 100 MIPs dynamic range
- Shaping time ~4 μs



Readout chain

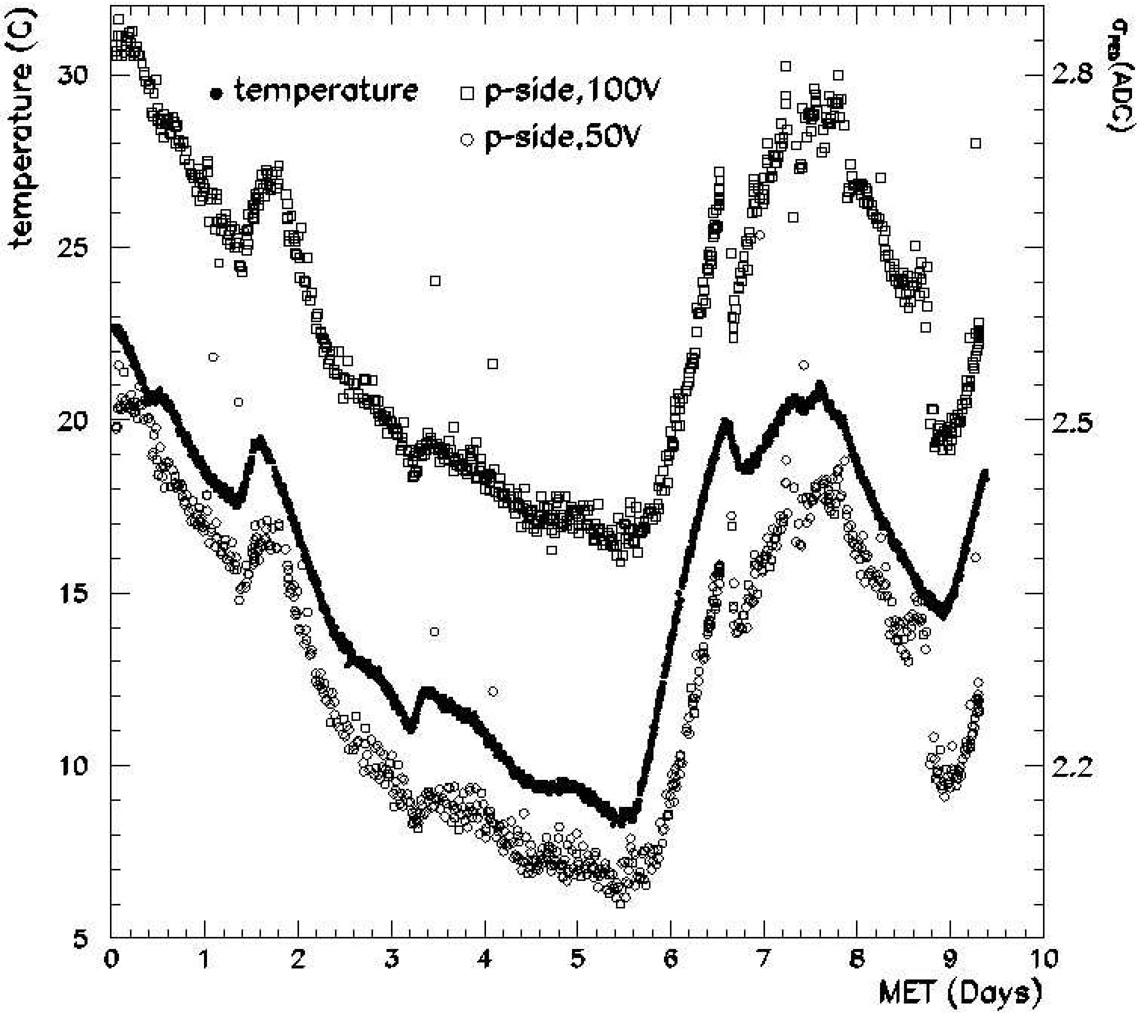
- 12 bit, low power ADC (CLC949)
- Data compression performed by the ADSP–2181
- On n–side Vbias is decoupled after the data compression



The STS–91 mission

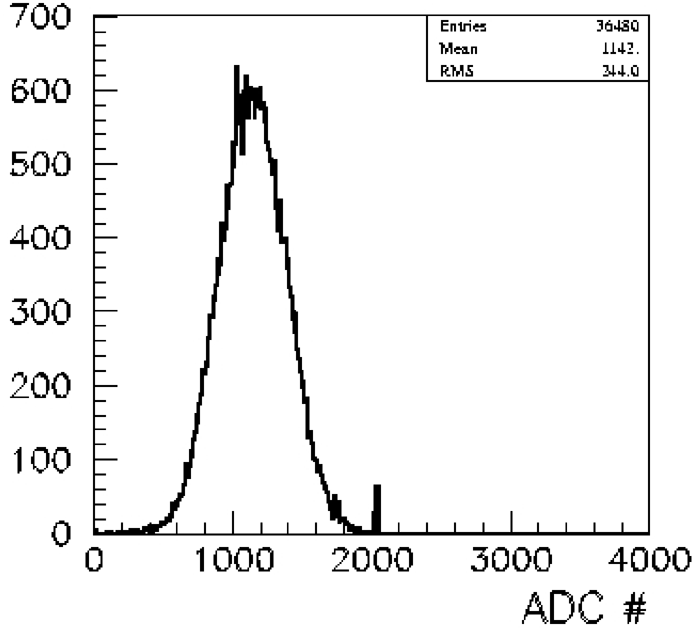
- AMS had a 10 day mission on board the Space Shuttle Discovery, on June 2–12 1998
- Performance of the detector in flight were comparable to the ground test results
- No failures has been observed in the Silicon Tracker system

Noise evolution
(738 calibrations during the STS–91 mission)

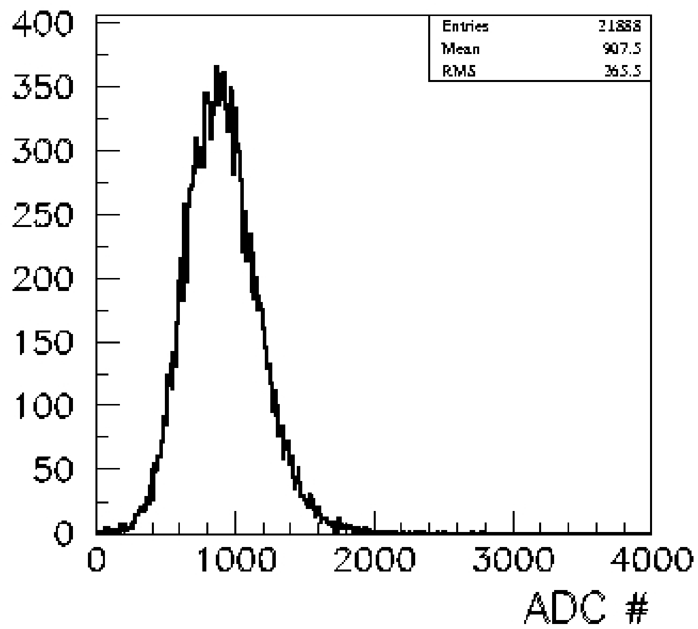


1 MIP = 28 ADC #

Pedestal spread
(one calibration during the STS–91 mission)



P side



N side

1 MIP = 28 ADC #

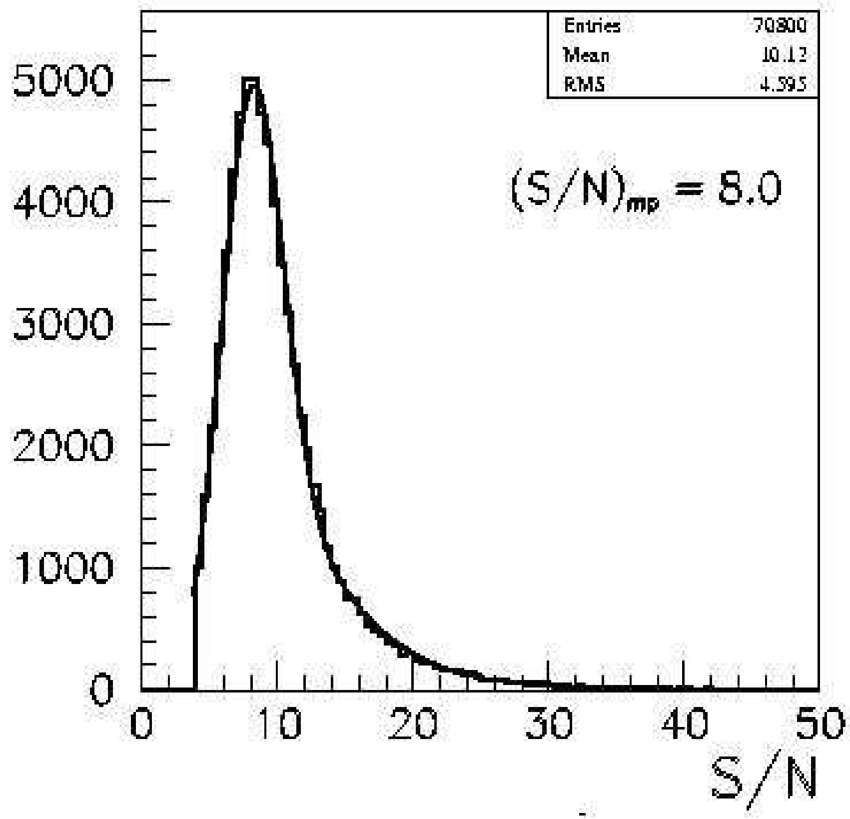
Signal to noise ratio for MIPs

- S/N defined as

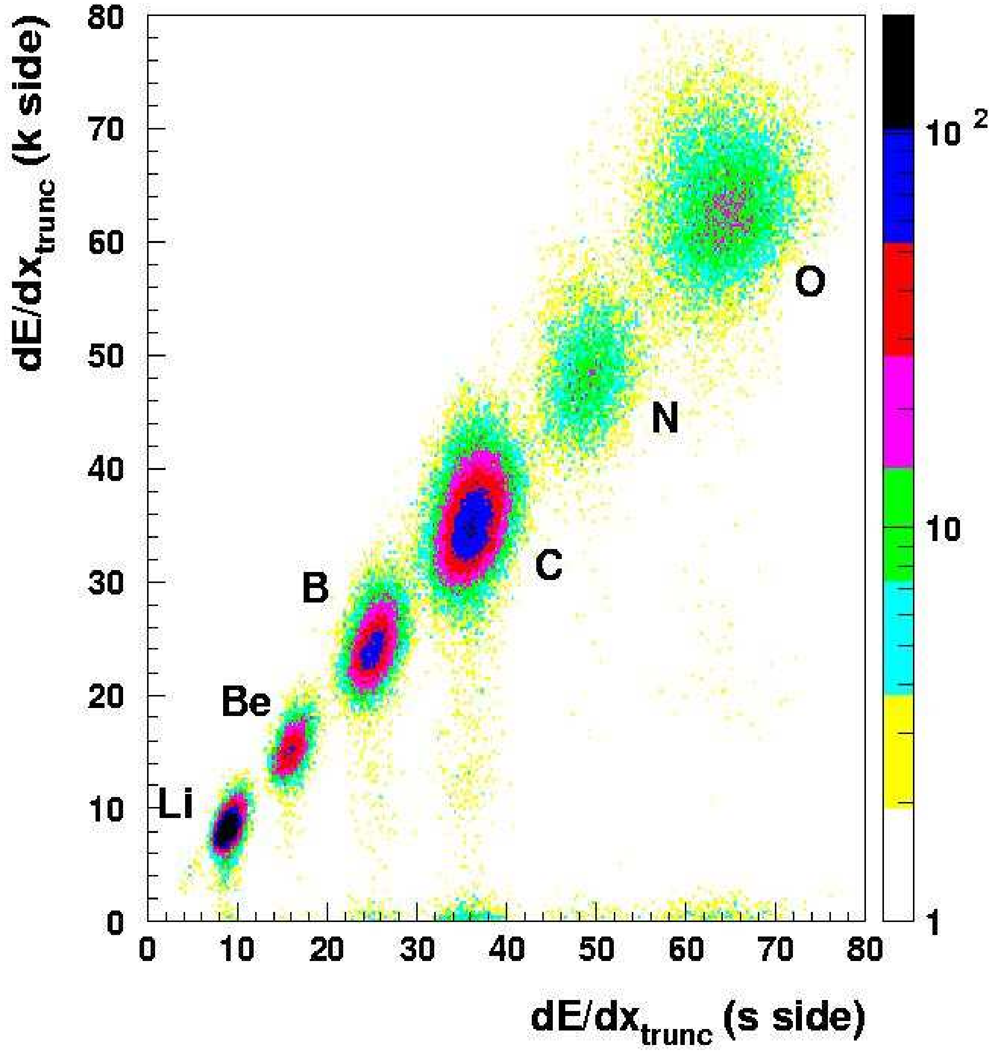
  $\sum Q_i / (\sum \sigma_i^2)^{1/2}$

  Q_i = strip signal, σ_i = strip noise

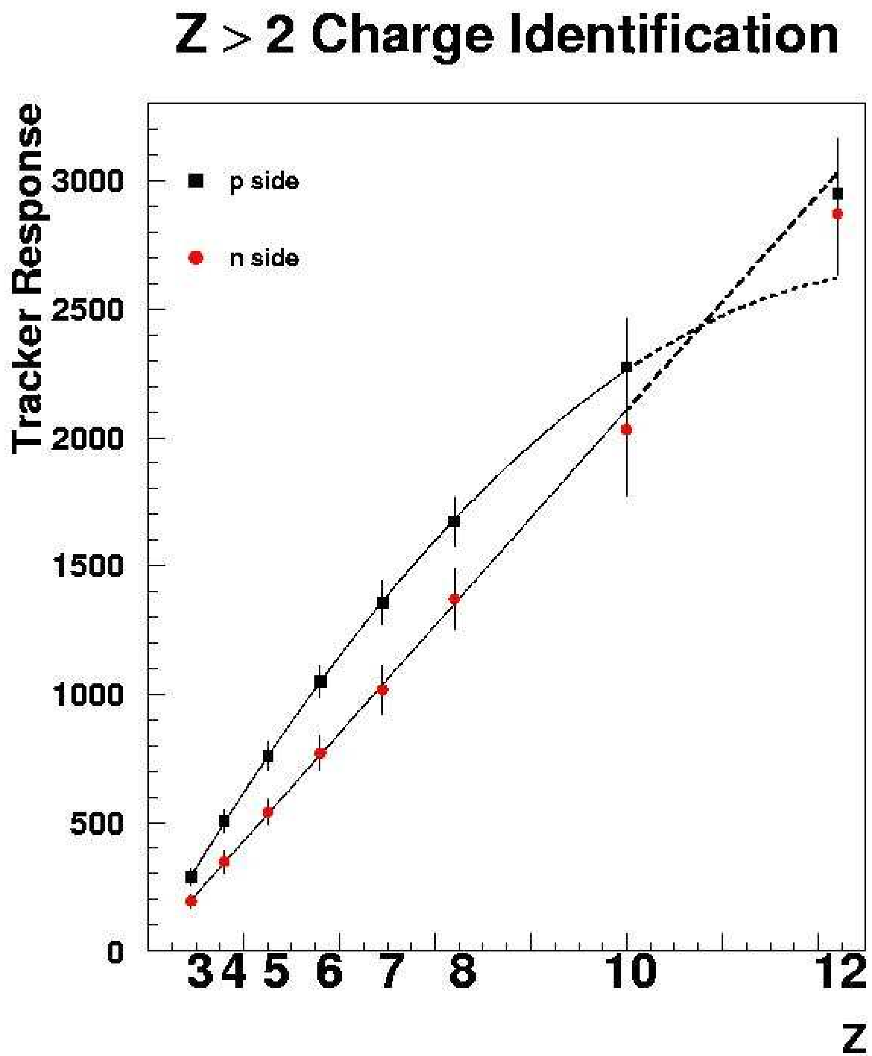
- Fit performed with a Gaussian plus a Landau



dE/dx measurement in the Tracker

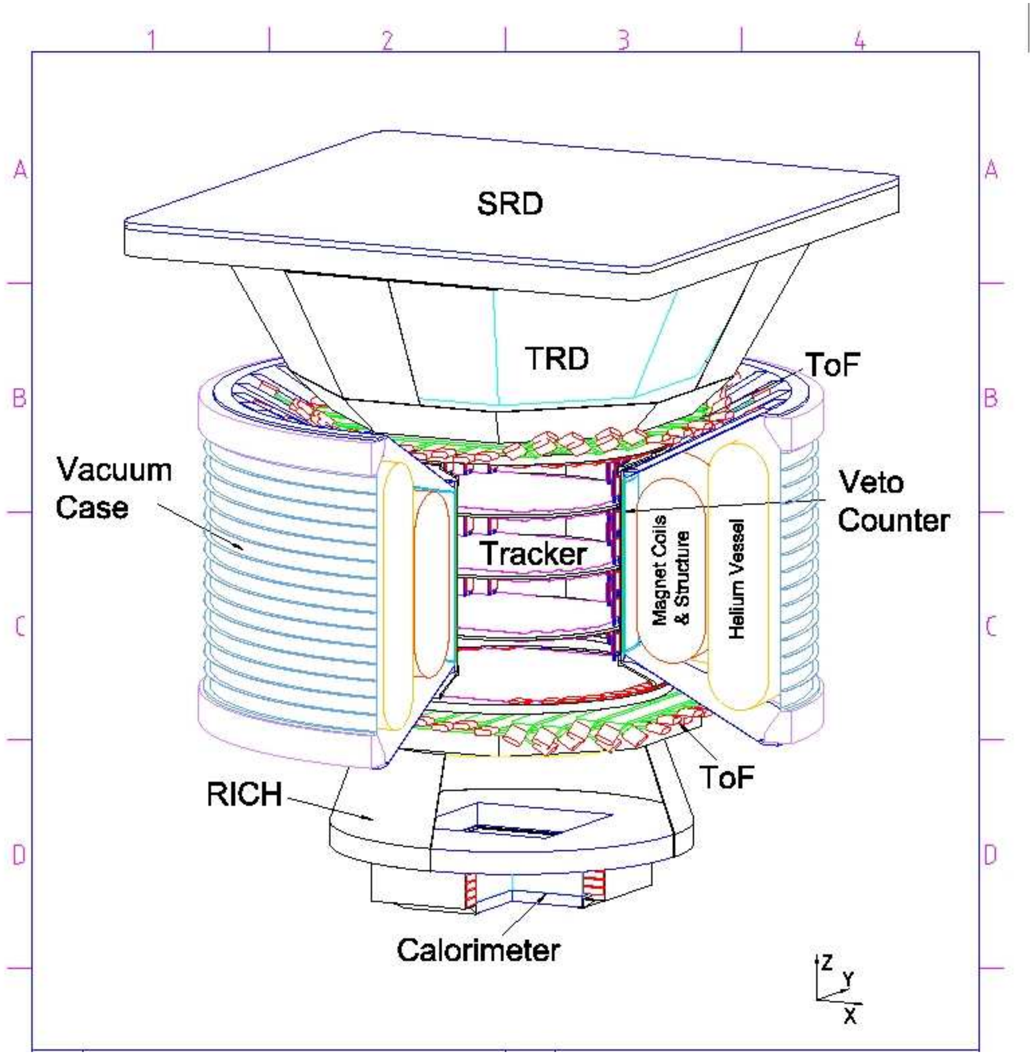


|Z| measurement by the Tracker



AMS – 02

Next flight will be on January 2004 for a three year stay on the International Space Station



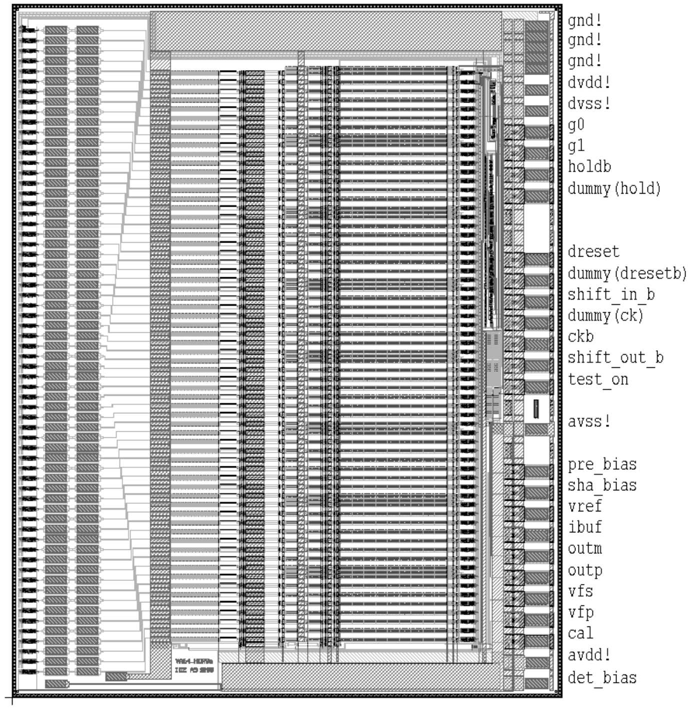
Reasons for a better chip:

- Smaller pedestal spread
- Higher gain (not too much)
- Higher radiation tolerance:
  - ➔ total dose
  - ➔ latch–up immunity
- Avoid parameter setting

The ’new’ chip: VA_hdr9a

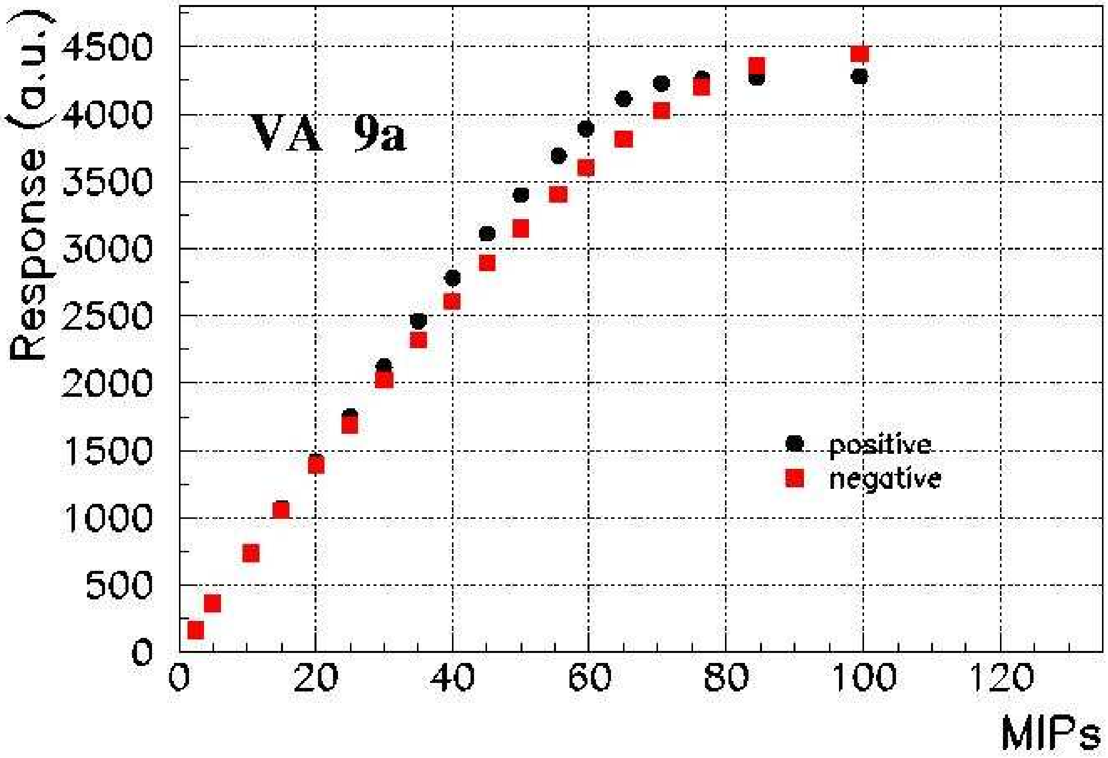
- Nominal shaping time 6 μs
- Nominal gain 1.4 μA/fC
- Internally generated biases

  (Ipre, Ish, Ibuf, VFS, VFP)
- Internal calibration capa.
- ENC = (300 + C_{det}* 5/pF) e^-
- Sample available in 0.8 μm



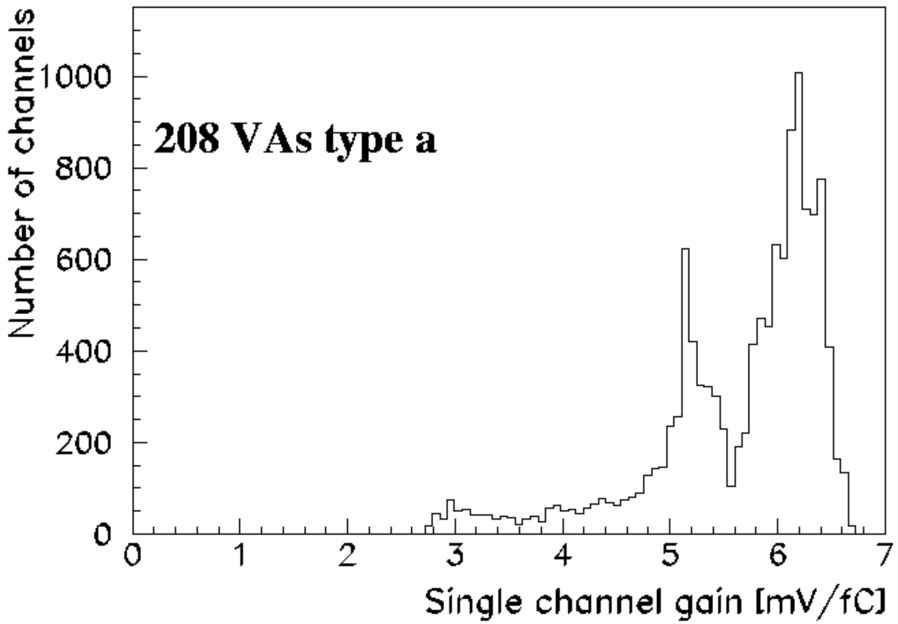
VA_hdr9a test results 1

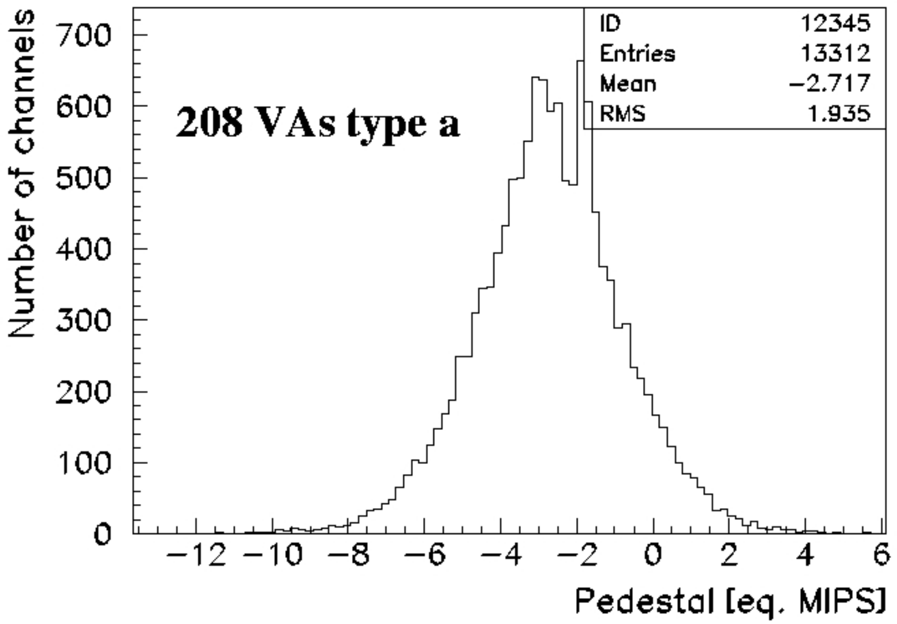
- Gain and dynamic range as expected



VA_hdr9a test results 2

- Good gain uniformity
- Small pedestal spread



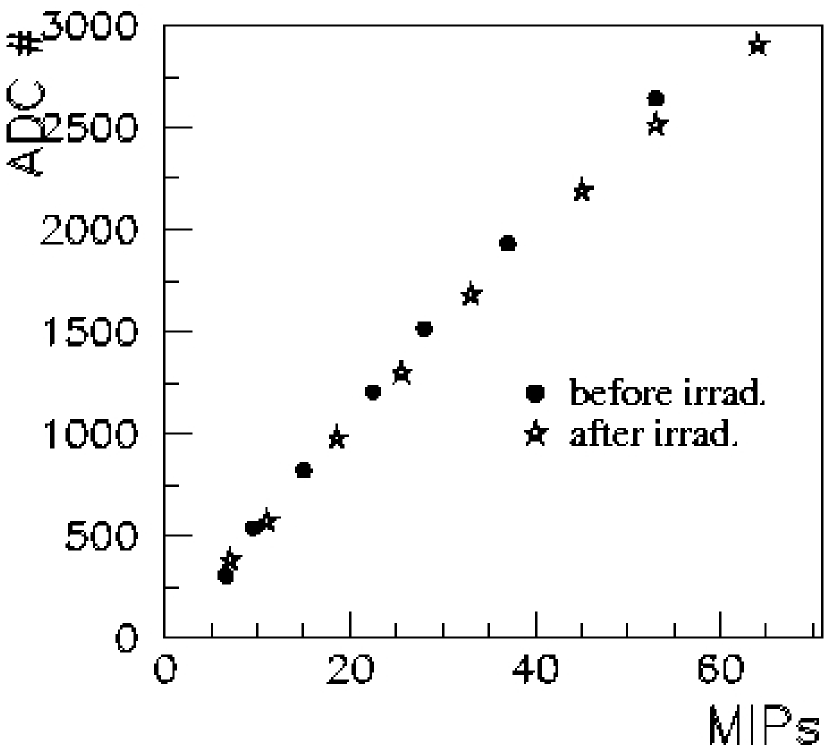


Total dose tests

'low' radiation level (30 Krad or .03 Mrad)
with a ^{60}Co

- Using the same parameters (only VFP is external):
  - ➔ no gain variations
  - ➔ no noise increase

    (noise < 350 e^-)



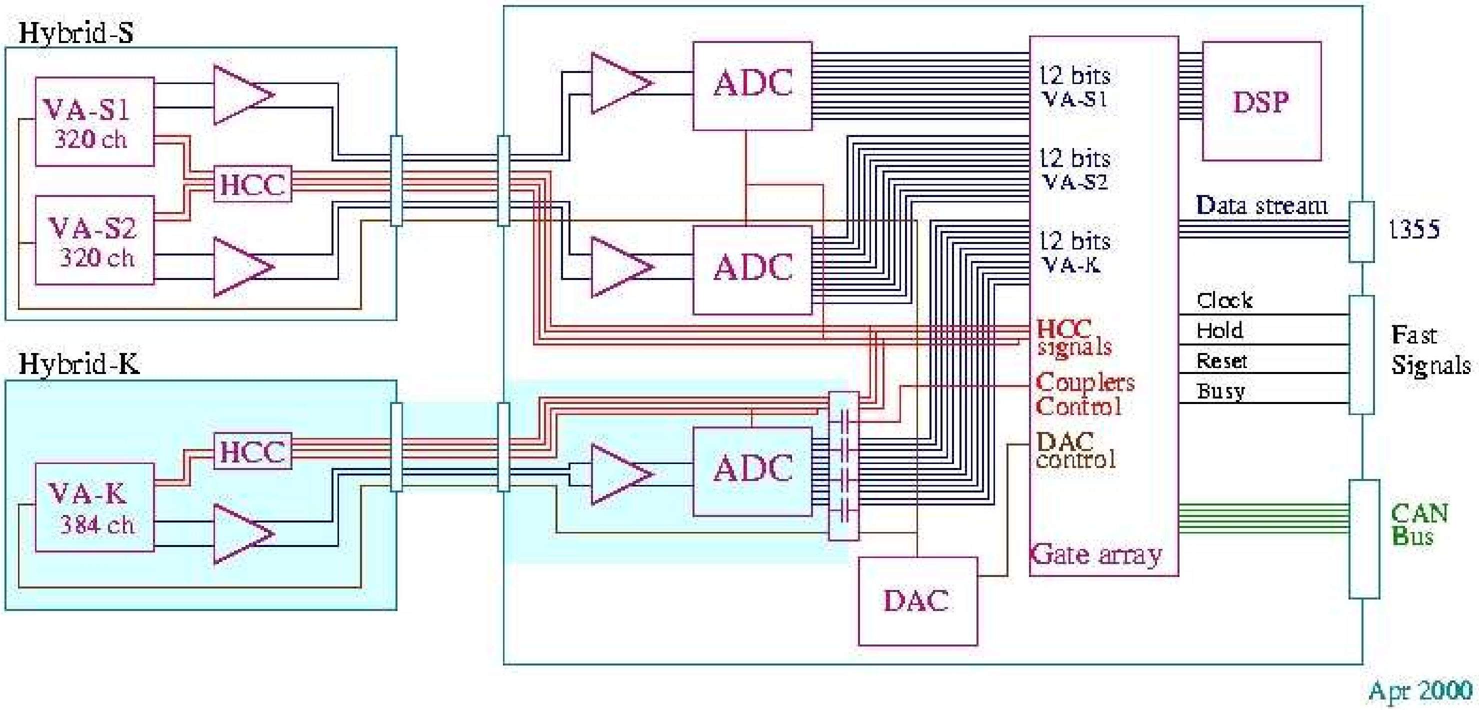
Latch–up tests

- Measurement with ions are foreseen in the next months in Dubna
- Preliminary measurement of laser–induced latch–up done in Perugia: latch–up is seen only on chips (VA_hdr.64) without epitaxial layer

Towards a better system

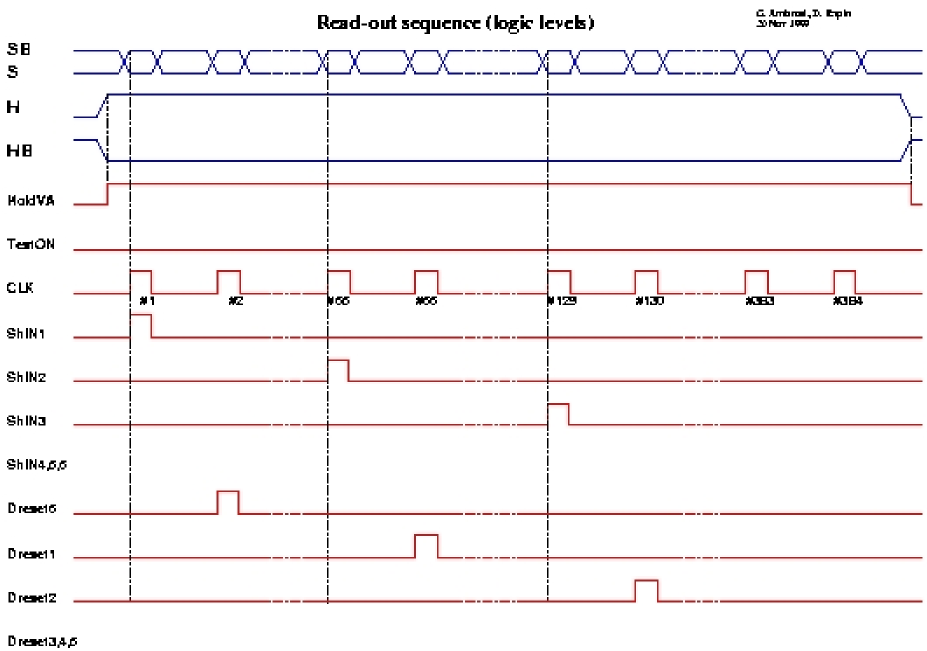
- Better performance of the front –end chip
- Analog and digital part will be decoupled on both *p* and *n*
- Digital electronic will be powered at 3.3 V
- Better daisy chain control (HCC)

’New’ readout scheme



HCC
(Hybrid Control Circuit)

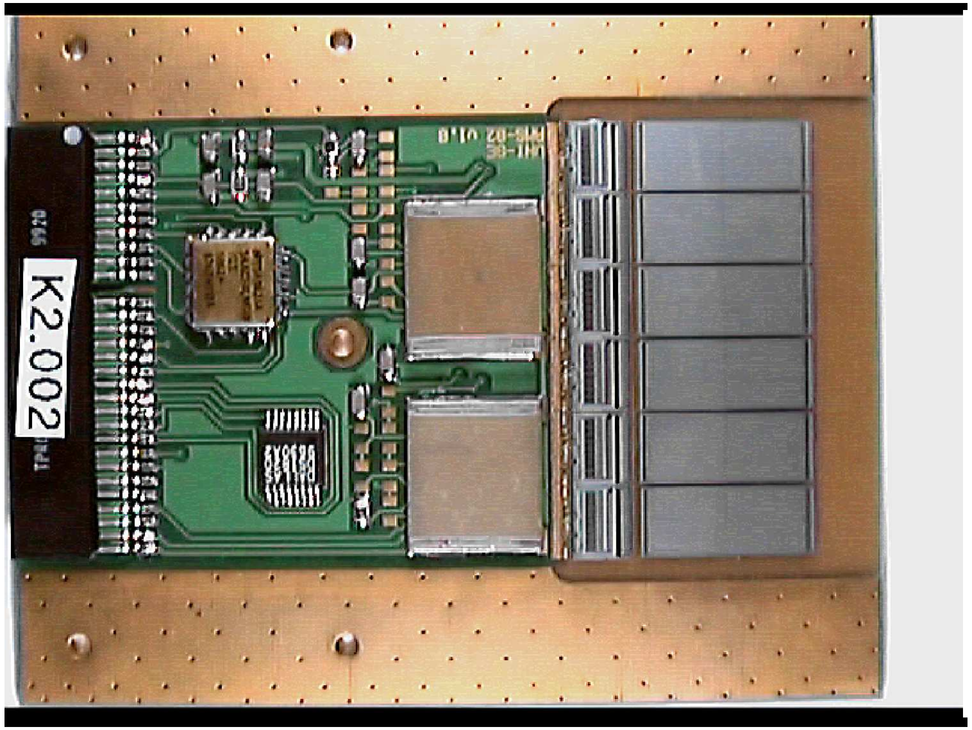
- Designed by Aurelia μ (C.A.E.N.) on our specs.
- Minimize the digital line on the cable
- Control the daisy chain of the VA
- Increase the system reliability (0.8 μm plus epitaxial layer from AMS)
- Designed according to 'space' rules (triple redundancy plus majority vote)

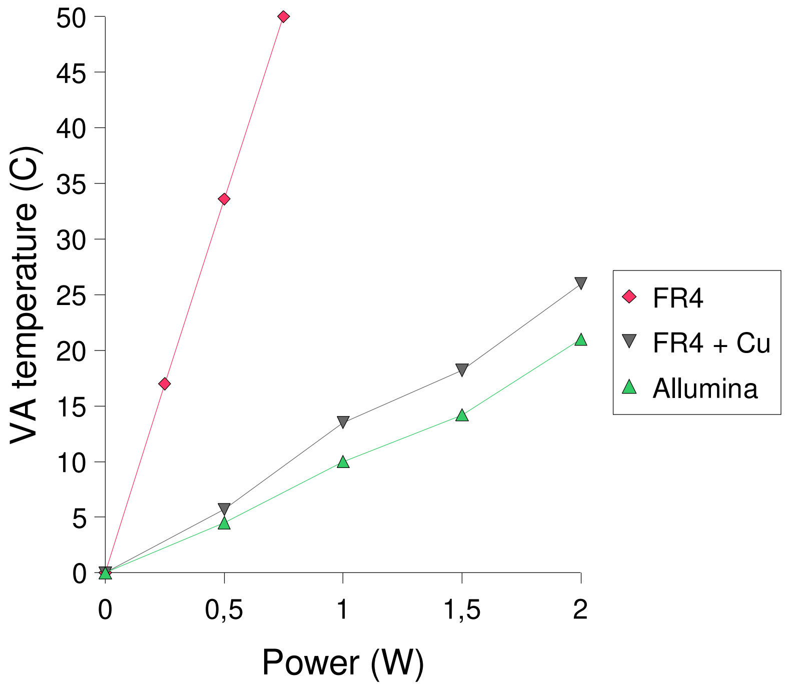


’New’ hybrid (TFE)

- Pure FR4 substrate, 4 layer

  (easy to design and fast to produce)





Space constraints

- ✔ Vacuum: ➔ assembly
- ✔ Vibration: ➔ assembly
- ✔ Limited power: ➔ design and component choice
- ✔ Limited temp. control: ➔ elec. + mechanics
- ✔ Total dose: ➔ electronics production tech.
- ✔ SEL: ➔ electronics production tech.
- ✔ SEU: ➔ Elect. Design and production tech.

Conclusions

- HEP detector and electronics technology are suited for space based experiment
- Thanks to the successful experience with AMS – 01 we are preparing a better system
- The basic element for the front – end and readout system of the Silicon Tracker are ready
- We look forward for the AMS – 02 flight