T-crate and TPD slowcontrol tests

July 18, 2005

1 LeCroy syntax

The LeCroy command is composed of 32 bits. By convention, the MSB is bit 1 (written "S1"). The S1 is always 1, the S2 is the parity bit, while in our case S3 and S4 are ignored and arbitrarily set to 1 and 0 respectively. Thus in hexadecimal notation the command will always either be 0xannn or 0xennn, depending on the parity.

2 Actelbrother control

See Sándor's documentation. For all boards (S9011AT, TPSFE, TBS) the Actel status and Actel control registers (address 1) structure is as follows:

Read	
Bit	Meaning
0	Actelbrother off status
1	Actelbrother on status
4	Actel status (stat. reg.)
8	Actel trip (stat. reg.)

Write		
Bit	Meaning	Comment
0	Actelbrother off	
1	Actelbrother on	(supersedes bit 0)
4		
8		

Note: For the control register, only the Actelbrother bit combination 01 (i.e. 0x0001) switches off the Actelbrother. The default bit configuration is 10 (i.e. 0x0002): both FPGAs are on.

3 Remark about the FPGAs

It is important to mention that the LAST COMMAND register only describes the last command the FPGA sent: it is not necessarily the actual state of the system. For this one need to look at the FEEDBACK register. Indeed FEEDBACK corresponds to the OR of the command register of both FPGAs, which is the real command taken into account. See section 4.7 for an example.

4 S9011AT

4.1 LeCroy commands

As we only have one S9011AT, the address will remain the same, i.e. bits 5 to 7 are 0, bits 8 and 9 are 1: this corresponds to address 3 (this value is the result of a misunderstanding, see Sándor's documentation). We need four bits to address the S9011AT registers, thus bit 12 will be used as the MSB for the register address. Thus a LeCroy command has following structure:

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
0xA or 0xE				0	0	0	1	1	0	0	reg_3	R/W	reg_2	reg_1	reg_0

The next 16 bits are data bits (register content), if the write mode is chosen, or just 0's in the read mode.

4.2 Bus, half

There are two LeCroy cables connecting the TBP to the S9011AT. Each JINF has access to both connections (named HALF A and HALF B).

The buses are related to the two FPGAs (Hot and Cold) of the S9011AT. From the 3.3 V power supply point of view (fig. 1), JINF A as well as the FPGA Hot of the S9011AT are powered by S9053 half A. JINF B as well as the FPGA Cold of the S9011AT are powered by S9053 half B. So, one JINF (A or B) has four ways to do slow control communication: using FPGA ("bus") Hot or Cold via the connections ("halves") A or B.

This leads us to a particular aspect of the 3.3 V supply.

4.3 S9011AT FPGA and 3.3 V control

As the FPGAs are themselves supplied with 3.3 V, the S9011AT scheme (see fig. 2) is done in such a way that if an FPGA asks to its own S9053 to stop supplying 3.3 V, the S9053 will be switched on again.
Thus it is not possible to completely switch off the 3.3 V supply.

4.4 Read Registers description

- Register 0 is the SEL register, bit 0 is set to 1 after a switch on and is automatically cleared after readout.
- Register 1 is the Actel status and last command register, see section 2.
- Register 2 describes the low voltage DCDC converters (±2 V and 5.6 V) *last command*, according to following table:

bit	DCDC	Comment
0	9051_0 A (±2, 5.6 S_0)	1=off, 0=on
1	9051_0 B (±2, 5.6 K_0)	1=off, 0=on
2	9051_1 A (±2, 5.6 S_1)	1=off, 0=on
3	9051_1 B (±2, 5.6 K_1)	1=off, 0=on
4	9051_2 A (±2, 5.6 S_2)	1=off, 0=on
5	9051_2 B (±2, 5.6 K_2)	1=off, 0=on
6	9051_3 A (±2, 5.6 S_3)	1=off, 0=on
7	9051_3 B (±2, 5.6 K_3)	1=off, 0=on
8		

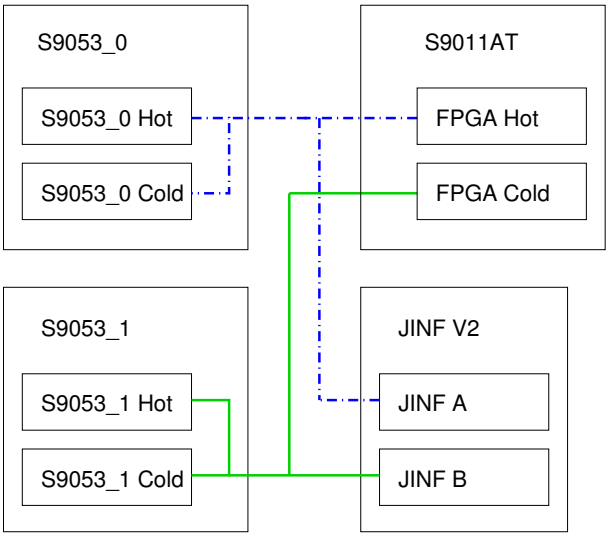

Figure 1: Simplified scheme of the 3.3 V supply distribution

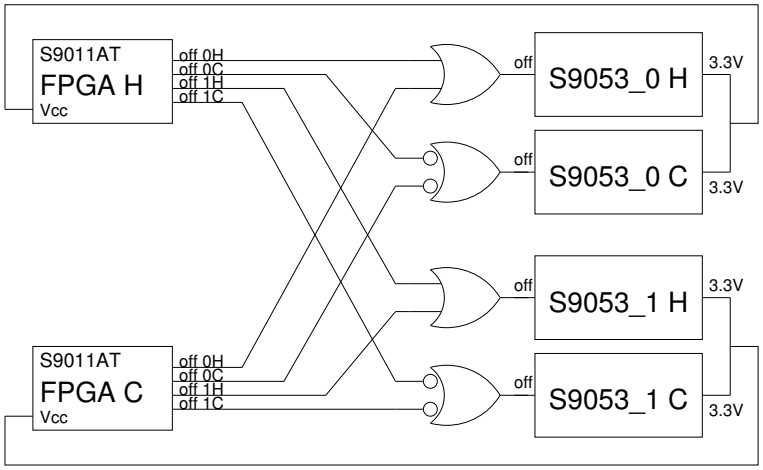

Figure 2: Control of the 3.3 V by the S9011AT FPGAs: if the FPGA switches off its own supply, it will be re-established.

- Register 3 indicates if a trip occurred to one of the low voltage DCDC converter, following the same relation bit↔DCDC converter as for register 2.
- Register 4 describes the high voltage DCDC converters (120 V/±6 V and 3.3 V) *last command*, according to following table:

bit	DCDC	Comment
0	9053_0 Hot	1=off
1	9053_0 Cold	0=off
2	9053_1 Hot	1=off
3	9053_1 Cold	0=off
4	9055_0 Hot	1=off
5	9055_0 Cold	1=off
6	9055_1 Hot	1=off
7	9055_1 Cold	1=off
8		

- Register 5 indicates if a trip occurred to one of the low voltage DCDC converter, following the same relation bit↔DCDC converter as for register 2.
- Register 6 is the *feedback* of the on/off control for low voltage DCDC converters (same bit correspondences as register 2).
- Register 7 is the *feedback* of the on/off control for high voltage DCDC converters (same bit correspondences as register 4).

4.5 Write Registers description

- Register 0 allows to clear the SEL bit (if bit 0 is set to 1).
- Register 1 controls the Actelbrother (see section 2).
- Register 2 controls the low voltage DCDC converters, following the same convention as for the read register 2.
- Register 4 controls the high voltage DCDC converters, following the same convention as for the read register 4.

4.6 AMSWire commands

The AMSW command used to send LeCroy commands is as follows:

$$\texttt{0x2E1D addr lecroy}_1\ \texttt{lecroy}_2$$

`addr` indicates the FPGA and half to be used. In the case of the S9011AT, we have $addr = 0x40 + (half << 5) + (fpga << 4)$ i.e.

Half	FPGA	Address
A	Hot	0x0040
A	Cold	0x0050
B	Hot	0x0060
B	Cold	0x0070

4.6.1 Data read

Command name	Syntax	Comment
Read SEL status	`E180 0000`	Set to 1 at startup, autoclear
Read Actelbrother status	`A181 0000`	Default is 2
Read DCDC-L last cmd	`A182 0000`	
Read DCDC-L tripped	`E183 0000`	Autoclear
Read DCDC-H last cmd	`A184 0000`	
Read DCDC-H tripped	`E185 0000`	Autoclear
Read DCDC-L feedback	`E186 0000`	
Read DCDC-H feedback	`A187 0000`	
Read DCDC-L status	`A190 0000`	
Read DCDC-H status	`E191 0000`	

4.6.2 Data write

Command name	Write	Comments
Turn off Actelbrother	`A189 0001`	
Turn on Actelbrother	`A189 0002`	
Turn on/off DCDC-L	`n18A 00nn`	
Turn on all 120 V / ±6 V	`E18C 000n`	n=3.3 V control
Turn off 120 V / ±6 V	`E18C 00fn`	
Set 120 V / ±6 V to Cold only	`E18C 005n`	
Set 120 V / ±6 V to Hot only	`E18C 00an`	
Turn off S9053_1 (S9053_0 Hot on)	`A18C 00n4`	n=120/±6 V control
Turn off S9053_0 (S9053_1 Hot on)	`A18C 00n1`	
S9053_0 and _1 Hot on (Cold are off)	`E18C 00n0`	
S9053_0 and _1 Cold on (Hot are off)	`E18C 00nF`	

4.7 S9053 Hot ↔ Cold switching

To save power consumption, the 3.3 V Hot and Cold DCDC converters are ORed with FET. This has a drawback: *Hot and Cold must not be operated simultaneously.* As for now the FPGAs do not control this particular state, the user has to pay attention for it. A special case is the one for which the user asks to switch from Hot to Cold. Consider a state where all 3.3 V Hot are on. The sequence would be following (see figure 2):

Step	Description	Reg. 4, bits 0→3		Feedback	Comment
		FPGA H	FPGA C		
0	Initial state: Hot 3.3 V are on	0000	0000	0000	
1	FPGA C switches off S9053_0 H	0000	0001	0001	
2	FPGA C switches on S9053_0 C	0000	0011	0011	
3	FPGA H switches off S9053_1 H	0111	0011	0111	
4	FPGA H switches on S9053_1 C	1111	0000	1111	Cold off: bits are 0
5	Final state: Cold 3.3 V are on	1111	0000	1111	Cold after start: default is 0

Due to the fact that the feedback registers reflect the real command sent to the S9053, and is the OR of the registers of the two FPGAs Hot and Cold, the way to go back to cold is non-trivial. The following sequence, for instance does not work:

Step	Description	Reg. 4, bits 0→3		Feedback	Comment
		FPGA H	FPGA C		
0	Initial state: Cold 3.3 V are on	1111	0000	1111	
1	FPGA C switches off S9053_0 C	1111	1101	1111	No effect !
2	FPGA C switches on S9053_0 H	1111	1100	1111	No effect !
3	FPGA H switches off S9053_1 C	0100	1100	1100	Glitch on A !
4	FPGA H switches on S9053_1 H	0000	1100	1100	No effect !

Starting with FPGA Hot does not help either:

Step	Description	Reg. 4, bits 0→3		Feedback	Comment
		FPGA H	FPGA C		
0	Initial state: Cold 3.3 V are on	1111	0000	1111	
1	FPGA H switches off S9053_1 C	0111	0000	0111	
2	FPGA H switches on S9053_1 H	0011	0000	0011	
3	FPGA C switches off S9053_0 C	0011	0001	0011	No effect !
4	FPGA C switches on S9053_0 H	0011	0000	0011	No effect !

The best way to proceed is to switch off the Actelbrother when needed:

Step	Description	Reg. 4, bits 0→3		Feedback	Comment
		FPGA H	FPGA C		
0	Initial state: Hot 3.3 V are on	0000	0000	0000	
1	FPGA C switches off S9053_0 H	0000	0001	0001	
2	FPGA C switches on S9053_0 C	0000	0011	0011	
3	FPGA H “copies” register of Cold	0011	0011	0011	
4	FPGA H switches off S9053_1 H	0111	0011	0111	
5	FPGA H switches on S9053_1 C	1111	0000	1111	
6	FPGA C switches off S9053_0 C	1111	1101	1111	
7	FPGA C switches off FPGA H	0000	1101	1101	
8	FPGA C switches on S9053_0 H	0000	1100	1100	
9	FPGA C switches on FPGA H	0000	1100	1100	
10	FPGA H switches off S9053_1 C	0100	1100	1100	
11	FPGA H switches off FPGA C	0100	0000	0100	
12	FPGA H switches on S9053_1 H	0000	0000	0000	
13	FPGA H switches on FPGA C	0000	0000	0000	

5 S9011AT test sequence

5.1 Initialization

1. Set slave mask `0x00FFFFFF` to JINF A
2. Set slave mask `0x00FFFFFF` to JINF B

5.2 Reading status

Following sequence is executed for the four combinations FPGA A/B, Half A/B:

1. Read SEL status
2. Read Actelbrother status
3. Read DCDC-L last command
4. Read DCDC-L trip status
5. Read DCDC-H last command
6. Read DCDC-H trip status
7. Read DCDC-L feedback
8. Read DCDC-H feedback
9. Read DCDC-L status
10. Read DCDC-H status

5.3 Actel control

Done with half A only.

1. FPGA A turns off FPGA B
2. FPGA B reads Actelbrother status
3. FPGA A turns on FPGA B
4. FPGA B reads Actelbrother status
5. FPGA B turns off FPGA A
6. FPGA A reads Actelbrother status
7. FPGA B turns on FPGA A
8. FPGA A reads Actelbrother status

5.4 S/K voltages control

Done with half A and FPGA A.

1. Read DCDC-L trip status
2. Read DCDC-L last command
3. Turn off S_0, then K_0
4. Turn off S_1, then K_1
5. Turn off S_2, then K_2
6. Turn off S_3, then K_3
7. Read DCDC-L last command
8. Read data from TDRs:
   (a) Calibrate all TDRs
   (b) Read pedestals of channel 1 of S1, S2 and K (if ped=4095, then ± 2 V is off).
9. Turn on all S/K DCDC
10. Read DCDC-L trip status
11. Read data from TDR (see above)
12. Read DCDC-L last command
13. Turn off all S DCDC
14. Read DCDC-L last command
15. Turn on S, off K DCDC
16. Read DCDC-L trip status
17. Read DCDC-L last command
18. Turn on all S/K DCDC
19. Read DCDC-L trip status
20. Read DCDC-L last command

5.5 120 V control

This sequence is done via half A and FPGA A.

1. Read DCDC-H last command
2. Read TBS ADC 0 addr. 0 (primary LR A) and check value
3. Read TBS ADC 0 addr. 1 (primary LR B) and check value
4. Turn off all S9055

5. Read DCDC-H last command
6. Read TBS ADC 0 addr. 0 (primary LR A) and check value
7. Read TBS ADC 0 addr. 1 (primary LR B) and check value
8. Turn on all S9055 COLD (HOT remain off)
9. Read DCDC-H last command
10. Read TBS ADC 0 addr. 0 (primary LR A) and check value
11. Read TBS ADC 0 addr. 1 (primary LR B) and check value
12. Turn on all S9055 HOT (COLD remain off)
13. Read DCDC-H last command
14. Read TBS ADC 0 addr. 0 (primary LR A) and check value
15. Read TBS ADC 0 addr. 1 (primary LR B) and check value
16. Turn on all S9055 (both HOT and COLD)
17. Read DCDC-H last command
18. Read TBS ADC 0 addr. 0 (primary LR A) and check value
19. Read TBS ADC 0 addr. 1 (primary LR B) and check value

5.6 3.3 V control

Half A.

1. JINF A, via FPGA A, turns off S9053_1
2. Ping JINF B
3. JINF A, via FPGA A, turns on S9053_1
4. Ping JINF B
5. JINF B, via FPGA B, turns off S9053_0
6. Ping JINF A
7. JINF B, via FPGA B, turns on S9053_0
8. Ping JINF A
9. JINF A, via FPGA B, turns off S9053_1 (glitch of S9053_1)
10. Status of JINF B is checked (time after boot)
11. JINF B, via FPGA A, turns off S9053_0 (glitch of S9053_0)
12. Status of JINF A is checked (time after boot)
13. JINF B, via FPGA B, turns off S9053_0 Hot

14. JINF B, via FPGA B, turns on S9053_0 Cold
15. JINF A, via FPGA A, turns off S9053_1 Hot
16. JINF A, via FPGA A, turns on S9053_1 Cold
17. JINF A, via FPGA B, reads the DCDC-H feedback
18. Check status of JINF A (time after boot)
19. Check status of JINF B (time after boot)
20. JINF B, via FPGA B, turns off S9053_0 Cold
21. JINF B, via FPGA B, turns off FPGA A (previous step only takes effect now)
22. JINF B, via FPGA B, turns on S9053_0 Hot
23. JINF B, via FPGA B, turns on FPGA A
24. JINF A, via FPGA A, turns off S9053_1 Cold
25. JINF A, via FPGA A, turns off FPGA B (previous step only takes effect now)
26. JINF A, via FPGA A, turns on S9053_1 Hot
27. JINF A, via FPGA A, turns on FPGA B
28. JINF A, via FPGA B, read the DCDC-H feedback
29. Status of JINF A is checked (time after boot)
30. Status of JINF B is checked (time after boot)
31. Set slave mask `0x00FFFFFF` to JINF A
32. Set slave mask `0x00FFFFFF` to JINF B

5.7 Complete sequence

1. Executed by JINF A
   (a) Read status
   (b) Actel Control
   (c) S/K voltages control
   (d) 120 V control
2. 3.3 V control
3. Executed by JINF B
   (a) Read status
   (b) Actel Control
   (c) S/K voltages control
   (d) 120 V control

6 TBS

6.1 Introduction

The TBS is composed of four linear regulators, each producing either 80 or 60 V. It also produces the guard ring voltages for S- and K- sides. The power distribution is split into two halves (see figure 3):

- **half 0**, corresponding to TDR lines 0 to 5;
- **half 1**, which is related to TDR lines 6 to 11.

12 circuits are used to produce each S-guard ring voltage. Unless the ±6 V supply is switched off, there is no way to switch off the S-guard ring voltage.

The K-guard ring voltage is distributed by each linear regulator, while the local ground K is produced by two circuits, one for each half.

Each half is supplied by two regulators, called "Hot" and "Cold". The way those regulators interact is important:

- By design, Hot and Cold cannot be "on" at the same time (but there are protection diodes in case of failure).
- By default HOT is "on".
- If Hot stops supplying high voltage (whatever the reason is), Cold will do.
- To stop the supply of high voltage, one needs to explicitly send an "off" signal to both regulators.
- It is possible to set a different voltage level for Hot and Cold. It is thus important to apply the same settings to both regulators.

Following table summarizes these rules:

Hot off	Cold off	GRINGK
0	0	From Hot
0	1	From Hot
1	0	From Cold
1	1	0

The linear regulators are indexed from 0 to 3, with following correspondence:

Index	LR
0	Hot 0
1	Hot 1
2	Cold 0
3	Cold 1

6.2 Buses, halves, addresses

"HALF A/B" corresponds to FPGA Hot/Cold, i.e. to bus A/B... The address refers to each TBS board.

Circuit		Bus	Addr. bits S5 to S8, *S9=1*
TBS 5	FPGA Hot	0x0000	2
	FPGA Cold	0x0020	
TBS 15	FPGA Hot	0x0010	7
	FPGA Cold	0x0030	

As S9 is now set to 1, we will have to add 0x80 to the byte containing the register address and write bit.

6.3 LeCroy commands

As we need five bits to address the registers, bits 11 and 12 will be used as the MSBs for the register address. Thus a LeCroy command has following structure:

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
0xA or 0xE				$addr_3$	$addr_2$	$addr_1$	$addr_0$	0	0	reg_4	reg_3	R/W	reg_2	reg_1	reg_0

The next 16 bits are data bits (register content), if the write mode is chosen, or just 0's in the read mode.

6.4 Linear regulators addressing

LR index	LR type
0	Hot A
1	Hot B
2	Cold A
3	Cold B

6.5 Read registers

- Register 0 is the FPGA SEL status.
- Register 1 describes the FPGA last command (bits 0 and 1), and status (bit 4 = status, bit 8 = tripped).
- Register 2:

Bits	Content	Comment
0→3	Last off command	1=off, 0=on
4→7	Last 60 V command	1=60 V, 0=80 V
8	Hot A status	1=not functional
9	Hot B status	1=not functional

- Register 3: feedback register.

Bits	Content	Comment
0→3	off command	1=off
4→7	60 V command	1=60 V, 0=80 V

- Register 6, ADC mode: default mode is 0x000F.

- Registers 16 to 31: get ADC value. A request to read one of those registers triggers a new conversion.

Register	Content
16→19	LR 0→3 volt
20→31	Gring S 0→11 μA

6.6 Read commands

Command name	Syntax	Comment
Read SEL status	`xx80 0000`	Set to 1 at startup, autoclear
Read brother FPGA status	`xx81 0000`	
Read LR stats + last cmd	`xx82 0000`	
Read LR feedback	`xx83 0000`	
Read JINF status	`xx85 0000`	
Read ADC mode	`xx86 0000`	
Read LR 0 volt. (ADC 0, addr 0)	`xxA0 0000`	
⋮	⋮	
Read LR 3 volt. (ADC 0, addr 3)	`xxA3 0000`	
Read GringS 0 curr. (ADC 0, addr 4)	`xxA4 0000`	
⋮	⋮	
Read GringS 3 curr. (ADC 0, addr 7)	`xxA7 0000`	
Read GringS 4 curr. (ADC 1, addr 0)	`xxB0 0000`	
⋮	⋮	
Read GringS 11 curr. (ADC 1, addr 7)	`xxB7 0000`	

6.7 Write registers

- Register 0: see TPSFE.
- Register 1: see TPSFE.
- Register 2: Bias voltage control.

Bits	Control	Comment
0→3	LR 0→3 off	1=off
4→7	LR 0→3 60 V mode	1=60 V, 0=80 V

6.8 Write commands

Command name	Syntax	Comment
Turn off Actelbrother	`xx89 0001`	
Turn on Actelbrother	`xx89 0002`	
Switch off LRs both halves	`xx8A 000F`	
Switch on LRs both halves	`xx8A 0000`	see section 6.1
Set all LRs to 60 V	`xx8A 00F0`	
Switch on LRs Cold	`xx8A 00n3`	i.e. switch off Hot

6.9 TBS test sequence

Sequence done for TBS 5 and 15, via JINF A and FPGA Hot. Then for TBS 5 and 15, via JINF B and FPGA Cold, if not otherwise mentioned.

6.9.1 Reading status

1. Read sel status
2. Read brother FPGA status
3. Read LR status and last command
4. Read LR feedback
5. Read ADC mode
6. Read LR 0, 1, 2, and 3 voltages, and check that COLD are off.
7. Read GringS 0 to 11 currents, and check the values are not 0.

6.9.2 Actel control

1. FPGA Hot turns off FPGA Cold
2. Read SEL register of Cold
3. FPGA Hot turns on FPGA Cold
4. Read SEL register of Cold
5. FPGA Cold turns off FPGA Hot
6. Read SEL register of Hot
7. FPGA Cold turns on FPGA Hot
8. Read SEL register of Hot

6.9.3 80 V control

1. Switch off all LR
2. Read all LR voltages, check they are compatible with 0
3. Switch on LRs
4. Read all LR voltages, check that Hot voltages are compatible with 80 V
5. Set voltages to 60 V
6. Read all LR voltages, check that Hot voltages are compatible with 60 V
7. Set voltages to 80 V
8. Read all LR voltages, check that Hot voltages are compatible with 80 V
9. Switch off LR Hot, i.e. switch on LR Cold

10. Read all LR voltages, check they are compatible with Hot at 0 V and Cold at 80 V
11. Switch 60 V Cold
12. Read all LR voltages, check they are compatible with Hot at 0 V and Cold at 60 V
13. Switch on LR Hot at 80 V, i.e. switch off LR Cold
14. Read all LR voltages, check they are compatible with Hot at 80 V and Cold at 0 V.

7 TPSFE

7.1 Buses, halves, addresses

"HALF A/B" corresponds to FPGA Hot/Cold, i.e. to bus A/B... The address refers to each TPSFE board.

Circuit		Bus	Addr. bits S5 to S8, S9=0
TPSFE 4	FPGA Hot	0x0000	2
	FPGA Cold	0x0020	
TPSFE 6	FPGA Hot	0x0000	3
	FPGA Cold	0x0020	
TPSFE 14	FPGA Hot	0x0010	7
	FPGA Cold	0x0030	
TPSFE 16	FPGA Hot	0x0010	8
	FPGA Cold	0x0030	

7.2 LeCroy commands

As we need four bits to address the registers, bit 12 will be used as the MSB for the register address. Thus a LeCroy command has following structure:

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
0xA or 0xE				$addr_3$	$addr_2$	$addr_1$	$addr_0$	0	0	0	reg_3	R/W	reg_2	reg_1	reg_0

The next 16 bits are data bits (register content), if the write mode is chosen, or just 0's in the read mode.

7.3 Read Registers content structure

- For registers 2, 3, 4 and 5, the structure is the same: bits 0→5 refer to TDR 0→5 (status byte 0), bits 8→13 to TDR 0→ 5 (status byte 1). Following summarizes the status for those registers:

Register	Byte 0	Byte 1
2	LR last cmd S	LR status S
3	LR last cmd K	LR status K
4	LR feedback S	LR feedback K
5	TDR last cmd	TDR status

- Register 6 describes if the automatic shutdown of the LRs (bit 0) and TDRs (bit 1) is on or not. Default is 11 (both on).
- Register 7 counts the number of Actel brother failures (bits 0 to 3). The counter is cleared after reading.
- Registers 8 and 9 , resp. 10 and 11 contain the LR S-side, resp. K-side failure counters:

register	bits	Lin. Reg.
8/10	0→3	0
	4→7	1
	8→11	2
	12→15	3
9/11	0→3	4
	4→7	5

- Registers 13 and 14 contain the TDR 3.3V failure counters:

register	bits	TDR
13	0→3	0
	4→7	1
	8→11	2
	12→15	3
14	0→3	4
	4→7	5

7.4 Write Registers description

Register	Name	Control bits	Comments
0	clear sel	bit 0	
1	Actel ctrl	bits 0,1	
2	LR-S ctrl	bits 0→5	
3	LR-K ctrl	bits 0→5	
4			not used
5	TDR ctrl	bits 0→5	
6			not used
7	LR counters	bits 9 and 10	9=reset, 10=auto-off mode
8	TDR counters	bits 9 and 10	9=reset, 10=auto-off mode

7.5 TDR indexing

See figure 3.

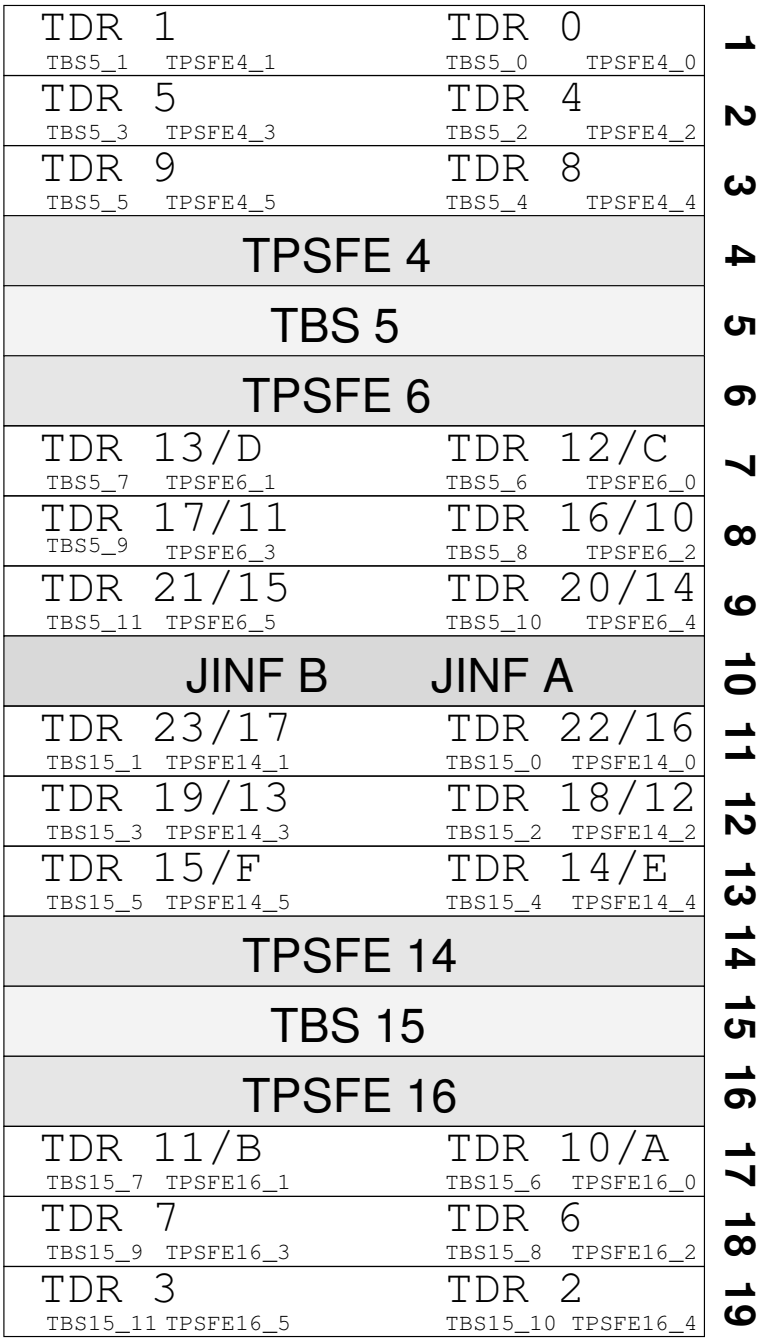

Figure 3: T-crate

7.6 Read commands

Command name	Syntax	Comment
Read SEL status	`xx00 0000`	Set to 1 at startup, autoclear
Read Actelbrother status	`xx01 0000`	Default is 2
Read LR S last cmd / status	`xx02 0000`	
Read LR K last cmd / status	`xx03 0000`	
Read LR feedback	`xx04 0000`	
Read TDR last cmd / status	`xx05 0000`	
Read Actelbrother counter	`xx07 0000`	Autoclear
Read LR-S 0→3 counters	`xx10 0000`	
Read LR-S 4 and 5 counters	`xx11 0000`	
Read LR-K 0→3 counters	`xx12 0000`	
Read LR-K 4 and 5 counters	`xx13 0000`	
Read TDRs 0→3 counters	`xx15 0000`	
Read TDRs 4 and 5 counters	`xx16 0000`	
Read LR/TDR auto-off mode status	`xx06 0000`	

7.7 Write commands

Command name	Syntax	Comment
Turn off Actel brother	`xx09 0001`	
Turn on Actel brother	`xx09 0010`	
Switch on all LR-S	`xx0A 0000`	
Switch off all LR-S	`xx0A 003F`	
Switch on all LR-K	`xx0B 0000`	
Switch off all LR-K	`xx0B 003F`	
Switch on TDRs (3.3 V SSF)	`xx0D 0000`	
Switch off TDRs (3.3 V SSF)	`xx0D 003F`	
Enable LR auto-off mode	`xx0F 0400`	
Disable LR auto-off mode	`xx0F 0000`	
Enable TDR auto-off mode	`xx18 0400`	
Disable TDR auto-off mode	`xx18 0000`	
Reset LR cnt and disable auto-off	`xx0F 0200`	
Reset TDR cnt and disable auto-off	`xx18 0200`	

8 TPSFE Test sequence

The following steps are executed for TPSFE 4, 6, 14 and 16. The commands are executed by JINF A, FPGA Hot, if not specified.

8.1 Read status

1. Read SEL status
2. Read Actelbrother status
3. Read LR-S status and last commands (reg. 2)
4. Read LR-K status and last commands (reg. 3)
5. Read LR feedback (reg. 4)
6. Read TDR status and last commands (reg. 5)
7. Read auto-off mode register (reg. 6)
8. Read Actel trip counters (reg. 7)
9. Read LR-S trip counters (reg. 8 and 9)
10. Read LR-K trip counters (reg. 10 and 11)
11. Read TDRs trip counters (reg. 13 and 14)

8.2 Actel control

1. FPGA Hot, turns off FPGA Cold
2. Read SEL status of FPGA Cold
3. FPGA Hot turns on FPGA Cold
4. Read SEL status of FPGA Cold
5. FPGA Cold turns off FPGA Hot
6. Read SEL status of FPGA Hot
7. FPGA Cold turns on FPGA Hot
8. Read SEL status of FPGA Hot
9. Read trip counter of FPGA Hot (reg. 7)
10. Read trip counter of FPGA Cold (reg. 7)
11. Read trip counter of FPGA Hot (reg. 7) (autoclear test)
12. Read trip counter of FPGA Cold (reg. 7) (autoclear test)
13. FPGA Hot turns off and on FPGA Cold, fourteen times.
14. Read trip counter of FPGA Cold (reg. 7)

15. FPGA Cold turns off and on FPGA Hot, fourteen times.
16. Read trip counter of FPGA Hot (reg. 7)
17. Read trip counter of FPGA Hot (reg. 7) (autoclear test)
18. Read trip counter of FPGA Cold (reg. 7) (autoclear test)

Note: For the short tests, the FPGA are switched off and on only twice instead of 14 times.

8.3 TDR control

1. Switch off all LR S-side
2. Calibrate all TDRs
3. Read peds of TDRs (1st channel of S1, S2 and K) and check the values (for off TDRs should be 4095)
4. Switch on all LR S-side
5. Switch off all LR K-side
6. Calibrate all TDRs
7. Read peds of TDRs (1st channel of S1, S2 and K) and check the values (for off TDRs should be 4095)
8. Switch on all LR K-side
9. Switch off all TDRs 3.3 V SSF
10. Successively ping all TDRs controlled by this TPSFE
11. Switch on all TDRs 3.3 V SSF
12. Successively ping all TDRs controlled by this TPSFE

Note: for the short tests, only the 6 TDRs associated to the TPSFE under test are examined. Only one TDR is pinged.

8.4 Auto-off and reset registers

1. Disable LR auto-off mode
2. Read LR-TDR auto-off status
3. Disable TDR auto-off mode
4. Read LR-TDR auto-off status
5. Reset LR trip counters and disable LR auto-off mode
6. Read LR-S trip counters (reg. 8 and 9)
7. Read LR-K trip counters (reg. 10 and 11)

8. Reset TDR trip counters and disable TDR auto-off mode
9. Read TDRs trip counters (13 and 14)
10. Enable LR auto-off mode
11. Enable TDR auto-off mode
12. Read LR-TDR auto-off status