DAC calibration: FPGA

The FPGA executes the following steps:

1. The FPGA sets the VAs in test mode.
2. The FPGA selects channel 1 of groups S_1, S_2 and K.
3. A calibration pulse is sent to S and K-sides, and the VA output signal is acquired 4 μs later on S, 5 μs on K.
4. Steps 2 and 3 are repeated for channels 2 to 384 (321 to 384 are ignored on S).

Unlike the TDR EM version, in the QM/FM TDRs, the acquisition time (4 μs on S, 5 μs on K) cannot be changed . The choice of those times is based on Eduardo's work presented in July 2003 (TK meeting and TIM). Thus the gain calibration command has only one parameter: the pulse height.

To test the 1024 channels, *80 milliseconds* are needed. This is the time needed to acquire *one event*.

DAC calibration: DSP

The DSP executes the following steps:

1. The DSP asks the FPGA to set the VAs in TEST mode.
2. The DSP takes 2^n dac events.
3. The DSP computes the mean, in making a shift right of n on the sum of the events.

- No pedestal subtraction is executed.
- The data are stored in memory in the S1-S2-K order. They still need to be reorganized.
- As of now, a test on the solid state fuse bits is done: if the +/-2V or +5V (S or K) is not present on the TDR, the calibration is aborted.
- To be under the limit of 2 seconds (and avoid a timeout), 16 events are acquired.

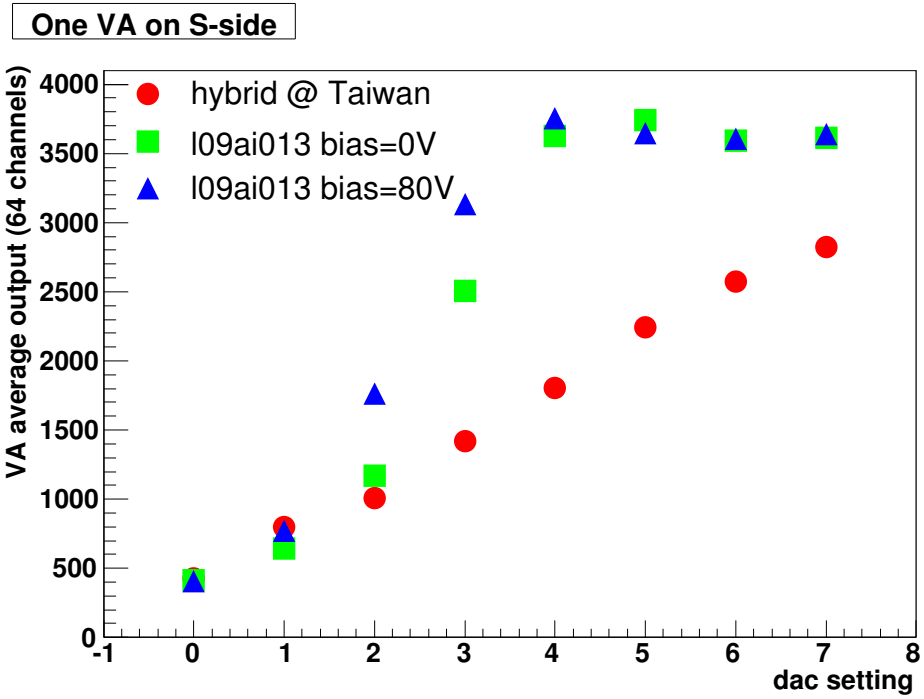
DAC calibration: pulse height

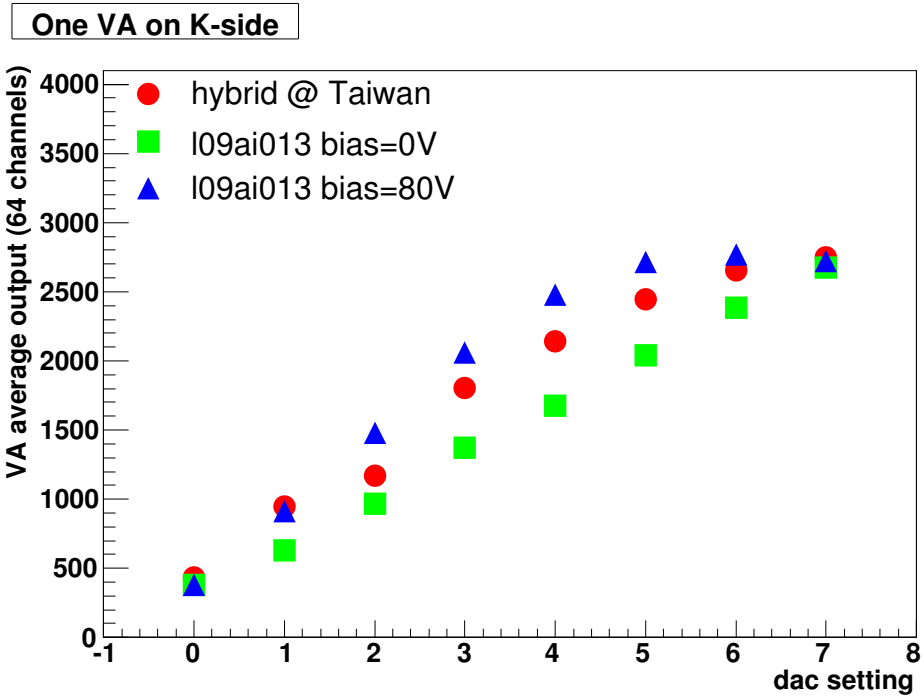
The DAC calibration circuits are different on S and on K. This was based on the assumption that the gain is lower on S than on K. Thus the pulse on S is four times higher than on K:

DAC parameter	S signal (MIP)	K signal (MIP)
1	43	11
2	87	22
3	130	33
4	174	43
5	217	54
6	261	65
7	304	76

DAC calibration: some results

The measurements are right now a bit disconcerting, in particular for the S-side. We clearly miss statistics (tests with ladders and with hybrids alone) regarding the DAC calibration.





Remarks

In the next weeks, we will have to answer the following questions:

- Do we want to subtract pedestals (my guess: no). This operation is right now commented in the code...
- How many events to use for the average ? Using more than 16 means a calibration time larger than 2 seconds, i.e. a timeout for a standard AMSW command.
- Do we want to check the power bits ? (my guess: no).