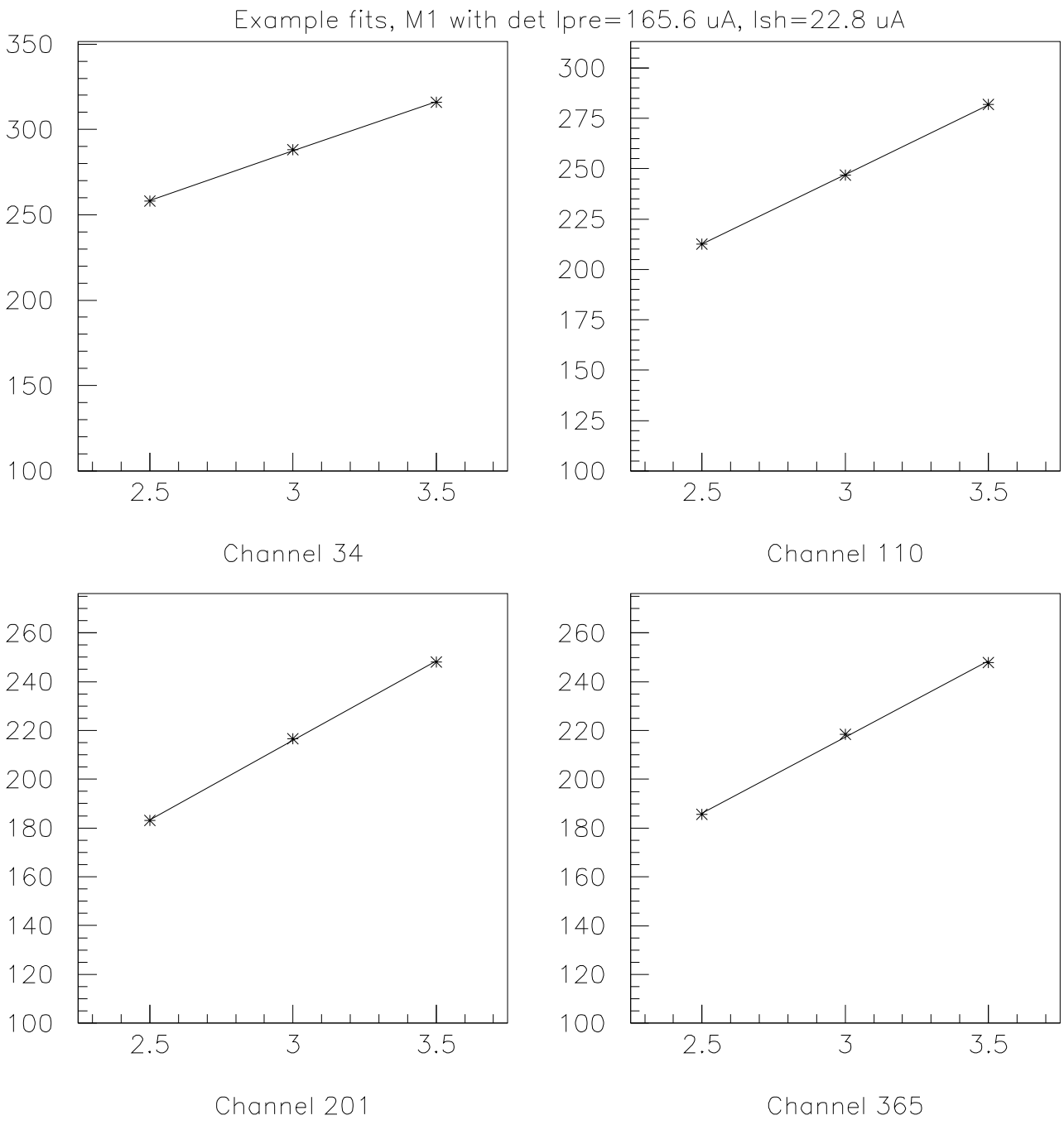
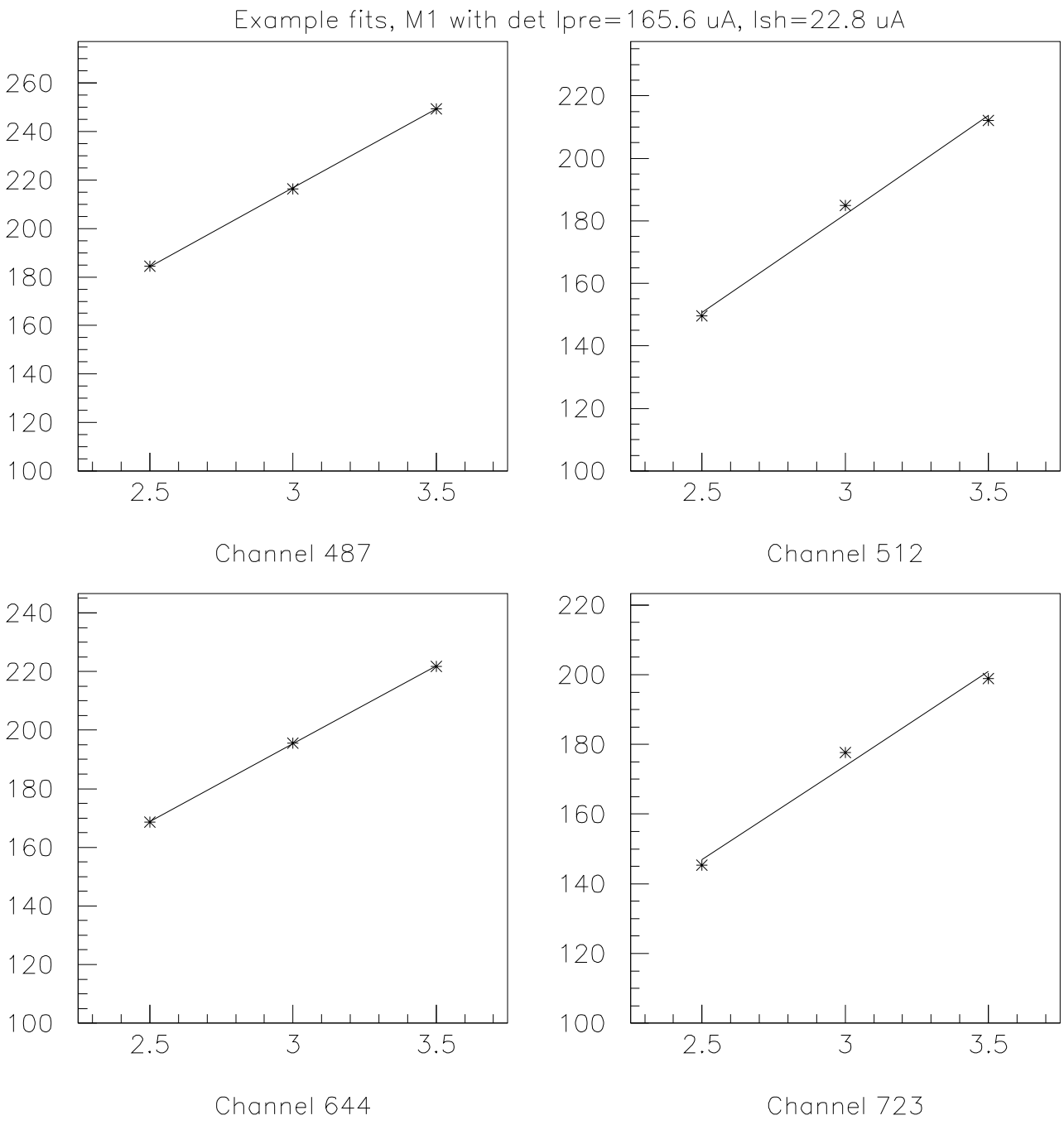
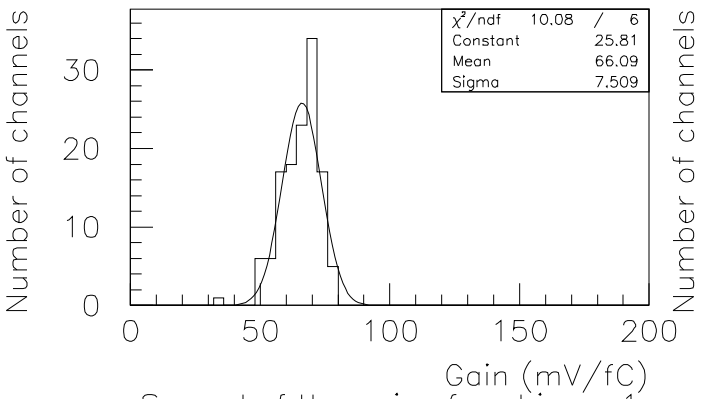
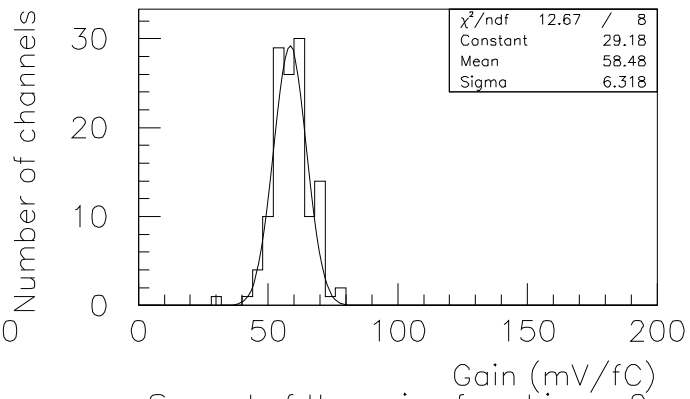

Example fits, M1 with det Ipre=165.6 uA, Ish=22.8 uA
350
300
250
200
150
100
2.5
3
3.5
Channel 34
300
275
250
225
200
175
150
125
100
2.5
3
3.5
Channel 110
260
240
220
200
180
160
140
120
100
2.5
3
3.5
Channel 201
260
240
220
200
180
160
140
120
100
2.5
3
3.5
Channel 365


Example fits, M1 with det Ipre=165.6 uA, Ish=22.8 uA
260
240
220
200
180
160
140
120
100
2.5
3
3.5
Channel 487
220
200
180
160
140
120
100
2.5
3
3.5
Channel 512
240
220
200
180
160
140
120
100
2.5
3
3.5
Channel 644
220
200
180
160
140
120
100
2.5
3
3.5
Channel 723

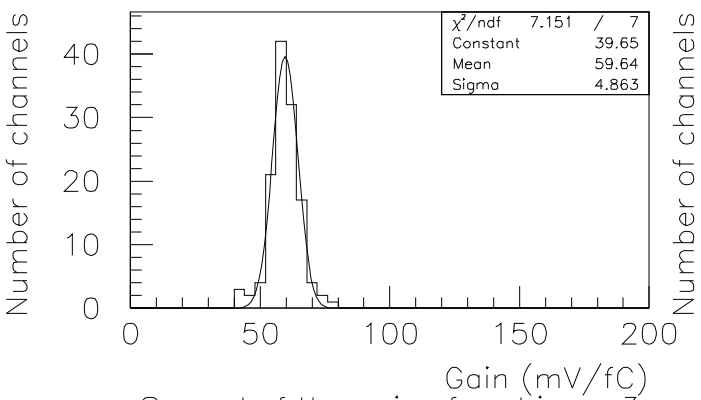
Gains for the 6 chips, M1 with det Ipre=165.6 uA, Ish=22.8 uA



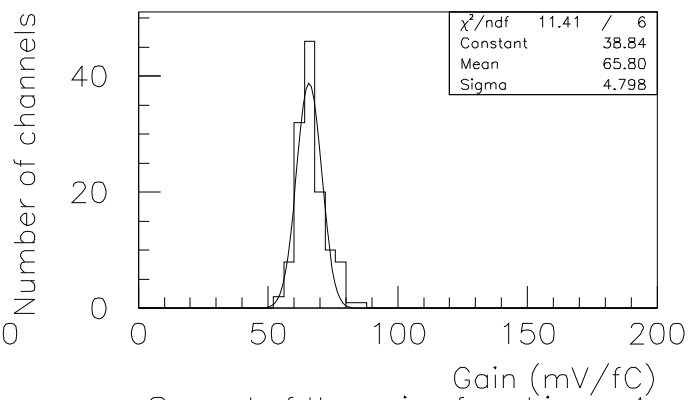
Spread of the gains for chip no.1



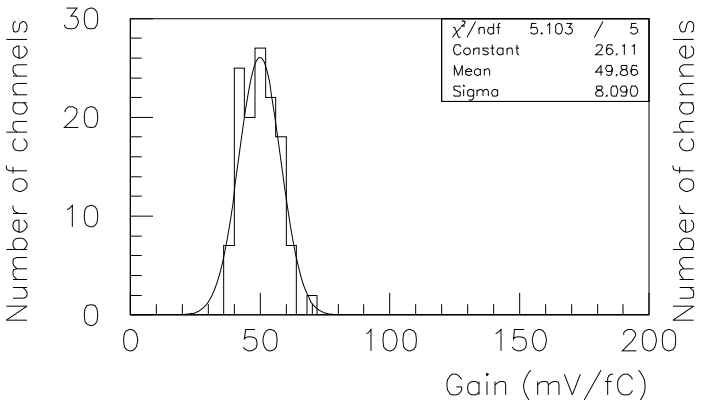
Spread of the gains for chip no.2



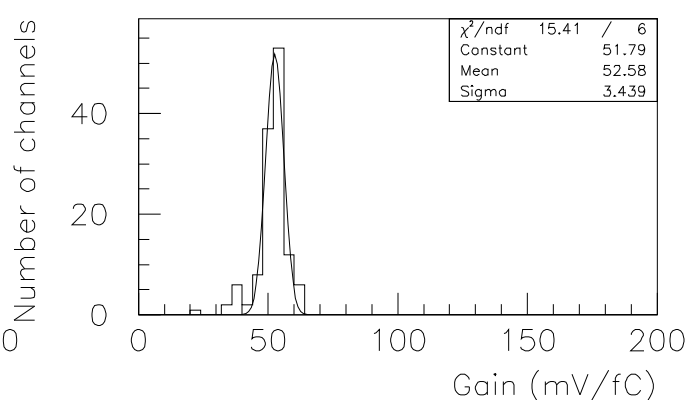
Spread of the gains for chip no.3



Spread of the gains for chip no.4

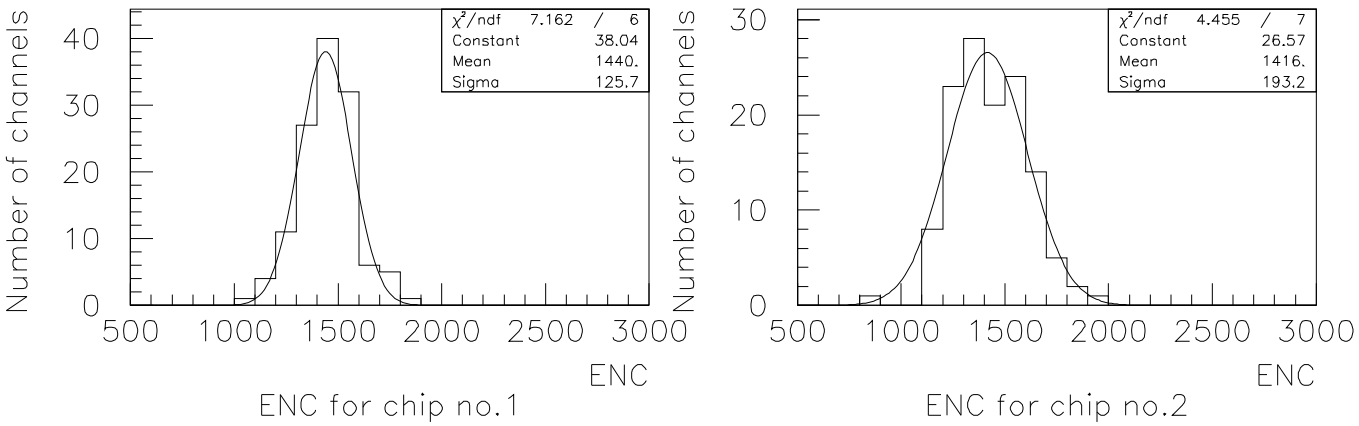


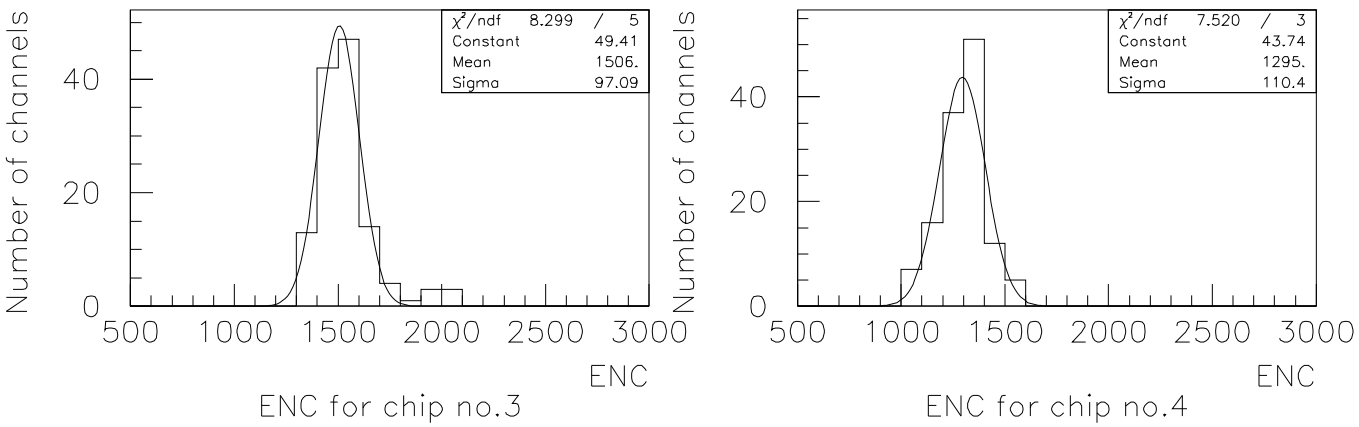
Spread of the gains for chip no.5

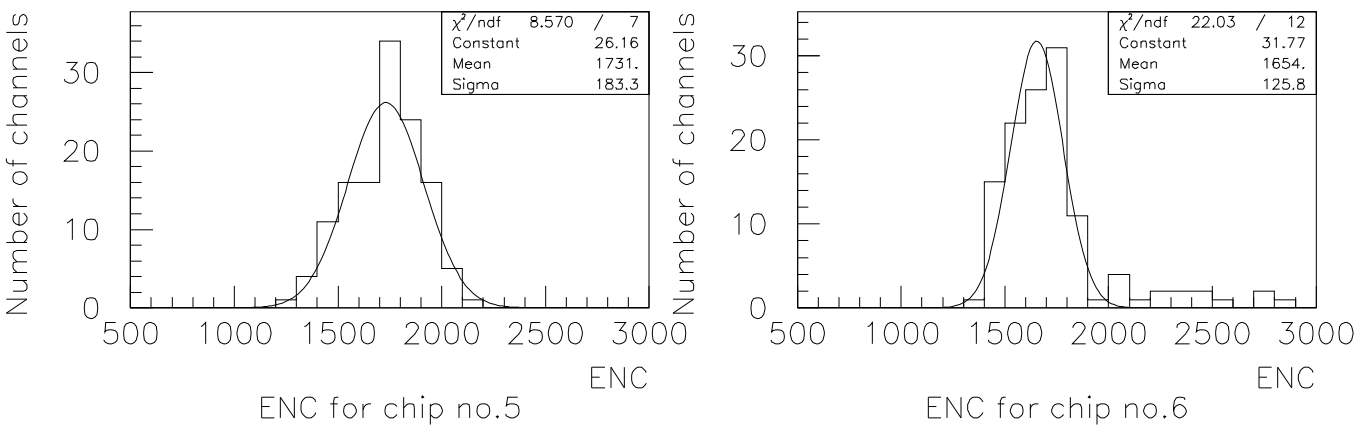


Spread of the gains for chip no.6

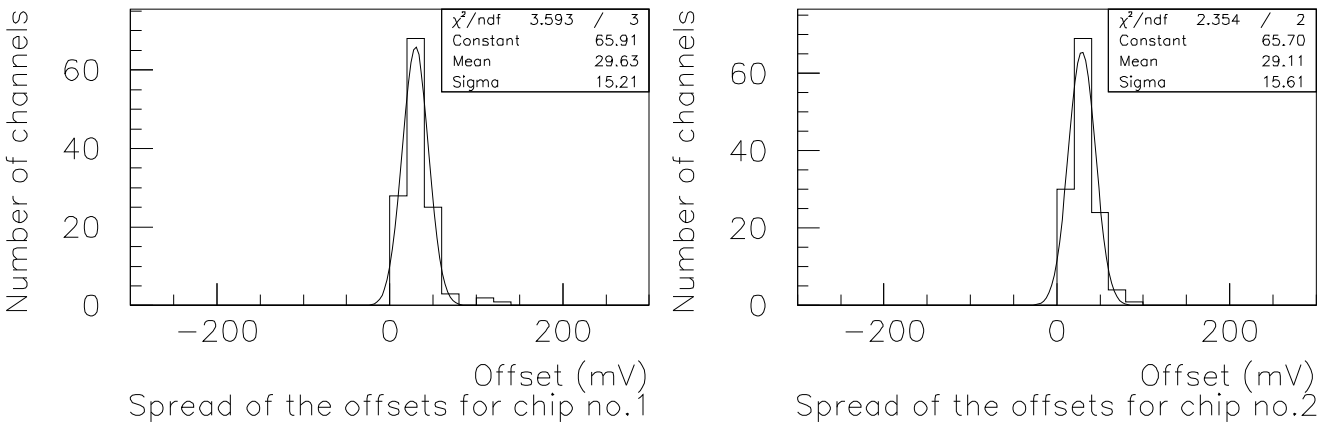
Noises for the 6 chips, M1 with det Ipre=165.6 uA, Ish=22.8 uA





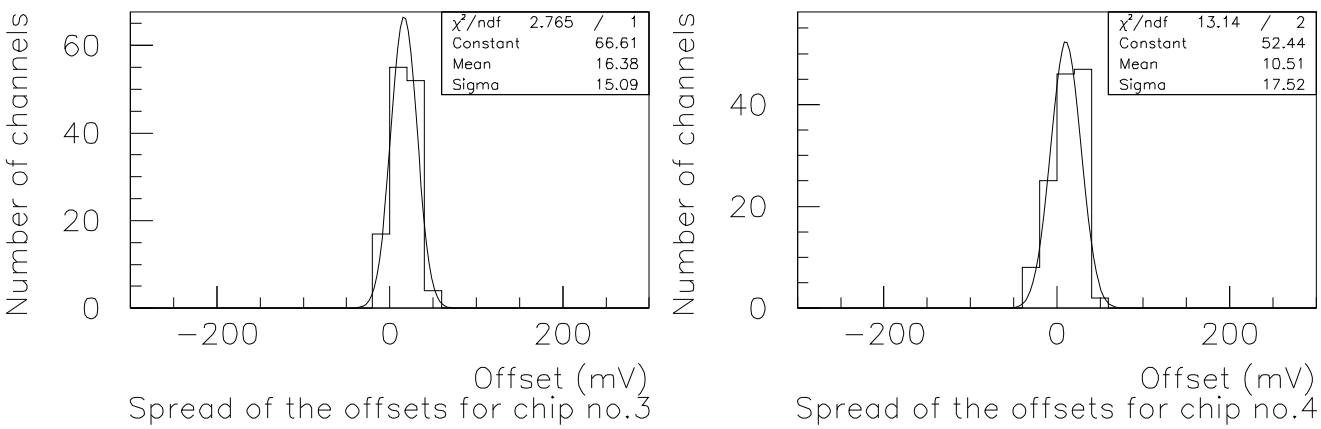


Offsets for the 6 chips, M1 with det Ipre=165.6 uA, Ish=22.8 uA



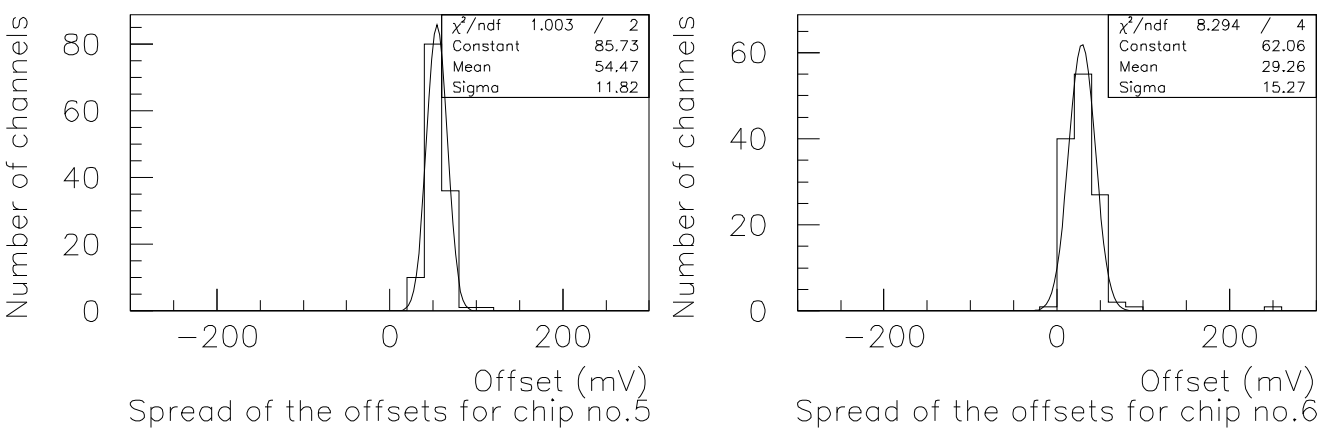
Spread of the offsets for chip no.1

Spread of the offsets for chip no.2



Spread of the offsets for chip no.3

Spread of the offsets for chip no.4



Spread of the offsets for chip no.5

Spread of the offsets for chip no.6