

Module 7

Report on the last investigation made

November 1, 2010

Investigation made at CERN and at UniGe.
Thanks to Nobu for some investigation and inspection,

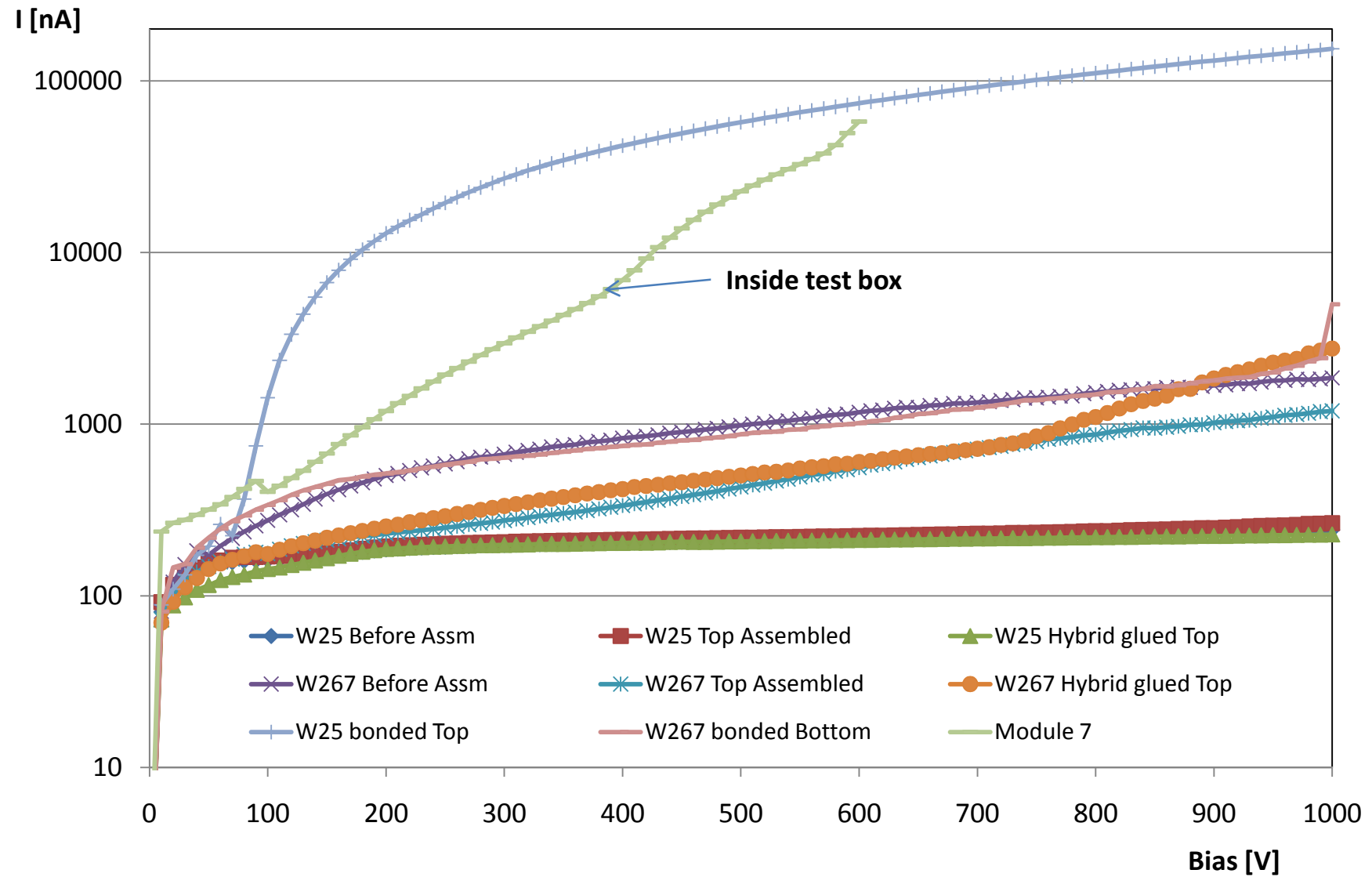
Module 7 status as of 29 October 2010

Step	Date	Comments
Assembly completion	13.10	IV was OK before bonding No IV made just right after bonding
1 st tests at CERN	14.10	IV trip on ISEG around 250V – Dry air ON Identified that it was due to top side
Module back at UNI	15.10	Module mounted on Storage/bonding jig for investigation. Nothing seen! IV done with Keithley by probing side by side and 150A at 1000V. Module mounted back into test box and tested in IV with Keithley but got destroyed. With another Keithley I still could ramp-up the module but did not exceed 400V!
Module back at CERN 1 st readout at CERN	18.10	IV tripped at 250V → test done at 200V 1 st results presented by Sergio where top side was noisier . All hybrids could be readout
Module back at Uni for investigation	19.10	R11 (1 k Ω) resistors were found broken on all 4 hybrids. Bypass all the 4 resistors. Tested with Keithley and OK but did not go higher than 500V
Module back at CERN	20.10	Still problem with ISEG since HV tripped were seen
Module back at Uni	21.10	Decided to replace the resistors and the decoupling capacitors. New capacitors ordered on 22.10

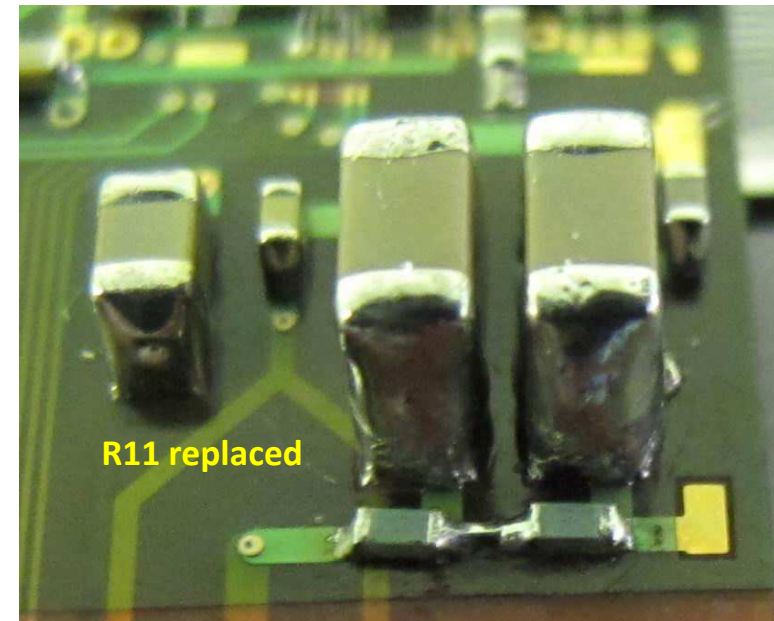
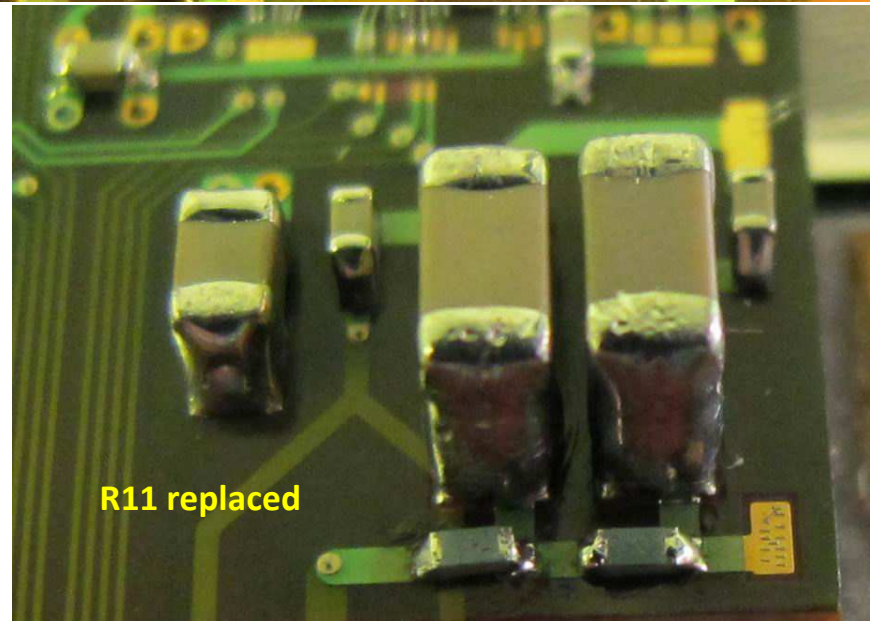
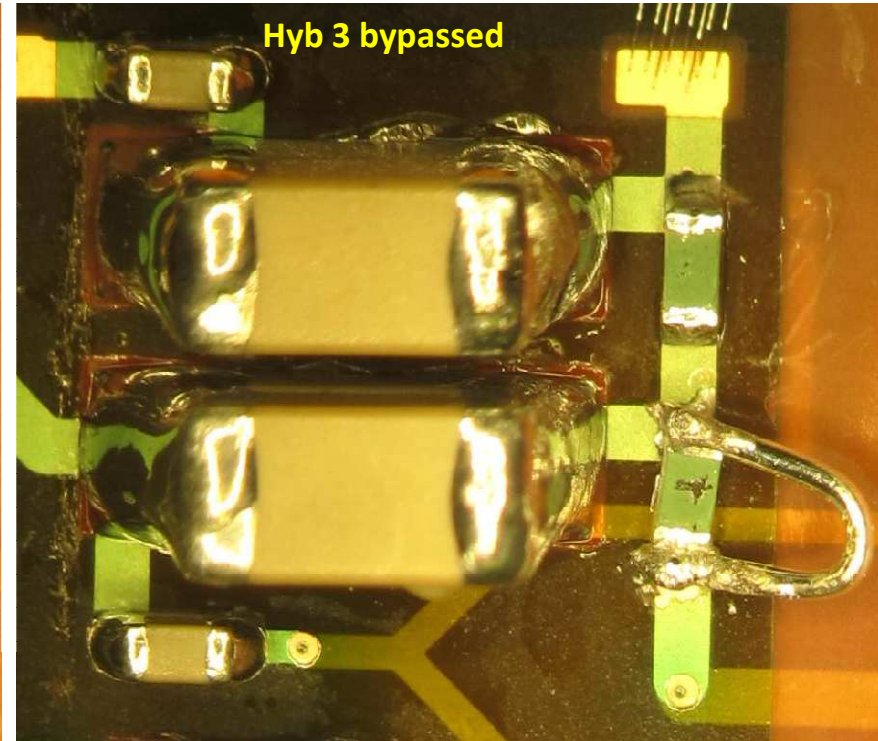
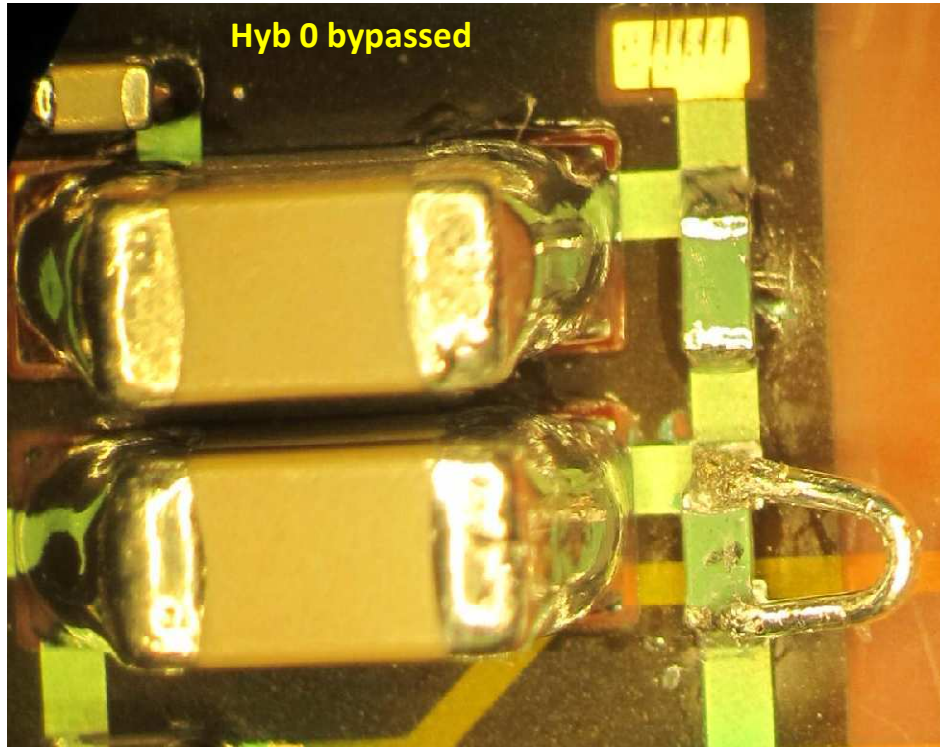
Module 7 status as of 29 October 2010 – Con't

Step	Date	Comments
SMD HV replacement	26.10	All resistors and capacitors are now replaced. IV done with Keithley up to 600V after 2h stabilization at 500V.
Module back at CERN for test	27.10	Still HV trips seen ~ 200V with the ISEG. A Keithley has been transported at CERN such that characterization can be done at more than 200V!
CERN investigation	28.10	Tried to do readout tests but observed that as soon as the Chips are biased 10 microA more is seen on the HV line: 4 μ A when chips OFF and 14 μ A when chips are ON → 20 M Ω resistor more is added. Hybrid 0 could not be configured properly: Pipeline test shows problem on col0 and col1. Other 3 hybrids are OK.
Readout tests	29.10	Readout test of the 3 hybrids: H1, H2 and H3. All are OK and noise is ~ or below 600 e- as expected Nobu inspected in detail and under the microscope the module, sensors, chips, the SMD components, the Samtec connectors and could not find anything wrong. Nobu and Didier investigated the current problem via the HV and the chip power supply. It is connected to the 2.5V on hybrid and not even to the ground.

IV of Module 7 at various assembly/test steps



Pictures of broken R11 and replacement

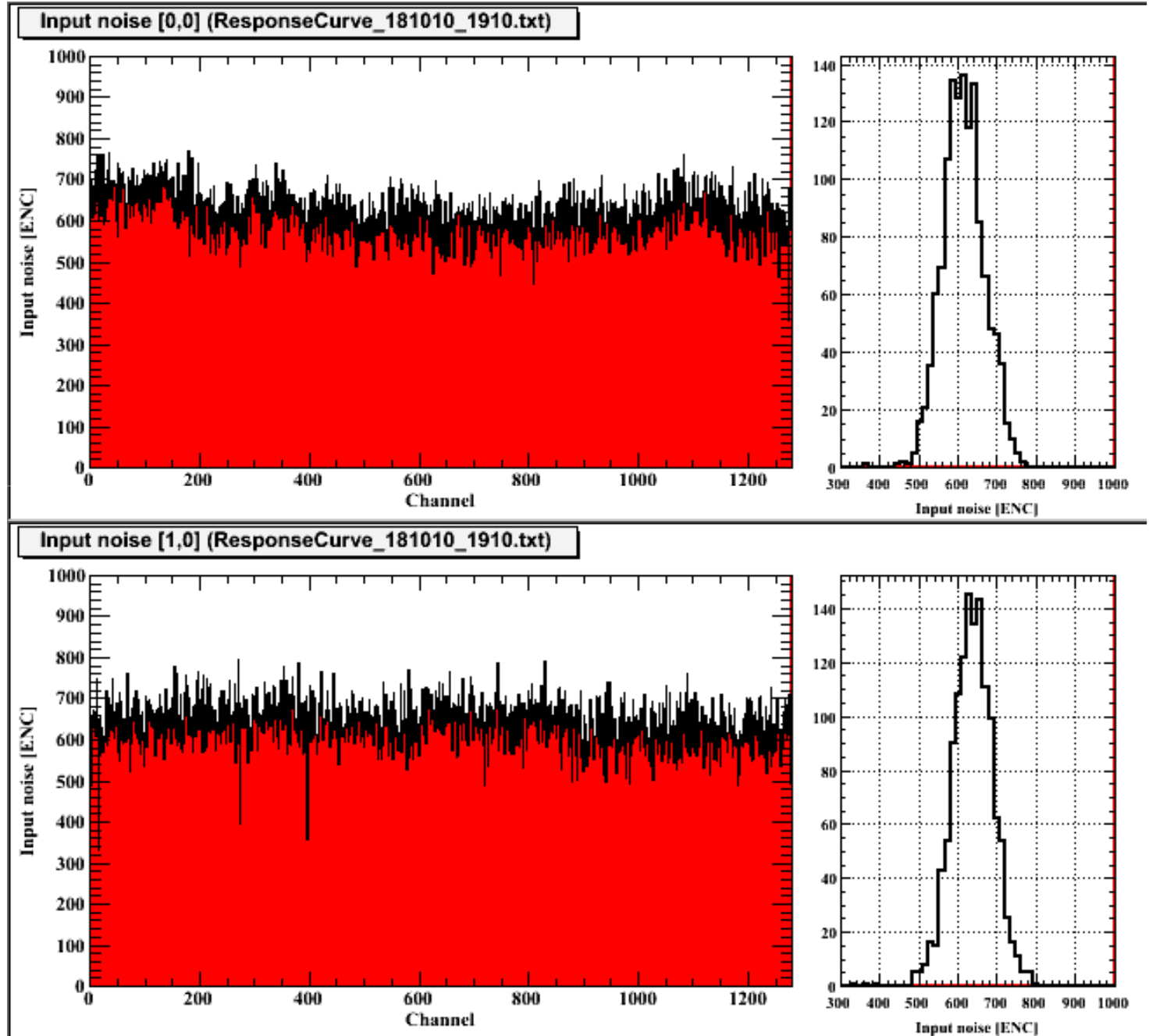


Noise – Test made on October 18th - Con't

200V bias on ISEG

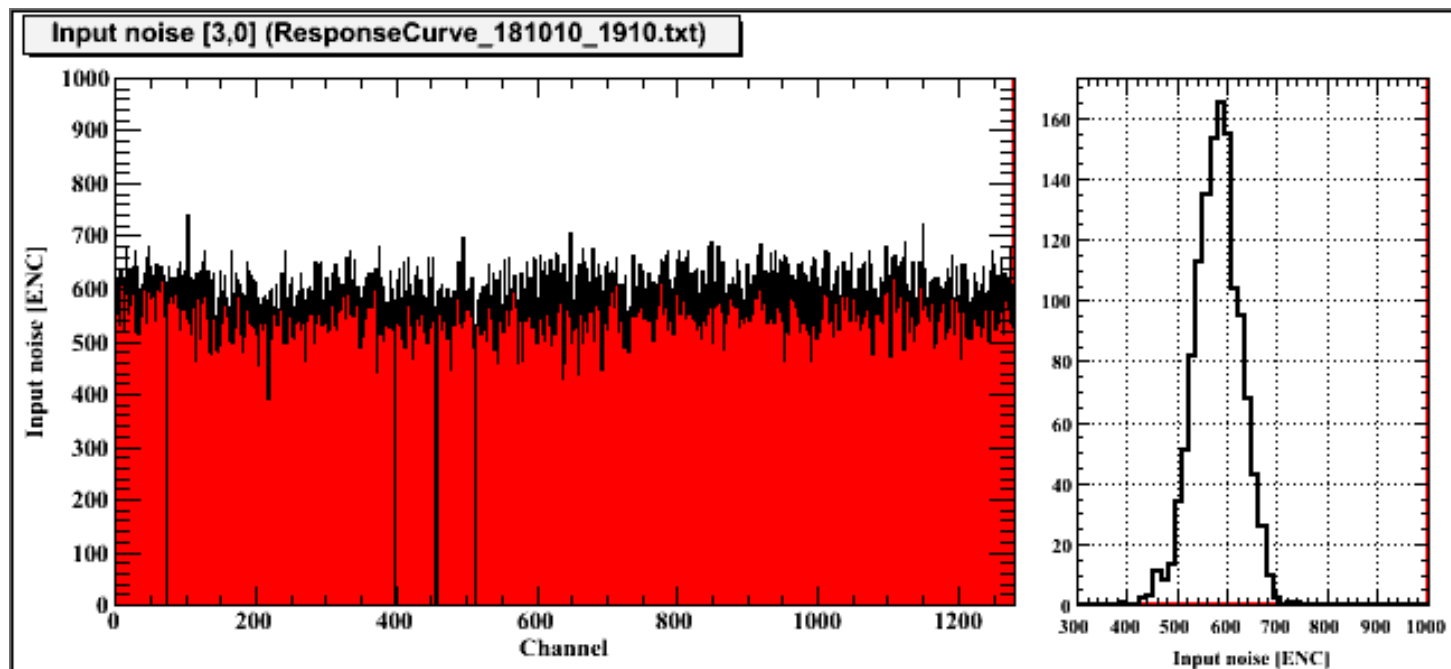
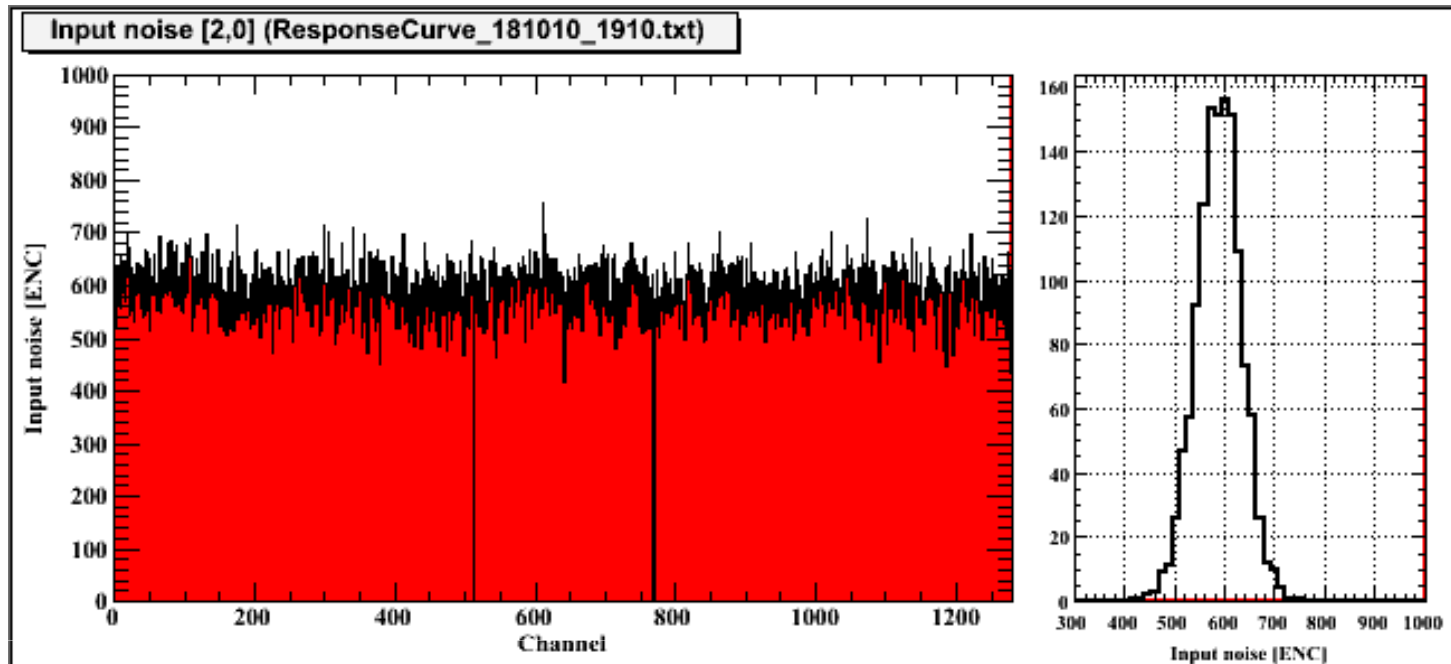
But

it is suspected that due to
broken resistors the
effective bias was ~100V



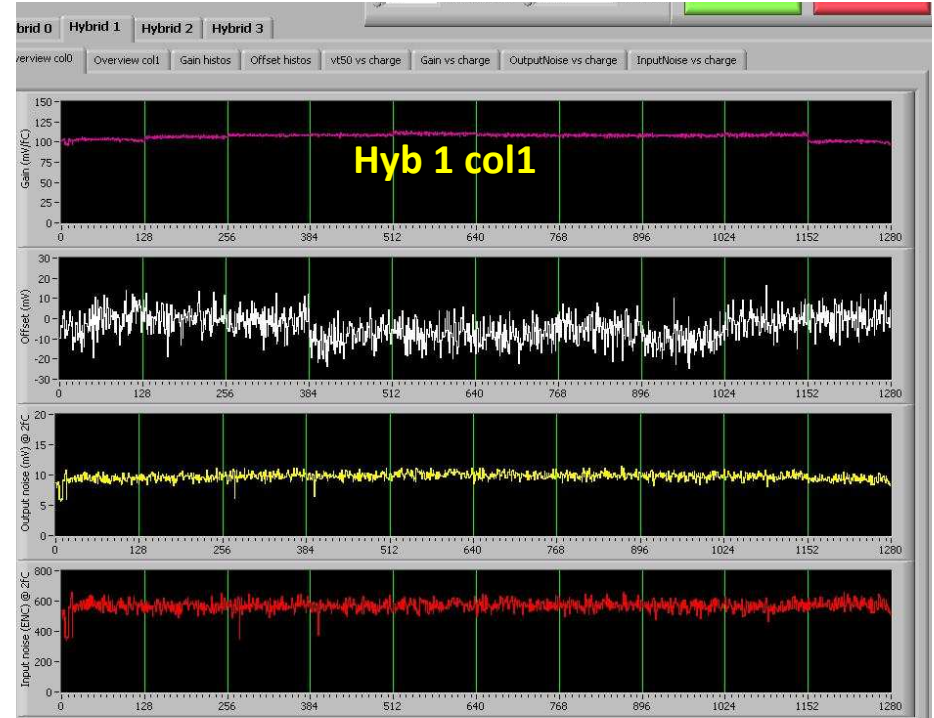
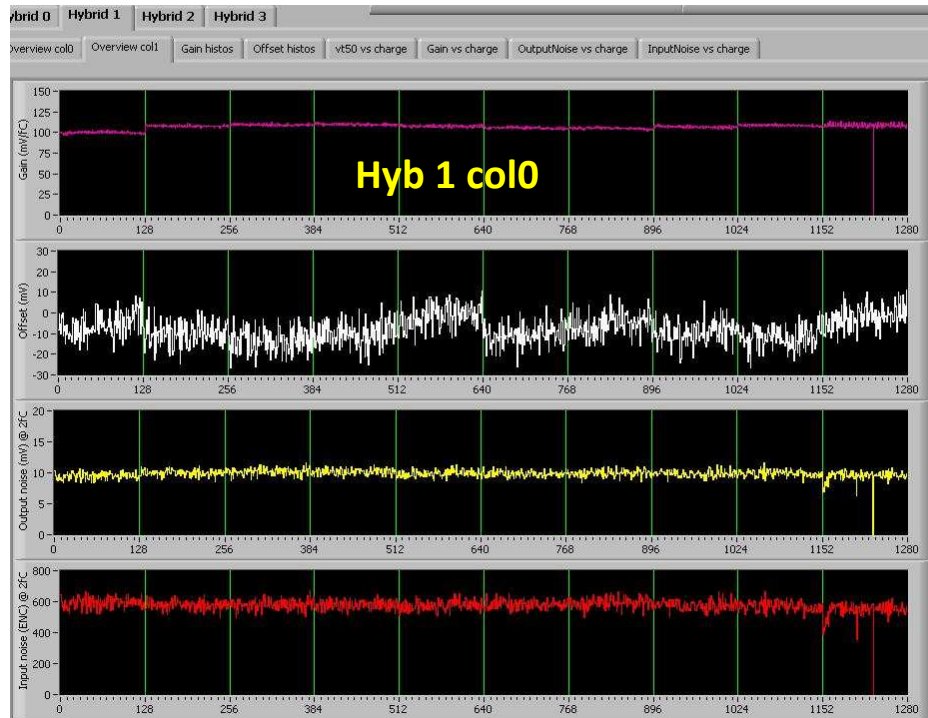
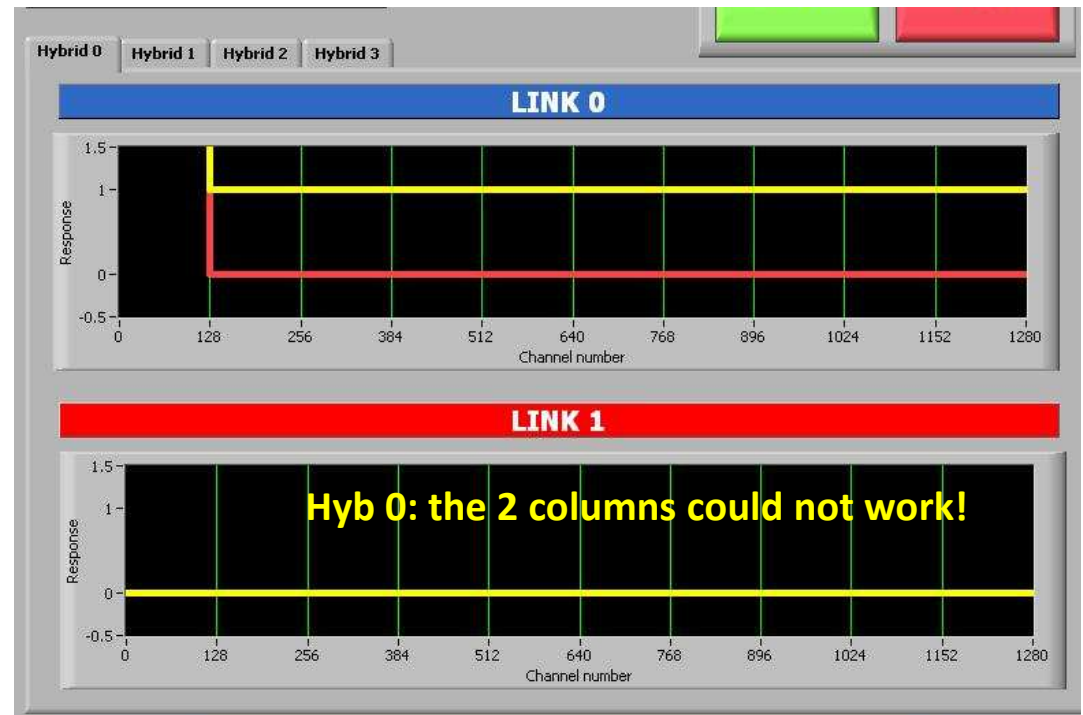
Noise – Test made on October 18th

200V bias

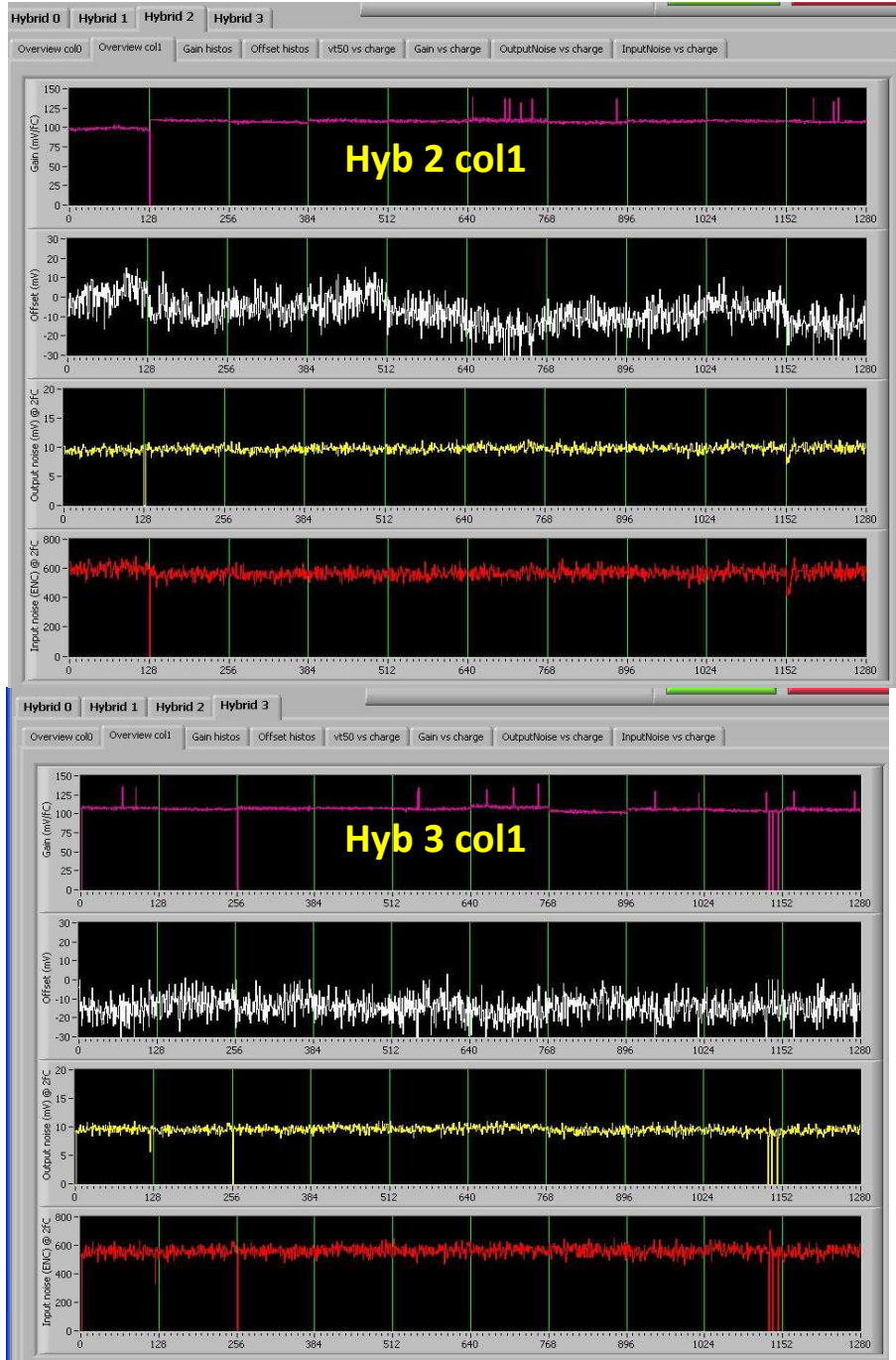
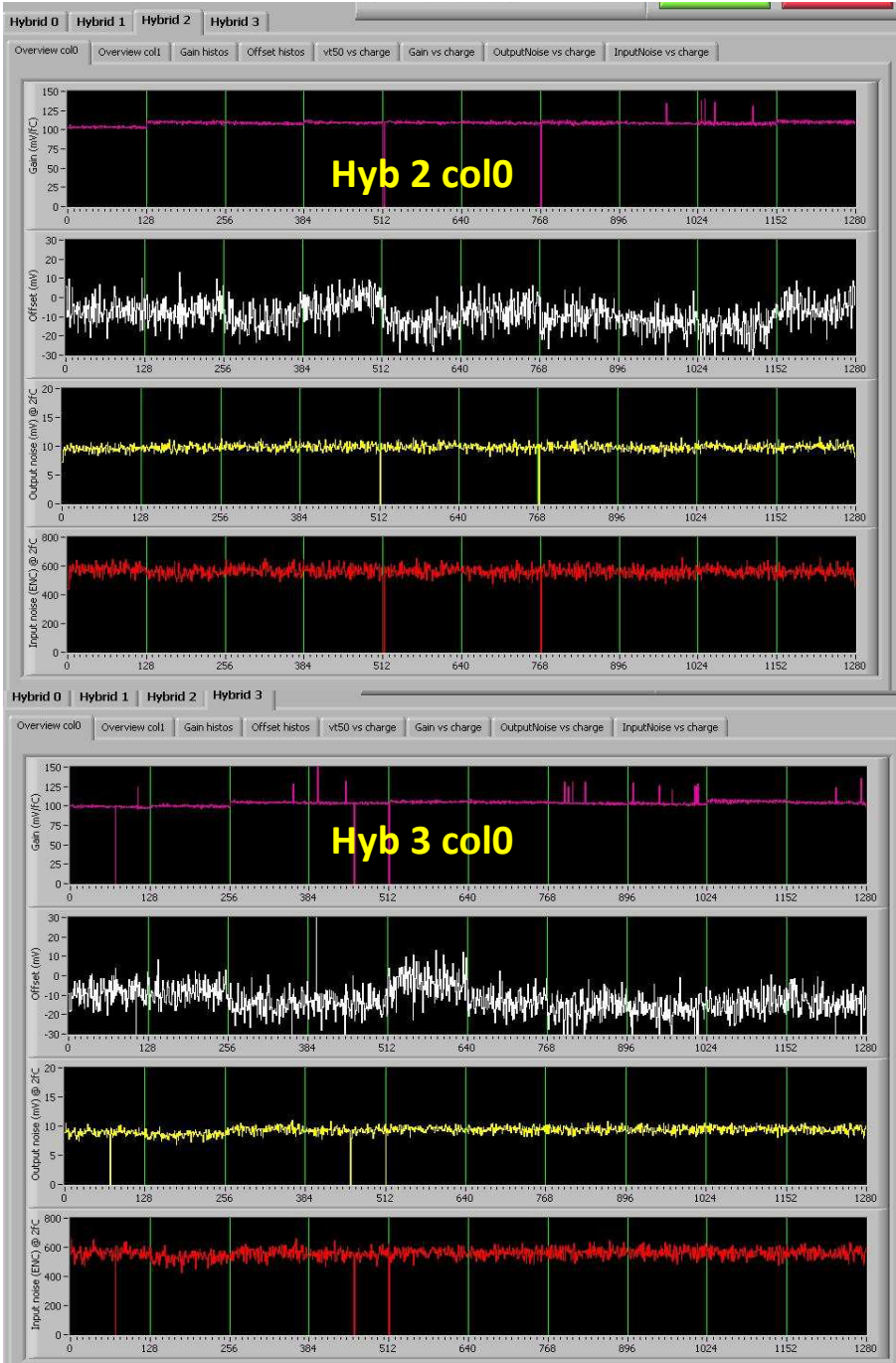


Noise – Test made on October 29th

Top side



Noise – Test made on October 29th



Summary of the understanding so far

- Module 7 always tripped with ISEG power supply around 200V or below
 - Module 7 is OK with Keithley power supply (no visible current spike) BUT when Vdd is ON and HV set at 200V there is 100 microA current that is added.
- After investigation with Nobu one understood that there is a resistor of $\sim 20\text{M}\Omega$ between the HV line and Vdd of hybrid 0
- When measuring with the multimeter the resistance between Vdd and HV it is found $\sim 28\text{M}\Omega$ on all hybrids. Problem not seen when hybrid 0 pigtail is disconnected.
- There is one possible place on the hybrid where Vdd could be connected to the HV. It could be below the HV traces/via of the top 2 layers to the deeper layers. It is not direct since it could be coupled 1st to AGND and then in the last layer to Vcc. But measuring the interconnection between Vcc and Vdd there is $\sim 1\text{M}\Omega$ connection may be through the ABCN chips.
- **In conclusion:** Module 7 is still performing correctly with 3 hybrids namely H1, H2 and H3. But if using ISEG HV power supply one may need to decouple the GND and the VDD of this hybrid 0 to the others.