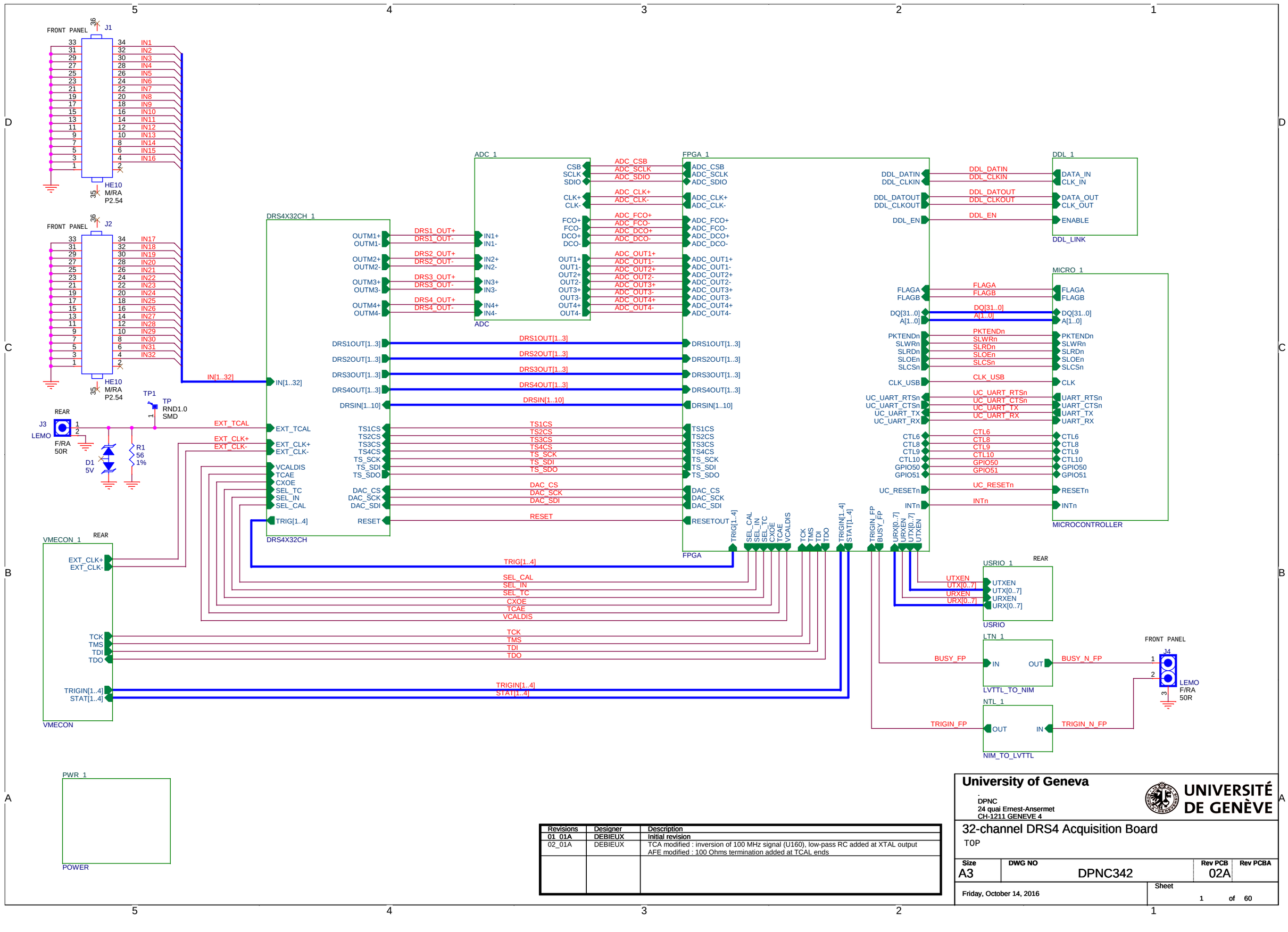


Revisions	Designer	Description
01_01A	DEBIEUX	Initial revision
02_01A	DEBIEUX	TCA modified : inversion of 100 MHz signal (U160), low-pass RC added at XTAL output AFE modified : 100 Ohms termination added at TCAL ends

University of Geneva

.
DPNC
24 quai Ernest-Ansermet
CH-1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

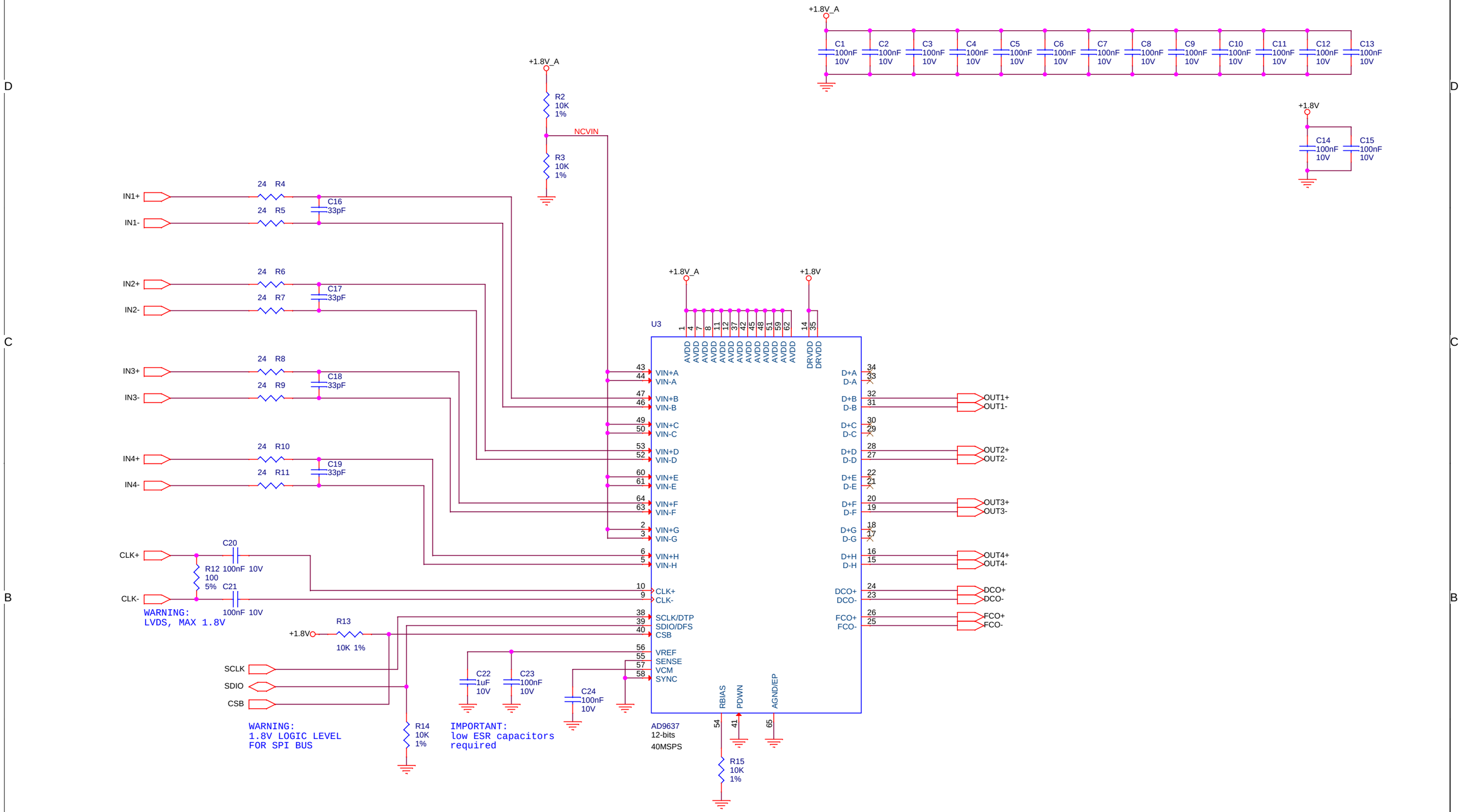
32-channel DRS4 Acquisition Board

TOP

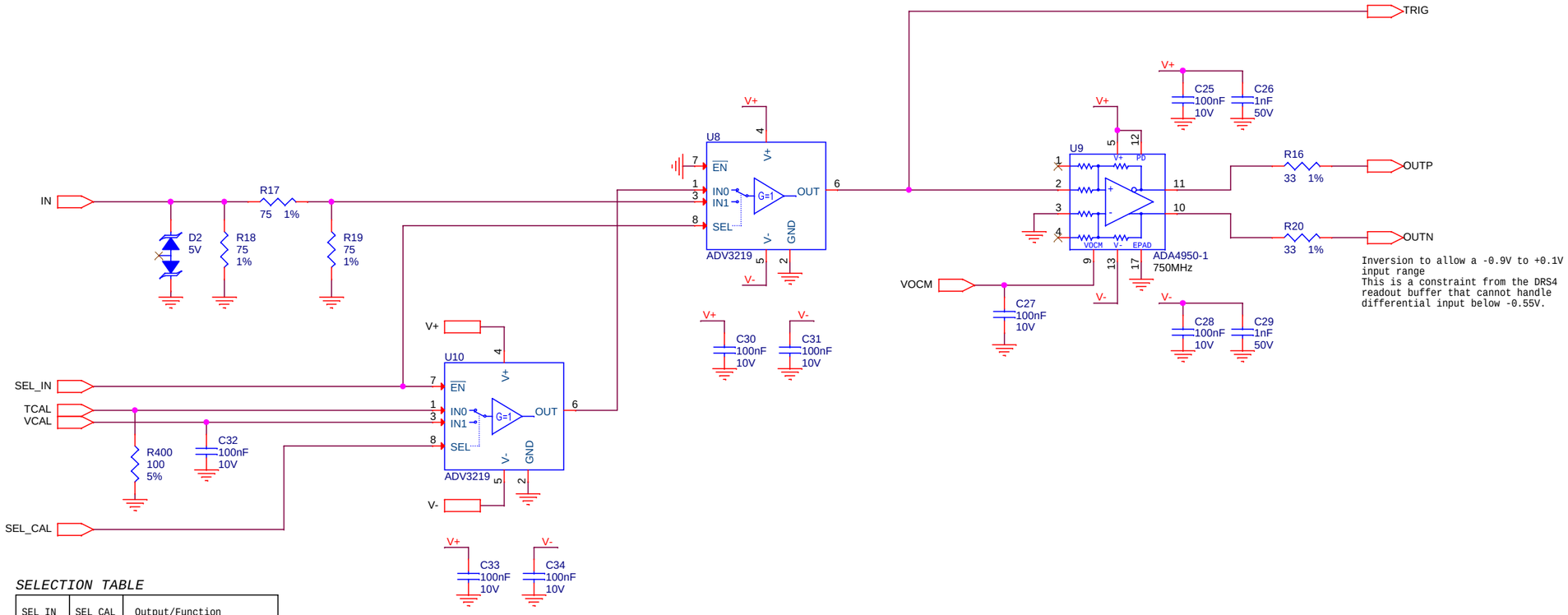
Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Friday, October 14, 2016

Sheet 1 of 60



University of Geneva	UNIVERSITÉ DE GENÈVE
. DPNC 24 quai Ernest-Ansermet CH1211 GENEVE 4	
32-channel DRS4 Acquisition Board	
ADC	Schematic Path = /ADC_1
Size A3 / **DWG NO** DPNC342 / **Rev PCB** 02A / **Rev PCBA**	
Thursday, September 29, 2016	**Sheet** 2 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

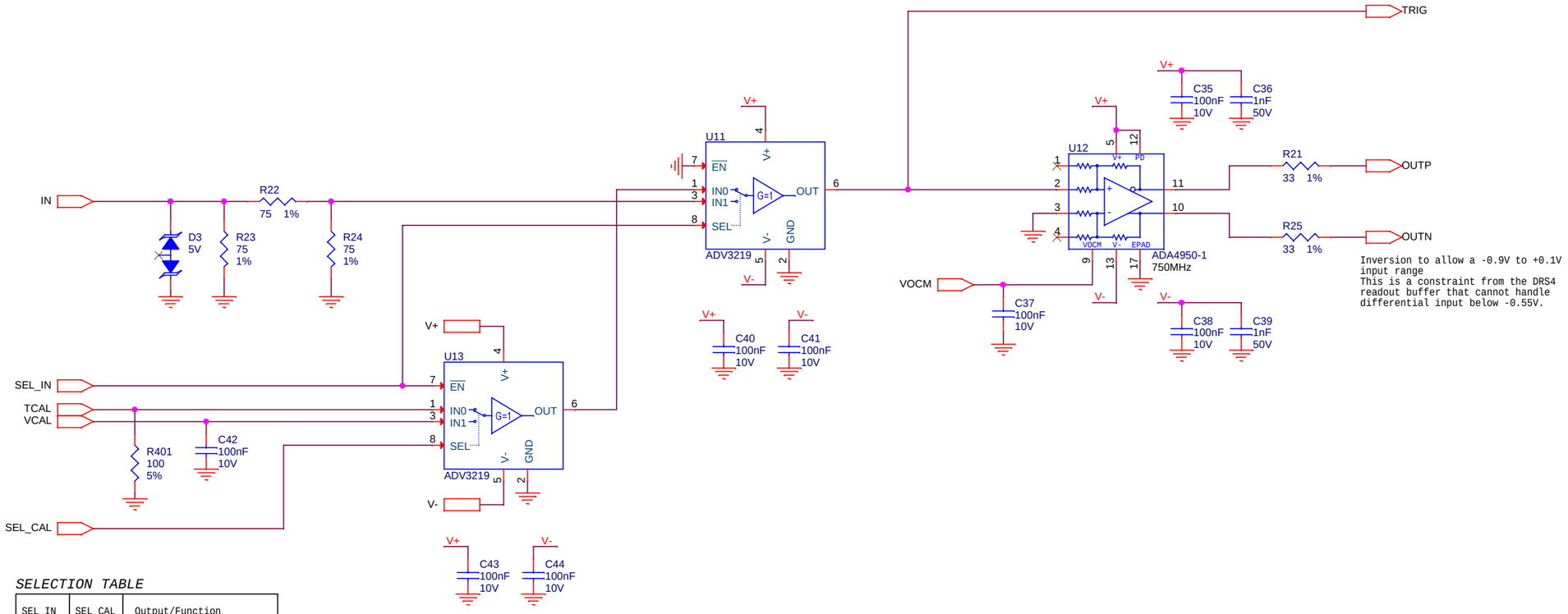
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_1/AFE_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 3 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

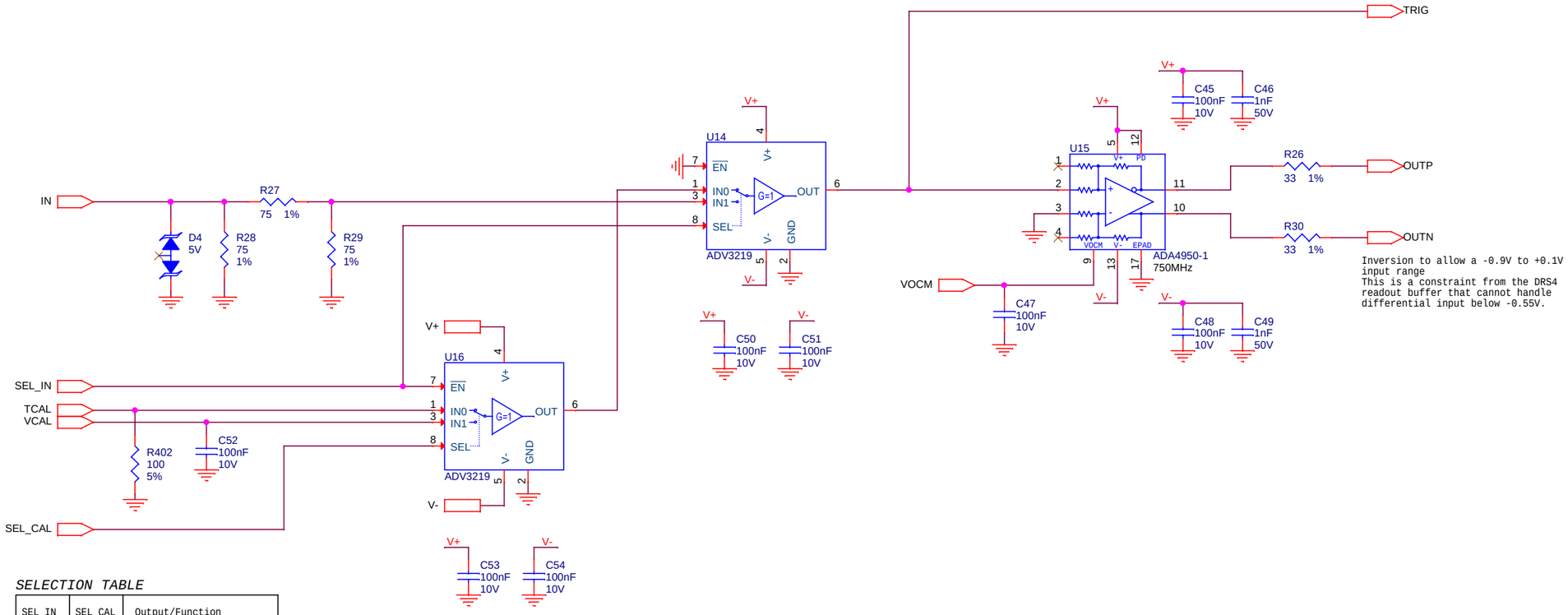
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_1/AFE_2

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 4 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

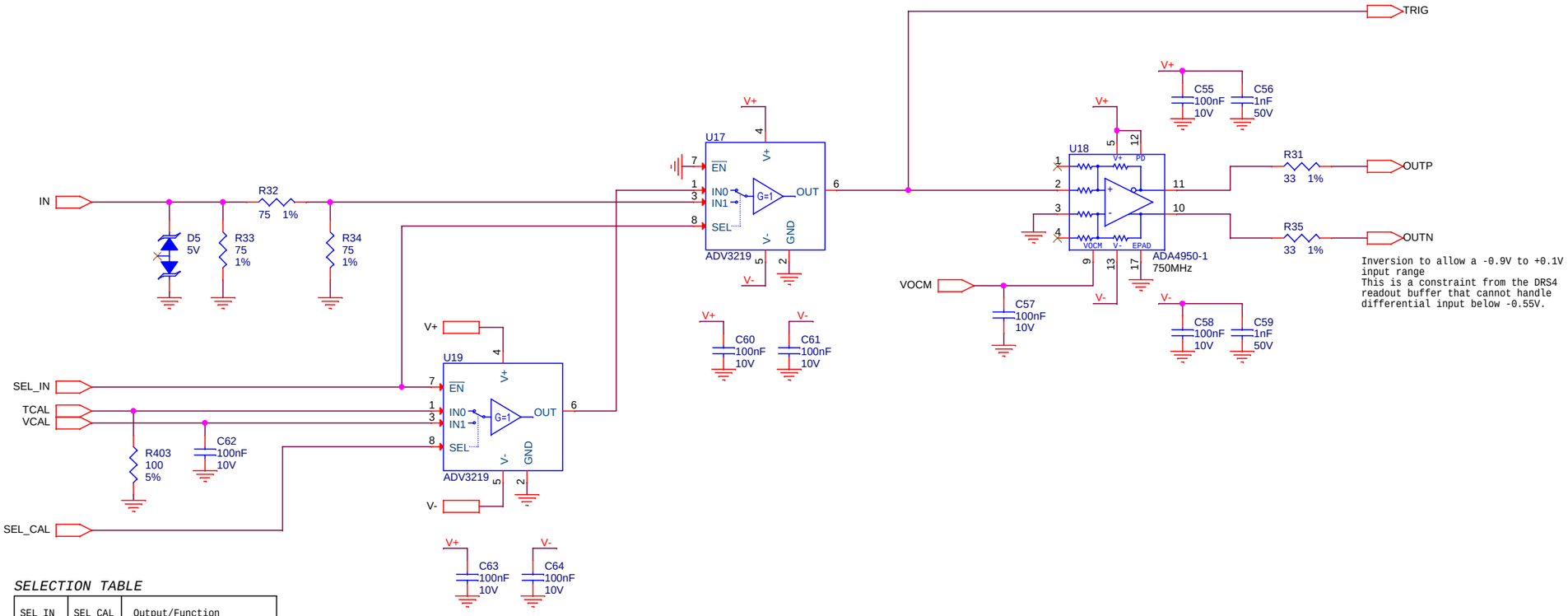
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_1/AFE_3

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 5 of 60



Inversion to allow a -0.9V to +0.1V input range
This is a constraint from the DRS4 readout buffer that cannot handle differential input below -0.55V.

SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

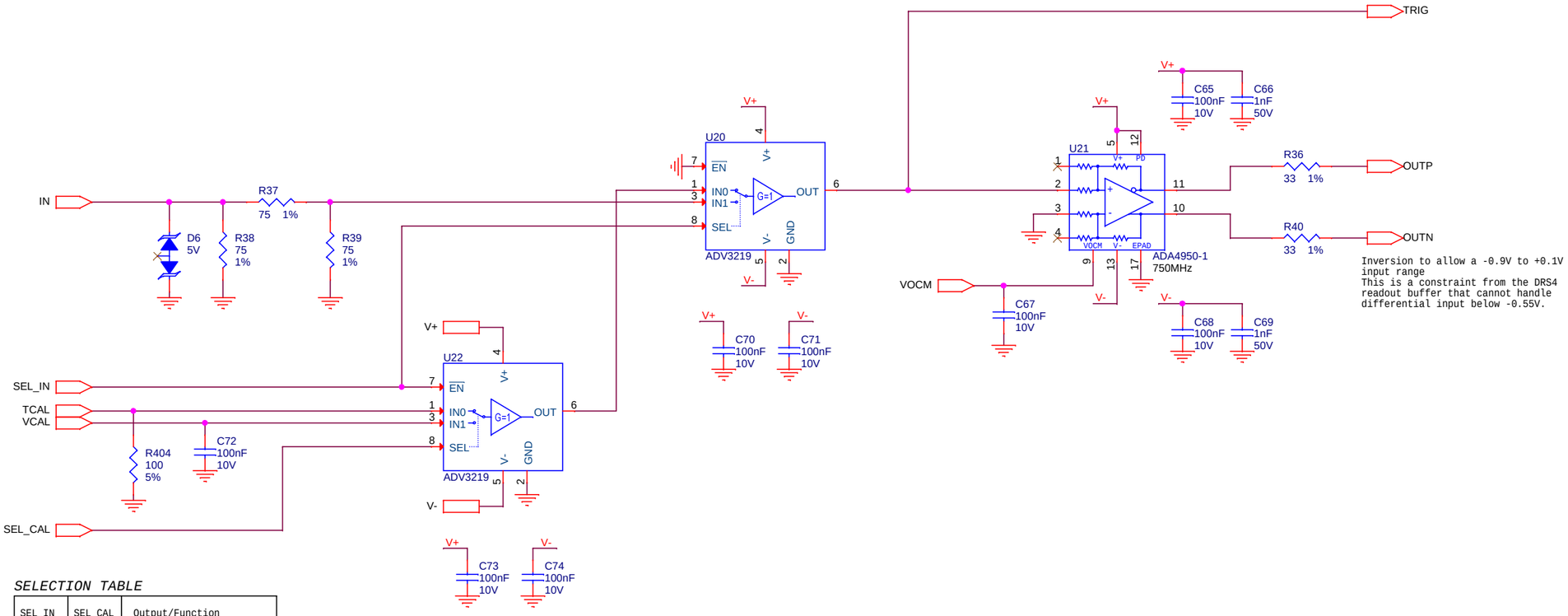
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_1/AFE_4

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 6 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

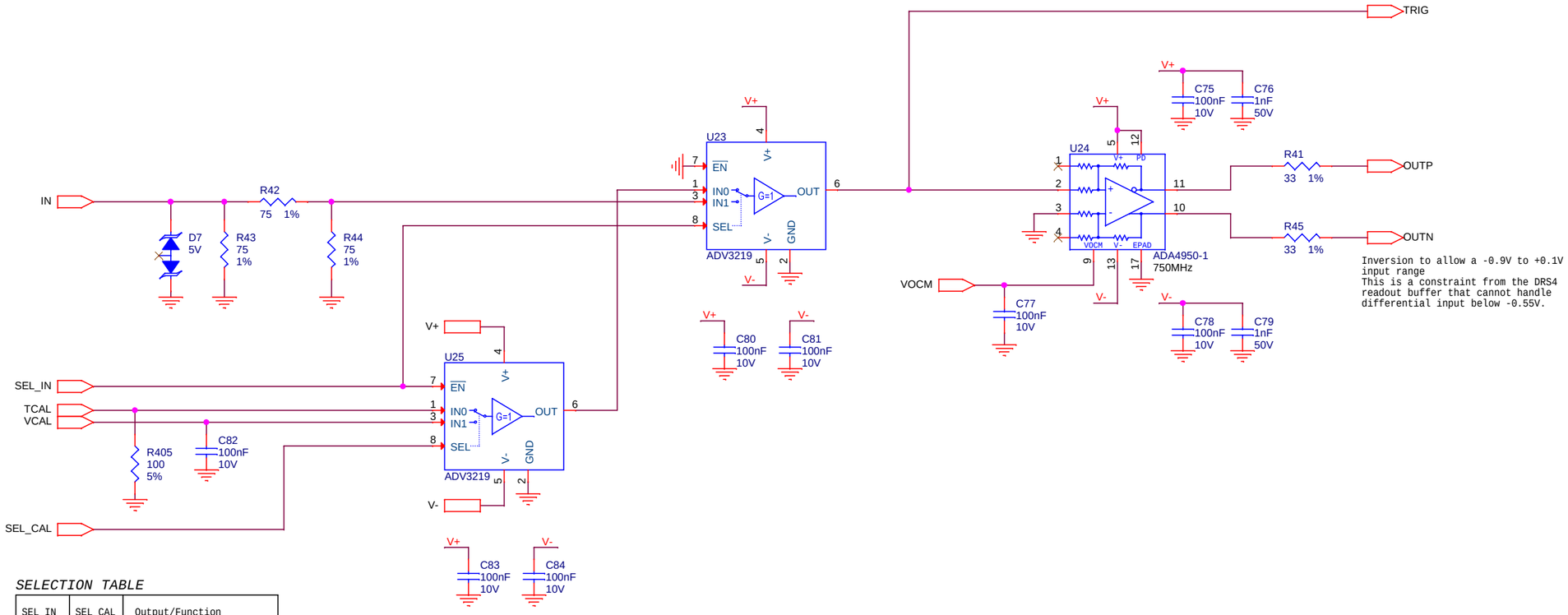
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_1/AFE_5

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 7 of 60



Inversion to allow a -0.9V to +0.1V input range
This is a constraint from the DRS4 readout buffer that cannot handle differential input below -0.55V.

SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

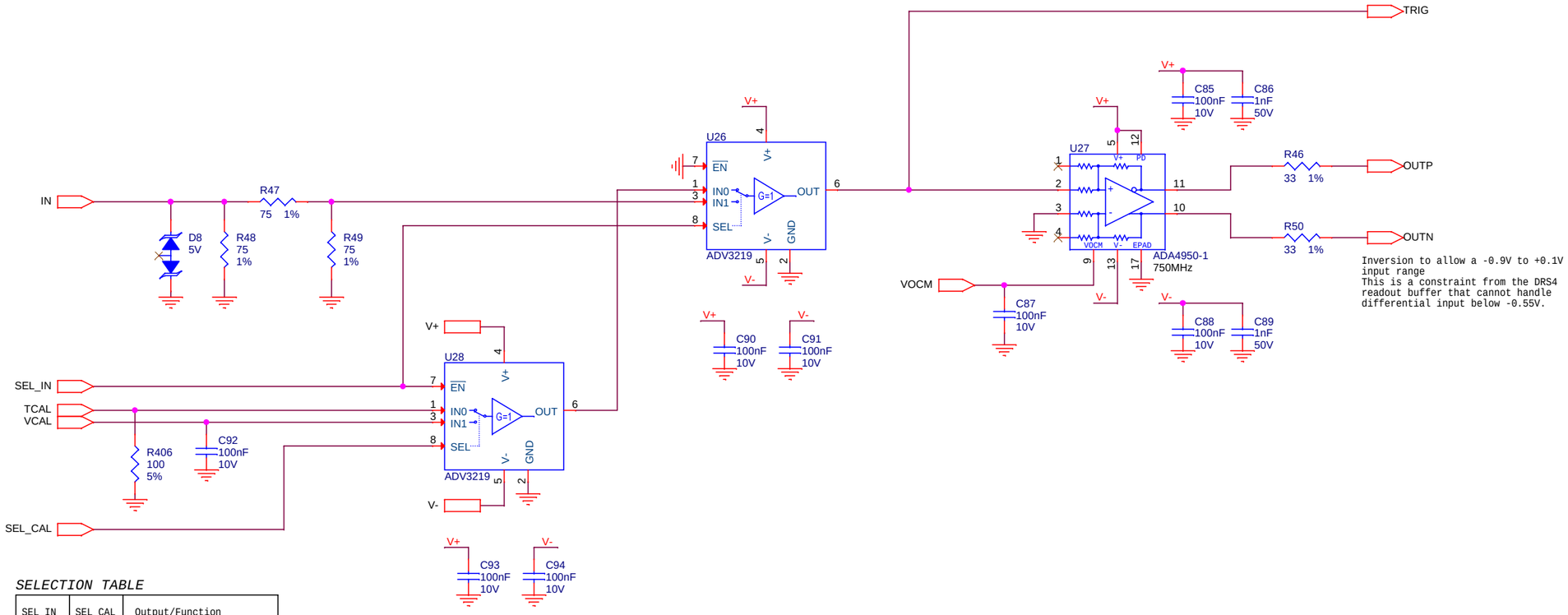
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_1/AFE_6

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 8 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

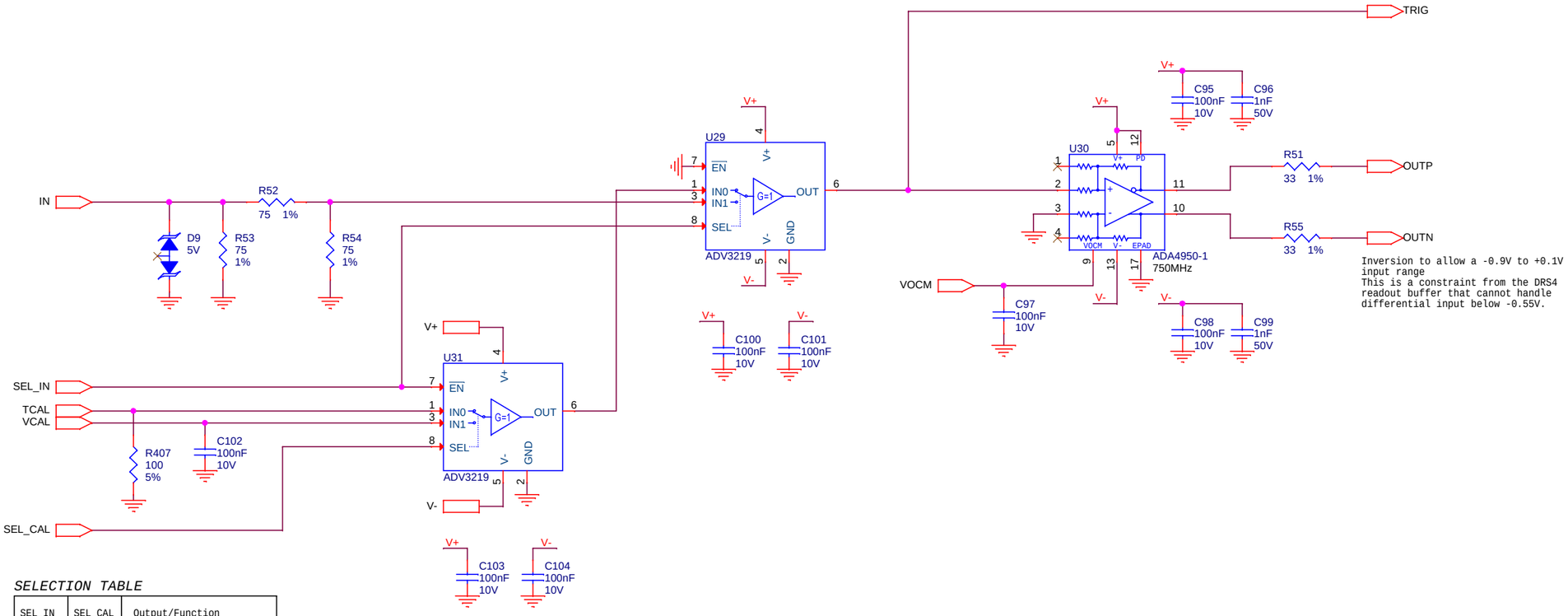
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_1/AFE_7

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 9 of 60



Inversion to allow a -0.9V to +0.1V input range
This is a constraint from the DRS4 readout buffer that cannot handle differential input below -0.55V.

SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

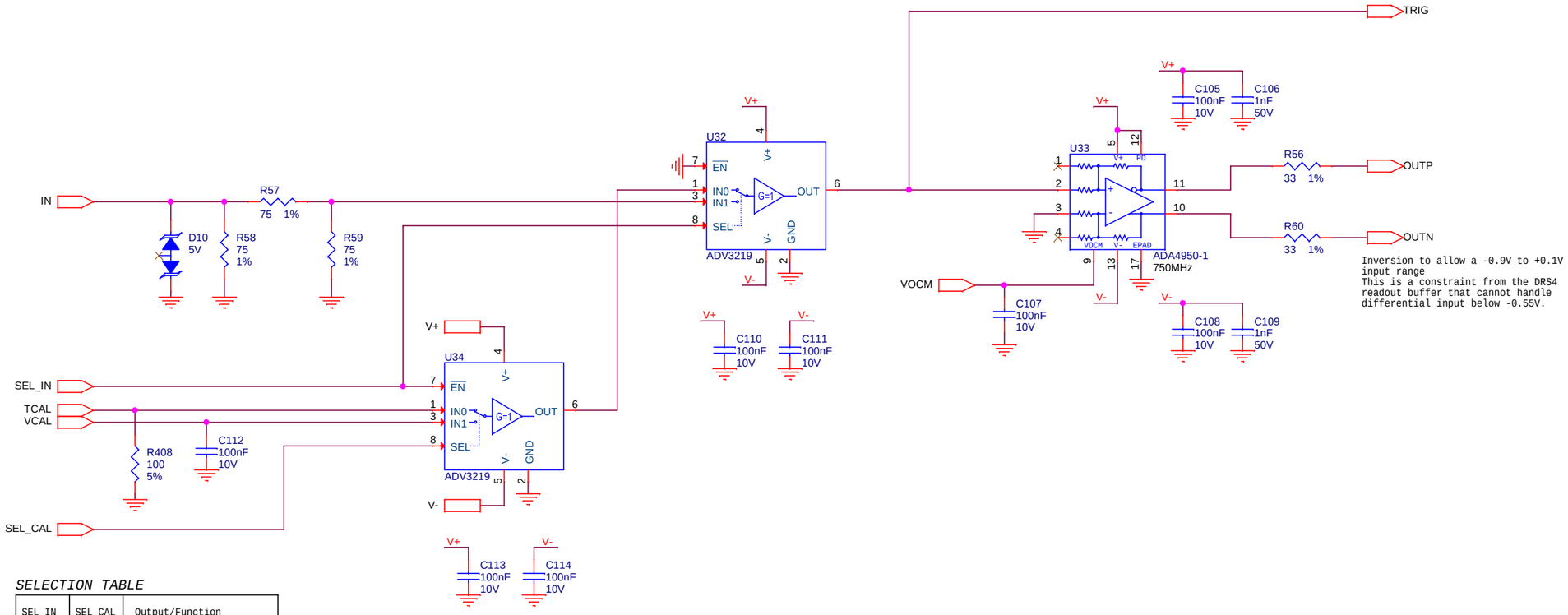
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_1/AFE_8

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 10 of 60



Inversion to allow a -0.9V to +0.1V input range
This is a constraint from the DRS4 readout buffer that cannot handle differential input below -0.55V.

SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

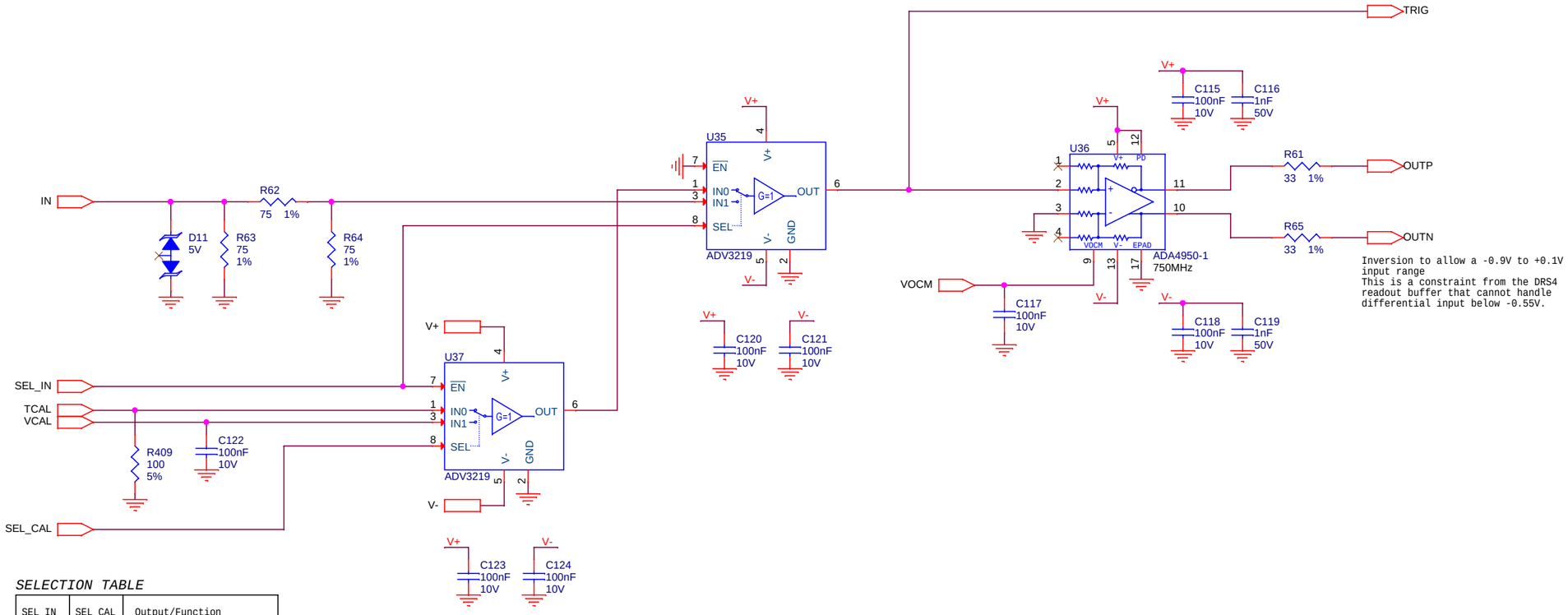
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_2/AFE_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 11 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

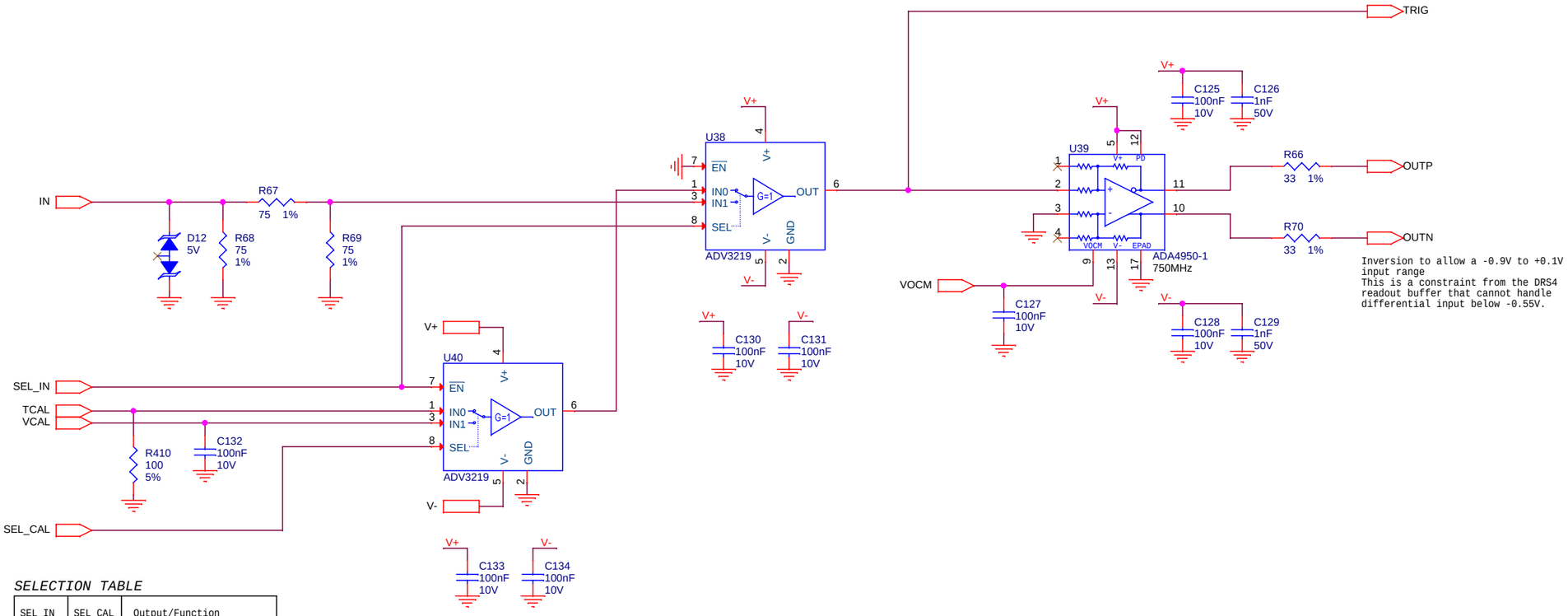
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_2/AFE_2

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 12 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

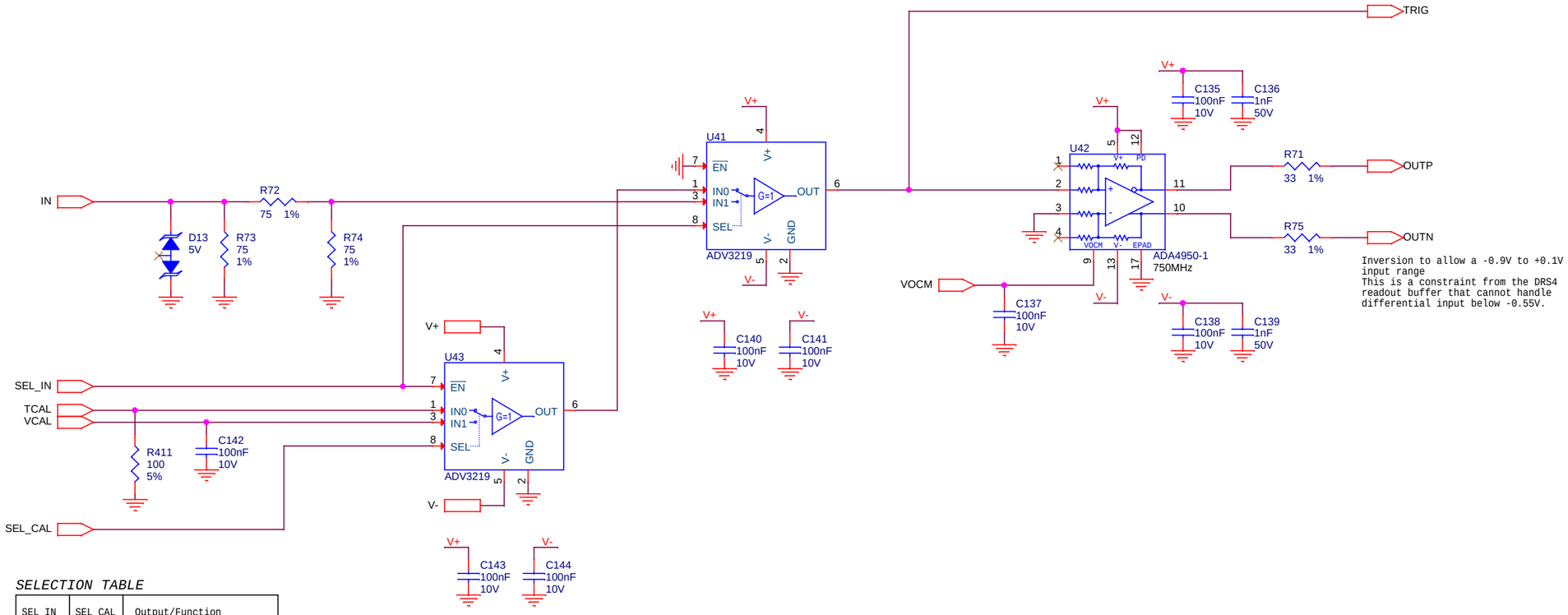
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_2/AFE_3

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 13 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

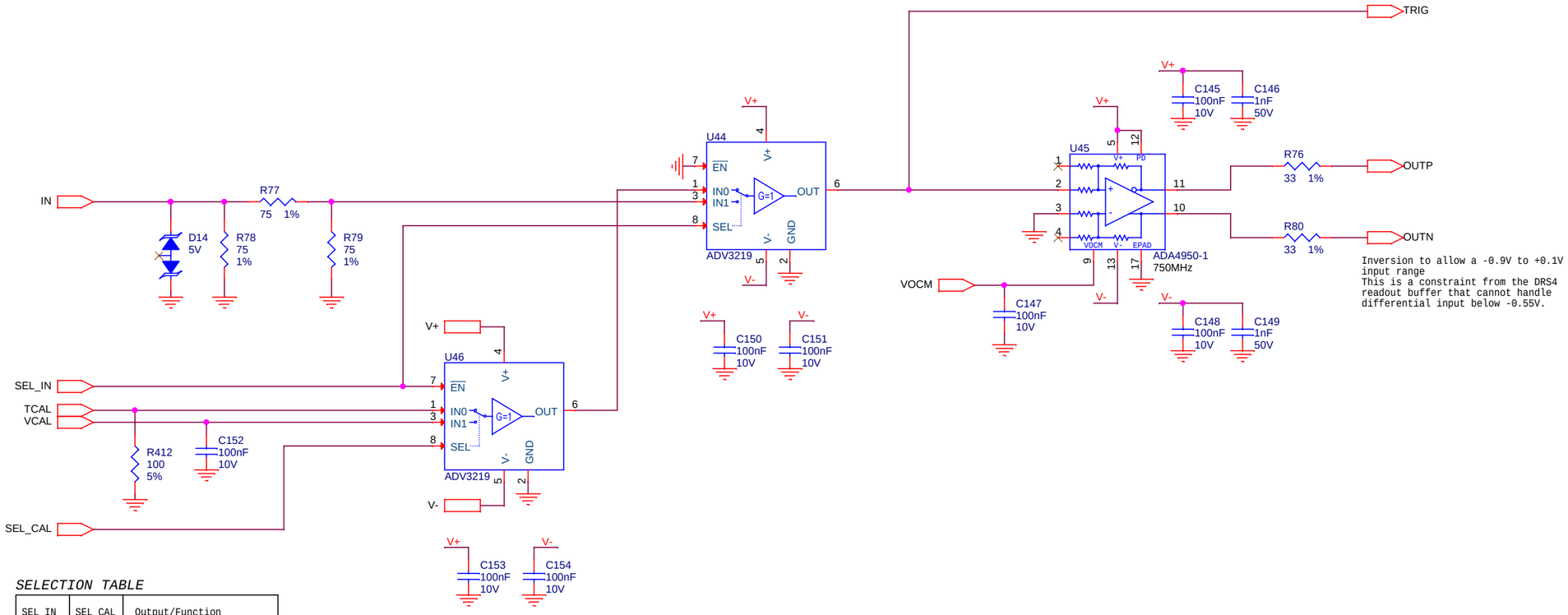
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_2/AFE_4

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 14 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

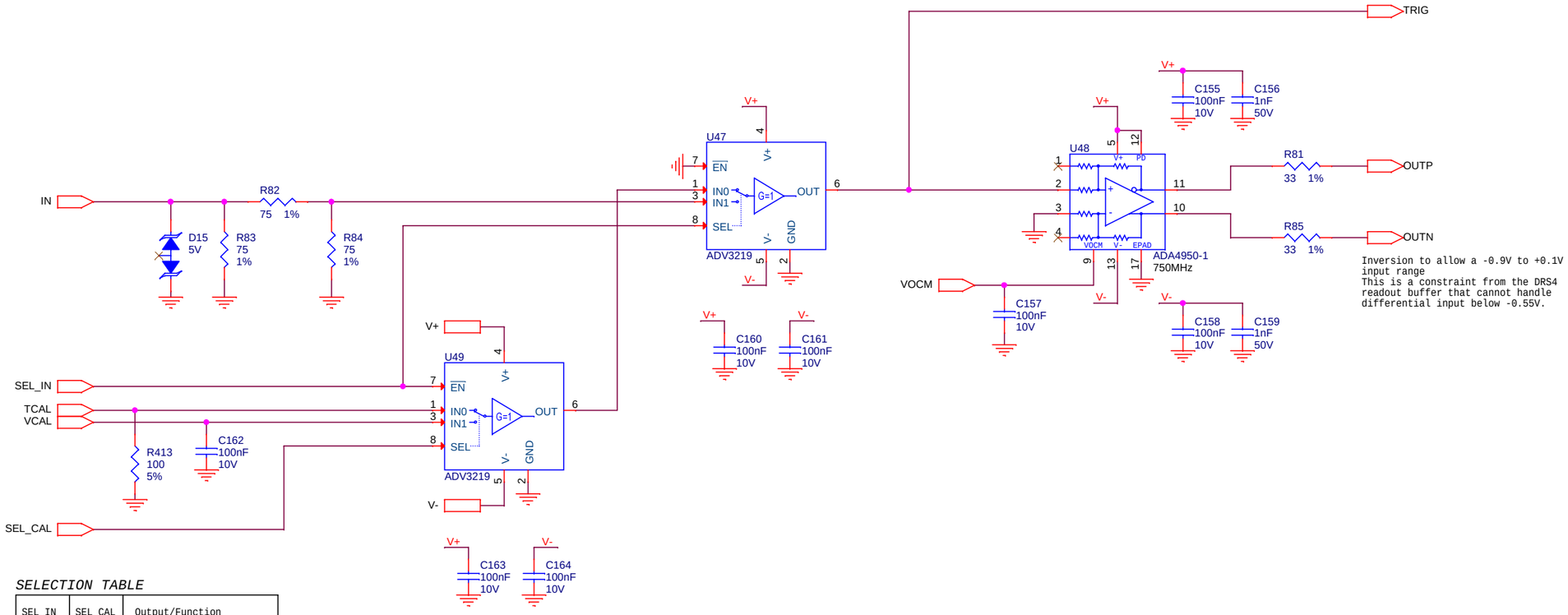
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_2/AFE_5

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 15 of 60



Inversion to allow a -0.9V to +0.1V input range
This is a constraint from the DRS4 readout buffer that cannot handle differential input below -0.55V.

SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

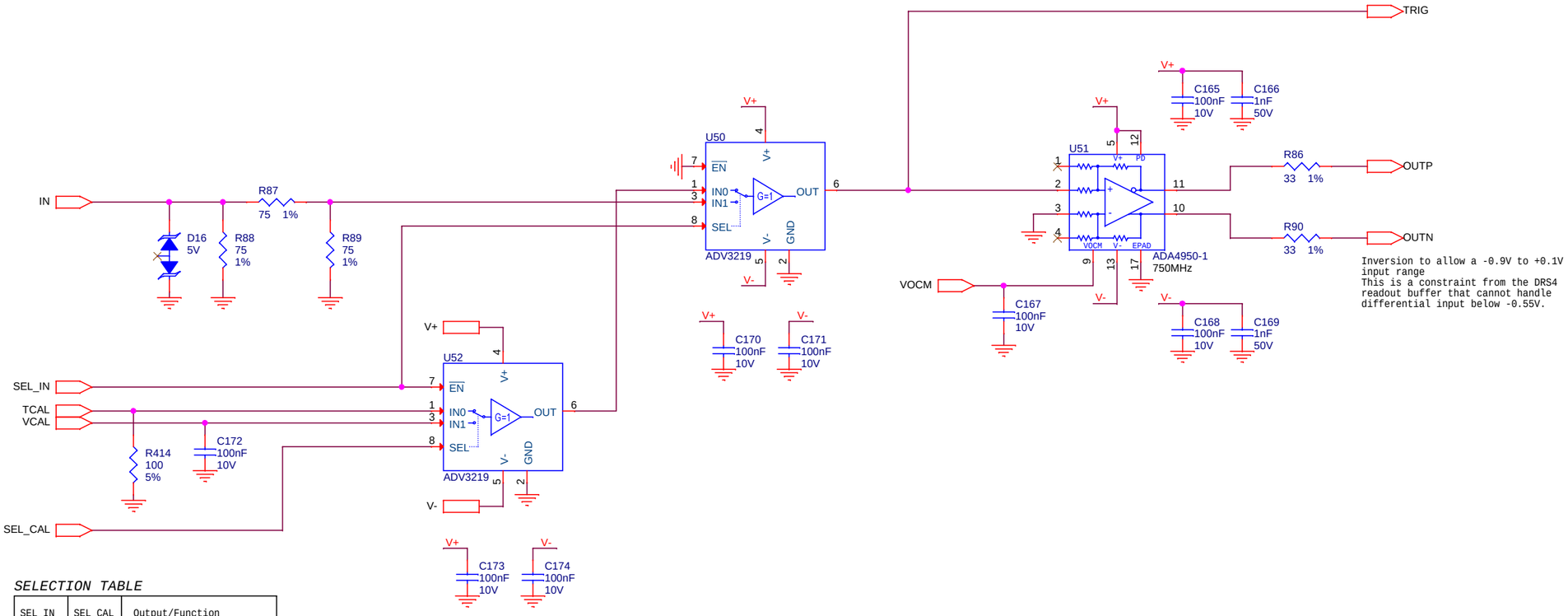
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_2/AFE_6

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 16 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

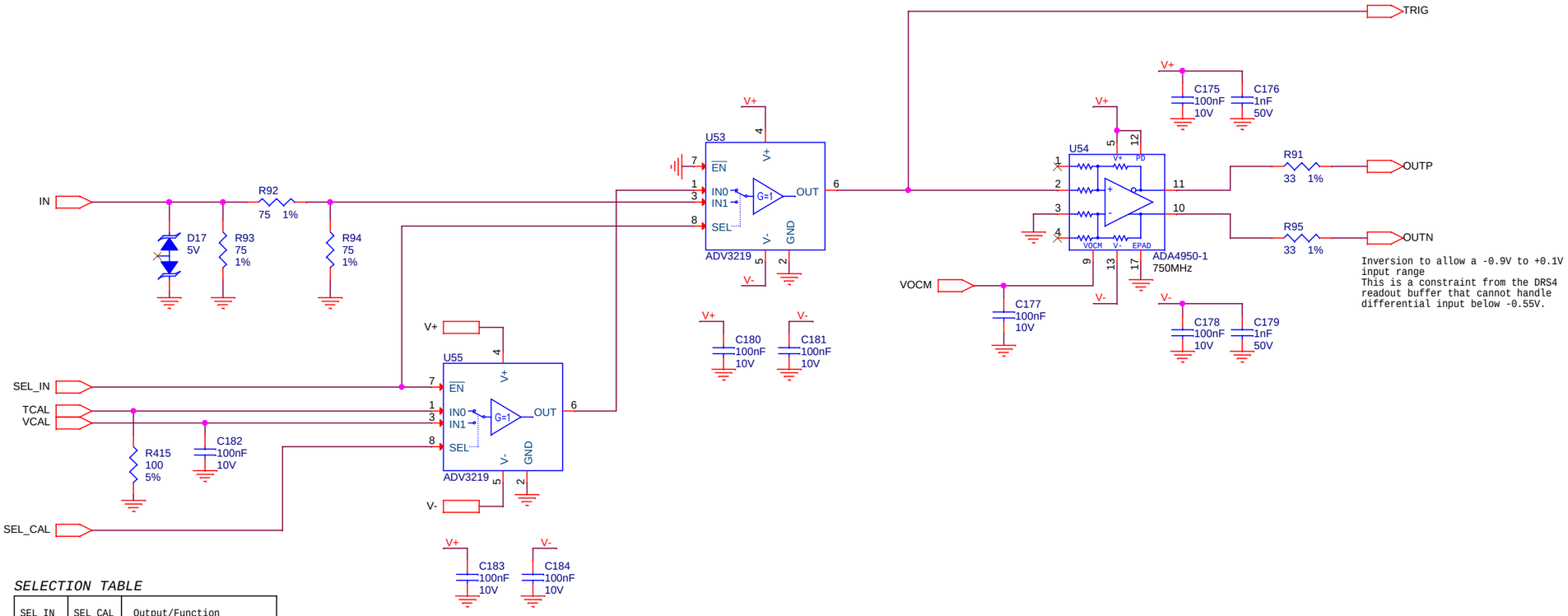
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_2/AFE_7

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 17 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

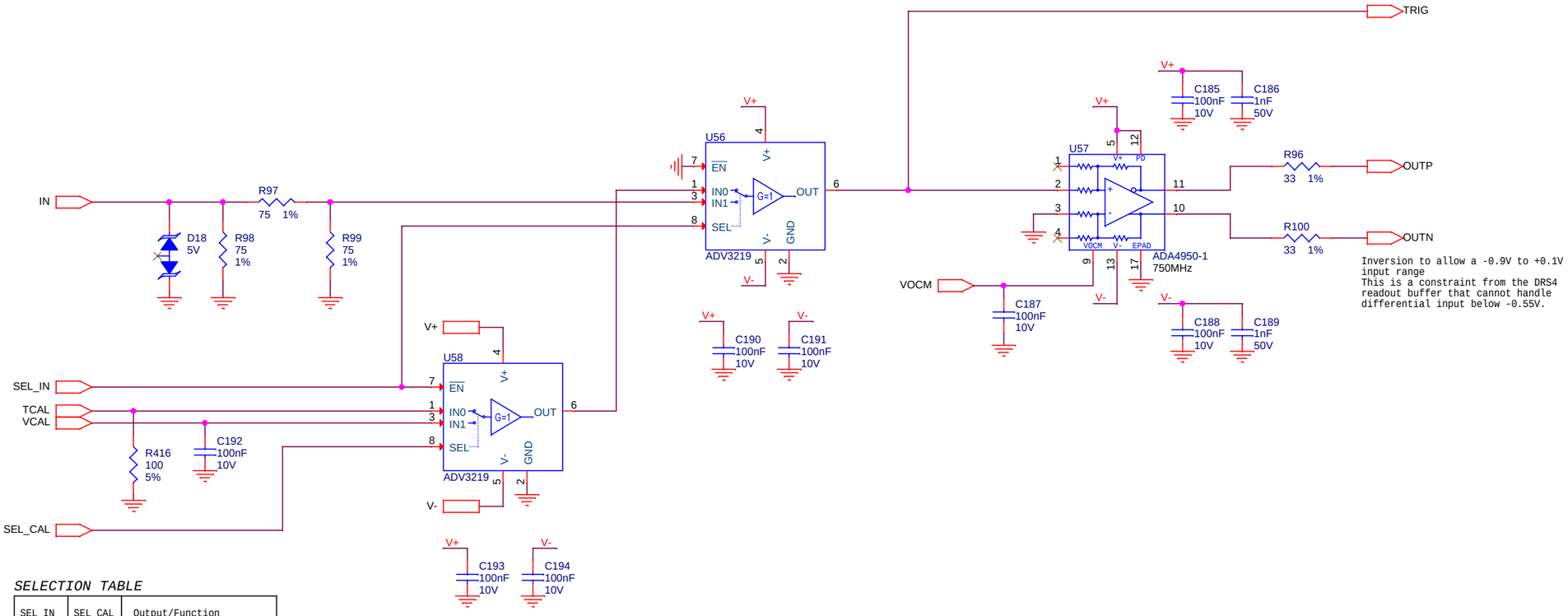
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_2/AFE_8

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 18 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

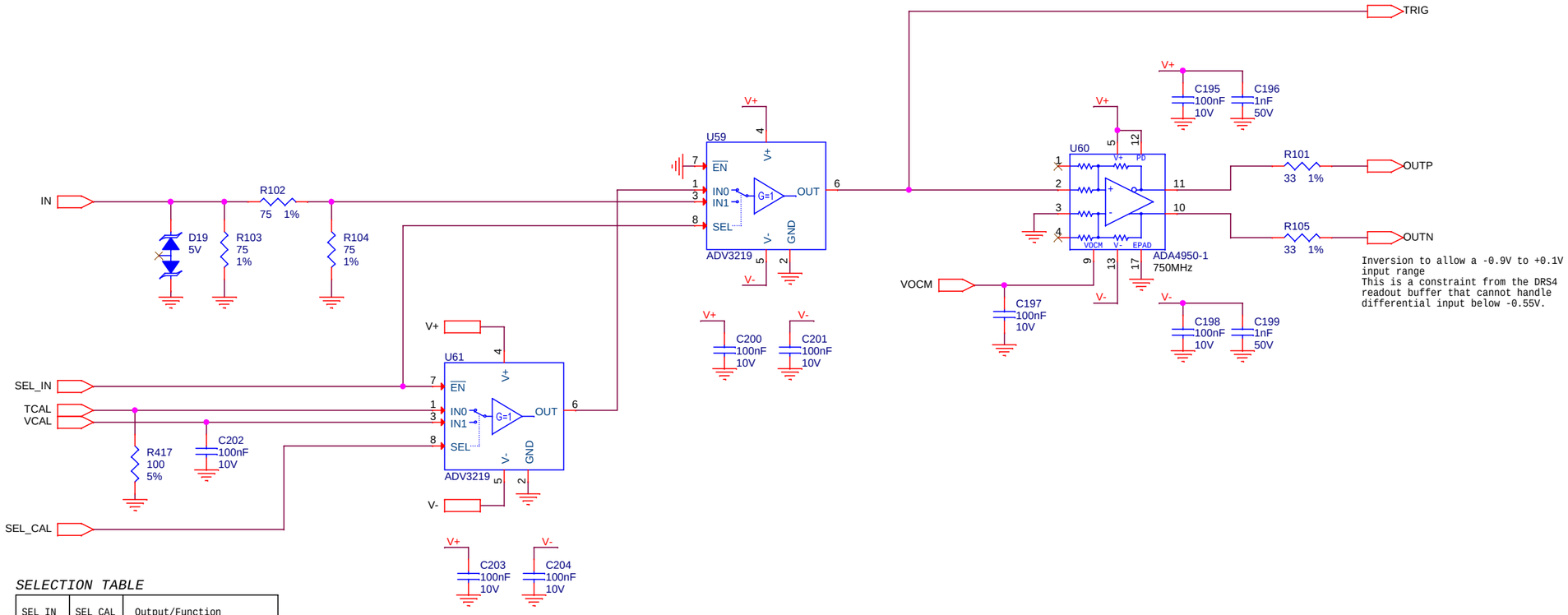
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_3/AFE_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 19 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

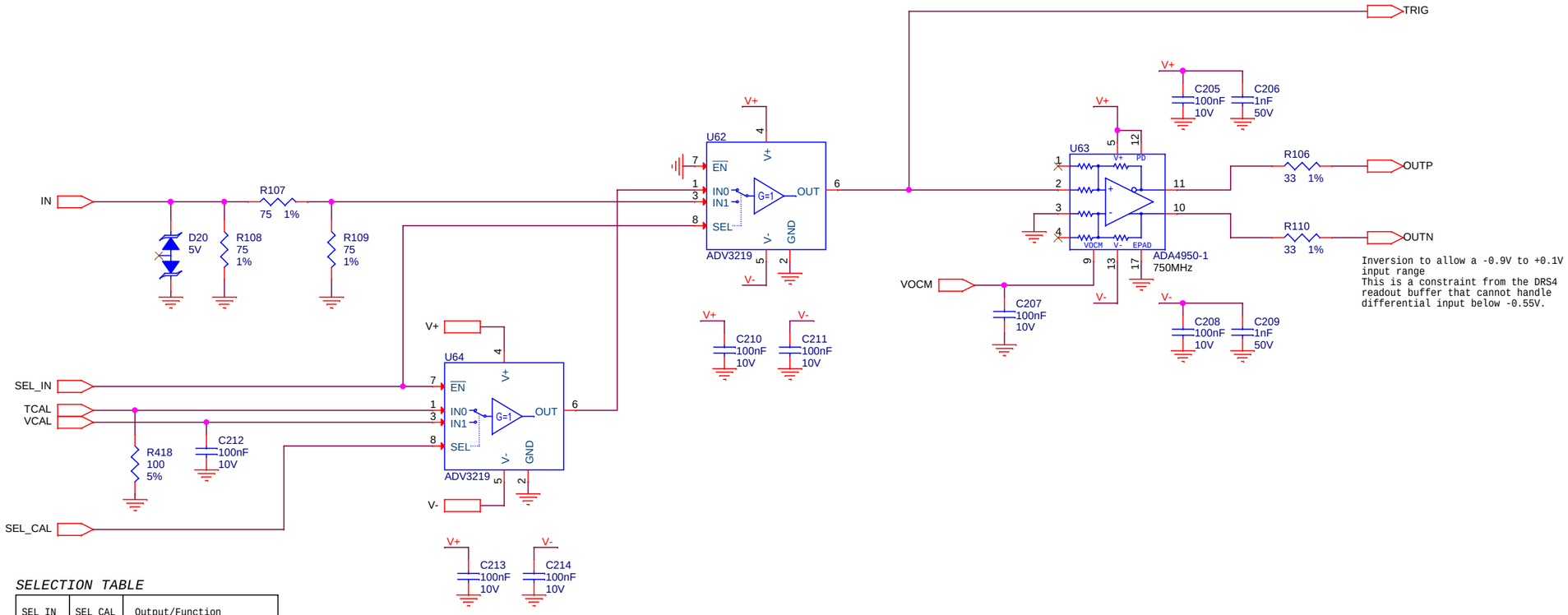
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_3/AFE_2

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 20 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

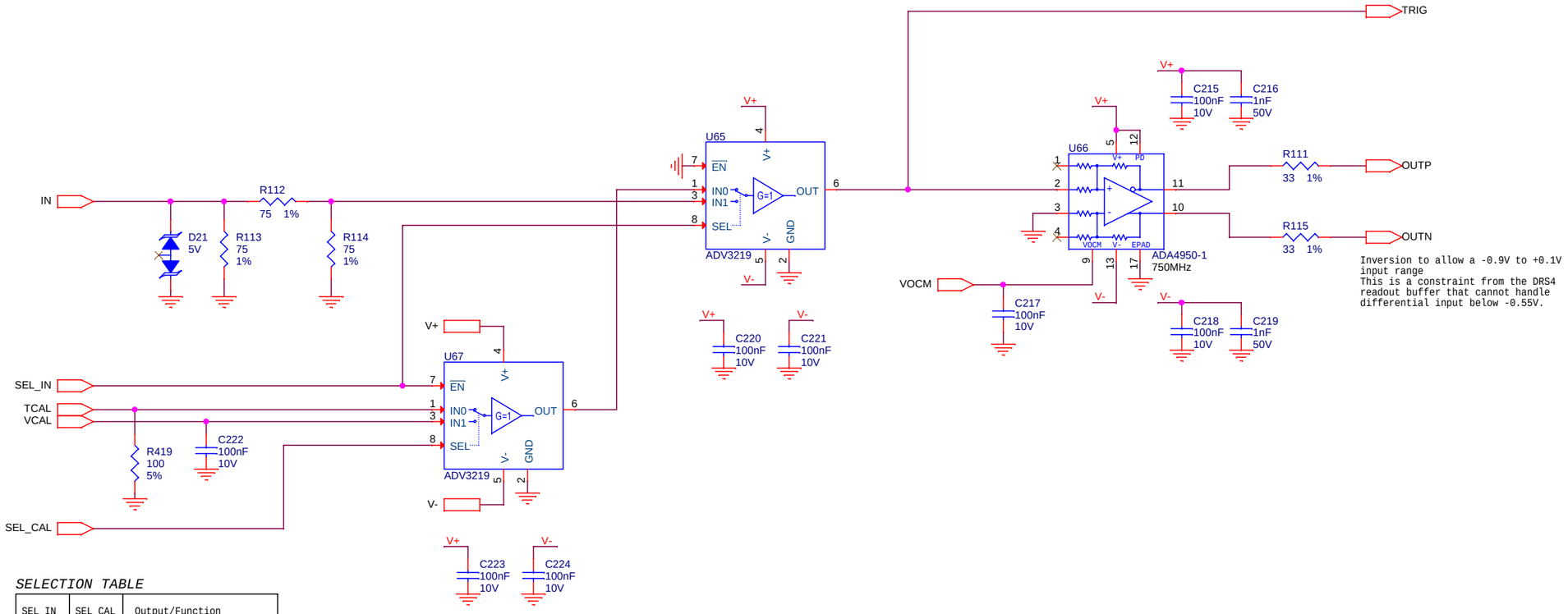
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_3/AFE_3

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 21 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

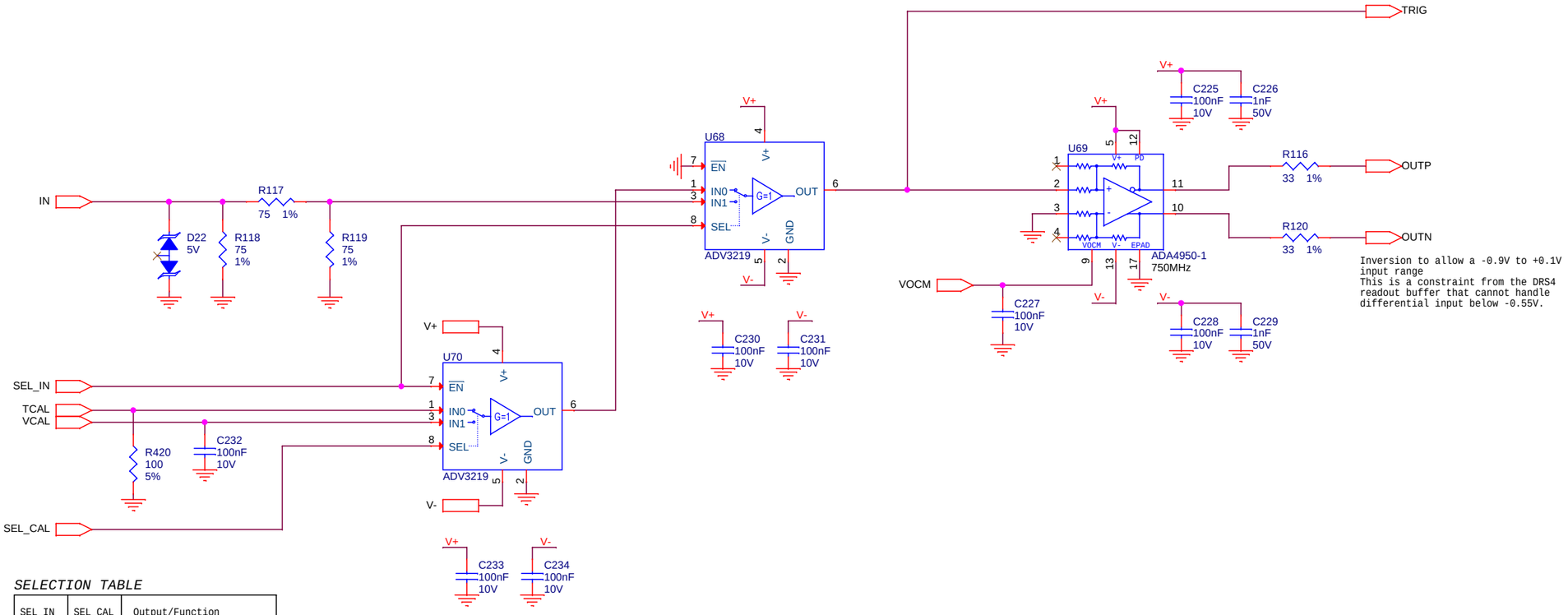
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_3/AFE_4

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 22 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

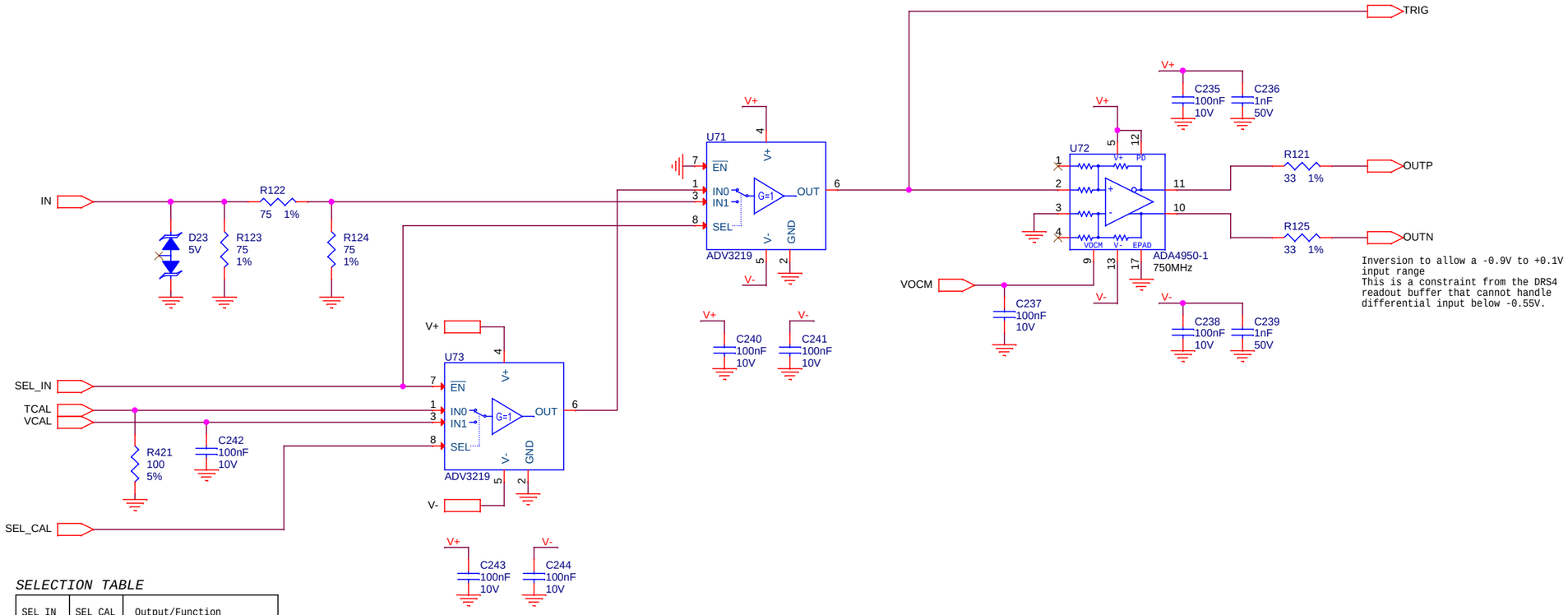
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_3/AFE_5

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 23 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

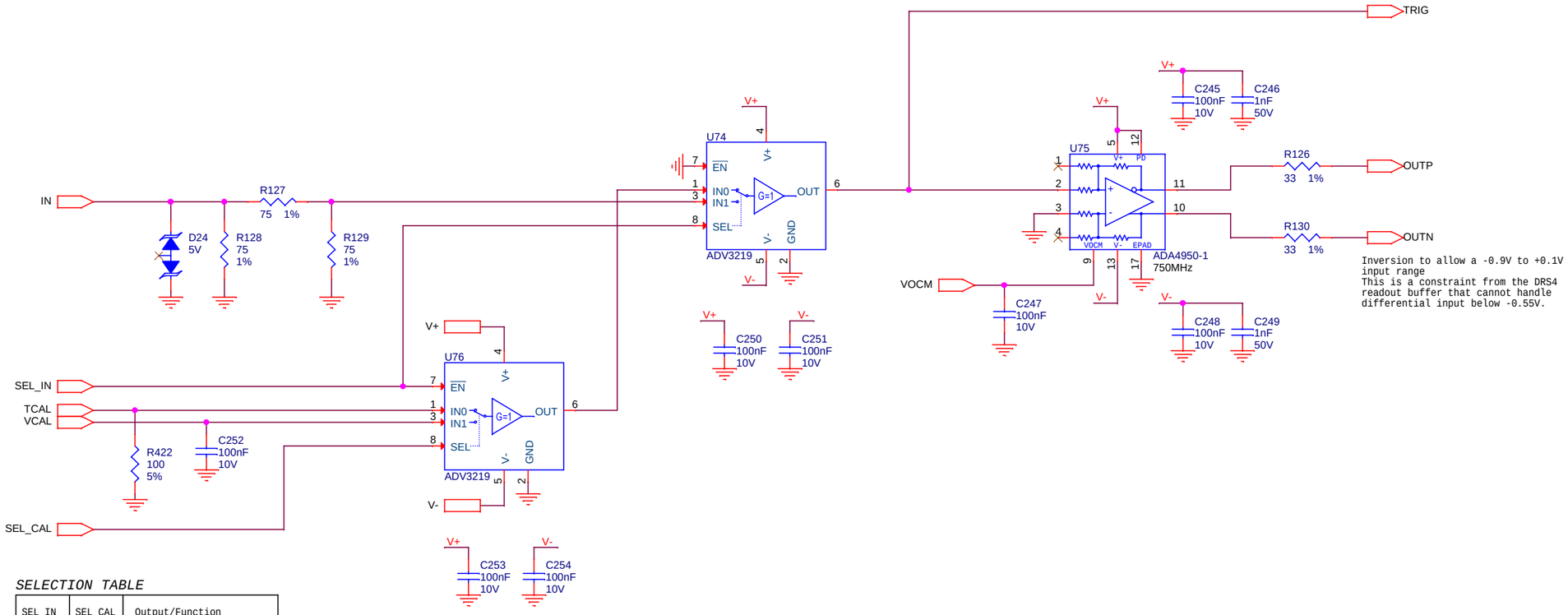
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_3/AFE_6

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 24 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

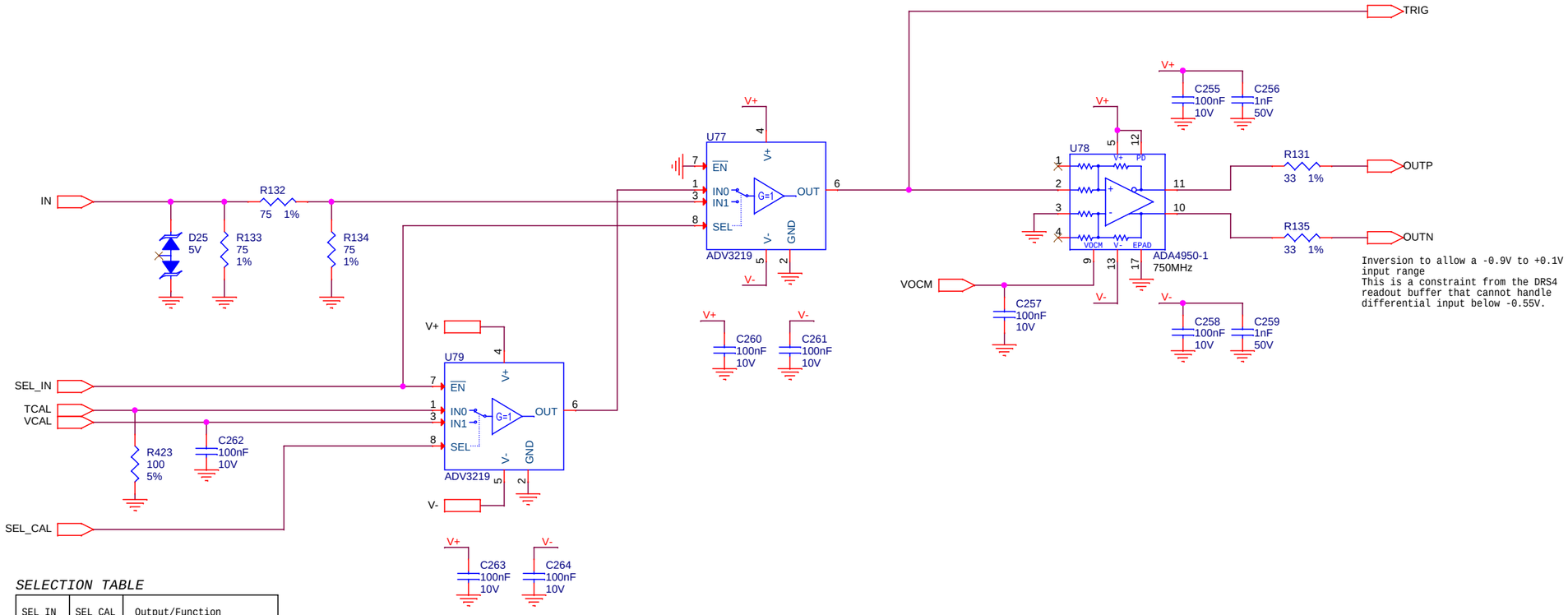
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_3/AFE_7

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 25 of 60



Inversion to allow a -0.9V to +0.1V input range
This is a constraint from the DRS4 readout buffer that cannot handle differential input below -0.55V.

SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

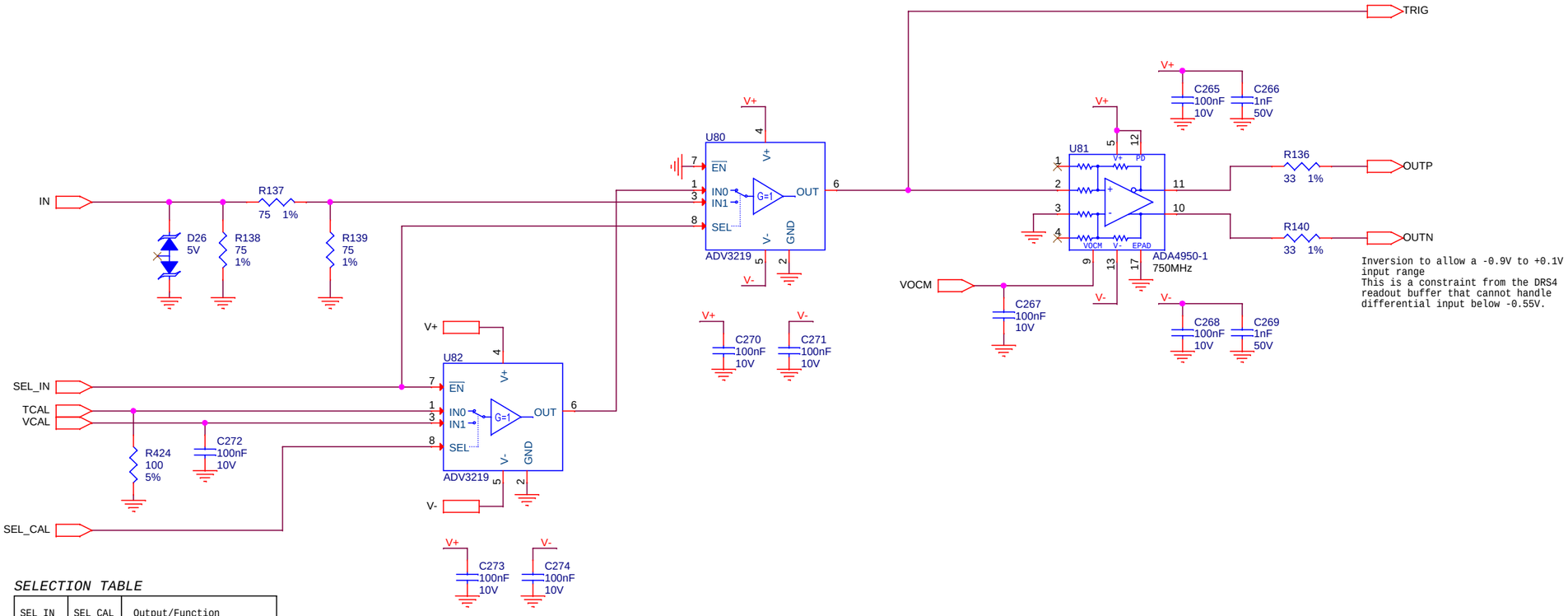
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_3/AFE_8

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 26 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

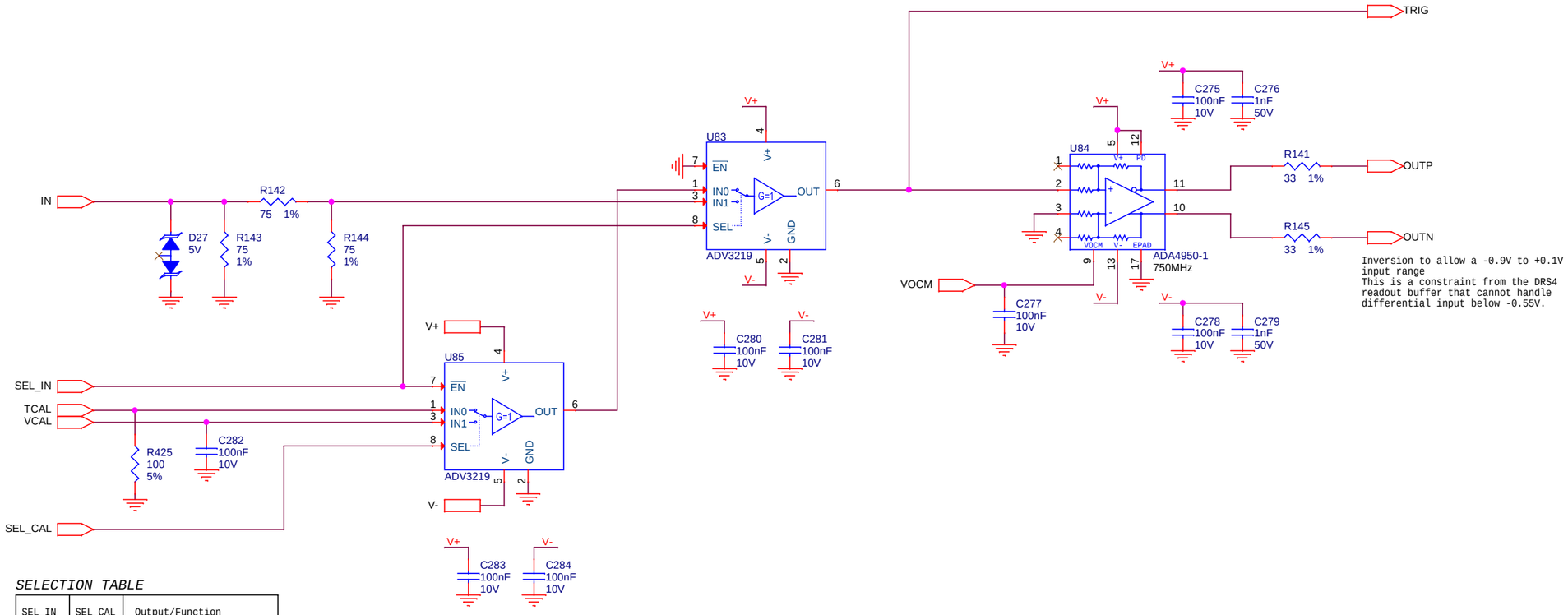
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_4/AFE_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 27 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

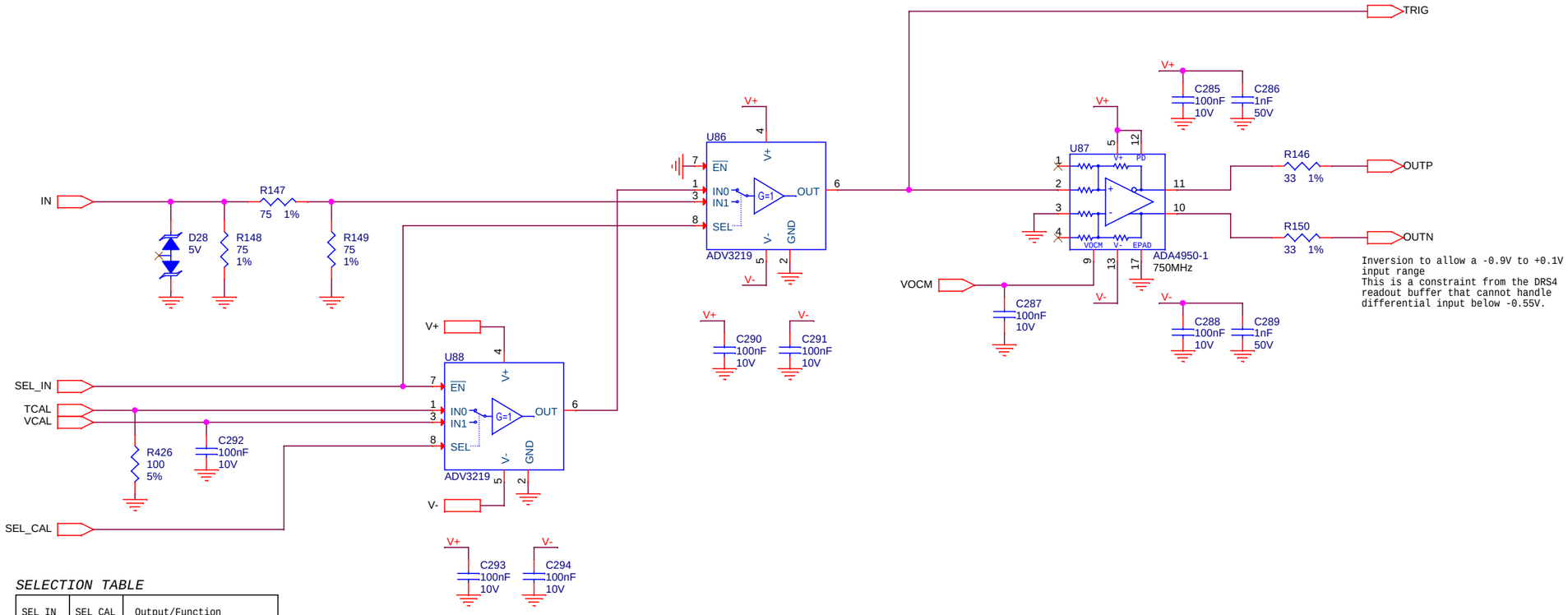
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_4/AFE_2

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 28 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

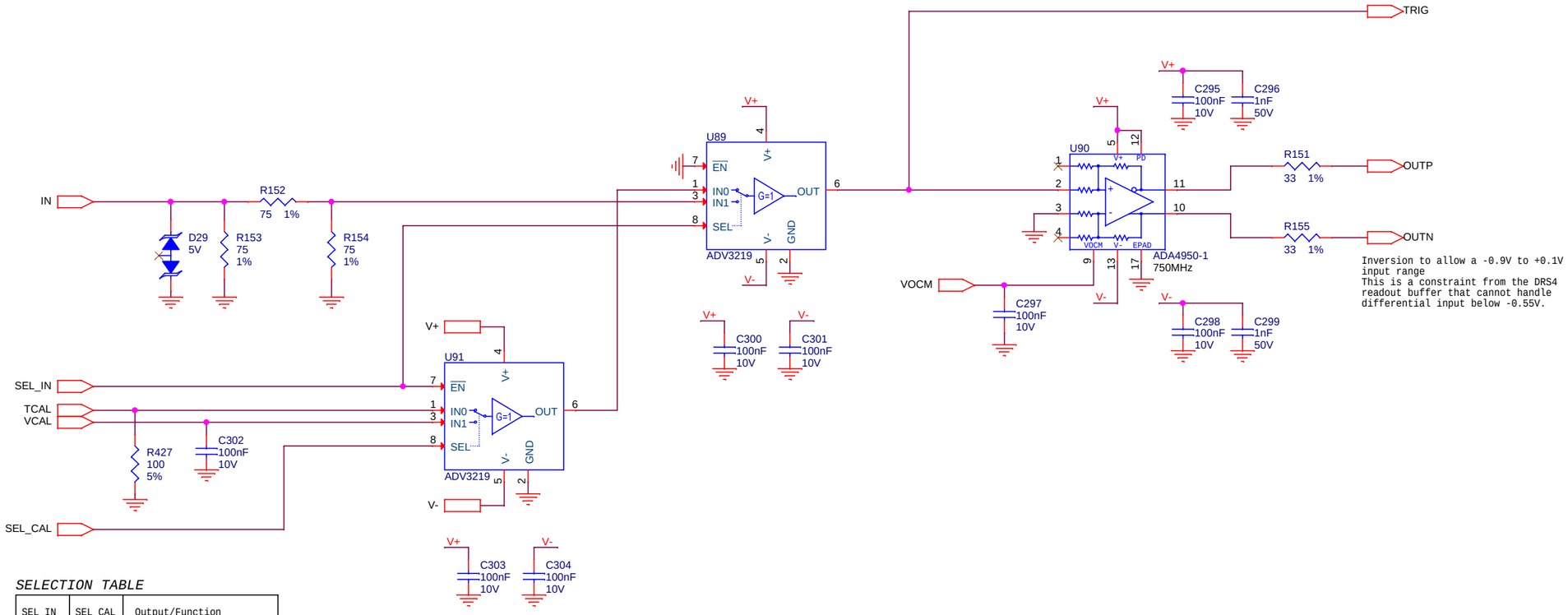
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_4/AFE_3

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 29 of 60



Inversion to allow a -0.9V to +0.1V input range
This is a constraint from the DRS4 readout buffer that cannot handle differential input below -0.55V.

SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

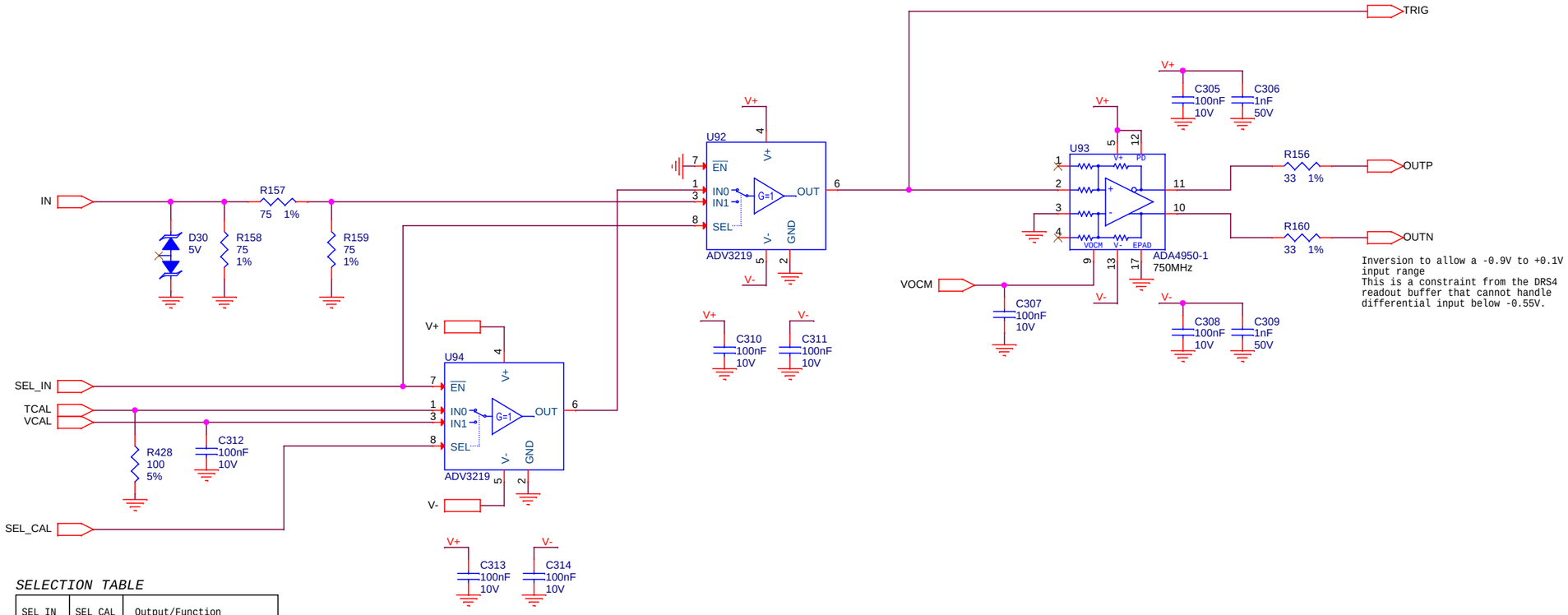
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_4/AFE_4

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 30 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

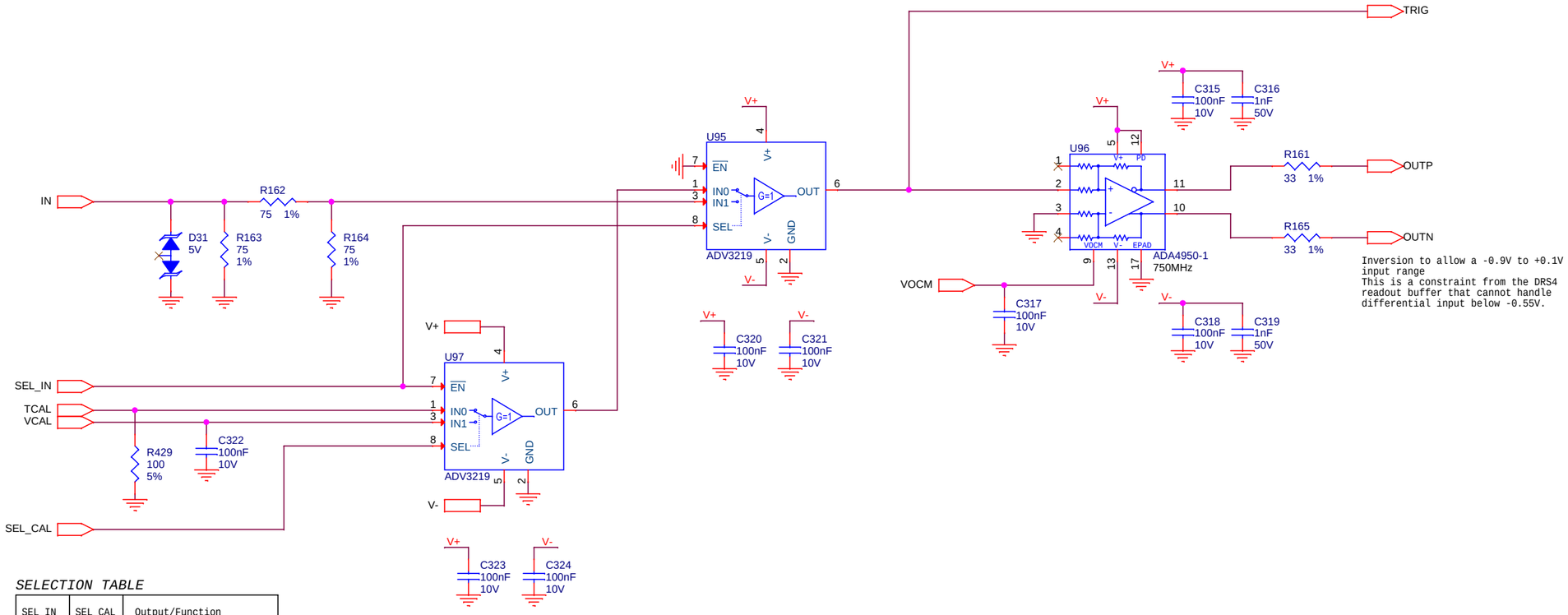
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_4/AFE_5

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 31 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

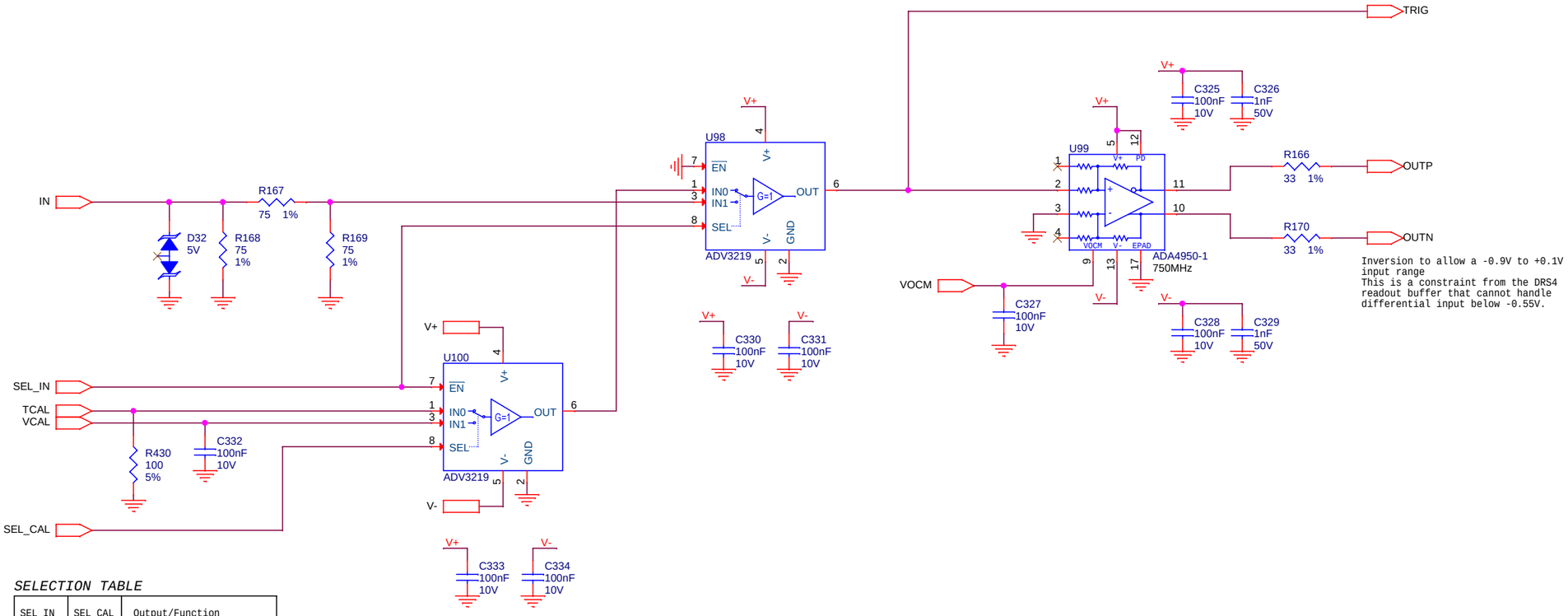
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_4/AFE_6

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 32 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

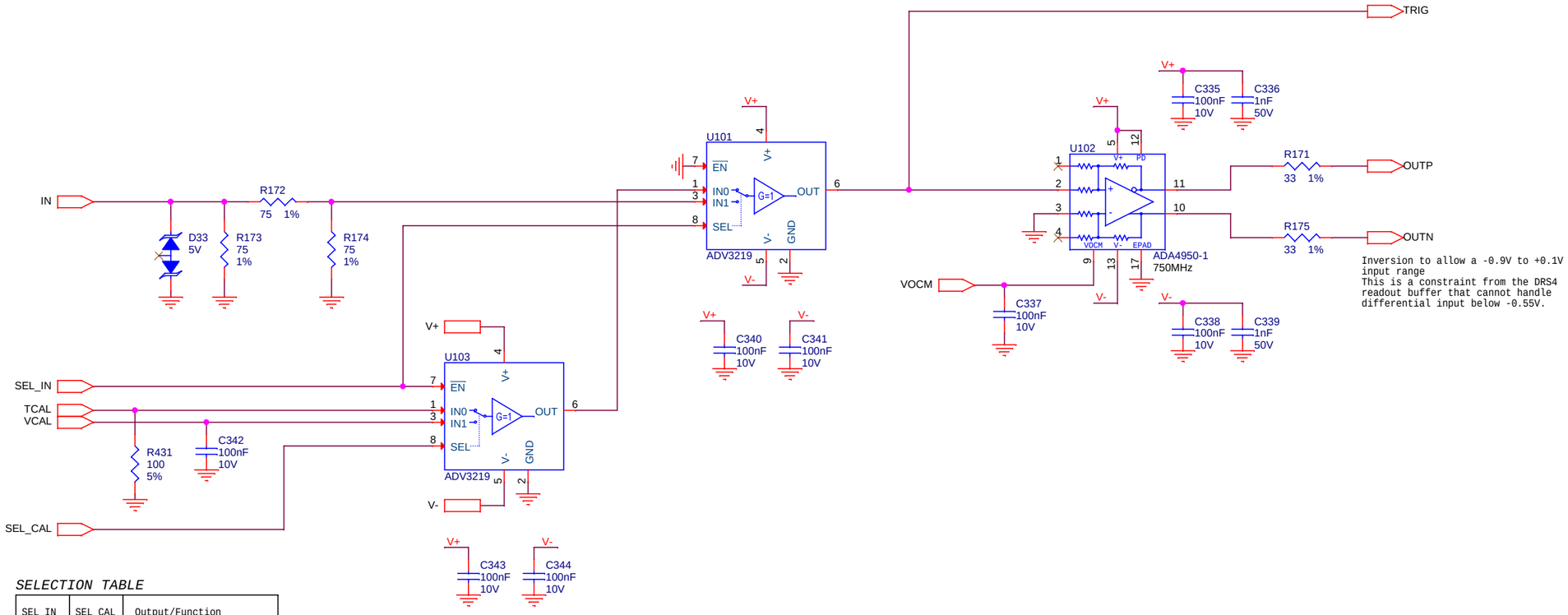
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_4/AFE_7

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 33 of 60



SELECTION TABLE

SEL_IN	SEL_CAL	Output/Function
0	0	Timing Calibration
0	1	Voltage Calibration
1	X	Input Signal (SiPM)

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

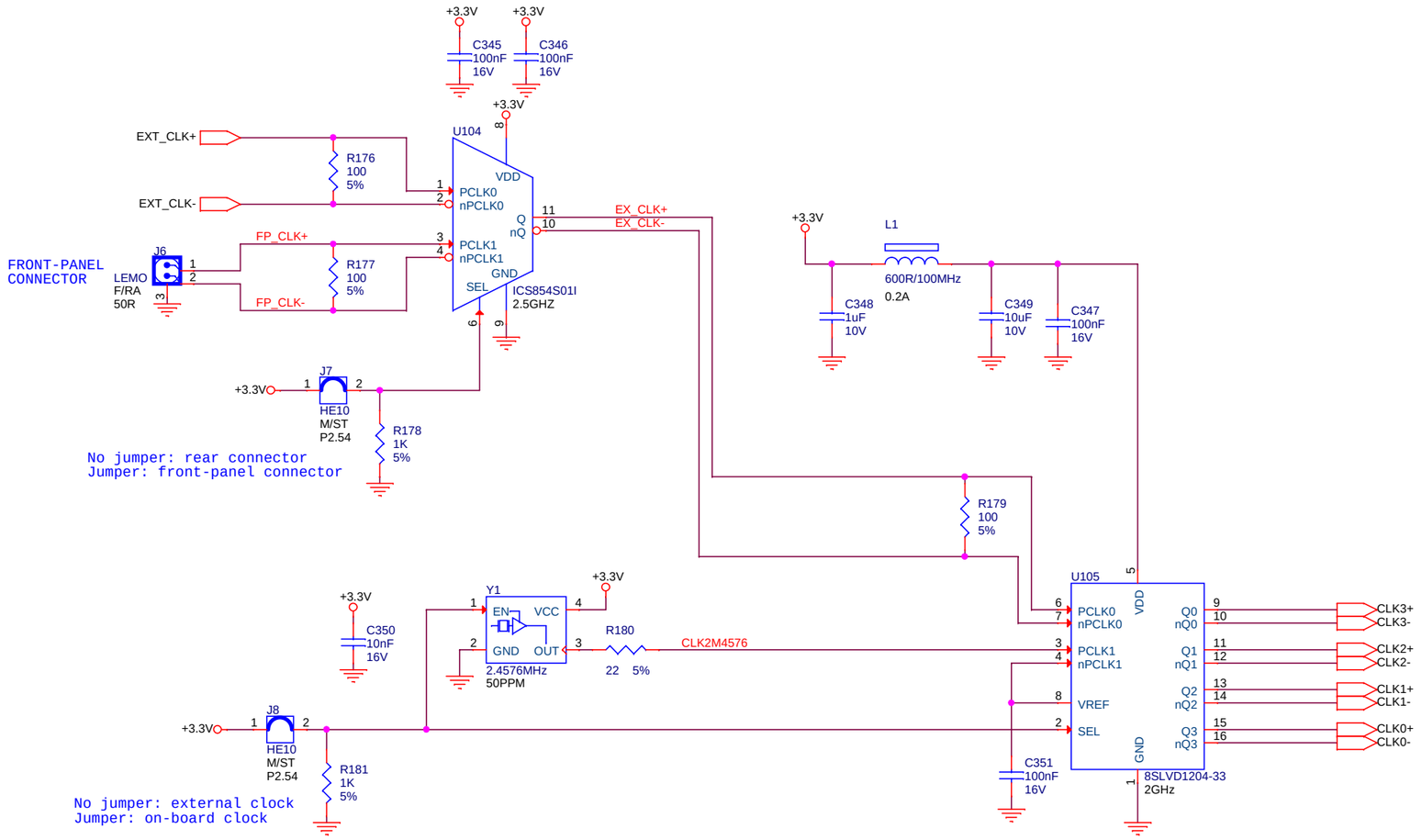
ANALOG FRONT-END STAGE

Schematic Path = /DRS4X32CH_1/DRS4X8CH_4/AFE_8

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Monday, October 03, 2016

Sheet 34 of 60



University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

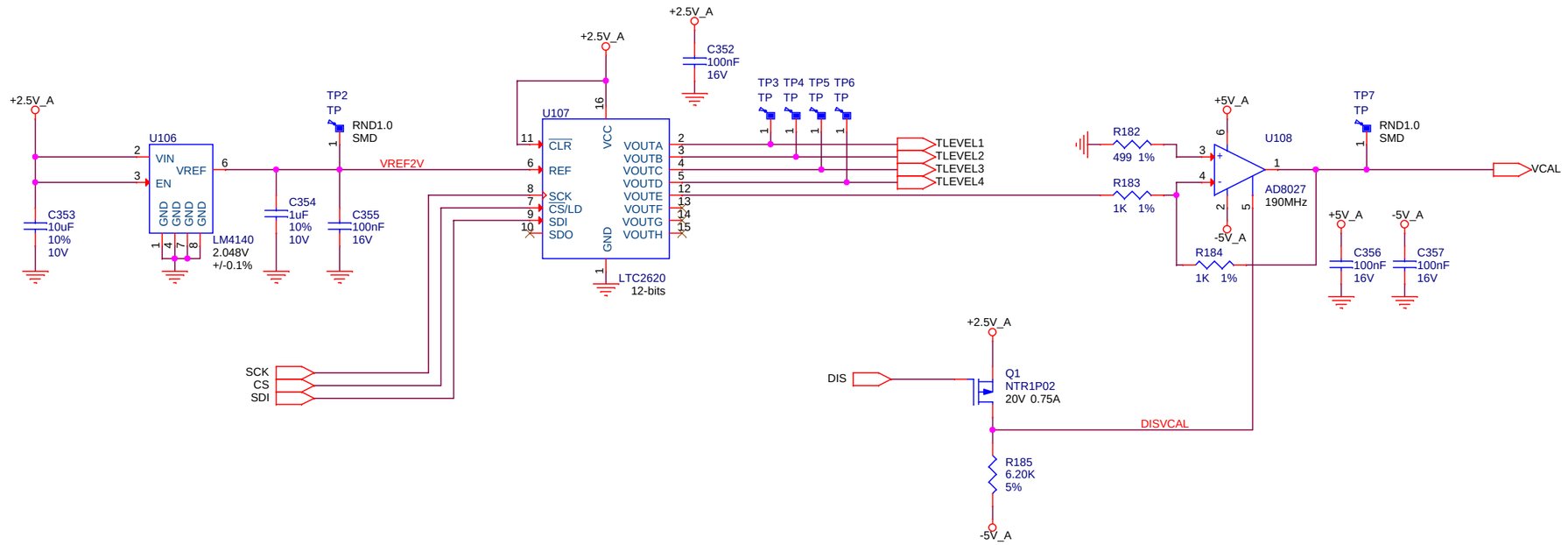
CLOCK MUX/BUFFER

Schematic Path = /DRS4X32CH_1/CLK_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 35 of 60



University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

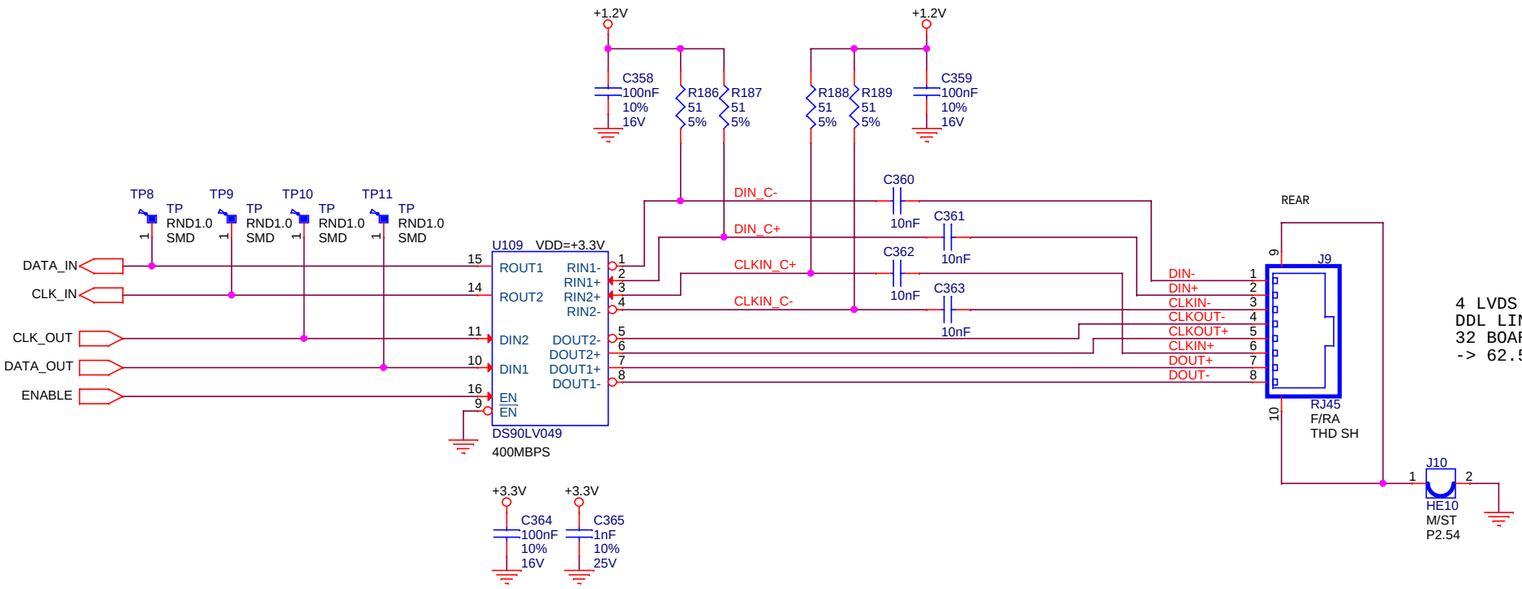
DAC8

Schematic Path = /DRS4X32CH_1/DAC8_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 36 of 60



4 LVDS PAIRS TO CONNECT TO DDL LINK CONCENTRATOR
DDL LINK: 2 Gbps
32 BOARDS PER DDL LINK
-> 62.5 Mbps/board

University of Geneva

.
DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

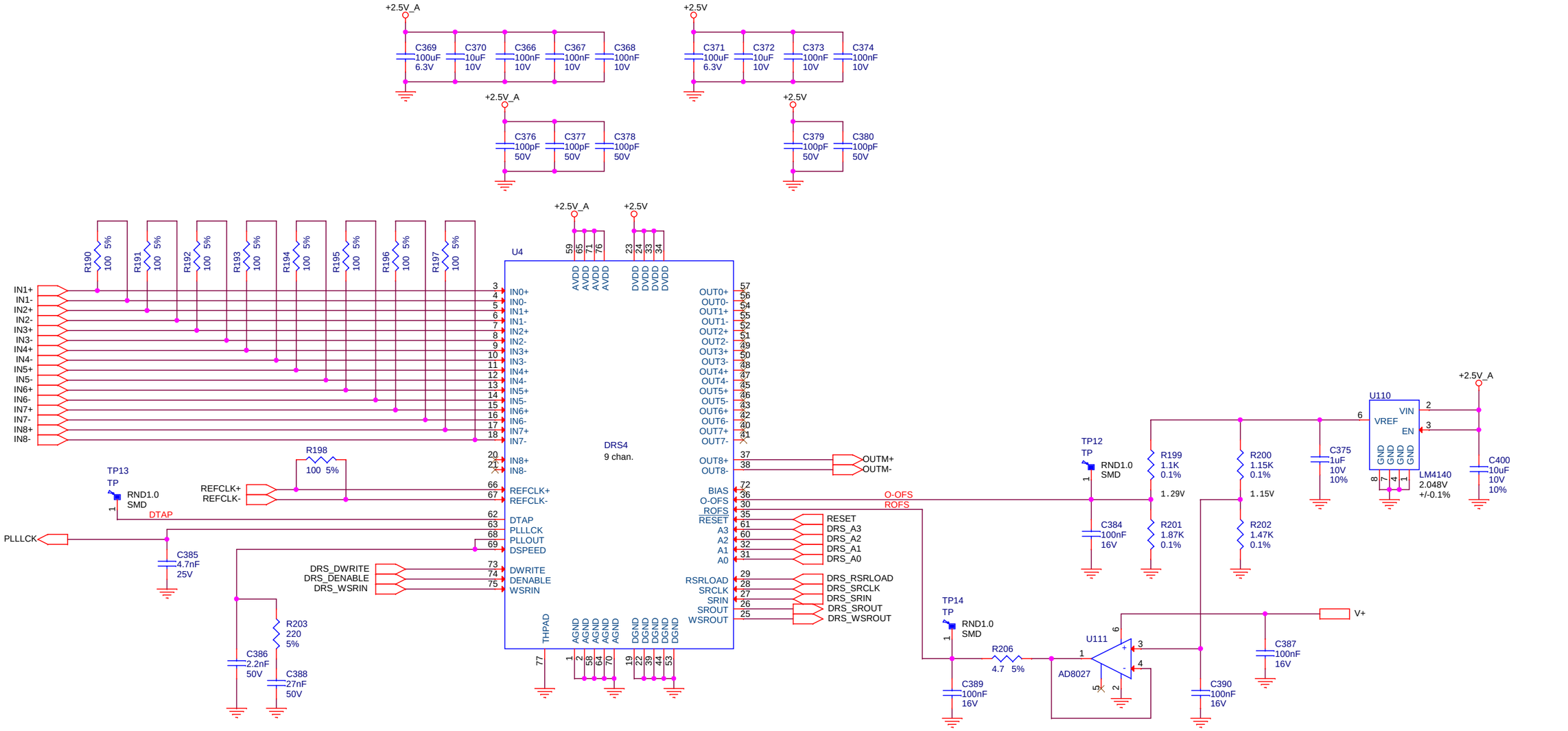
CONNECTION TO DDL LINK CONCENTRATOR

Schematic Path = /DDL_1

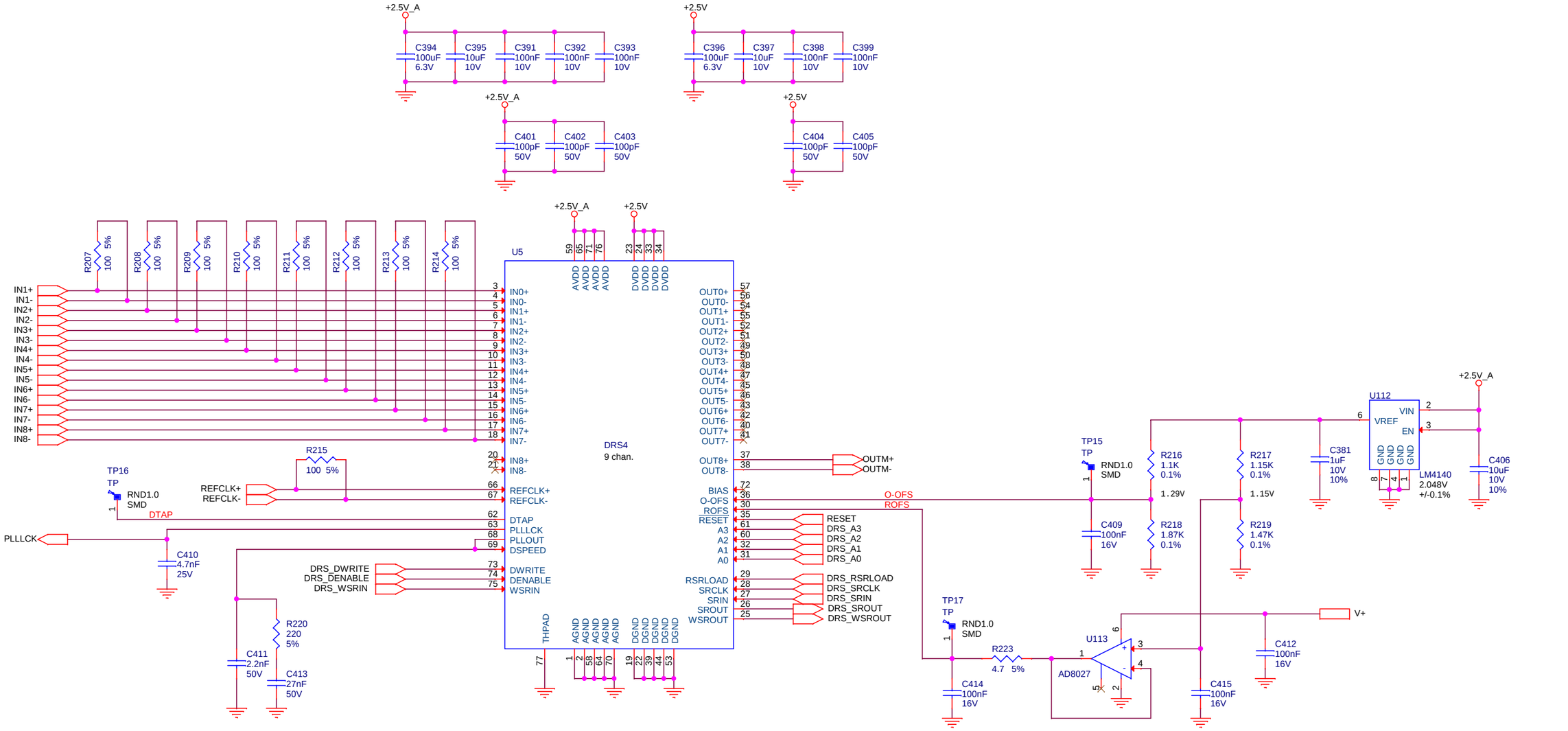
Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

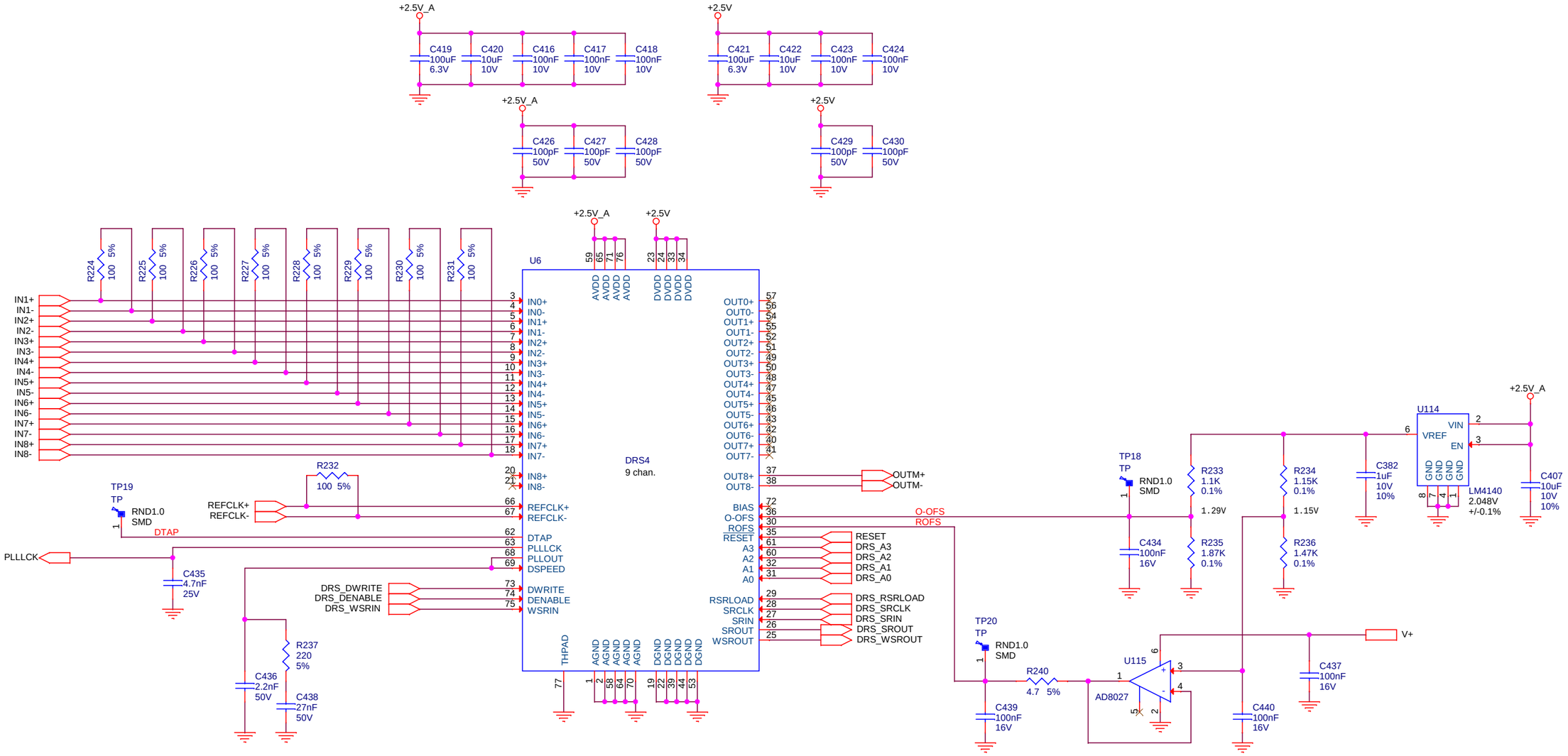
Sheet 37 of 60



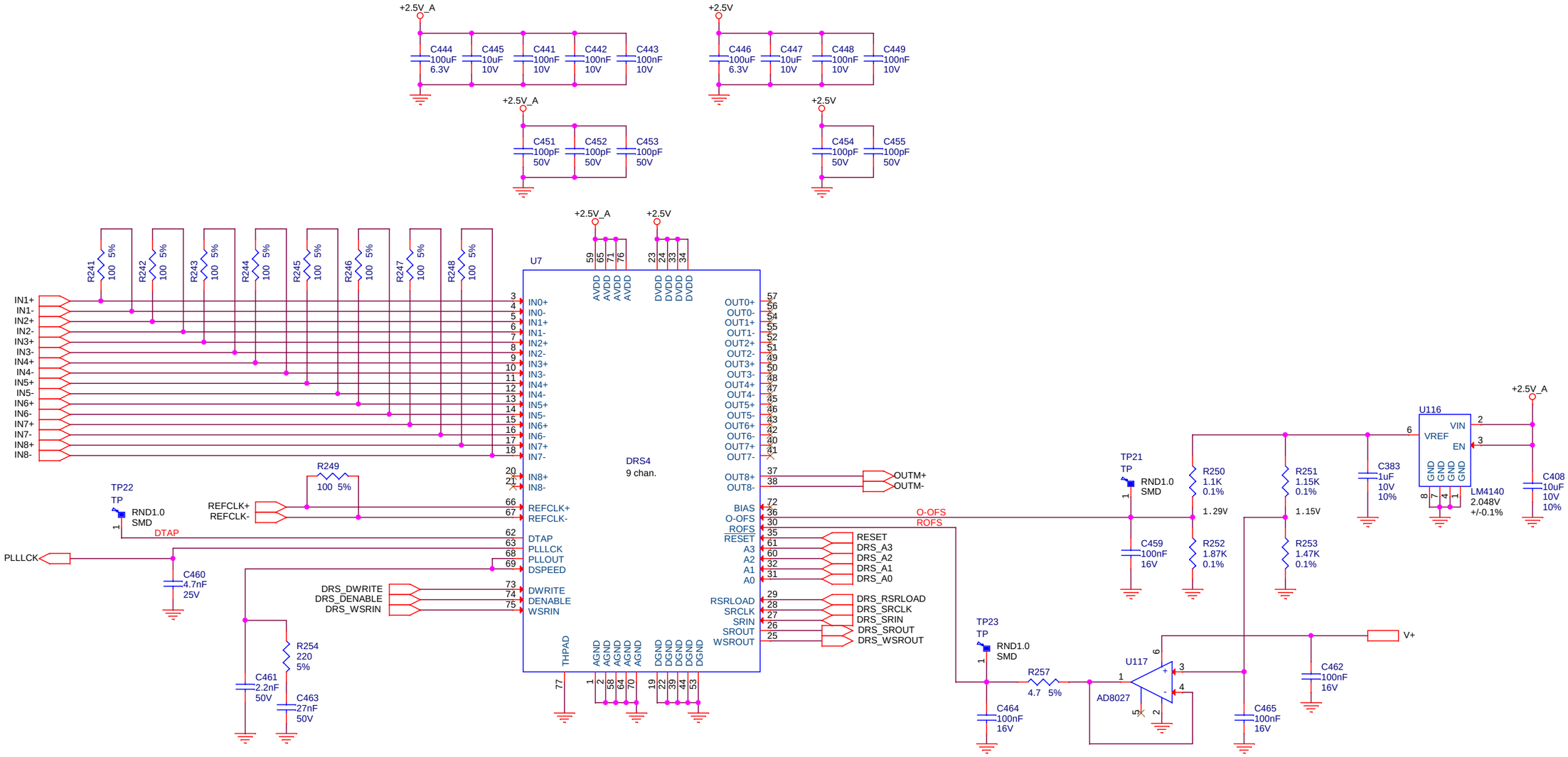
University of Geneva	UNIVERSITÉ DE GENÈVE
. DPNC 24 quai Ernest-Ansermet CH1211 GENEVE 4	
32-channel DRS4 Acquisition Board	
DRS4	Schematic Path = /DRS4X32CH_1/DRS4X8CH_1/DRS4_1
Size: A3	DWG NO: DPNC342
Rev PCB: 02A	Rev PCBA:
Thursday, September 29, 2016	Sheet: 38 of 60



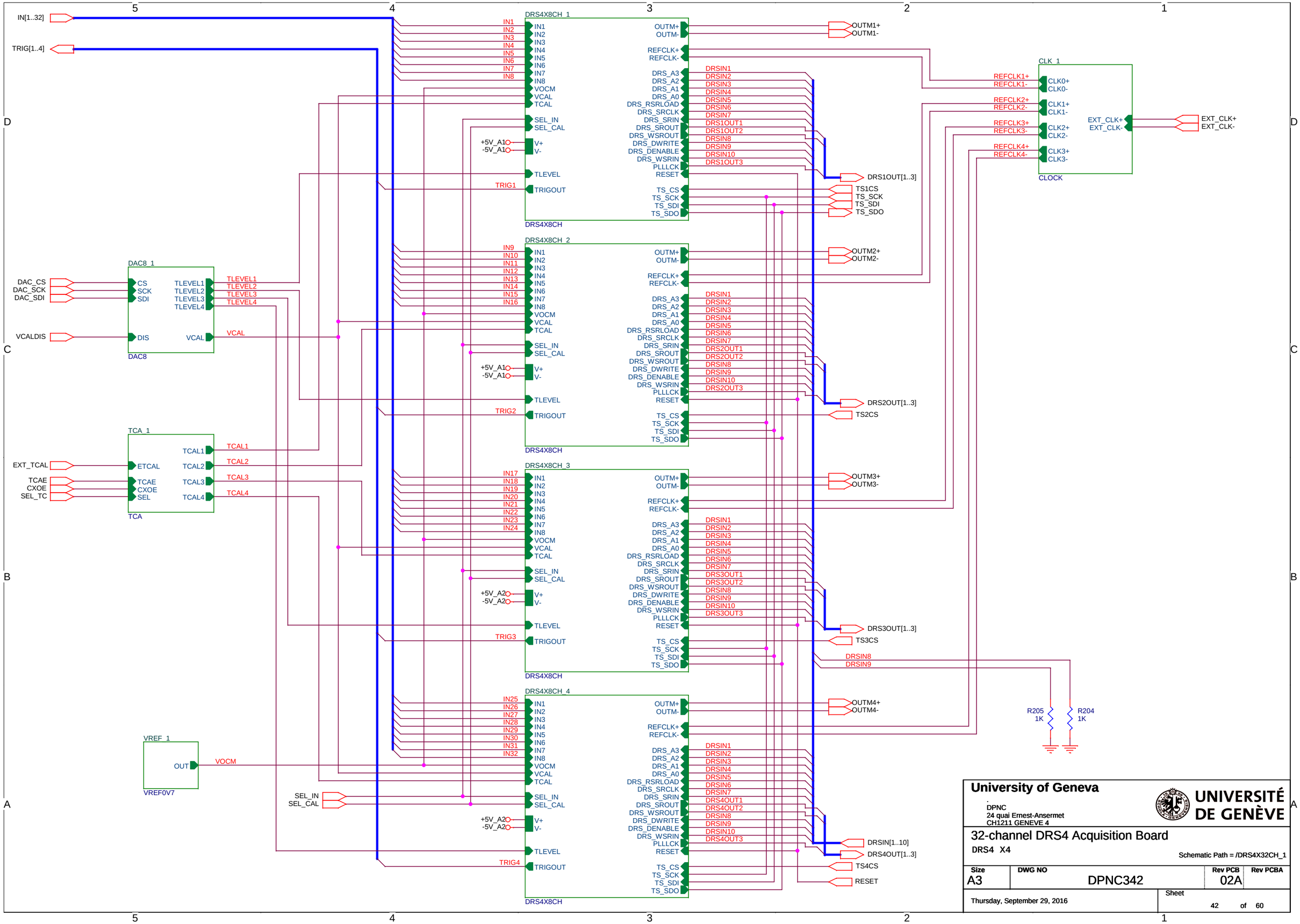
University of Geneva	UNIVERSITÉ DE GENÈVE
. DPNC 24 quai Ernest-Ansermet CH1211 GENEVE 4	
32-channel DRS4 Acquisition Board	
DRS4	Schematic Path = /DRS4X32CH_1/DRS4X8CH_2/DRS4_1
Size: A3 | DWG NO: DPNC342 | Rev PCB: 02A | Rev PCBA:	
Thursday, September 29, 2016	Sheet: 39 of 60

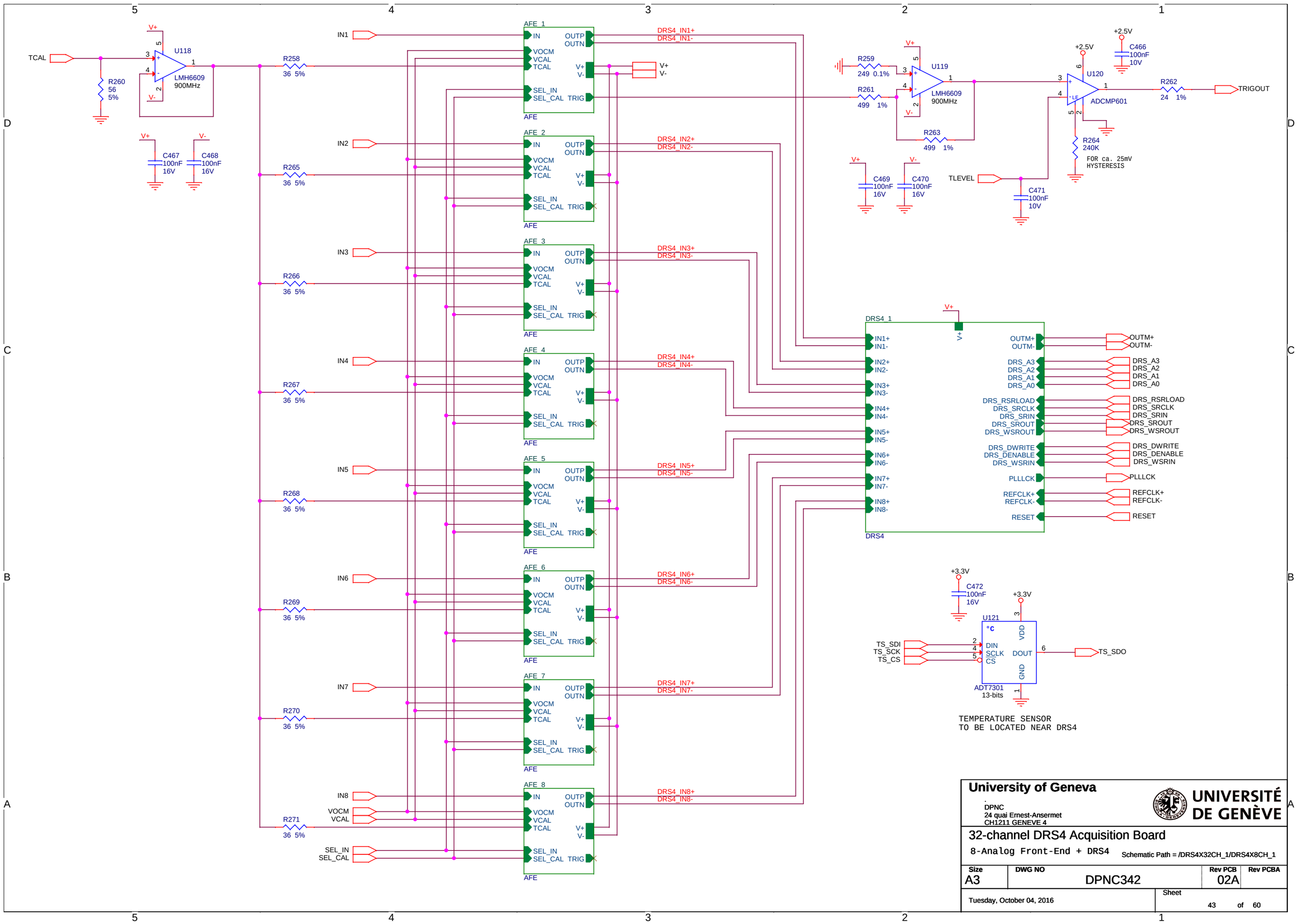


University of Geneva	UNIVERSITÉ DE GENÈVE
. DPNC 24 quai Ernest-Ansermet CH1211 GENEVE 4	
32-channel DRS4 Acquisition Board	
DRS4	Schematic Path = /DRS4X32CH_1/DRS4X8CH_3/DRS4_1
Size: A3	DWG NO: DPNC342
Rev PCB: 02A	Rev PCBA:
Thursday, September 29, 2016	Sheet: 40 of 60



University of Geneva	UNIVERSITÉ DE GENÈVE
. DPNC 24 quai Ernest-Ansermet CH1211 GENEVE 4	
32-channel DRS4 Acquisition Board	
DRS4	Schematic Path = /DRS4X32CH_1/DRS4X8CH_4/DRS4_1
Size A3 / **DWG NO** DPNC342 / **Rev PCB** 02A / **Rev PCBA**	
Thursday, September 29, 2016	**Sheet** 41 of 60


IN[1..32]
TRIG[1..4]
DRS4X8CH_1
DRS4X8CH_2
DRS4X8CH_3
DRS4X8CH_4
DRS4X8CH
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
VOCM
VCAL
TCAL
SEL_IN
SEL_CAL
+5V_A1
-5V_A1
+5V_A2
-5V_A2
V+
V-
TLEVEL
TRIGOUT
TRIG1
TRIG2
TRIG3
TRIG4
OUTM+
OUTM-
OUTM1+
OUTM1-
OUTM2+
OUTM2-
OUTM3+
OUTM3-
OUTM4+
OUTM4-
REFCLK+
REFCLK-
DRSIN1
DRSIN2
DRSIN3
DRSIN4
DRSIN5
DRSIN6
DRSIN7
DRSIN8
DRSIN9
DRSIN10
DRS_A3
DRS_A2
DRS_A1
DRS_A0
DRS_RSRLOAD
DRS_SRCLK
DRS_SRIN
DRS_SROUT
DRS_WSROUT
DRS_DWRITE
DRS_DENABLE
DRS_WSRIN
PLLLCK
RESET
DRS1OUT1
DRS1OUT2
DRS1OUT3
DRS2OUT1
DRS2OUT2
DRS2OUT3
DRS3OUT1
DRS3OUT2
DRS3OUT3
DRS4OUT1
DRS4OUT2
DRS4OUT3
DRS1OUT[1..3]
DRS2OUT[1..3]
DRS3OUT[1..3]
DRS4OUT[1..3]
TS_CS
TS_SCK
TS_SDI
TS_SDO
TS1CS
TS2CS
TS3CS
TS4CS
TS_SCK
TS_SDI
TS_SDO
DRSIN[1..10]
RESET
CLK_1
CLOCK
REFCLK1+
REFCLK1-
REFCLK2+
REFCLK2-
REFCLK3+
REFCLK3-
REFCLK4+
REFCLK4-
CLK0+
CLK0-
CLK1+
CLK1-
CLK2+
CLK2-
CLK3+
CLK3-
EXT_CLK+
EXT_CLK-
DAC8_1
DAC8
DAC_CS
DAC_SCK
DAC_SDI
CS
SCK
SDI
TLEVEL1
TLEVEL2
TLEVEL3
TLEVEL4
VCALDIS
DIS
VCAL
TCA_1
TCA
EXT_TCAL
ETCAL
TCAE
CXOE
SEL_TC
SEL
TCAL1
TCAL2
TCAL3
TCAL4
VREF_1
VREF0V7
OUT
VOCM
R205
1K
R204
1K
University of Geneva
.
DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4
UNIVERSITÉ DE GENÈVE
32-channel DRS4 Acquisition Board
DRS4 X4
Schematic Path = /DRS4X32CH_1
Size
A3
DWG NO
DPNC342
Rev PCB
02A
Rev PCBA
Thursday, September 29, 2016
Sheet
42 of 60



University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

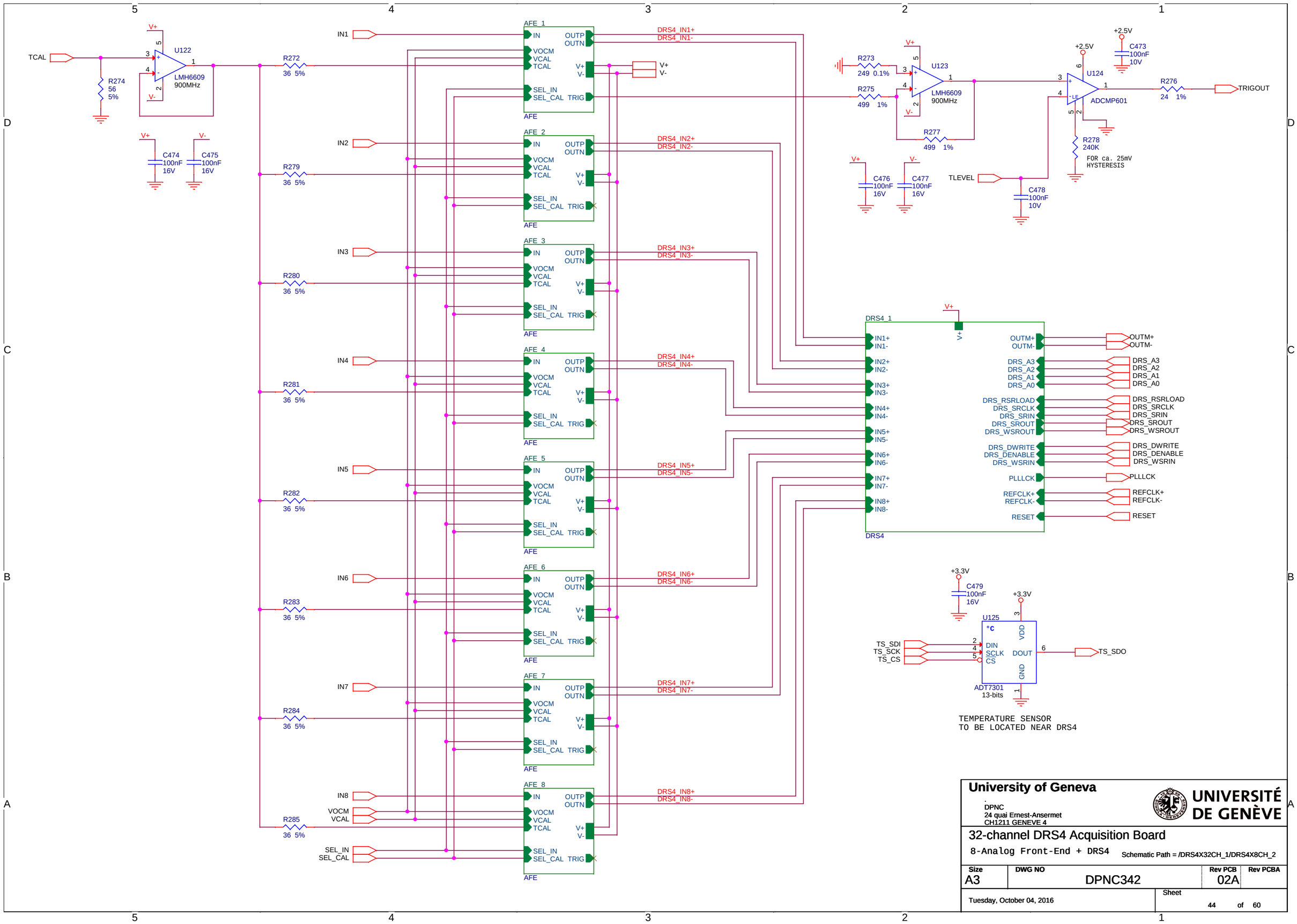
8-Analog Front-End + DRS4

Schematic Path = /DRS4X32CH_1/DRS4X8CH_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Tuesday, October 04, 2016

Sheet 43 of 60



University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

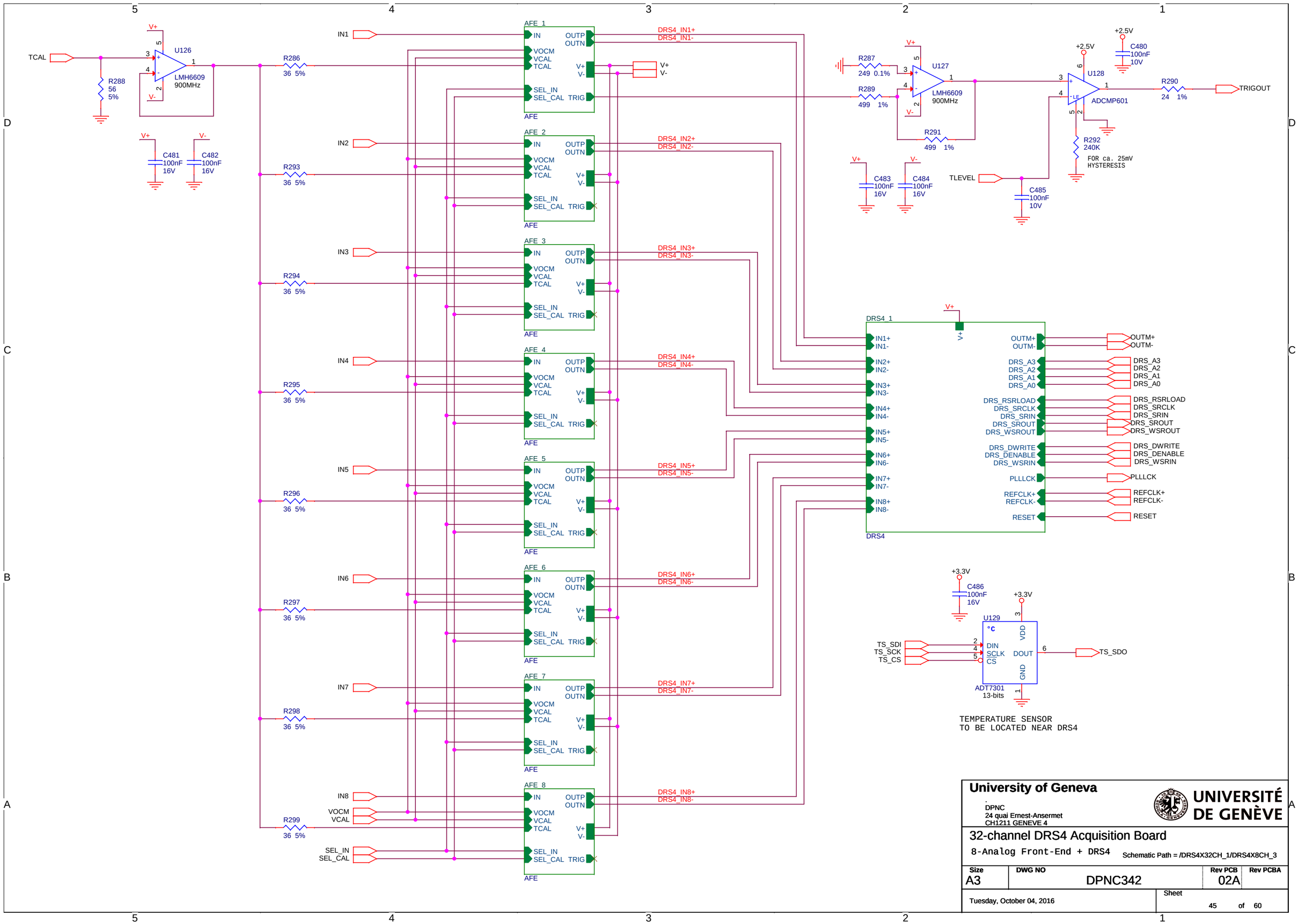
8-Analog Front-End + DRS4

Schematic Path = /DRS4X32CH_1/DRS4X8CH_2

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Tuesday, October 04, 2016

Sheet 44 of 60



University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

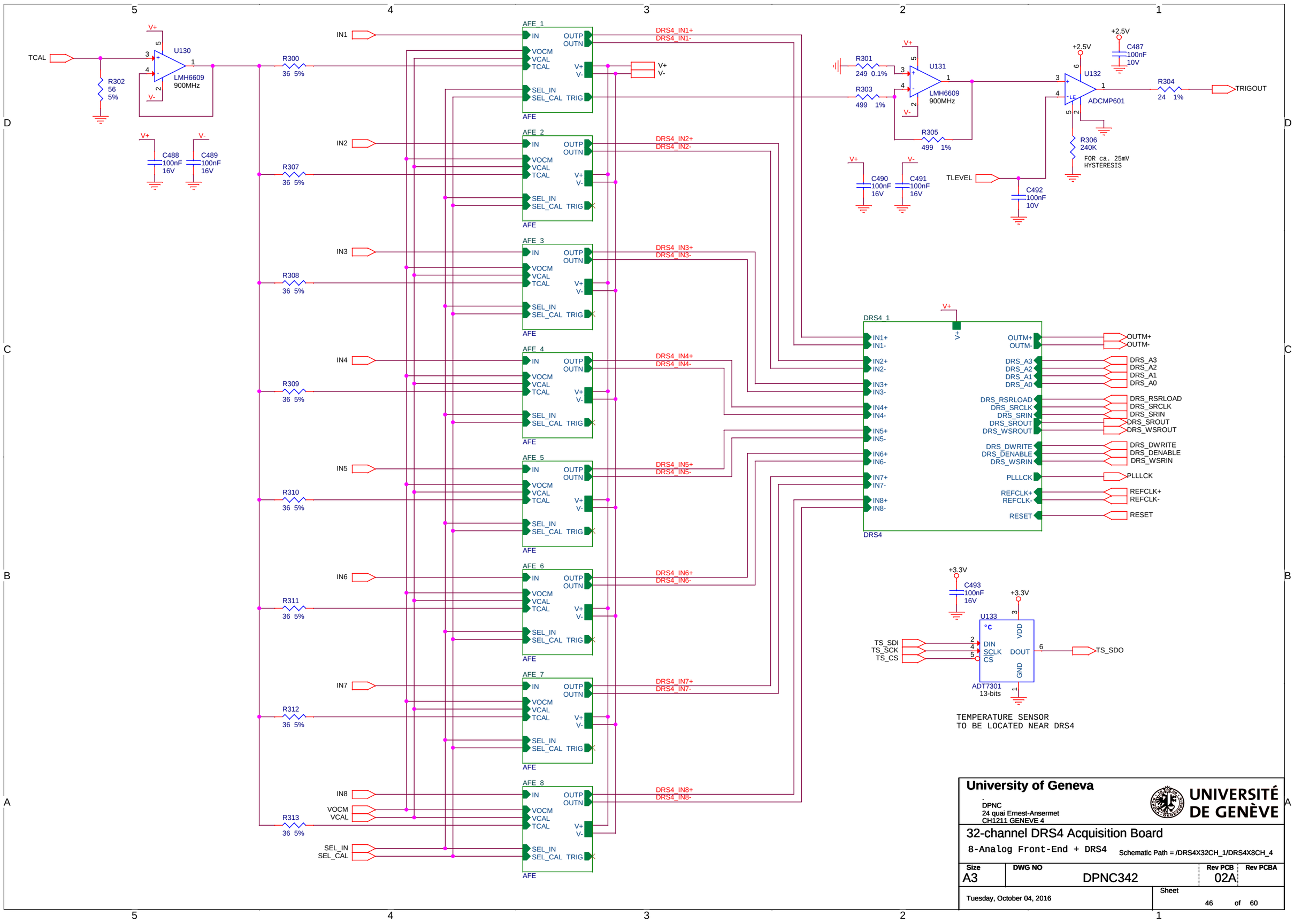
8-Analog Front-End + DRS4

Schematic Path = /DRS4X32CH_1/DRS4X8CH_3

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Tuesday, October 04, 2016

Sheet 45 of 60



University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

8-Analog Front-End + DRS4

Schematic Path = /DRS4X32CH_1/DRS4X8CH_4

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Tuesday, October 04, 2016

Sheet 46 of 60

DRSIN1	A3
DRSIN2	A2
DRSIN3	A1
DRSIN4	A0
DRSIN5	RSRLOAD
DRSIN6	SRCLK
DRSIN7	SRIN
DRSIN8	DWRITE
DRSIN9	DENABLE
DRSIN10	WSRIN
DRSxOUT1	SROUT
DRSxOUT2	WSROUT
DRSxOUT3	PLLLCK

DRSIN[1..10]

TRIG[1..4]

DRS1OUT[1..3]

DRS2OUT[1..3]

U1-2

TESTIO4	M8	IO_3B_M8/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B31N
TESTIO3	M9	IO_3B_M9/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B31P
ADC_CLK-	AB10	
ADC_CLK+	AB11	IO_3B_AB10/FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTN/DIFFIO_TX_B37N/DQ3B IO_3B_AB11/FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTP,FPLL_BL_FB/DIFFIO_TX_B37P/DQ3B
TS1CS	P7	IO_3A_P7/DIFFIO_TX_B8P/DQ1B
DRS1OUT1	AB6	IO_3B_AB6/DIFFIO_TX_B25N
VCALDIS	V9	IO_3B_V9/DIFFIO_RX_B26N/DQ2B
DRS1OUT3	AB5	IO_3B_AB5/DIFFIO_TX_B25P/DQ2B
DAC_SDI	V10	IO_3B_V10/DIFFIO_RX_B26P/DQ2B
TESTIO8	P8	IO_3B_P8/DIFFIO_RX_B27N/DQSN2B
DRS2OUT3	AA7	IO_3B_AA7/DIFFIO_TX_B28N/DQ2B
TESTIO6	N8	IO_3B_N8/DIFFIO_RX_B27P/DQS2B
DRS1OUT2	AB7	IO_3B_AB7/DIFFIO_TX_B28P
DRS2OUT1	AA8	IO_3B_AA8/DIFFIO_TX_B29N/DQ2B
TESTIO13	T9	IO_3B_T9/DIFFIO_RX_B30N/DQ2B
DRS2OUT2	AB8	IO_3B_AB8/DIFFIO_TX_B29P/DQ2B
DAC_CS	U10	IO_3B_U10/DIFFIO_RX_B30P/DQ2B
	AA10	IO_3B_AA10/DIFFIO_TX_B32N/DQ2B
	AA9	IO_3B_AA9/DIFFIO_TX_B32P/DQ2B
TRIG2	Y10	IO_3B_Y10/DIFFIO_TX_B33N
TESTIO14	T10	IO_3B_T10/DIFFIO_RX_B34N/DQ3B
TRIG1	Y9	IO_3B_Y9/DIFFIO_TX_B33P/DQ3B
TESTIO10	R9	IO_3B_R9/DIFFIO_RX_B34P/DQ3B
DAC_SCK	U11	IO_3B_U11/DIFFIO_RX_B35N/DQSN3B
TESTIO12	R12	IO_3B_R12/DIFFIO_TX_B36N/DQ3B
	U12	IO_3B_U12/DIFFIO_RX_B35P/DQS3B
TESTIO1	P12	IO_3B_P12/DIFFIO_TX_B36P
TESTIO9	R10	IO_3B_R10/DIFFIO_RX_B38N/DQ3B
TESTIO11	R11	IO_3B_R11/DIFFIO_RX_B38P/DQ3B
RESETOUT	Y11	IO_3B_Y11/DIFFIO_TX_B40N/DQ3B
	AA12	IO_3B_AA12/DIFFIO_TX_B40P/DQ3B

5CEBA7F23
149.5K LE
C8

Cyclone V 5CEBA7F23
VERSION : 1.1
PAGE : 2 of 10
DATE : JUN_ 2012

U1-3

ADC_OUT1-	V13	IO_4A_V13/DIFFIO_RX_B42N/DQ4B
	AB12	IO_4A_AB12/DIFFIO_TX_B41P/DQ4B
ADC_OUT1+	U13	IO_4A_U13/DIFFIO_RX_B42P/DQ4B
TESTIO15	T12	IO_4A_T12/DIFFIO_RX_B43N/DQSN4B
	AA14	IO_4A_AA14/DIFFIO_TX_B44N/DQ4B
	T13	IO_4A_T13/DIFFIO_RX_B43P/DQS4B
	AA13	IO_4A_AA13/DIFFIO_TX_B44P
	AB15	IO_4A_AB15/DIFFIO_TX_B45N/DQ4B
ADC_OUT2-	Y14	IO_4A_Y14/DIFFIO_RX_B46N/DQ4B
	AA15	IO_4A_AA15/DIFFIO_TX_B45P/DQ4B
ADC_OUT2+	Y15	IO_4A_Y15/DIFFIO_RX_B46P/DQ4B
	AB17	IO_4A_AB17/DIFFIO_TX_B48N/DQ4B
	AB18	IO_4A_AB18/DIFFIO_TX_B48P/DQ4B
DRSIN4	AB20	IO_4A_AB20/DIFFIO_TX_B49N
ADC_OUT3-	Y16	IO_4A_Y16/DIFFIO_RX_B50N/DQ5B
DRSIN5	AB21	IO_4A_AB21/DIFFIO_TX_B49P/DQ5B
ADC_OUT3+	Y17	IO_4A_Y17/DIFFIO_RX_B50P/DQ5B
	T14	IO_4A_T14/DIFFIO_RX_B51N/DQSN5B
	AA17	IO_4A_AA17/DIFFIO_TX_B52N/DQ5B
	U15	IO_4A_U15/DIFFIO_RX_B51P/DQS5B
	AA18	IO_4A_AA18/DIFFIO_TX_B52P
DRSIN3	AA19	IO_4A_AA19/DIFFIO_TX_B53N/DQ5B
DRS4OUT1	V20	IO_4A_V20/DIFFIO_RX_B54N/DQ5B
DRSIN9	AA20	IO_4A_AA20/DIFFIO_TX_B53P/DQ5B
DRSIN1	W19	IO_4A_W19/DIFFIO_RX_B54P/DQ5B
DRSIN6	AB22	IO_4A_AB22/DIFFIO_TX_B56N/DQ5B
DRSIN7	AA22	IO_4A_AA22/DIFFIO_TX_B56P/DQ5B
DRS3OUT2	Y22	IO_4A_Y22/DIFFIO_TX_B57N
DRSIN10	Y20	IO_4A_Y20/DIFFIO_RX_B58N/DQ6B
DRS3OUT1	W22	IO_4A_W22/DIFFIO_TX_B57P/DQ6B
DRSIN2	Y19	IO_4A_Y19/DIFFIO_RX_B58P/DQ6B
TESTIO0	P14	IO_4A_P14/DIFFIO_RX_B59N/DQSN6B
DRSIN8	Y21	IO_4A_Y21/DIFFIO_TX_B60N/DQ6B
TESTIO2	R14	IO_4A_R14/DIFFIO_RX_B59P/DQS6B
DRS3OUT3	W21	IO_4A_W21/DIFFIO_TX_B60P
TRIG4	U22	IO_4A_U22/DIFFIO_TX_B61N/DQ6B
DRS4OUT3	V19	IO_4A_V19/DIFFIO_RX_B62N/DQ6B
DRS4OUT2	V21	IO_4A_V21/DIFFIO_TX_B61P/DQ6B
	V18	IO_4A_V18/DIFFIO_RX_B62P/DQ6B
	U16	IO_4A_U16/DIFFIO_RX_B63N
ADC_OUT4-	U21	IO_4A_U21/DIFFIO_TX_B64N/DQ6B
TRIG3	U17	IO_4A_U17/DIFFIO_RX_B63P
ADC_OUT4+	U20	IO_4A_U20/DIFFIO_TX_B64P/DQ6B

5CEBA7F23
149.5K LE
C8

Cyclone V 5CEBA7F23
VERSION : 1.1
PAGE : 3 of 10
DATE : JUN_ 2012

DRS4OUT[1..3]

DRS3OUT[1..3]

J11

HE10
M/ST
P2.54

		2	1		
	+2.5V	4	3	+2.5V	
TP24	1	TESTIO1 6	5 TESTIO0	1	TP26
TP25	1	TESTIO3 8	7 TESTIO2	1	TP27
TP30	1	10	9 TESTIO4	1	TP31
TESTIO5					
TESTIO7					
TP28	1	12	11 TESTIO6	1	TP29
TP32	1	TESTIO9 14	13 TESTIO8	1	TP33
TP36	1	TESTIO11 16	15 TESTIO10	1	TP37
TP34	1	TESTIO13 18	17 TESTIO12	1	TP35
TP38	1	TESTIO15 20	19 TESTIO14	1	TP39

University of Geneva

.
DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

FPGA - DRS4 + TRIG + ADC (1/4)

Schematic Path = /FPGA_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 47 of 60

DQ[31..0]

RN15 22
DQ0 5 4 DQ0_R
DQ1 6 3 DQ1_R
DQ2 7 2 DQ2_R
DQ3 8 1 DQ3_R

RN16 22
DQ4 5 4 DQ4_R
DQ5 6 3 DQ5_R
DQ6 7 2 DQ6_R
DQ7 8 1 DQ7_R

RN17 22
DQ8 5 4 DQ8_R
DQ9 6 3 DQ9_R
DQ10 7 2 DQ10_R
DQ11 8 1 DQ11_R

RN18 22
DQ12 5 4 DQ12_R
DQ13 6 3 DQ13_R
DQ14 7 2 DQ14_R
DQ15 8 1 DQ15_R

RN19 22
DQ16 5 4 DQ16_R
DQ17 6 3 DQ17_R
DQ18 7 2 DQ18_R
DQ19 8 1 DQ19_R

RN20 22
DQ20 5 4 DQ20_R
DQ21 6 3 DQ21_R
DQ22 7 2 DQ22_R
DQ23 8 1 DQ23_R

RN21 22
DQ24 5 4 DQ24_R
DQ25 6 3 DQ25_R
DQ26 7 2 DQ26_R
DQ27 8 1 DQ27_R

RN22 22
DQ28 5 4 DQ28_R
DQ29 6 3 DQ29_R
DQ30 7 2 DQ30_R
DQ31 8 1 DQ31_R

CLK_USB
R399
22 5%

U1-4

DQ11_R M22 IO_5B_M22/FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTP,FPLL_BR_FB/DIFFIO_TX_R36P/DQ2R
L22 IO_5B_L22/FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTN/DIFFIO_TX_R36N/DQ2R

BOARDID9 T15 IO_5A_T15/DIFFIO_RX_R4P/DQ1R
BOARDID5 R15 IO_5A_R15/DIFFIO_RX_R4N/DQ1R
BOARDID1 P19 IO_5A_P19/DIFFIO_TX_R7P/DQ1R
BOARDID3 P16 IO_5A_P16/DIFFIO_RX_R8P/DQ1R
BOARDID2 P18 IO_5A_P18/DIFFIO_TX_R7N
BOARDID0 P17 IO_5A_P17/DIFFIO_RX_R8N/DQ1R

DQ4_R N20 IO_5B_N20/DIFFIO_TX_R34P/DQ2R
DQ3_R N21 IO_5B_N21/DIFFIO_TX_R34N/DQ2R
DQ2_R N19 IO_5B_N19/DIFFIO_RX_R35P/DQ2R
DQ0_R M18 IO_5B_M18/DIFFIO_RX_R35N/DQ2R
DQ19_R K17 IO_5B_K17/DIFFIO_RX_R37P/DQS2R
DQ6_R M20 IO_5B_M20/DIFFIO_TX_R38P
DQ13_R L17 IO_5B_L17/DIFFIO_RX_R37N/DQSN2R
DQ1_R M21 IO_5B_M21/DIFFIO_TX_R38N/DQ2R
DQ12_R L19 IO_5B_L19/DIFFIO_RX_R39P/DQ2R
DQ14_R K21 IO_5B_K21/DIFFIO_TX_R40P/DQ2R
DQ10_R L18 IO_5B_L18/DIFFIO_RX_R39N/DQ2R
DQ9_R K22 IO_5B_K22/DIFFIO_TX_R40N

5CEBA7F23
149.5K LE
C8

Cyclone V 5CEBA7F23
VERSION : 1.1
PAGE : 4 of 10
DATE : JUN_ 2012

U1-5

** NO CONNECT BECAUSE OF DEVICE MIGRATION **

H21 IO_7A_H21/DIFFIO_RX_T1P
E21 IO_7A_E21/DIFFIO_TX_T2P/DQ1T
G21 IO_7A_G21/DIFFIO_RX_T1N
D21 IO_7A_D21/DIFFIO_TX_T2N/DQ1T
E19 IO_7A_E19/DIFFIO_RX_T3P/DQ1T
C20 IO_7A_C20/DIFFIO_TX_T4P/DQ1T
D19 IO_7A_D19/DIFFIO_RX_T3N/DQ1T
B20 IO_7A_B20/DIFFIO_TX_T4N/DQ1T
J21 IO_7A_J21/DIFFIO_RX_T5P/DQS1T
B18 IO_7A_B18/DIFFIO_TX_T6P
J22 IO_7A_J22/DIFFIO_RX_T5N/DQSN1T
B17 IO_7A_B17/DIFFIO_TX_T6N/DQ1T
C21 IO_7A_C21/DIFFIO_RX_T7P/DQ1T
G22 IO_7A_G22/DIFFIO_TX_T8P/DQ1T
B21 IO_7A_B21/DIFFIO_TX_T7N/DQ1T
F22 IO_7A_F22/DIFFIO_TX_T8N
G20 IO_7A_G20/DIFFIO_RX_T9P
E22 IO_7A_E22/DIFFIO_TX_T10P/DQ2T
H20 IO_7A_H20/DIFFIO_RX_T9N
D22 IO_7A_D22/DIFFIO_TX_T10N/DQ2T
C19 IO_7A_C19/DIFFIO_RX_T11P/DQ2T
B22 IO_7A_B22/DIFFIO_TX_T12P/DQ2T
C18 IO_7A_C18/DIFFIO_RX_T11N/DQ2T
A22 IO_7A_A22/DIFFIO_TX_T12N/DQ2T
F19 IO_7A_F19/DIFFIO_RX_T13P/DQS2T
E20 IO_7A_E20/DIFFIO_TX_T14P
F18 IO_7A_F18/DIFFIO_RX_T13N/DQSN2T
F20 IO_7A_F20/DIFFIO_TX_T14N/DQ2T
A18 IO_7A_A18/DIFFIO_RX_T15P/DQ2T
A20 IO_7A_A20/DIFFIO_TX_T16P/DQ2T
A17 IO_7A_A17/DIFFIO_RX_T15N/DQ2T
A19 IO_7A_A19/DIFFIO_TX_T16N
K20 IO_7A_K20/DIFFIO_RX_T17P
B16 IO_7A_B16/DIFFIO_TX_T18P/DQ3T
K19 IO_7A_K19/DIFFIO_RX_T17N
C16 IO_7A_C16/DIFFIO_TX_T18N/DQ3T
D17 IO_7A_D17/DIFFIO_RX_T19P/DQ3T
G17 IO_7A_G17/DIFFIO_TX_T20P/DQ3T
E16 IO_7A_E16/DIFFIO_RX_T19N/DQ3T
G16 IO_7A_G16/DIFFIO_TX_T20N/DQ3T
G18 IO_7A_G18/DIFFIO_RX_T21P/DQS3T
J19 IO_7A_J19/DIFFIO_TX_T22P
H18 IO_7A_H18/DIFFIO_RX_T21N/DQSN3T
J18 IO_7A_J18/DIFFIO_TX_T22N/DQ3T
E15 IO_7A_E15/DIFFIO_RX_T23P/DQ3T
A15 IO_7A_A15/DIFFIO_TX_T24P/DQ3T
F15 IO_7A_F15/DIFFIO_RX_T23N/DQ3T
A14 IO_7A_A14/DIFFIO_TX_T24N
J17 IO_7A_J17/DIFFIO_TX_T26P/DQ4T
K16 IO_7A_K16/DIFFIO_TX_T26N/DQ4T
C15 IO_7A_C15/DIFFIO_RX_T27P/DQ4T
G15 IO_7A_G15/DIFFIO_TX_T28P/DQ4T
B15 IO_7A_B15/DIFFIO_RX_T27N/DQ4T
F14 IO_7A_F14/DIFFIO_TX_T28N/DQ4T
H14 IO_7A_H14/DIFFIO_RX_T29P/DQS4T
B13 IO_7A_B13/DIFFIO_TX_T30P
J13 IO_7A_J13/DIFFIO_RX_T29N/DQSN4T
A13 IO_7A_A13/DIFFIO_TX_T30N/DQ4T
E14 IO_7A_E14/DIFFIO_RX_T31P/DQ4T
J11 IO_7A_J11/DIFFIO_TX_T32P/DQ4T
F13 IO_7A_F13/DIFFIO_RX_T31N/DQ4T
H10 IO_7A_H10/DIFFIO_TX_T32N
G11 IO_7A_G11/DIFFIO_TX_T34P/DQ5T
F12 IO_7A_F12/DIFFIO_TX_T34N/DQ5T
D13 IO_7A_D13/DIFFIO_RX_T35P/DQ5T
B12 IO_7A_B12/DIFFIO_TX_T36P/DQ5T
C13 IO_7A_C13/DIFFIO_RX_T35N/DQ5T
A12 IO_7A_A12/DIFFIO_TX_T36N/DQ5T
H11 IO_7A_H11/DIFFIO_RX_T37P/DQS5T
L8 IO_7A_L8/DIFFIO_TX_T38P
G12 IO_7A_G12/DIFFIO_RX_T37N/DQSN5T
K9 IO_7A_K9/DIFFIO_TX_T38N/DQ5T
D12 IO_7A_D12/DIFFIO_RX_T39P/DQ5T
C11 IO_7A_C11/DIFFIO_TX_T40P/DQ5T
E12 IO_7A_E12/DIFFIO_RX_T39N/DQ5T

5CEBA7F23
149.5K LE
C8

Cyclone V 5CEBA7F23
VERSION : 1.1
PAGE : 5 of 10
DATE : JUN_ 2012

DQ8_R
DQ15_R
CTL6_R
DQ30_R
DQ28_R
DQ25_R
DQ24_R
DQ18_R
DQ22_R
DQ21_R
DQ27_R
CTL8_R
DQ26_R
CTL9_R
DQ17_R
DQ20_R
SLRDn_R
DQ29_R
PKTENDn_R
SLWRn_R
DQ31_R
CTL10_R
UC_UART_CTSn_R
SLCSn_R
LED4
SLOEn_R
STAT2
LED6
UC_RESETn
A1_R
UC_UART_RX_R
A0_R
UC_UART_RTSn
LED5
BUSY_FP
LED7
TRIGIN_FP
GPIO51_R
GPIO50_R
INTn

FLAGB
FLAGA

RN8 22
CTL6 5 4
CTL8 6 3
CTL9 7 2
CTL10 8 1

RN13 22
SLRDn 5 4
SLWRn 6 3
SLCSn 7 2
SLOEn 8 1

RN23 22
PKTENDn 5 4
UC_UART_CTSn 6 3
UC_UART_RX 7 2
8 1

A[1..0]
RN14 22
A1 5 4
A0 6 3
GPIO51 7 2
GPIO50 8 1

STAT[1..4]
STAT1

TESTIO7
TESTIO5

U1-7

ADC_FCO- P9 CLK1N_P9/DIFFIO_RX_B39N
ADC_FCO+ N9 CLK1P_N9/DIFFIO_RX_B39P
ADC_DCO- V14 CLK2N_V14/DIFFIO_RX_B47N
ADC_DCO+ V15 CLK2P_V15/DIFFIO_RX_B47P
V16 CLK3N_V16/DIFFIO_RX_B55N
W16 CLK3P_W16/DIFFIO_RX_B55P
DQ5_R N16 CLK6P_N16/DIFFIO_RX_R33P
DQ7_R M16 CLK6N_M16/DIFFIO_RX_R33N
DQ16_R H16 CLK11P_H16/DIFFIO_RX_T25P
DQ23_R H15 CLK11N_H15/DIFFIO_RX_T25N
H13 CLK10P_H13/DIFFIO_RX_T33P
STAT3 G13 CLK10N_G13/DIFFIO_RX_T33N
CLK40M G10 CLK9P_G10/DIFFIO_RX_T41P
TRIGIN3 F10 CLK9N_F10/DIFFIO_RX_T41N

AB13 RZQ_0_AB13/DIFFIO_TX_B41N
BOARDID8 T19 RZQ_1_T19/DIFFIO_TX_R1P/DQ1R
UC_UART_TX B11 RZQ_2_B11/DIFFIO_TX_T40N

Y7 VREFB3AN0
Y12 VREFB3BN0
AB16 VREFB4AN0
R20 VREFB5AN0
L20 VREFB5BN0
C14 VREFB7AN0
B8 VREFB8AN0

5CEBA7F23
149.5K LE
C8

Cyclone V 5CEBA7F23
VERSION : 1.1
PAGE : 7 of 10
DATE : JUN_ 2012

Y2
EN VCC
GND OUT
40MHz
25PPM
+3.3V
R314
22 5%

+3.3V
C494
10nF
10%
16V

LED7 FW UPDATE
LED6 TIMING CAL
LED5 DATA TRANSFER
LED4 TRIG IN

R315 200 5%
R316 200 5%
R317 200 5%
R318 200 5%
D34 G1/G2
D35 G1/G2

FRONT PANEL

University of Geneva

.
DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

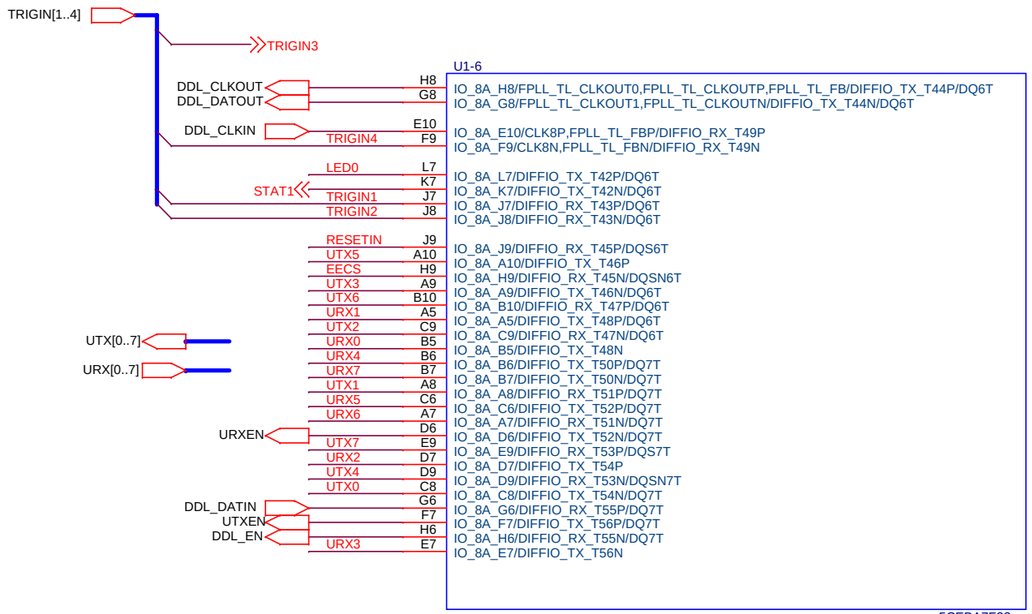
FPGA - MCU + CLOCKS (2/4)

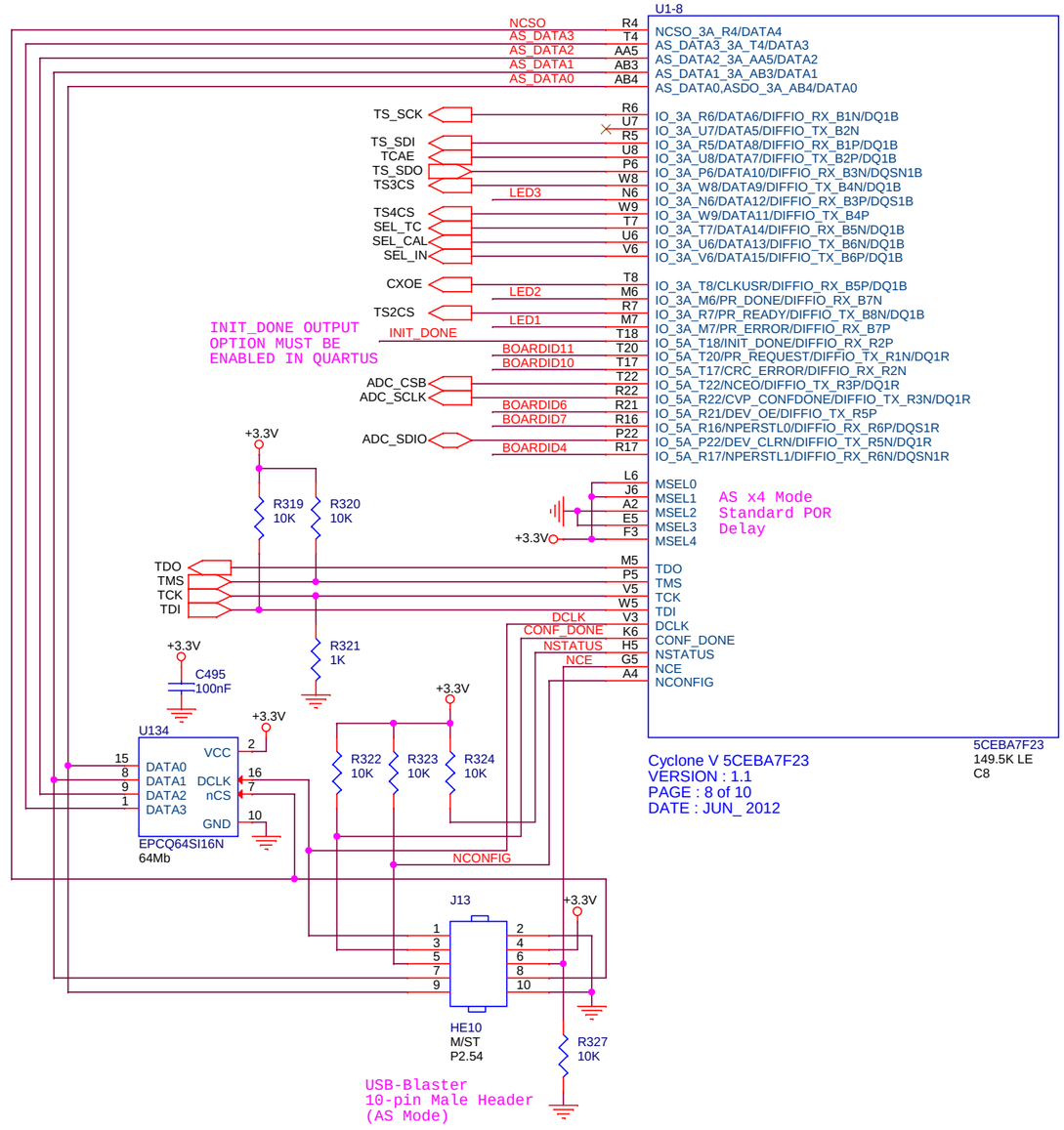
Schematic Path = /FPGA_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

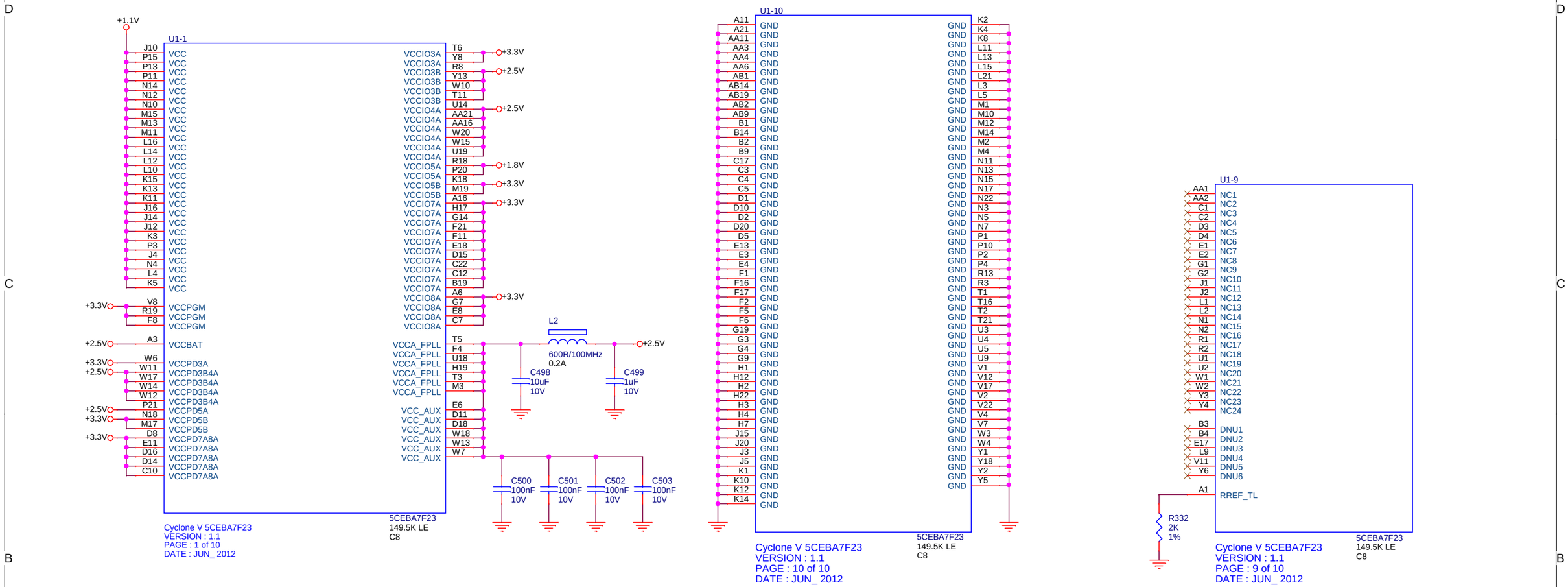
Thursday, September 29, 2016

Sheet 48 of 60



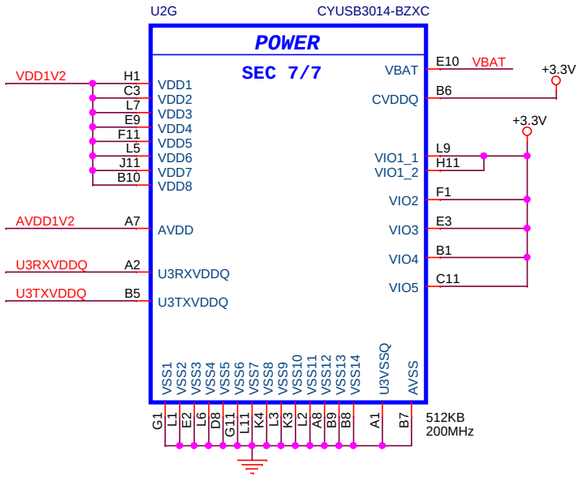


University of Geneva	UNIVERSITÉ DE GENÈVE
DPNC 24 quai Ernest-Ansermet CH1211 GENEVE 4	
32-channel DRS4 Acquisition Board	
FPGA - DDL + USER IO + EEPROM + CONFIG BOARDID + RESET + LEDS (3/4)	Schematic Path = /FPGA_1
Size: A3	DWG NO: DPNC342
Rev PCB: 02A	Rev PCBA:
Thursday, September 29, 2016	Sheet: 49 of 60

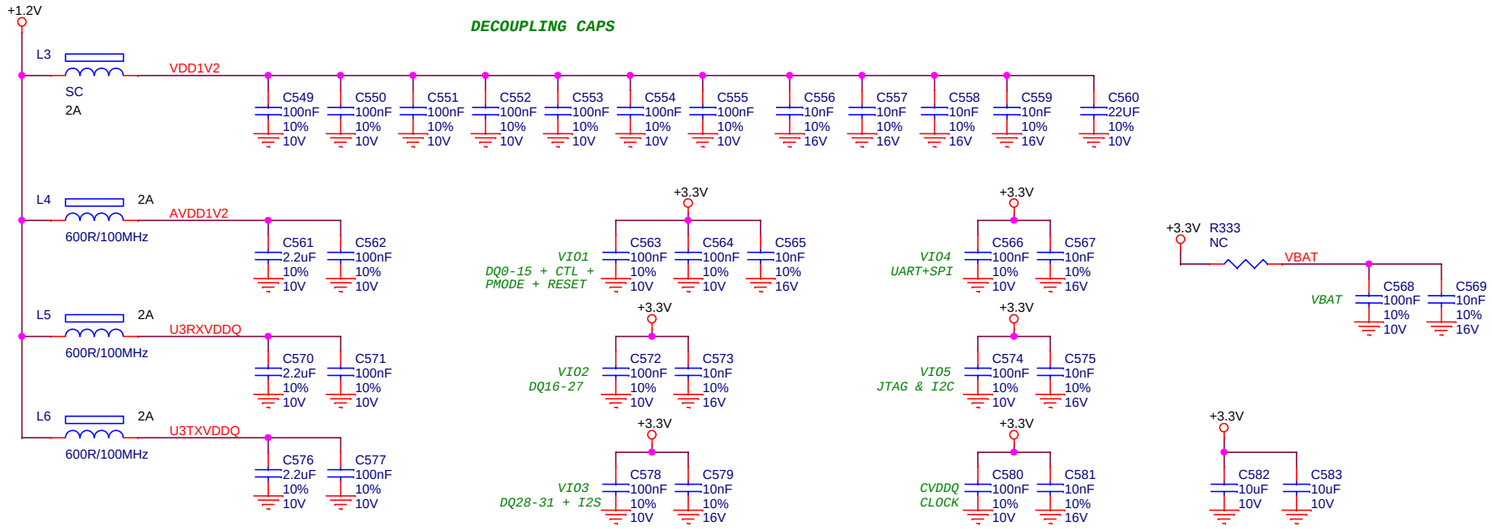


University of Geneva	UNIVERSITÉ DE GENÈVE
DPNC 24 quai Ernest-Ansermet CH1211 GENEVE 4	
32-channel DRS4 Acquisition Board	
FPGA - POWER SUPPLY + NC/DNU (4/4)	Schematic Path = /FPGA_1
Size: A3	DWG NO: DPNC342
Rev PCB: 02A	Rev PCBA:
Thursday, September 29, 2016	Sheet: 50 of 60

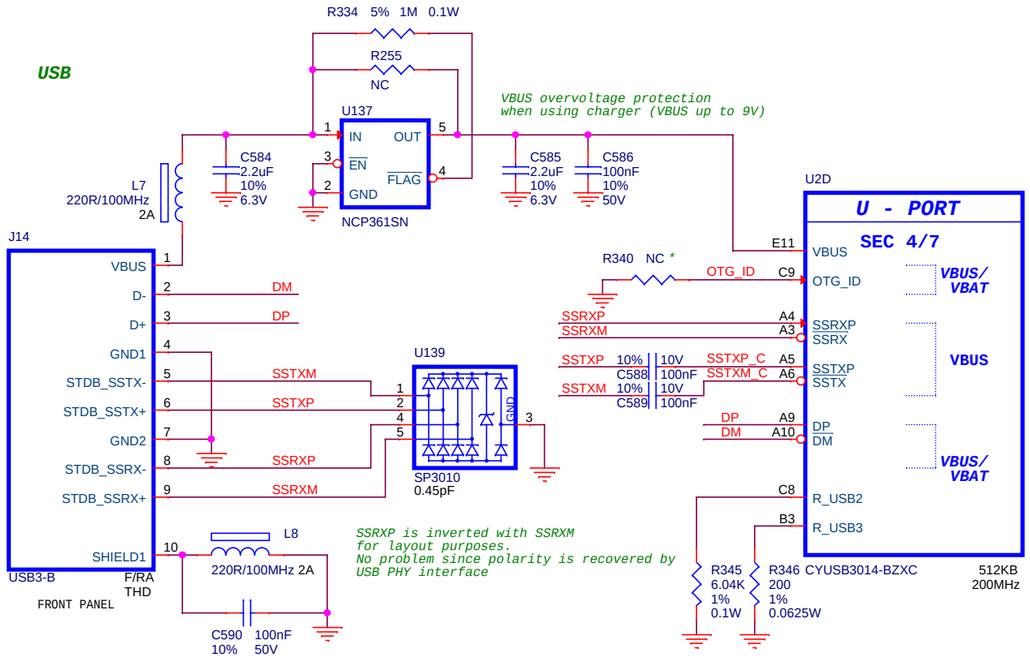
POWER SUPPLIES



DECOUPLING CAPS



USB



JTAG/EEPROM

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

MICROCONTROLLER (1/2)

Schematic Path = /MICRO_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 51 of 60

FIFO INTERFACE

U2A

P - PORT

SEC 1/7

VIO1

3V3 on VIO1

DQ0	F10	DQ_UC0	RN1 22 5 4 DQ0
DQ1	F9	DQ_UC1	6 3 DQ1
DQ2	F7	DQ_UC2	7 2 DQ2
DQ3	G10	DQ_UC3	8 1 DQ3
DQ4	G9	DQ_UC4	
DQ5	F8	DQ_UC5	RN3 22 5 4 DQ4
DQ6	H10	DQ_UC6	6 3 DQ5
DQ7	H9	DQ_UC7	7 2 DQ6
DQ8	J10	DQ_UC8	8 1 DQ7
DQ9	J9	DQ_UC9	RN5 22 5 4 DQ8
DQ10	K11	DQ_UC10	6 3 DQ9
DQ11	L10	DQ_UC11	7 2 DQ10
DQ12	K10	DQ_UC12	8 1 DQ11
DQ13	K9	DQ_UC13	RN7 22 5 4 DQ12
DQ14	J8	DQ_UC14	6 3 DQ13
DQ15	G8	DQ_UC15	7 2 DQ14
			8 1 DQ15
PCLK/CLK	J6		→ CLK
CTL0/SLCS	K8		→ SLCSn
CTL1/SLWR	K7		→ SLWRn
CTL2/SLOE	J7		→ SLOEn
CTL3/SLRD	H7		→ SLRDn
CTL4/FLAGA	G7	FLAGA_UC	RN9 22 5 4 → FLAGB
CTL5/FLAGB	G6	FLAGB_UC	6 3 → FLAGA
CTL6/GPIO	K6	CTL6_UC	7 2
CTL7/PKTEND	H8		8 1 → PKTENDn
CTL8/GPIO	G5	CTL8_UC	RN11 22 5 4 → CTL6
CTL9/GPIO	H6	CTL9_UC	6 3 → CTL8
CTL10/GPIO	K5	CTL10_UC	7 2 → CTL9
CTL11/A1	J5		8 1 → CTL10
CTL12/A0	H5		→ A1 → A0
PMODE0	G4	PMODE0	
PMODE1	H4	PMODE1	
PMODE2	L4	PMODE2	
INT/CTL15	L8		→ INTn
RESET	C5		→ RESETn

DQ[31..0]

A[1..0]

+3.3V

R356 10K 5%

R357 10K

CYUSB3014-BZXC 512KB 200MHz

U2B

S0 - PORT

SEC 2/7

VIO2

3V3 on VIO2

DQ16	K2	DQ_UC16	RN2 22 5 4 DQ16
DQ17	J4	DQ_UC17	6 3 DQ17
DQ18	K1	DQ_UC18	7 2 DQ18
DQ19	J2	DQ_UC19	8 1 DQ19
DQ20	J3	DQ_UC20	
DQ21	J1	DQ_UC21	RN4 22 5 4 DQ20
DQ22	H2	DQ_UC22	6 3 DQ21
DQ23	H3	DQ_UC23	7 2 DQ22
DQ24	F4	DQ_UC24	8 1 DQ23
DQ25	G2	DQ_UC25	RN6 22 5 4 DQ24
DQ26	G3	DQ_UC26	6 3 DQ25
DQ27	F3	DQ_UC27	7 2 DQ26
			8 1 DQ27
GPIO45	F2		

+3.3V

R354 200 1%

D42 Y 5MCD

Q2 2N7002 0.1A 60V

R355 100K 5%

CYUSB3014-BZXC 512KB 200MHz

U2C

S1 - PORT

SEC 3/7

VIO3

3V3 on VIO3

VIO4

3V3 on VIO4

DQ28	F5	DQ_UC28	RN10 22 5 4 DQ28
DQ29	E1	DQ_UC29	6 3 DQ29
DQ30	E5	DQ_UC30	7 2 DQ30
DQ31	E4	DQ_UC31	8 1 DQ31
I2S-CLK/GPIO50	D1		RN12 22 5 4 GPIO50
I2S-SD/GPIO51	D2		6 3 GPIO51
I2S-WS/GPIO52	D3	1 TP41	7 2 UART_RTSn
UART-RTS/SPI-SCK/GPIO53	D4		8 1 UART_TX
UART-CTS/SPI-SSN/I2S_CLK/GPIO54	C1		→ UART_CTSn
UART-TX/SPI-MISO/I2S_SD/GPIO55	C2		
UART-RX/SPI-MOSI/I2S_WS/GPIO56	D5		→ UART_RX
I2S-MCLK/GPIO57	C4	1 TP42	

CYUSB3014-BZXC 512KB 200MHz

CLOCK

U2E

XTAL / CLK

SEC 5/7

CVDDQ

3V3 on CVDDQ

19.2MHz crystal configuration

FSLC0	B2	
FSLC1	B4	
FSLC2	E6	
XTALIN	C6	Y3 19M2 30PPM
XTALOUT	C7	
CLKIN	D7	C591 12pF 5%
CLKIN_32	D6	C592 12pF 5%

CYUSB3014-BZXC 512KB 200MHz

3V3 on VIO1

+3.3V +3.3V +3.3V

R358 NC 5%

R359 10K 5%

R360 NC 5%

PMODE0

PMODE1

PMODE2

R361 NC

R362 NC

R363 NC

I2C, on failure USB

BOOT MODE

PMODE[2:0] Pins			Boot Option
PMODE[2]	PMODE[1]	PMODE[0]	
Z	0	0	Sync ADMUX (16-bit)
Z	0	1	Async ADMUX (16-bit)
Z	0	Z	Async SRAM (16-bit)
Z	1	1	USB Boot
1	Z	Z	I²C
Z	1	Z	I²C; On Failure, USB Boot is Enabled
0	Z	1	SPI; On Failure, USB Boot is Enabled

University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

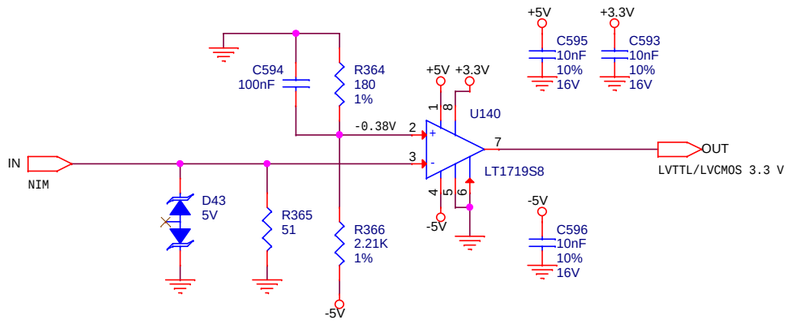
MICROCONTROLLER (2/2)

Schematic Path = /MICRO_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 52 of 60



University of Geneva

.
DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

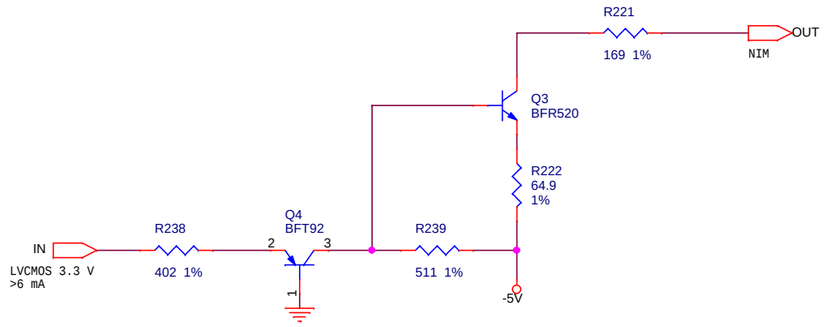
NIM_TO_LVTTL

Schematic Path = /NTL_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 53 of 60



University of Geneva

.
DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

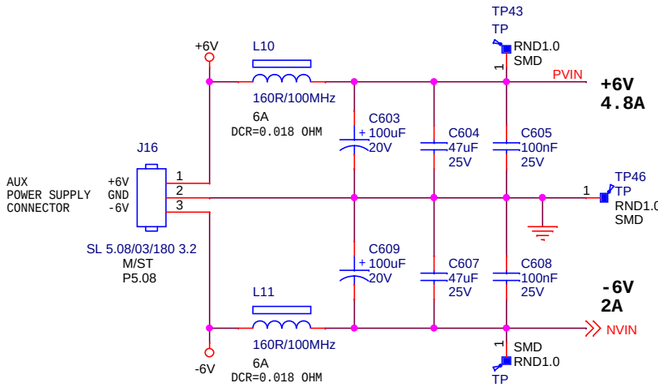
LVTTL_TO_NIM

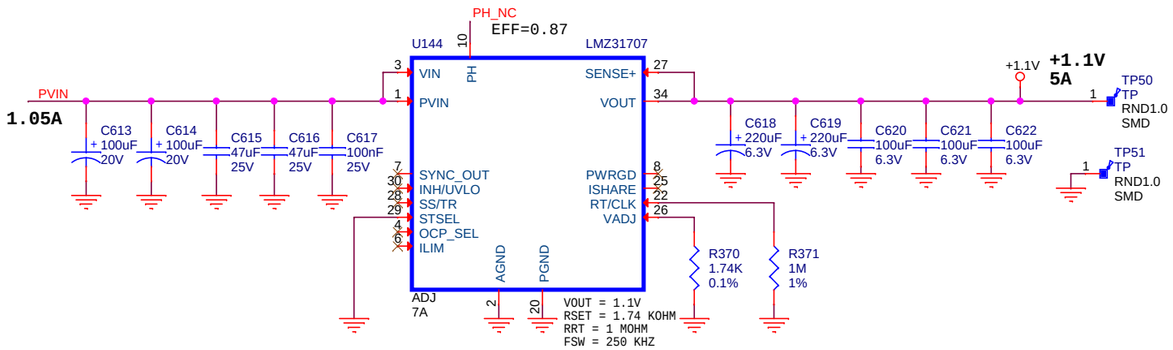
Schematic Path = /LTN_1

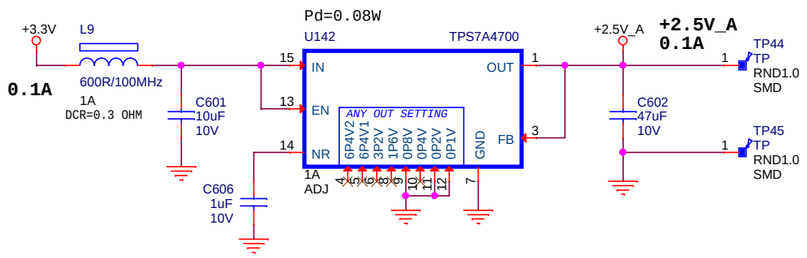
Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

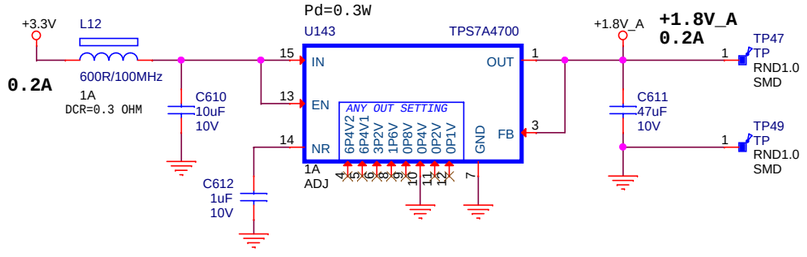
Thursday, September 29, 2016

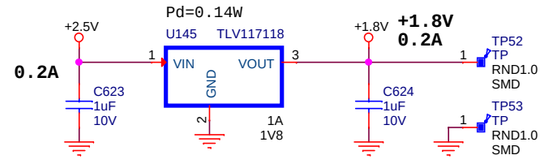
Sheet 54 of 60

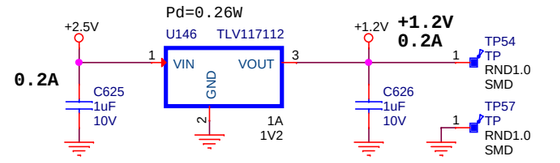


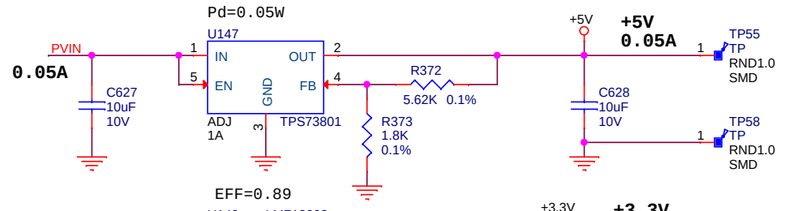


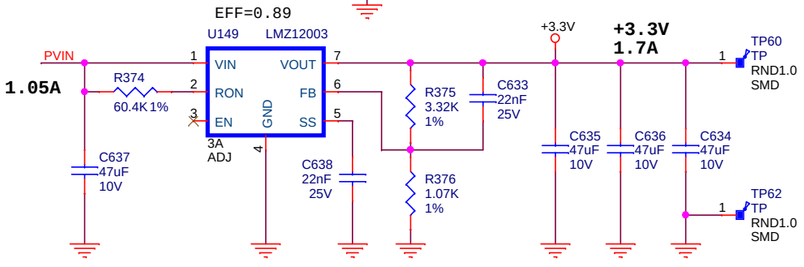


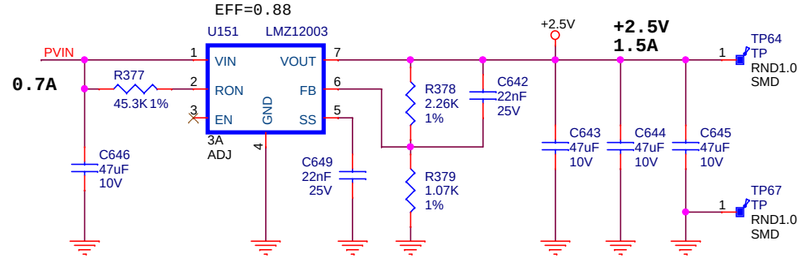


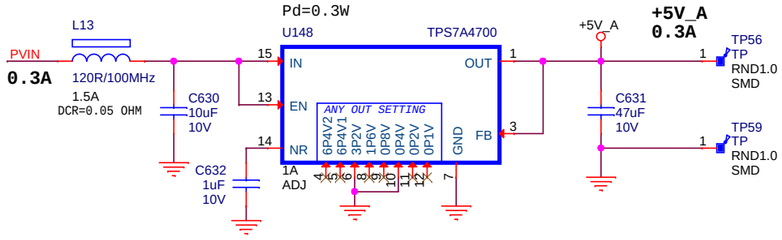


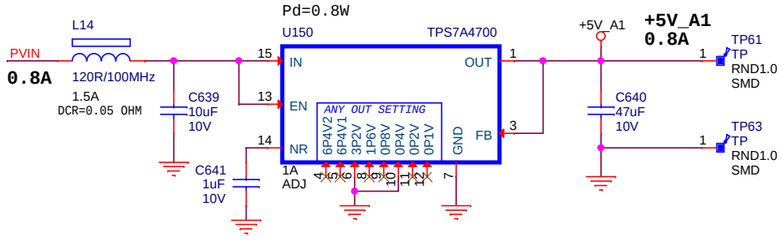


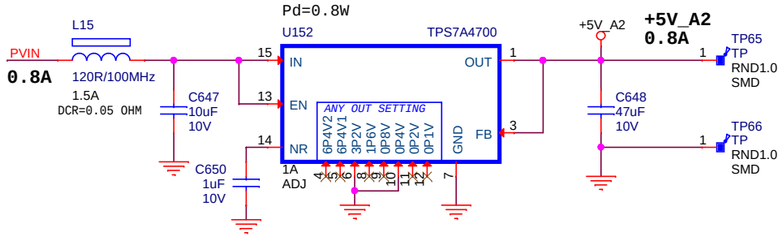


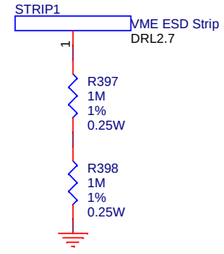












University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

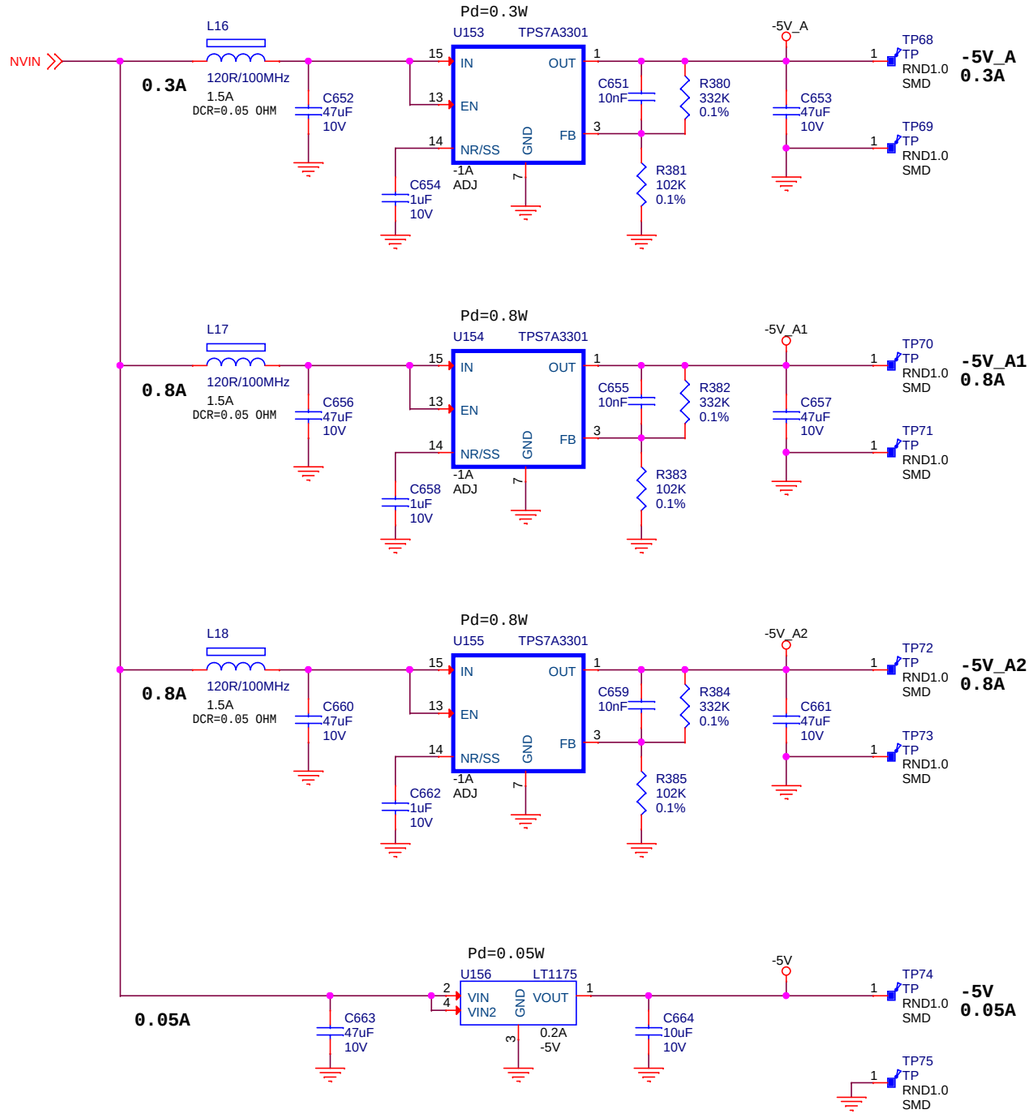
POWER (1/2)

Schematic Path = /PWR_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 55 of 60



University of Geneva

.
DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

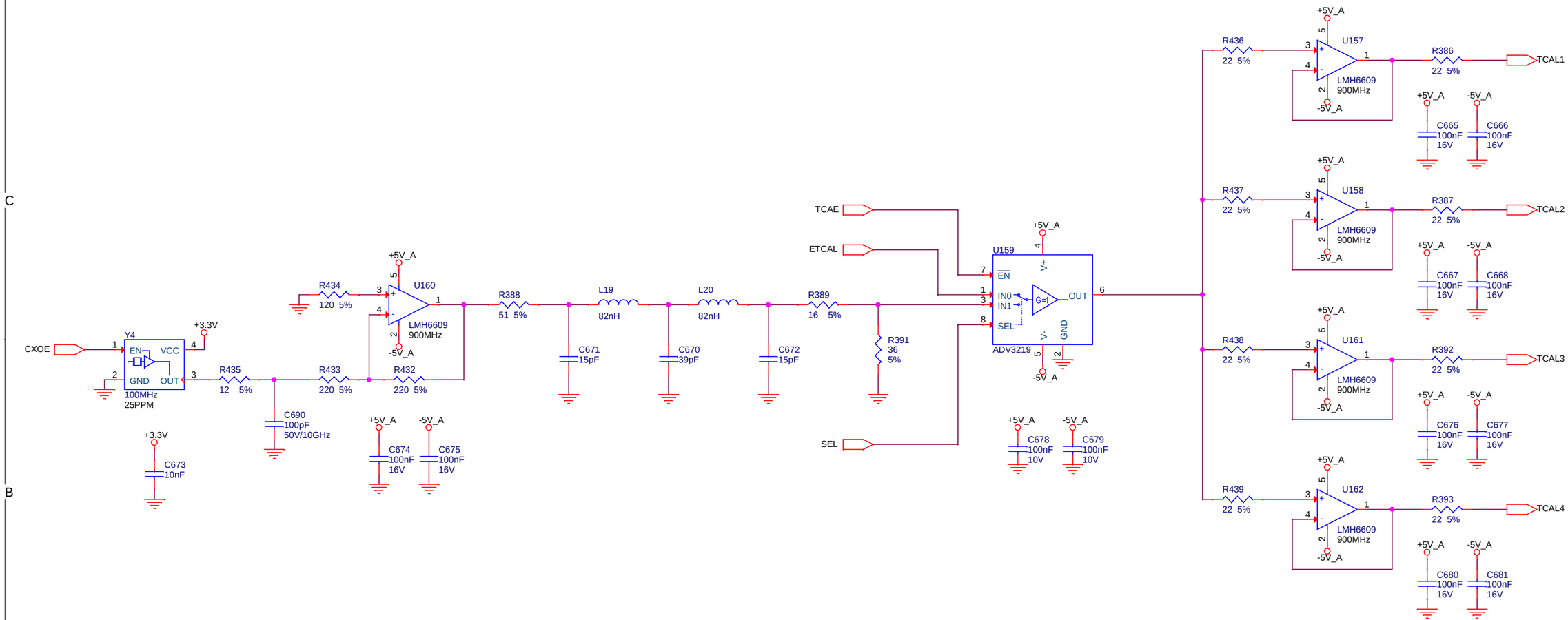
POWER (2/2)

Schematic Path = /PWR_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 56 of 60



University of Geneva

.
DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

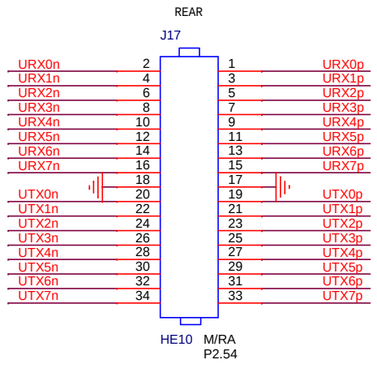
TIMING CALIBRATION - SOURCE

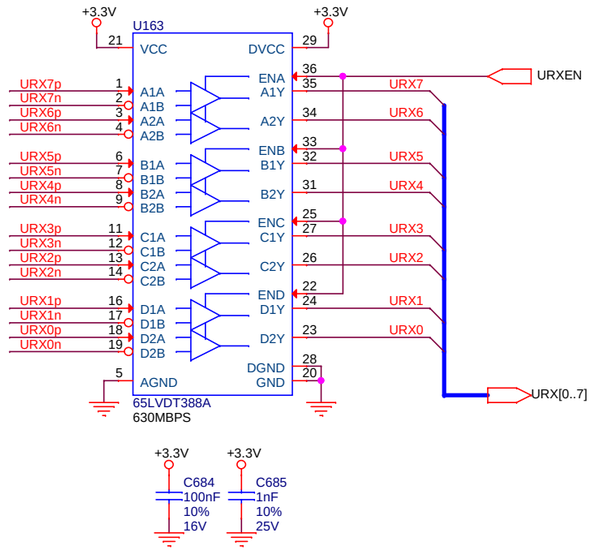
Schematic Path = /DRS4X32CH_1/TCA_1

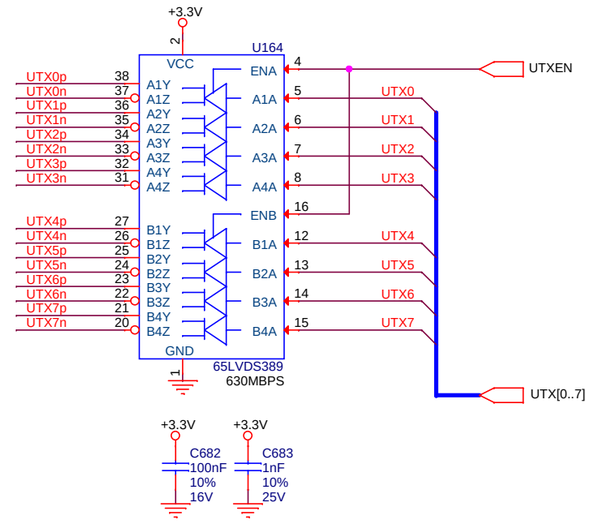
Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, October 06, 2016

Sheet 57 of 60







University of Geneva

DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

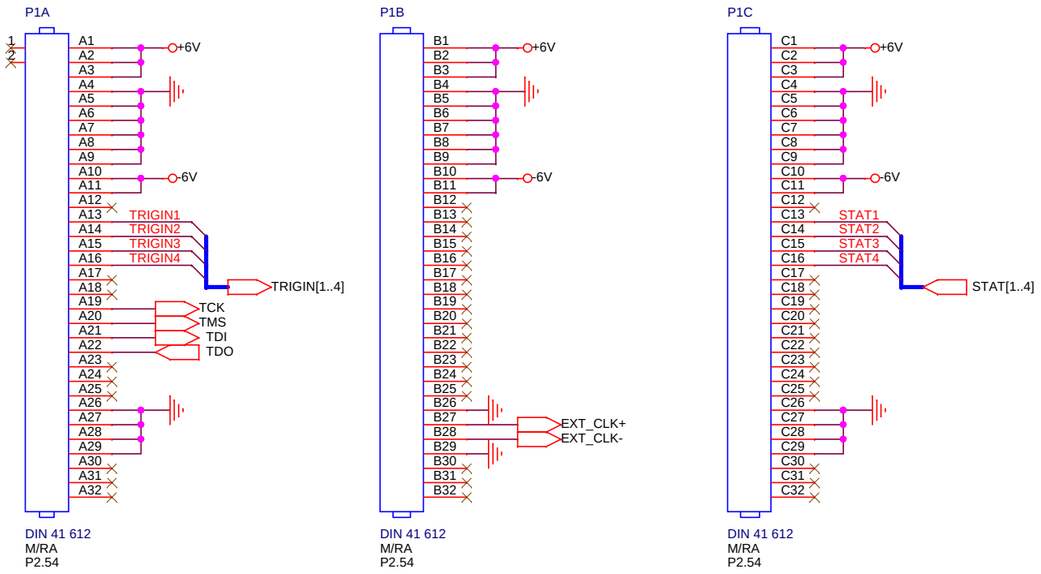
USER LVDS I/O

Schematic Path = /USRIO_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 58 of 60



University of Geneva

.
DPNC
24 quai Ernest-Ansermet
CH1211 GENEVE 4

UNIVERSITÉ DE GENÈVE

32-channel DRS4 Acquisition Board

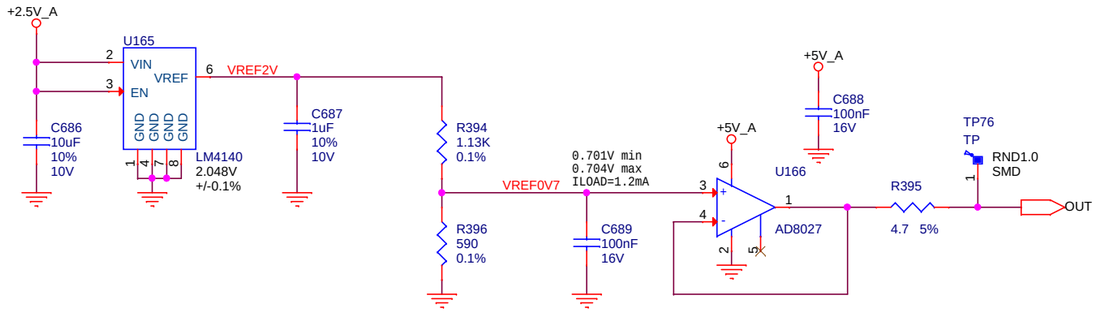
VME P1 CONNECTOR

Schematic Path = /VMECON_1

Size	DWG NO	Rev PCB	Rev PCBA
A3	DPNC342	02A	

Thursday, September 29, 2016

Sheet 59 of 60



University of Geneva . DPNC 24 quai Ernest-Ansermet CH1211 GENEVE 4			UNIVERSITÉ DE GENÈVE
32-channel DRS4 Acquisition Board			
0.7V VOLTAGE REFERENCE		Schematic Path = /DRS4X32CH_1/VREF_1	
Size A3	**DWG NO** DPNC342	**Rev PCB** 02A	**Rev PCBA**
Thursday, September 29, 2016		Sheet 60 of 60	