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MuTRiG: a mixed signal Silicon Photomultiplier readout ASIC with high timing resolution and gigabit data link

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Abstract: MuTRiG is a mixed signal Silicon Photomultiplier readout ASIC designed in UMC 180 nm CMOS technology for precise timing and high event rate applications in high energy physics experiments and medical imaging. It is dedicated to the readout of the scintillating fiber detector and the scintillating tile detector of the Mu3e experiment. The MuTRiG chip extends the excellent timing performance of the STiCv3 chip with a fast digital readout for high rate applications. The high timing performance of the fully differential SiPM readout channels and 50 ps time binning TDCs are complemented by an upgraded digital readout logic and a 1.28 Gbps LVDS serial data link. The design of the chip and the characterization results of the analog front-end, TDC and the LVDS data link are presented.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout

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1 The Mu3e experiment

The Mu3e experiment [1] is a novel experiment designed to probe new physics by searching for the charged lepton-flavour violating decay $\mu^+ \to e^+e^+e^-$ with a branching ratio sensitivity of 10^{-16}, improving the current best limit [2] by four orders of magnitude. To achieve this goal in a reasonable time the Mu3e experiment will be ultimately running at a muon stopping rate of more than 10^9 Hz using a new high intensity muon beam being developed at the Paul Scherrer Institute (PSI) in Switzerland. At the same time any background signal has to be suppressed below a level of 10^{-16}. The $\mu^+ \to e^+e^+e^-$ signal event consists of one electron and two positron tracks which originate from the muon decaying at rest in a stopping target. The tracks come from a common vertex and are coincident in time. The sum of the their momenta is zero and their energies add up to the muon mass. There are two kinds of background signals: internal conversion decays $\mu^+ \to e^+e^+e^-\nu\nu$ with a small fraction of muon energy carried away by the neutrinos (internal conversion background), and the overlay of different processes forming three tracks similar to $\mu^+ \to e^+e^+e^-$ event (accidental background). The internal conversion background can be suppressed with precise momentum and energy reconstruction. The suppression of the accidental background relies on a good momentum, vertex and timing resolution of the detector.

As shown in figure 1, the Mu3e detector is composed of four pixelated silicon tracking layers [3] both around the double cone target and in the so-called recurl region, as well as a fiber detector [4] in the central region and a tile detector [5] in the recurl region. The silicon pixel detector is built from 50 μm thin High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) [6], providing precise vertex and momentum information in the 1 T solenoidal magnet field. The fiber detector is based on squared scintillating fibers with a thickness of 250 μm, which are read out by Silicon Photomultipliers (SiPMs). The tile detector is built from $6.5 \times 6.5 \times 5.0\,\mathrm{mm}^3$ plastic scintillating tiles coupled to

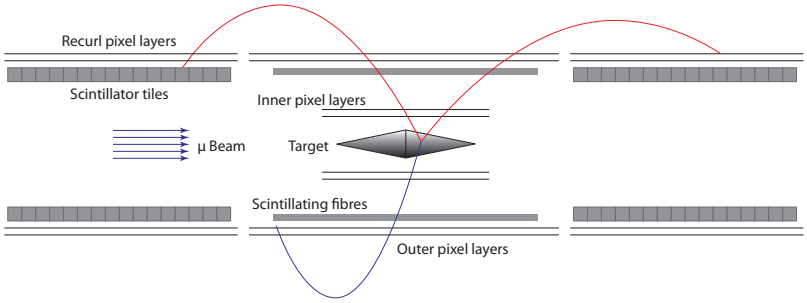

Figure 1. Schematic diagram of Mu3e detector system with a signal event comprising one electron (blue) and two positron (red) tracks.

SiPMs. The fiber detector and tile detector provide precise timing measurements. A good timing resolution of 500 ps (σ) and 100 ps (σ) is required for the fiber detector and the tile detector respectively, in order to reduce the accidental background to the desired level at high rates and to facilitate event reconstruction. Additionally the event rate in the fiber detector can be as high as 1.3 MHz/channel. Overall it puts a formidable challenge to the detector system and the readout electronics.

MuTRiG (Muon Timing Resolver including Gigabit-link) is a mixed signal SiPM readout Application Specific Integrated Circuit (ASIC) developed in UMC 180 nm CMOS technology. The MuTRiG chip aims at a high timing resolution and a high event rate capability for the Time-of-Flight (ToF) applications in high energy physics experiments and medical imaging. It is particularly dedicated to the readout of the Mu3e fiber detector and the Mu3e tile detector, to achieve the required timing resolution and at the same time to sustain the high event rate of the fiber detector.

2 Chip description

The MuTRiG prototype chip has been submitted in September 2016. A picture of the chip layout is presented in figure 2. It is designed with 32 high timing resolution analog front-end channels, Time-to-Digital Converters (TDCs) with a 50 ps bin size [7] and a digital part to process and transfer the event data to the data acquisition system (DAQ) via a gigabit LVDS link with 8b/10b encoding. The design details are presented in the following sections.

2.1 Analog front-end

The channel diagram of the MuTRiG chip is shown in figure 3. The analog front-end is designed using fully differential structures to suppress the common mode noise from the digital circuit on the chip as well as the noise from the external sources.

The incoming SiPM signal is received by the input stage and split into two branches: a timing branch and an energy branch. As shown in figure 4, two different thresholds are used for the leading edge discrimination in both branches. A low timing threshold extracts the time of arrival information at a threshold below the single pixel level and a higher energy threshold validates physical signals and provides energy information using a linearised Time-over-Threshold (ToT) method. The timing and energy trigger signals are combined into one single logic signal in the hit logic unit, preserving the rising edge of the timing trigger signal and the falling edge of the energy trigger signal. The timing

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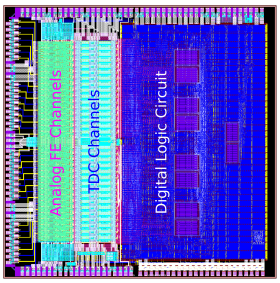

Figure 2. Layout of the MuTRiG prototype chip.

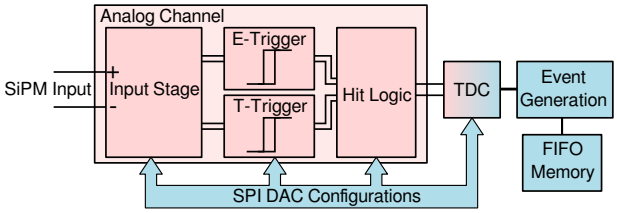

Figure 3. Schematic diagram of a MuTRiG readout channel.

and energy information are obtained from the rising edge of the timing trigger signal and the time difference between the rising edge of the timing trigger and the falling edge of the energy trigger.

2.2 Time-to-Digital Converter

The combined logic signals from the analog front-end are digitized by the integrated TDC. The TDC module was developed at ZITI Heidelberg and has been implemented in the PETA [7] and STiC [8] ASICs. The diagram of the TDC module is shown in figure 5. A global time base unit provides common time stamps to all channels. A Phase Lock Loop (PLL) locks a 16-stage Voltage Controlled Oscillator (VCO) to an external reference clock of 640 MHz. The output of the VCO also drives a 15-bit coarse counter implemented by a Linear Feedback Shift Register (LFSR). Each bin of the coarse counter is segmented by the 32 possible states of the VCO, generating fine counter bins of 50 ps. The channel-wise TDCs store the state of the VCO and coarse counter in latches at every rising edges of the incoming signals.

2.3 Event data processing and transmission

The digitized time data from the TDC are processed by the digital logic circuit of the MuTRiG chip. The block diagram of the MuTRiG chip is shown in figure 6. Event data are built using the time stamps for the rising edge of the timing trigger and the falling edge of the energy trigger. The event data are first stored in the L1 FIFO memory to be optionally validated by an external trigger signal. The valid data flow to the L2 FIFO memory and are then sent out of the chip in frames via a 1.28 Gbps LVDS serial data link with 8b/10b encoding.

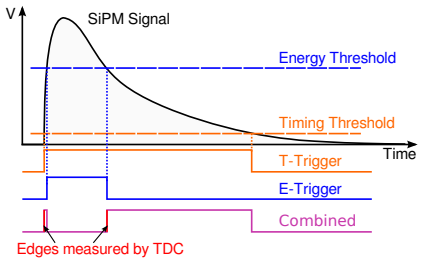

Figure 4. MuTRiG trigger principle.

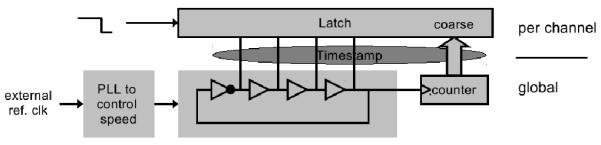

Figure 5. Diagram of the TDC module [7].

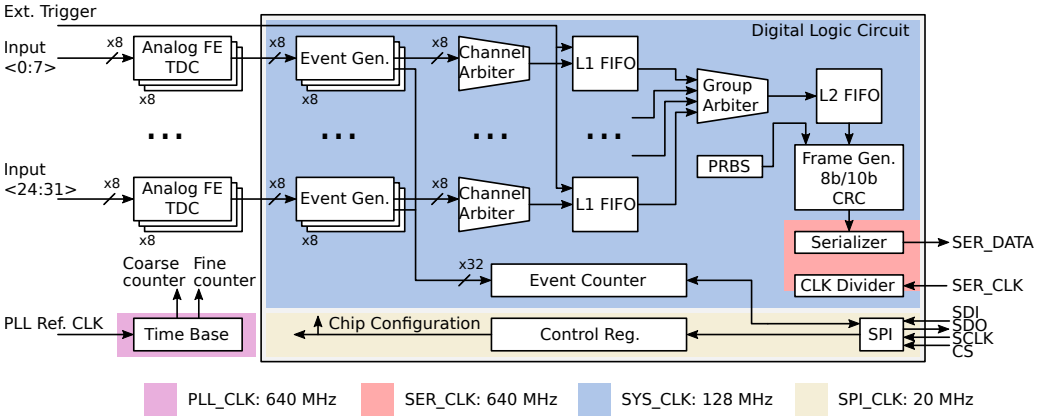

Figure 6. MuTRiG chip block diagram.

When packing the event data to a frame, a shorter event data structure can be used to further increase the event rate capability of the chip at a fixed bit rate on the data link. The shorter event data only contain the time of arrival information and a 1-bit energy information (passing or not passing the energy threshold) of an event, resulting in an shorter event size of 27 bits. A 16-bit Cyclic Redundancy Check (CRC) information is attached to the end of each frame for error detection during the data transmission.

12-bit binary counters have been implemented for monitoring the event rate on each channel. A Serial Peripheral Interface (SPI) is used for the readout of the channel event counters, as well as for the chip configuration.

2.3.1 External validation

An external validation functionality is implemented in the L1 FIFO of the MuTRiG chip to send out only the events which are close in time to an external trigger signal; this helps to reduce the load of the data link to the DAQ system. The working principle of the external validation functionality is presented in figure 7. All the events are written to the L1 FIFO and the oldest event will be overwritten first. Every 10 clock cycles the write pointer address is recorded in a corresponding table. As soon as an external trigger signal comes, the starting and stopping addresses of the valid events will be looked up in the address table; the read pointer will be set to the starting position of the valid events. Then the valid events will be read out to the L2 FIFO for transmission to the DAQ system. The offset and the width of the matching window can be configured with a resolution of 10 clock cycles ($\sim$ 78 ns). The maximum offset and width are 1.25 μs and 2.5 μs, respectively.

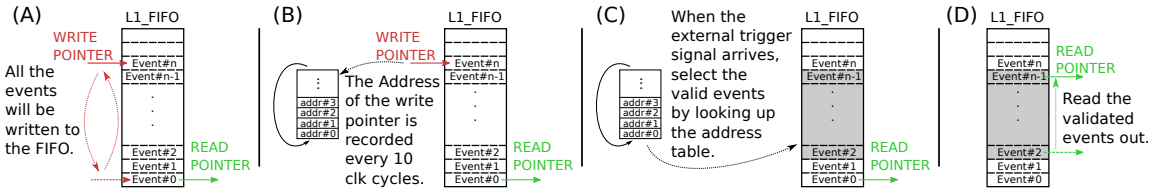

Figure 7. Working principle of the external validation functionality.

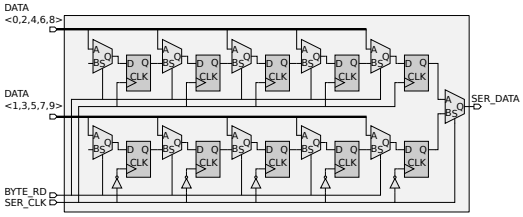

Figure 8. Schematic of the double data rate serializer.

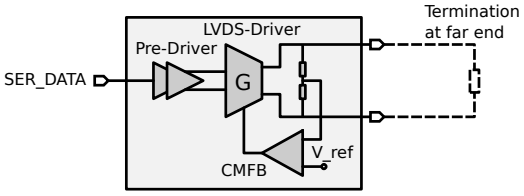

Figure 9. Schematic of the LVDS transmitter.

This functionality can be turned off; then the L1 FIFO will act as a normal FIFO buffer. In this case all events in the L1 FIFO are validated and transmitted further.

2.3.2 Gigabit LVDS data link

In order to sustain the high input event rate, a gigabit LVDS data link has been developed using a double data rate serializer and a customized LVDS transmitter. The double data rate serializer is realized by switching outputs from two rows of shift registers which are clocked at the rising and falling edge of the 640 MHz serial clock, as shown in figure 8. The even and odd bits of the 8b/10b encoded data will be loaded to the shift registers every 5 serial clock cycles (via the BYTE_RD signal). The serial data will change at both the rising and the falling edges of the serial clock, achieving a bit rate of 1.28 Gbps.

The serial output signal from the serializer is connected to the LVDS transmitter and is transmitted to the LVDS receiver in the DAQ system. As shown in figure 9, the LVDS transmitter consists of a pre-driver to ramp up the driving strength, a Current Source Switch Structure LVDS driver, as well as a common-mode feedback to correctly bias the LVDS driver and to modulate the common mode voltage of the output signal.

3 Characterization measurements

The analog front-end and the TDC implemented in the MuTRiG chip are silicon proven and have been extensively characterized in the STiCv3 prototypes. Since the MuTRiG chip is being fabricated, the timing performance presented here is characterized with the STiCv3 chip, in which the same analog front-end and TDC are implemented. In ref. [8], a Coincidence Timing Resolution (CTR) result of 214 ps FWHM has been presented using $3.1 \times 3.1 \times 15\,\mathrm{mm}^3$ LYSO:Ce crystals and Hamamatsu S12643-050CN(x) MPPCs read out by the STiCv3 chip at a temperature of 22°C. A Single Photon Timing Resolution (SPTR) measurement has been carried out recently in a dedicated optical setup with a 460 nm wavelength picosecond pulsed laser and two Hamamatsu S13360-1350CS MPPC sensors. The MPPCs are operating at a gain of $\sim 7 \times 10^6$ and read out by the STiCv3 chip using the full analog and digital chain. The laser is split into two paths: a low intensity path and a high path. In the low intensity path, the laser is focused to a spot smaller than 3 μm on a $50 \times 50\,\mu\mathrm{m}^2$ pixel of the MPPC sensor, generating single photon events. The laser in the high intensity path is not focused and illuminates a large amount of the pixels of the second MPPC, generating multi-photon signals as reference. The temperature of the setup is stabilized at 20°C. The time difference between the signals from the low intensity path and the high intensity path is

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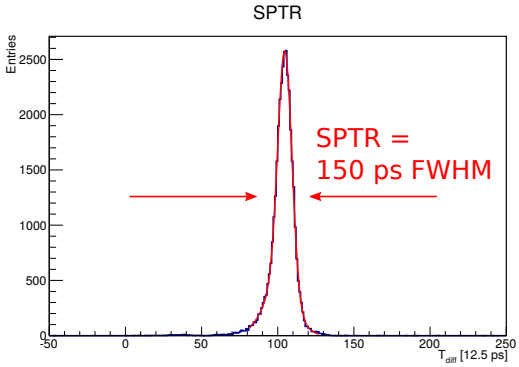

Figure 10. Single Photon Timing Resolution (SPTR) measurement result with 460 nm wavelength picosecond pulsed laser and Hamamatsu S13360-1350CS MPPCs read out by the STiCv3 chip.

evaluated. As shown in figure 10, a preliminary result of 150 ps FWHM has been obtained, which still includes the jitter from the reference signals and the laser.

A prototype chip has been designed and fabricated to characterize the performance of the gigabit LVDS data link. A mock-up digital circuit is implemented in this test chip including a Pseudo-Random Bit Sequence (PRBS) data generator, a data frame-generator, an 8b/10b encoder and the double data rate serializer connected to the customized LVDS transmitter, as shown in figure 11. A customized LVDS receiver is used to take in the clock signal from a fast differential arbitrary function generator. The output signal of the LVDS transmitter is measured by a high bandwidth 40 GSPS oscilloscope. An open eye diagram has been obtained for the 8b/10b encoded PRBS data up to a data rate of 1.5 Gbps, as shown in figure 12. The same LVDS receiver and LVDS data link has been implemented in the MuTRiG chip.

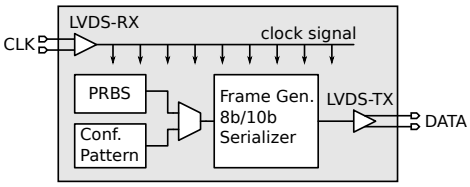

Figure 11. Schematic of the mock-up digital circuit on the LVDS data link test chip.

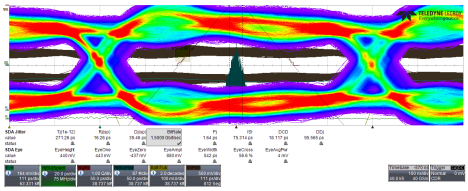

Figure 12. Eye diagram of the 8b/10b encoded PRBS data at 1.5 Gbps data rate.

4 Conclusion

MuTRiG is a mixed-mode SiPM readout ASIC for precise timing and high event rate applications in high energy physics experiments and medical imaging. The MuTRiG prototype chip design has been submitted in September 2016. It consists of 32 fully differential analog front-end channels digitized by the TDCs with 50 ps time binning and a dedicated digital logic circuit to store and transfer the event data to the DAQ system via a gigabit LVDS serial data link. An optional external validation functionality has been implemented in the MuTRiG chip validating the events by a matching window around the arrival of an external trigger signal. The offset and the width of the

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matching window can be configured in steps of 78 ns individually, with a maximum of 1.25 μs and 2.5 μs, respectively. A 1.28 Gbps LVDS serial data link has been designed for the MuTRiG chip with a double data rate serializer and a customized LVDS transmitter.

The analog front-end and the TDC channel have been extensively characterized in the STiCv3 chip and have proven an excellent timing performance. A preliminary SPTR result of 150 ps FWHM has been obtained with a 460 nm wavelength picosecond pulsed laser and two Hamamatsu S13360-1350CS MPPC sensors read out by the STiCv3 chip. The performance of the LVDS serial data link has been characterized with a separated prototype chip, on which a mock-up of the digital logic circuit for the data transmission has been implemented. An open eye diagram has been obtained for up to 1.5 Gbps with 8b/10b encoded PRBS data, showing the high output data rate capability of the MuTRiG chip.

Acknowledgments

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