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PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *November 15, 2013*
ACCEPTED: *January 6, 2014*
PUBLISHED: *February 10, 2014*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2013,
23–27 SEPTEMBER 2013,
PERUGIA, ITALY

STiC — a mixed mode silicon photomultiplier readout ASIC for time-of-flight applications

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ABSTRACT: STiC is an application specific integrated circuit (ASIC) for the readout of silicon photomultipliers. The chip has been designed to provide a very high timing resolution for time-of-flight applications in medical imaging and particle physics. It is dedicated in particular to the EndoToFPET-US project, which is developing an endoscopic PET detector combined with ultrasound imaging for early pancreas and prostate cancer detection. This PET system aims to provide a spatial resolution of 1 mm and a time-of-flight resolution of 200 ps FWHM. The analog frontend of STiC can use either a differential or single ended connection to the SiPM. The time and energy information of the detector signal is encoded into two time stamps. A special linearized time-over-threshold method is used to obtain a linear relation between the signal charge and the measured signal width, improving the energy resolution. The trigger signals are digitized by an integrated TDC module with a resolution of less than 20 ps. The TDC data is stored in an internal memory and transfered over a 160 MBit/s serial link using 8/10 bit encoding. First coincidence measurements using a $3.1 \times 3.1 \times 15\,\mathrm{mm}^3$ LYSO crystal and a S10362-33-50 Hamamtsu MPPC show a coincidence time resolution of less than 285 ps. We present details on the chip design as well as first characterization measurements.

KEYWORDS: Analogue electronic circuits; Front-end electronics for detector readout; Pixelated detectors and associated VLSI electronics

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doi:10.1088/1748-0221/9/02/C02003

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1 Introduction

STiC (SiPM Timing Chip) is a mixed mode ASIC for the readout of silicon photomultipliers (SiPMs) in particle physics and medical imaging applications [1]. It has been designed in the UMC 0.18 μm CMOS technology with the goal to achieve a very high timing resolution in time-of-flight (ToF) measurements. It is dedicated in particular to the EndoToFPET-US project [2], which is developing an endoscopic time-of-flight PET system for early stage pancreas and prostate cancer diagnosis. The ToF-PET scanner is depicted in figure 1 and consists of a small endoscopic probe and a larger external detector plate. The endoscopic probe can be positioned close to the desired observation region inside the body of the patient, while the external plate is located outside of the body. The internal probe uses an array of small $0.75 \times 0.75 \times 10\,\mathrm{mm}^3$ scintillating crystals for the detection of 511 keV photons. The scintillation light emitted by the $15 \times 7 \times 10\,\mathrm{mm}^3$ array is read out by a SPAD array designed in standard CMOS technology [3]. The external plate consists of 4096 LYSO crystals which are read out by 4×4 MPPC arrays from Hamamatsu. This PET system aims to achieve a time-of-flight resolution of 200 ps FWHM and a spatial resolution of 1 mm. The STiC ASIC is being developed for the readout of the MPPC arrays in the external plate and has been designed to meet the high timing resolution required by the detector system. We present details of the ASIC design as well as first characterization measurements with a 16-channel prototype version of STiC which was submitted in April 2012.

2 ASIC description

Figure 2a shows the readout method implemented in the ASIC. The time and energy information of the charge signals generated by the SiPM is encoded into time stamps by two discriminators with individual thresholds. The time discriminator uses a low threshold to provide a precise time trigger signal, while the energy discriminator uses a higher threshold for the Time-over-Threshold (ToT) measurement. A logic unit combines the discriminator outputs into a single trigger signal which preserves the leading edge of the time and the trailing edge of the energy discriminator. This combined signal contains the timing and energy information in the first trigger edge and the time difference between the first and second trigger edge, which are measured by a TDC module.

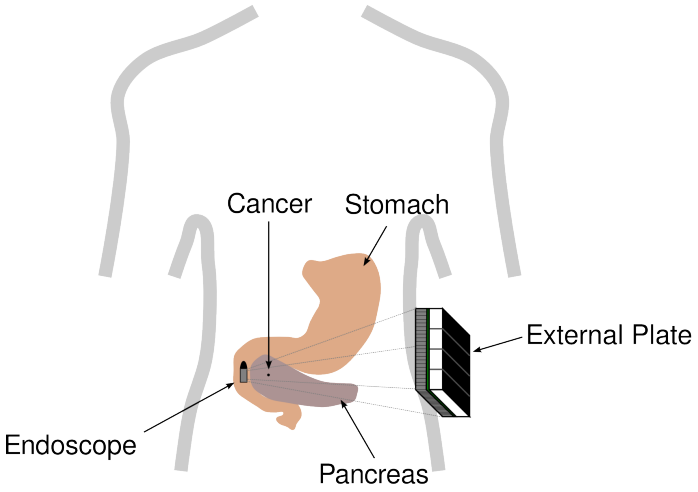

Figure 1. Design of the endoscopic ToF-PET system [1].

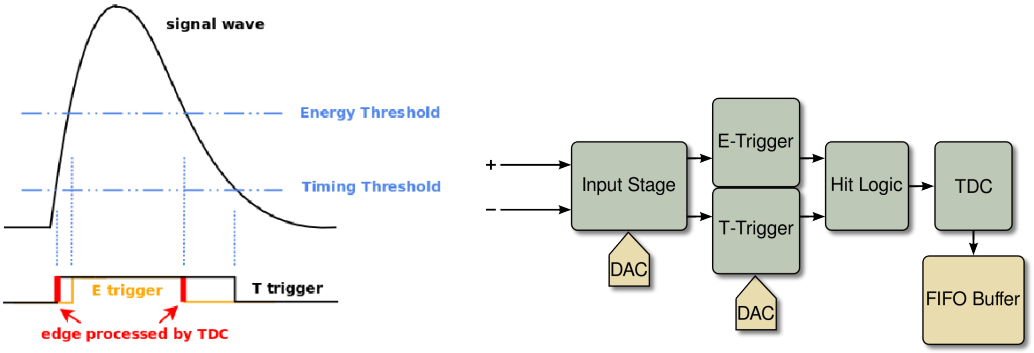

Figure 2. (a) SiPM measurement method implemented in STiC. (b) Diagram of a STiC readout channel.

The diagram of a single readout channel of STiC is shown in figure 2b. The design of the input stage allows either a single ended or a differential connection of the sensor to the ASIC. The differential readout structure provides the advantage of suppressing noise from the internal digital part as well as external sources.

The input stage uses a symmetric design with a common sub-unit for the negative and positive input terminals. To reduce the input impedance of the chip, a high bandwidth feedback scheme has been implemented. An 8-bit DAC is used to control the voltage at the input terminal of the channel in a range of more than 500 mV. This feature is used to tune the bias voltage of the connected SiPM providing the possibility to compensate for temperature fluctuations and differences in the breakdown voltage of the sensors. The bandwidth of this input stage is about 500 MHz with a signal rise time around 1.3 ns for a current impulse signal.

The structure of the input stage also provides a linear relationship between the input charge and the width of the discriminator signals. This linearized Time-over-Threshold method results in an improved resolution of the charge measurement.

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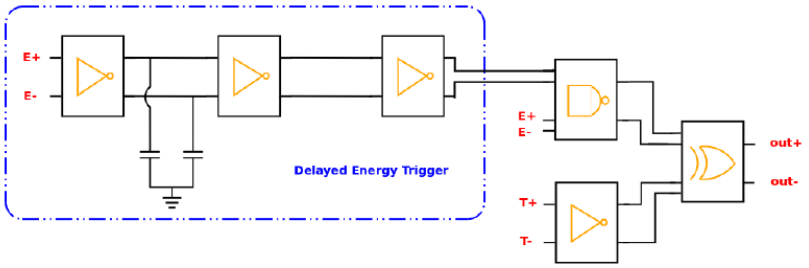

Figure 3. Diagram of the hit logic unit.

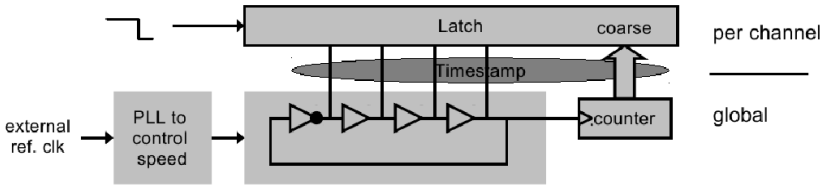

Figure 4. Diagram of the TDC module [4].

The input charge signal from the sensor is duplicated and sent to two discriminators. A low threshold discriminator is used to create a precise time trigger signal while a discriminator with a higher threshold provides a Time-over-Threshold charge measurement. The structure of these discriminators uses a positive feedback loop that also provides a hysteresis in the signal discrimination, which is used to suppress noise triggering events occurring especially in the signal tail.

Figure 3 shows a logic diagram of the hit logic unit which combines the output signals from the timing and energy discriminator into one output signal to the TDC module. All logic gates in this unit use the differential Current Mode Logic standard. The signal of the timing and energy discriminators are combined by a logic XOR function. The resulting output signal consists of two successive logic pulses generated by the leading edge of the time trigger and the trailing edge of the energy trigger. Because of the fast rise time of the input signal, the rising edges of the time and energy trigger will occur almost at the same time. To ensure a minimal width of the first logic pulse generated by these edges, two capacitors are used to create a delayed copy of the energy trigger. This delayed signal is combined with the original trigger signal, delaying the leading energy edge but preserving the trailing edge containing the desired energy information.

A more detailed description of the analog input stage has been published in [1].

The TDC module used in the STiC ASIC has been developed at ZITI Heidelberg using CMOS Current Mode Logic and is implemented in the PETA ASICs [4]. Figure 4 shows a diagram of this TDC module. A PLL with a 16-stage voltage controlled ring oscillator (VCO) is used to lock to an external frequency of 640 MHz. The output of the ring oscillator drives a 15-bit coarse counter implemented by a linear feedback shift register. By recording the state of the individual VCO elements in addition to the value of the coarse counter as indicated in figure 4, a timing subdivision of 50 ps is achieved and a time resolution of less than 20 ps. A time stamp which contains the state of the coarse counter and the VCO elements is stored for each hit in the corresponding TDC channel.

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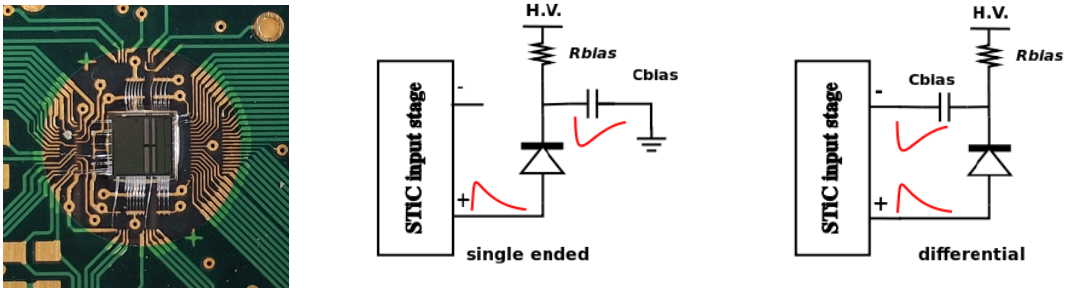

(a) (b)

Figure 5. (a) STiC2 prototype bonded to a test PCB. (b) Single ended and differential SiPM readout connections.

The recorded time stamps are processed by a digital control logic, which has been implemented using standard cell logic. A receiver unit groups the data to events with time and energy information. The event data is then stored in a 64 word deep FIFO buffer whose content is transmitted every 6.4 μs. The data transmission uses an 8/10 bit encoded serial LVDS link supporting transfer rates of up to 160 Mbit/s corresponding to about 10^6 recorded events per second. The configuration of the chip settings is performed by a SPI slow control interface.

The prototype ASIC has a die size of $3.2 \times 3.2\,\mathrm{mm}^2$ and contains 16 channels. In addition a test channel is implemented in order to characterize the performance of only the analog input stage. The power consumption of the final 64 channel ASIC is expected to be around 25 mW per channel.

3 Chip characterization measurements

Figure 5a shows a picture of the prototype ASIC bonded to a PCB for testing. The board has been used to characterize the performance of the chip using charge injection and SiPM measurements with single ended and differential connections.

The separate test channel is used to characterize the performance of the analog input stage. A charge injection method is used to inject defined charge signals into the test channel using a pulse generator and a capacitor. The output signals generated by the time and energy discriminators of the chip are measured with a high bandwidth oscilloscope. Figure 6a shows a scan of the output pulse width against the injected charge signal. A linear relation between the charge and the pulse width is observed for signals larger than 2.5 pC, verifying the functionality of the linearized time-over-threshold method.

To investigate the single photon timing response of a SiPM (MPPC S10362-11-100), the analog test channel is connected to the sensor using a single ended connection as shown in figure 5b. The light emitted by a fast pulsed laser system (PILAS PiL063SM) with a wavelength of 405 nm is focused by an optical system onto a single pixel of the sensor. A ToT measurement of the discriminator output signal is used to select only single pixel signals from the recorded events. The delay between the time trigger output of the chip and the trigger signal of the laser has been measured and is plotted in figure 6b. A timing resolution of $\sigma = 180$ ps is observed, which is consistent with measurements performed using a direct SiPM readout with a fast amplifier module. This

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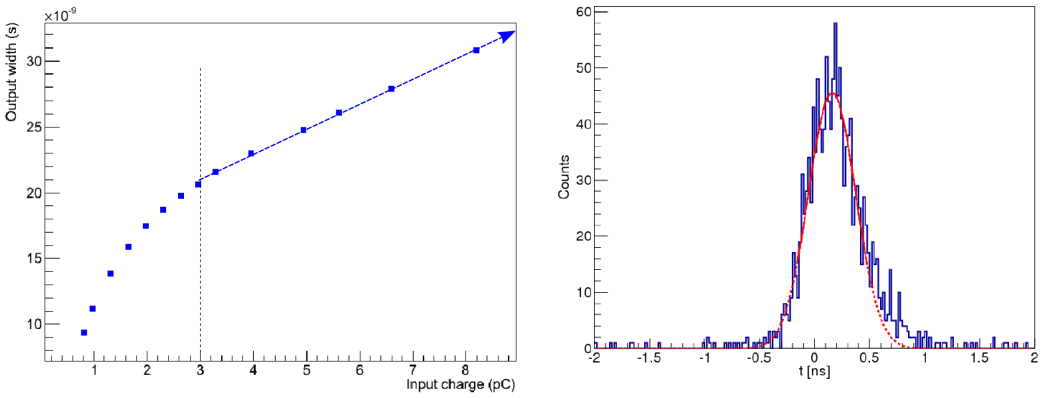

(a) (b)

Figure 6. (a) Pulse width of the discriminator output against the injected charge. (b) Single photon timing response with STiC2 and a MPPC S10362-11-100.

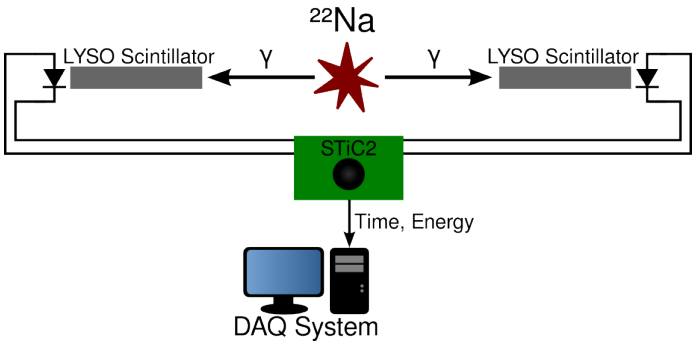

Figure 7. Coincidence measurement setup using STiC2.

measurement also confirms the results from analog design simulations of the trigger jitter for a MPPC S10362-11-50 device and shows that the analog input stage is performing according to its design specifications.

The key parameter of a Time-of-Flight PET system is the coincidence time resolution (CTR) of the readout chain. To characterize the performance of the chip in this respect, the CTR has been measured using a setup similar to the foreseen design of the external plate of the EndoToFPET-US project. The setup using a ^{22}Na source as a β^+ emitter is shown in figure 7. The resulting 511 keV photons from the positron annihilation are detected in LYSO crystals with a dimension of $3.1 \times 3.1 \times 15\,\text{mm}^3$. The crystals are wrapped in Teflon tape and coupled to $3 \times 3\,\text{mm}^2$ MPPCs from Hamamatsu (S10362-33-50C) with a nominal dark count rate of 8 MHz at room temperature.

A preliminary coincidence measurement using the full readout chain of the STiC ASIC and a single-ended connection of the MPPC to the chip has been performed. Figure 8a shows the recorded energy spectrum of the ^{22}Na source. Due to the linearized ToT method, the 511 keV and the 1.27 MeV peak are clearly visible in the spectrum. For the coincidence measurement, events within $1.0\,\sigma$ of the 511 keV photon peak are selected and the difference between the arrival time of the events is measured. A first measurement of the time spectrum without optimization of the

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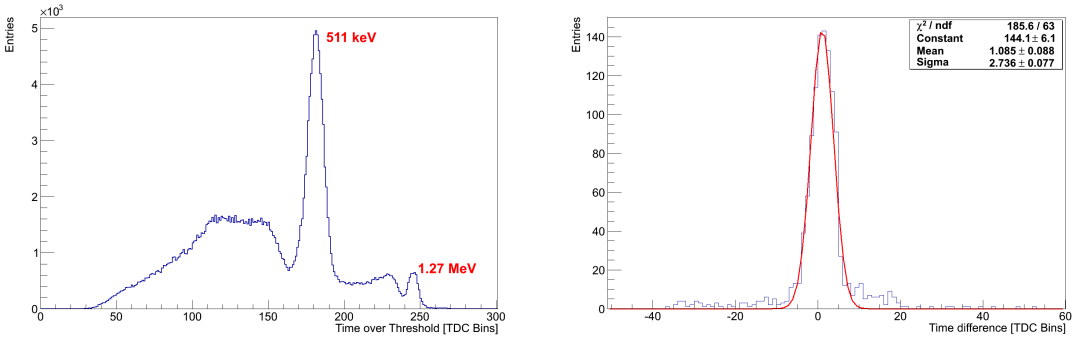

(a) **(b)**

Figure 8. (a) ^{22}Na energy spectrum recorded with STiC. (b) Recorded time spectrum for CTR measurement using Hamamatsu MPPCs (S10363-33-50C) at 28 °C.

chip configuration or the SiPM bias voltage shows a CTR resolution of less than 330 ps FWHM at 28 °C. Although no chip optimization has been performed and the ambient temperature is higher, this preliminary value is already consistent with coincidence measurements using only the analog input stage and an external TDC module and verifies the functionality of the full readout chain.

The CTR depends significantly on the applied high voltage of the SiPM. A scan of the CTR against the applied bias voltage on both SiPMs has been performed using only the analog input stage. The sensors are connected to two analog channels using a differential connection. The output of the discriminators is recorded by a HPTDC VME module from CAEN with a time binning of 25 ps [5]. Since the final PET system will be installed in an air conditioned operating room, a temperature chamber has been used to perform the measurements at a stable ambient temperature of 15 °C. The bias voltage has been tuned for both sensors individually by separate HV supplies and is plotted for one sensor in figure 9. The timing resolution increases with a higher gain of the sensor and decreases with higher dark count rates, which is reflected in the parabolic shape of the high voltage scan. For the optimal bias voltage a CTR of 285 ps FWHM is obtained.

Characterization measurements using the integrated TDC, further optimizations of the bias settings, and in particular the use of available SiPM sensors with lower dark count rates are expected to improve the coincidence timing resolution further.

4 Conclusion

STiC is a mixed mode readout ASIC for time-of-flight applications using silicon photomultipliers. A 16 channel prototype has been designed and submitted in April 2012. The chip provides a tuning range of 500 mV for the SiPM bias voltage, allowing to compensate for temperature fluctuations and differences in the SiPM breakdown voltages. The analog input stage allows to read out SiPMs using a single ended or a differential connection and creates a trigger output containing the time and energy information of the signal. A special linearized time-over-threshold method creates a linear relation between the pulse width of the energy discriminator for signal charges from 2.5 pC on. An integrated TDC module digitizes the information with a time binning of 50 ps.

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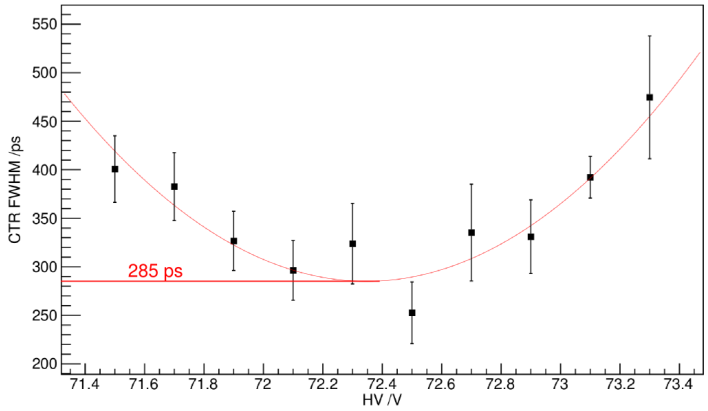

Figure 9. Scan of the CTR against the applied SiPM bias voltage using MPPC S10362-33-50C sensors at 15 °C.

First characterization measurements of the analog input stage show a SPTR of $\sigma = 180\,\text{ps}$ using a fast laser and a Hamamatsu MPPC S10362-11-100, which is consistent with simulations and direct SiPM readout measurements using a fast amplifier module.

CTR measurements using $3.1 \times 3.1 \times 15\,\text{mm}^3$ LYSO crystals and MPPC S10362-33-50 sensors from Hamamatsu with a dark count rate of 8 MHz yield a timing resolution of less than 285 ps FWHM. The CTR resolution is expected to be improved further by optimized chip settings and the use of available SiPM sensors with lower dark count rates.

A 64 channel version of the ASIC has been designed and submitted in September 2013. In addition to an extension of the digital part of the chip, the analog input stage has been improved using the results gained from the prototype characterization.

Acknowledgments

The research leading to these results has received funding from the European Union Seventh Framework Programme [FP7/2007-2013] under Grant Agreement n°256984 and by a Marie Curie Early Initial Training Network Fellowship of the European Community's Seventh Framework Programme under contract number (PITN-GA-2011-289355-PicoSEC-MCNet).

We also would like to thank the ASIC laboratory of Heidelberg for their outstanding support during the chip development.

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