DRS4 Evaluation Board User's Manual

Board Revision 4.0
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Revision History

Date	Modification
2 March 09	Initial Revision
27 April 09	Mention input range, added timing calibration description
3 Aug. 09	Added LED description
12 July 10	Updated documentation for evaluation board V3
12 Sept. 10	Added maximum input voltage
16. Feb. 12	Added info for external connectors

Table of Contents

1. Introduction

The DRS4 chip, which has been designed at the Paul Scherrer Institute, Switzerland by Stefan Ritt and Roberto Dinapoli is a Switched Capacitor Array (SCA) capable of digitizing eight channels at sampling speeds up to 5 GSPS. This chip is available through the PSI technology transfer program for other institutes and organizations. In order to simplify the design process to integrate the DRS4 chip into custom electronics, an evaluation board has been designed, which demonstrates the basic operation of the chip. It has SMA connectors for four input channels CH1 to CH4, an USB 2.0 connector and a LEMO trigger input (Figure 1). The board is powered through the USB port and contains an on-board trigger logic. It comes with MS Windows® and Linux drivers and two application programs. It is basically equivalent to a four channel 5 GSPS digital oscilloscope.

This manual describes the software installation, the usage of the application programs, and gives hints for developers seeking to build new electronics around the DRS4 chip.

1.1. Board description

Since the DRS4 chip has differential inputs, the board uses four active buffers (THS4508 from Texas Instruments®) to convert the 50-Ohm terminated single ended inputs into differential signals. Analog switches in front of the buffers (ADG901 form Analog Devices®) are used to de-couple the inputs during calibration. Two reference voltages are generated by the on-board 16-bit DAC to measure the offset and gain of all DRS4 storage cells for calibration. The four analog inputs are AC coupled and have a input range of 1 V peak-to-peak. The absolute maximum input voltage range is -0.5V to +2.8V. The DRS4 is read out with a 14-bit ADC (AD9245 from Analog Devices®) and a FPGA (Xilinx® Spartan 3). The USB connection is implemented with a micro controller (Cypress® CY2C68013A). The high speed modus of the USB 2.0 bus allows for data transfer rates of more than 20 MB/sec.

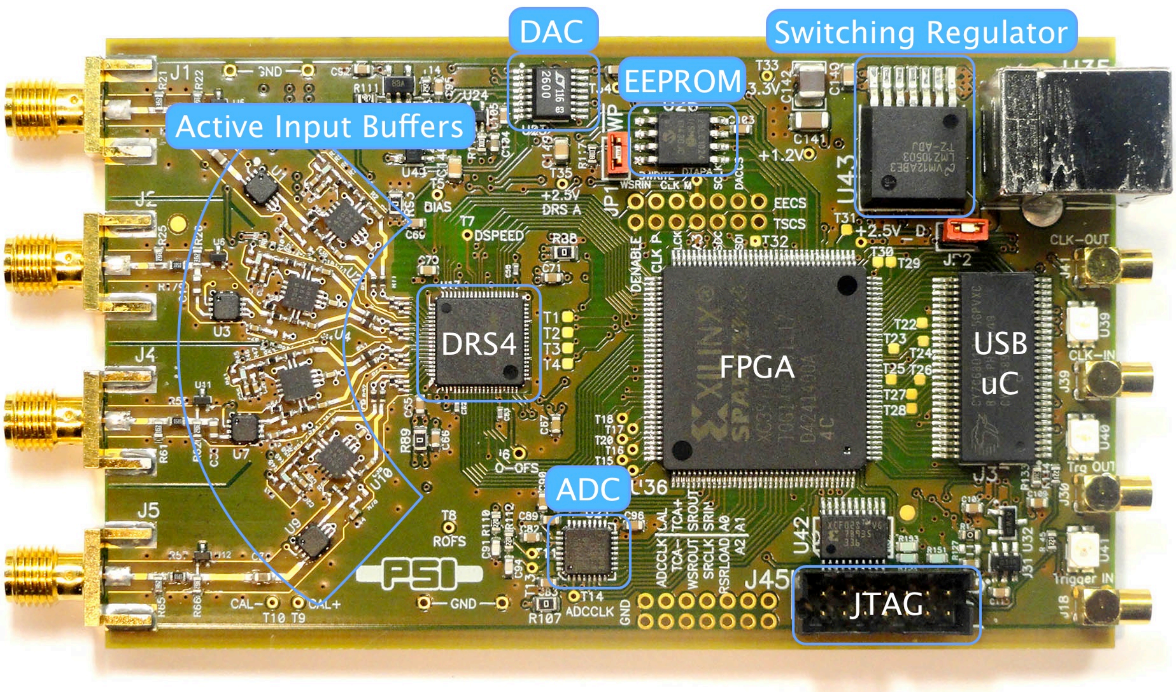


Figure 1: Picture of the DRS4 Evaluation Board V4 with different components

For trigger purposes and inter-board synchronization, four MMCX connectors are available, which can be seen on the right side of Figure 1. The **Trigger IN** works as an external trigger much like the one of an oscilloscope. The electrical standard is 5V TTL. Although a 50 Ω termination is possible, the resistor is not soldered by default. This allows using weaker sources, which cannot drive 5V into a 50 Ω load. Reflections on this line usually do not matter, since the first leading edge of the trigger is used. To connect a SMA cable to the trigger input, a commercial adapter can be used like the one shown in.

Figure 2: MMCX-SMA adapter which can be obtained for example form **www.digikey.com** (part number ACX1352-ND)

The **Trigger OUT** and the **Clock IN/OUT** signals will be supported in a later firmware version and will allow for inter-board triggering, so that small synchronized DAQ systems with several evaluation boards can be made.

Four on-board discriminators with programmable level allows for self triggering on any of the four input channels, or a combination of channels supporting coincidences for example. A 1 MBit EEPROM (25LC1025 from Microchip®) is used to store the board serial number and calibration information. Two 14-pin headers carry all important logical signals which allow easy debugging with a logic analyzer or oscilloscope. A JTAG adapter can be used to update the FPGA firmware through a Xilinx® Platform Cable Adapter.

The specifications of the board inputs is summarized in following table:

Analog inputs		
Termination	50 Ω	
Input range	1 V p-p	AC coupled
Maximum allowed input voltage		
DC	± 10V	
Long pulse (<2µs)	± 20V	
Short pulse (<200ns)	± 30V	
Trigger input/Clock input		
Termination	high impedance, optionally 50 Ω	
Maximum allowed input voltage	-0.5 V to +5.5 V	5 V TTL compatible
High Level Input Voltage	2.5 V (min)	
Trigger output/Clock output		
Level	5V TTL	

1.2. LEDs

The DRS4 evaluation board is equipped with four LEDs. They are operated by the micro controller and the FPGA and have following meaning:

LED	Meaning
Green	This LED becomes green when the on-board micro-controller booted successfully. If this LED stays dark, there is either no power or the micro-controller lost it's program, which requires a re-programming of the EEPROM.
Yellow	When the on-board FPGA boots correctly this LED becomes lit. If it stays dark, it might be that the FPGA program was lost and requires re-programming. After booting, this LED indicates the board status. If lit, the DRS4 chip is active and sampling data. If stopped by software or a trigger, this LED turns off. A special pulse stretcher ensures that even in high trigger rate environments this LED does not flash with more than ~10Hz so the blinking can still be seen by eye.
Red	When lit, this LED indicates a error condition

1.3. Firmware Description

Both the Windows and the Linux distribution contain a subdirectory "firmware" which contains the FPGA and Microcontroller firmware for the DRS4 Evaluation Board. The FPGA firmware is written in pure VHDL, thus making it easy to port it to other FPGA devices such as Altera® or Lattice®. Only a few Xilinx® basic components such as clock managers and I/O blocks have been instantiated and must be adapted when another FPGA manufacturer than Xilinx® is chosen. The FPGA source code is contained in several files with following contents:

`src/drs4_eval1.vhd`	Top level entity. Routing of clock signals, global reset signal, LEDs and LEMO input
`src/drs4_eval1_app.vhd`	Main file containing state machines for DRS4 readout, serial interface to DAC, EEPROM and temperature sensor, trigger logic and reference clock generation
`src/usb_dpram.vhd`	Instantiates block ram for waveform storage
`src/usb_racc.vhd`	Interface to CY2C68013A microcontroller in slave FIFO mode. Implements a set of status and control registers through which the main application can be controlled
`src/usr_clocks.vhd`	Generates 66 MHz, 132 MHz, 264 MHz and a phase shifted 66 MHz clock out of the 33 MHz quartz input frequency via the Xilinx® Digital Clock Managers (DCM)
`ucf/drs4_eval1.ucf`	Constraint file. Assigns package pins and defines clock constraints
`3s400/drs4_eval1.ise`	Xilinx® ISE 9.2i project file
`3s400/drs4_eval1.bit`	Compiled firmware image directly for Spartan 3s400 FPGA
`3s400/drs4_eval1.mcs`	Compiled firmware image for FPGA EEPROM XCF02S
`3s400/drs4_eval1.ipf`	Xilinx® Impact project file to program FPGA via download cable

The firmware for the USB microcontroller from Cypress® is written in C and must be compiled with the Keil® 8051 C compiler. It contains the standard include and library files from the Cypress EZ-USB® development kit plus some DRS specific files:

`CY7C68013A/drs_eval.c`	Main micro controller firmware file
`CY7C68013A/dscr.a51`	USB descriptor tables
`CY7C68013A/drs_eval.hex`	Compiled firmware file (Intel HEX format)
`CY7C68013A/drs_eval1.iic`	Compiled firmware file (For Cypress EZ-USB Console download)
`CY7C68014A/*`	Remaining files are standard files from EZ-USB development kit

The FPGA firmware implements a set of control and status registers, through which the DRS4 can be controlled and read out. The mapping of the control registers is as follows:

#	Ofs.	Bit	Name	Comment
0	0x00	0	start_trig	Write a "1" to start the domino wave
0	0x00	1	reinit_trig	Write a "1" to stop & reset the DRS chip
0	0x00	2	soft_trig	Write a "1" to stop the DRS chip & read the data to RAM
0	0x00	3	eeprom_write_trig	Write contents of RAM into EEPROM (32kB page)
0	0x00	4	eeprom_read_trig	Read contents of EEPROM into RAM (32kB page)
0	0x02	18	led	1=on, 0=blinks once at beginning of DRS chip readout
0	0x02	19	tcal_en	Switch on (1) / off (0) 264 MHz calib. sig. for DRS chips
0	0x02	20	tcal_source	System clock (0) or separate quartz (1) clock source
0	0x02	21	transp_mode	1=send DRS inputs to outputs ("transparent mode")
0	0x02	22	enable_trigger1	Write a "1" to enable external trigger (LEMO)
0	0x02	23	readout_mode	0:start from first bin, 1:start from domino stop
0	0x02	24	neg_trigger	1=trigger on high to low transition
0	0x02	25	acalib	Write "1" to enable amplitude calibration
0	0x02	27	dactive	0:stop domino wave during readout, 1:keep it running
0	0x02	28	standby	1: put chip in standby mode
1	0x04	31..16	DAC0	Set DAC 0 (=A, ROFS)
1	0x06	15..0	DAC1	Set DAC 1 (=B, CMOFS)
2	0x08	31..16	DAC2	Set DAC 2 (=C, CAL-)
2	0x0A	15..0	DAC3	Set DAC 3 (=D, CAL+)
3	0x0C	31..16	DAC4	Set DAC 4 (=E, BIAS)
3	0x0E	15..0	DAC5	Set DAC 5 (=F, TLEVEL)
4	0x10	31..16	DAC6	Set DAC 6 (=G, O-OFS)
4	0x12	15..0	DAC7	Set DAC 7 (=H, -)
5	0x14	31..24	configuration	Bit0: DMODE, Bit1: PLLEN, Bit2: WSRLOOP
5	0x14	23..16	channel_config	1=1x8k,0x11=2x4k,0x33=4x2k,0xFF=8x1k
5	0x16	7..4	first_chn	First channel address to read out (0..9)
5	0x16	3..0	last_chn	Last channel address to read out (1..9)
6	0x18	31..16	trigger_delay	Trigger delay in ticks of roughly 2.3 ns
6	0x1A	15..0	sampling_freq	Sampling frequency in ticks (=1024/f_{samp}*0.120-2)
7	0x1E	31..16	trigger_config	Trigger configuration
7	0x1E	15..0	eeprom_page	Page number for EEPROM communication

While the mapping of the status registers is like this:

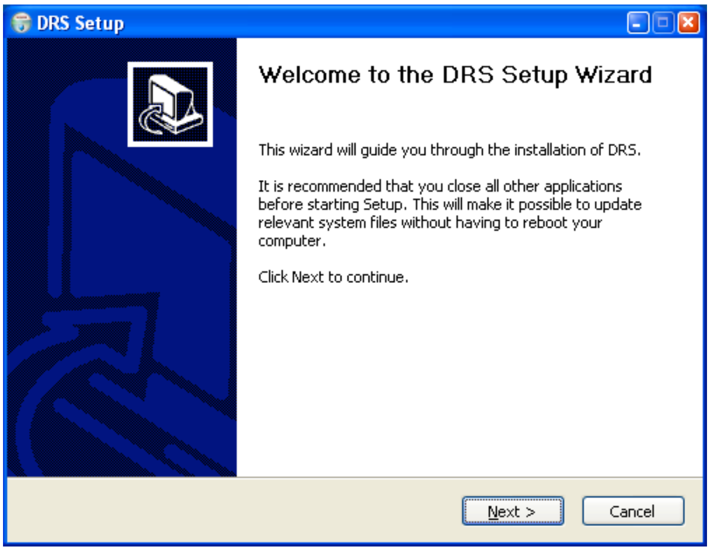
#	Ofs.	Bits	Name	Comment
0	0x00	31..16	board_magic	0xC0DE, Magic number for DRS board identification
0	0x02	15..8	board_type	5: Eval. Board V2; 7: Eval. Board V3
0	0x02	7..0	drs_type	4 for DRS4
1	0x04	0	running	"1" while domino wave running or readout in progress
2	0x08	31..16	stop_cell	position of cell where sampling stopped at last trigger
8	0x20	31..16	temperature	temperature in 0.0625 deg. C units
9	0x24	31..16	serial_cmc	Serial number CMC board
9	0x26	15..0	version_fw	firmware version (SVN revision)

All registers are implemented as 32-bit registers, so they can be mapped easily into some VME address space for example if one decides to build a VME board containing the DRS4.

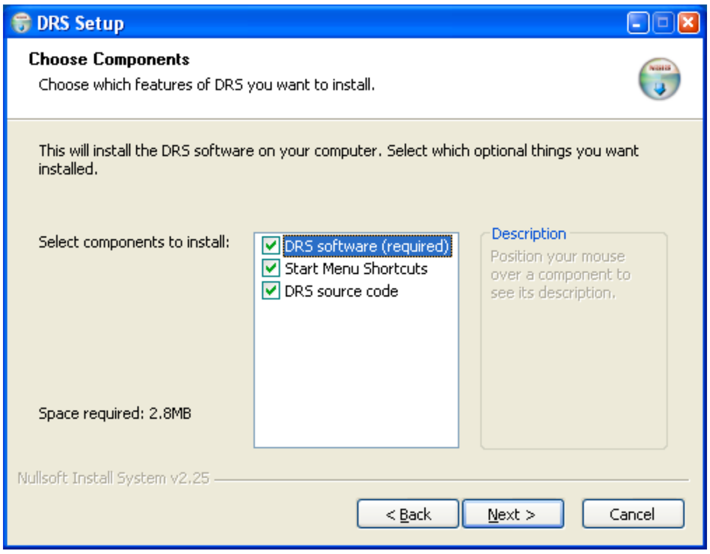
2. Installation

2.1. Windows XP

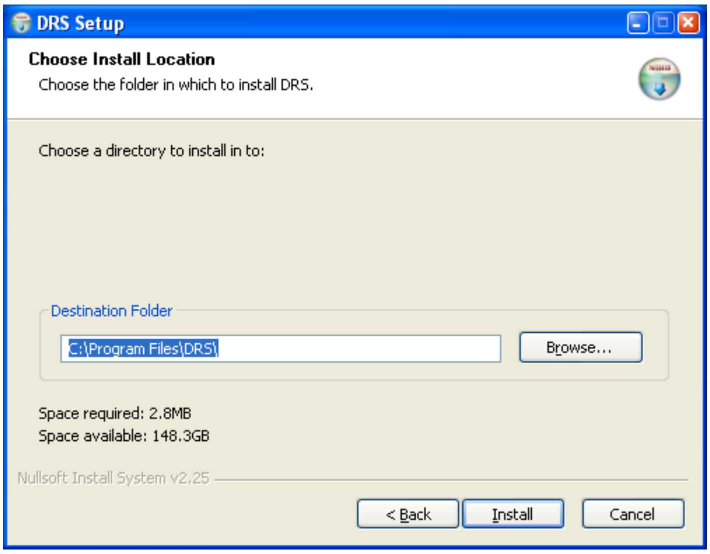
Under MS Windows® it is important to install the necessary driver before connection the DRS4 Evaluation Board with the PC. The current distribution can be downloaded from http://drs.web.psi.ch/download . The Windows version contains a single program **`drs-xx.exe`** (where **`xx`** is the version) which can be executed to install the driver, applications, documentation and source code. Executing this file starts the installer:



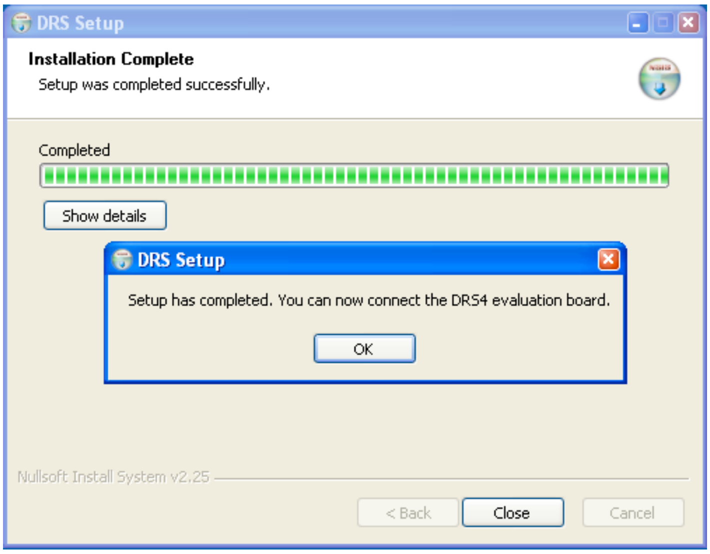
You can select which components to be installed:



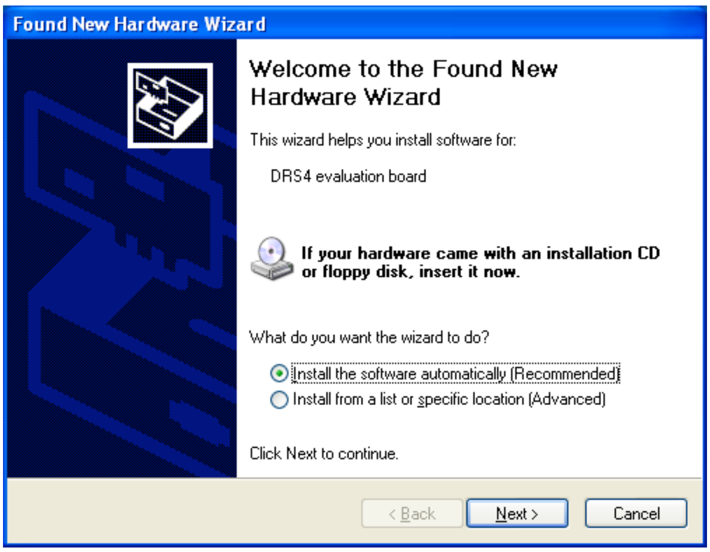
Then you can select the installation directory:



After the installer has finished, you can connect the DRS4 Evaluation Board to the Computer:

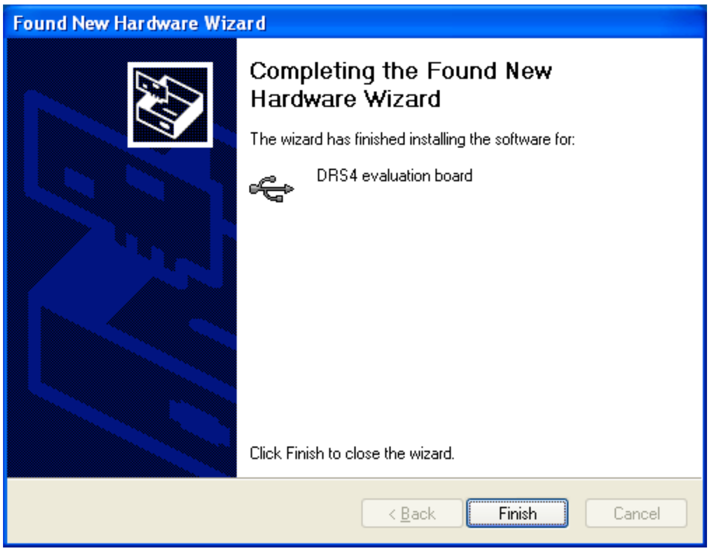


Now you will see the "Found New Hardware" dialog:

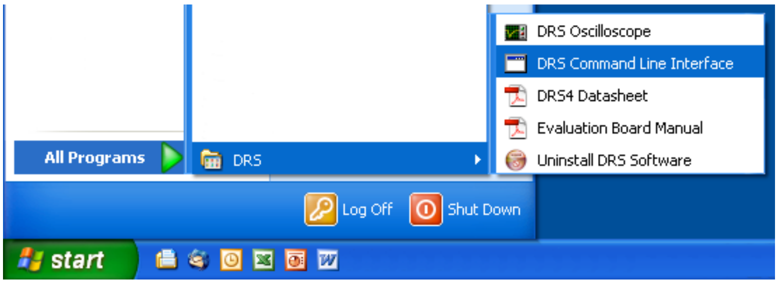


Where you can click "Install the software automatically" and then click "Next".

After successful installation of the driver, you will see the following window:



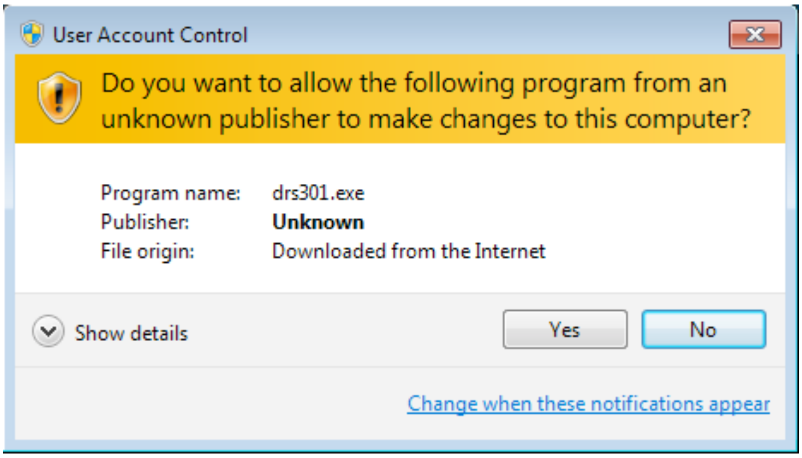
And a new group in your Start Menu:



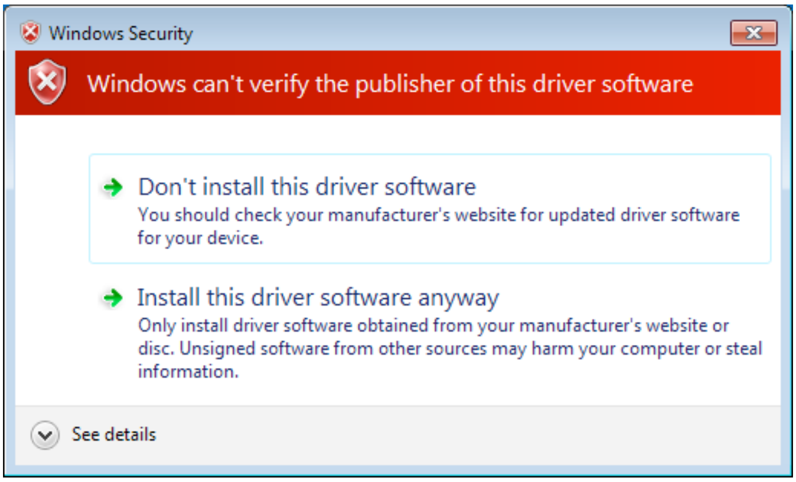
The software comes with two applications, a command line interface and an oscilloscope. These applications are explained in section 3.

2.2. Windows 7

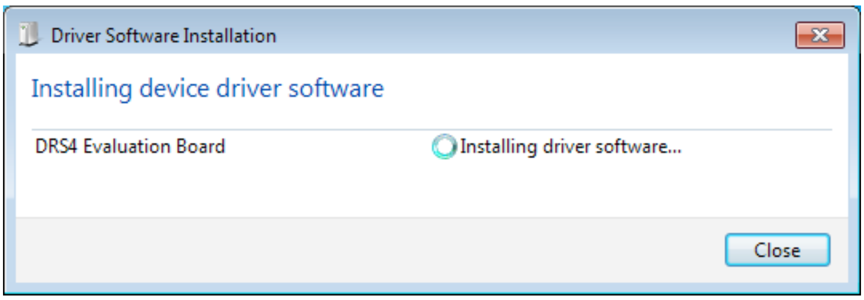
The installation under Windows 7 (32 and 64 bit) is basically the same than for Windows XP. You need the DRS software version 3.0.1 or later if you are using a 64-bit system, since version 3.0.0 and prior does not contain the 64-bit version of the **libusb** library. When you start the software installation, you get an additional screen which you have to confirm:



Make sure that you are logged in as an administrator to install the software. During the installation process, you will see a notice about some unverified driver software. Please select *"Install this driver software anyway"* to install the driver.



After the software has been installed, you can connect the DRS4 Evaluation Board to the computer. The driver installation should then start automatically and you will see this notification:



When this has finished, you can start the "drscl" and "drsosc" programs.

2.3. Linux

The drivers and applications are distributed for Linux in source code and must be compiled on each system. First untar the tar ball:

```
[/usr/local]$ tar -xzvf drs-1.0.tar.gz
drs-1.0/
drs-1.0/doc/
drs-1.0/doc/DRS4_rev06.pdf
drs-1.0/doc/manual.pdf
drs-1.0/include/
drs-1.0/include/ConfigDialog.h
drs-1.0/include/DOFrame.h
drs-1.0/include/DOScreen.h
. . .
```

Then change the directory and do a „make". Note that to compile the oscilloscope application it is necessary to have the wxWidgets package version 2.8.9 or later installed. You can obtain this package in source form from http://www.wxwidgets.org/downloads/. If this package is present, you can change to the drs directory and issue a make:

```
[/usr/local]$ cd drs-1.0
[/usr/local/drs-1.0]$ make
g++ -g -O2 -Wall -Wuninitialized -fno-strict-aliasing -Iinclude -DOS_LINUX
-DHAVE_LIBUSB -c src/musbstd.c
g++ -g -O2 -Wall -Wuninitialized -fno-strict-aliasing -Iinclude -DOS_LINUX
-DHAVE_LIBUSB -c src/mxml.c
...
```

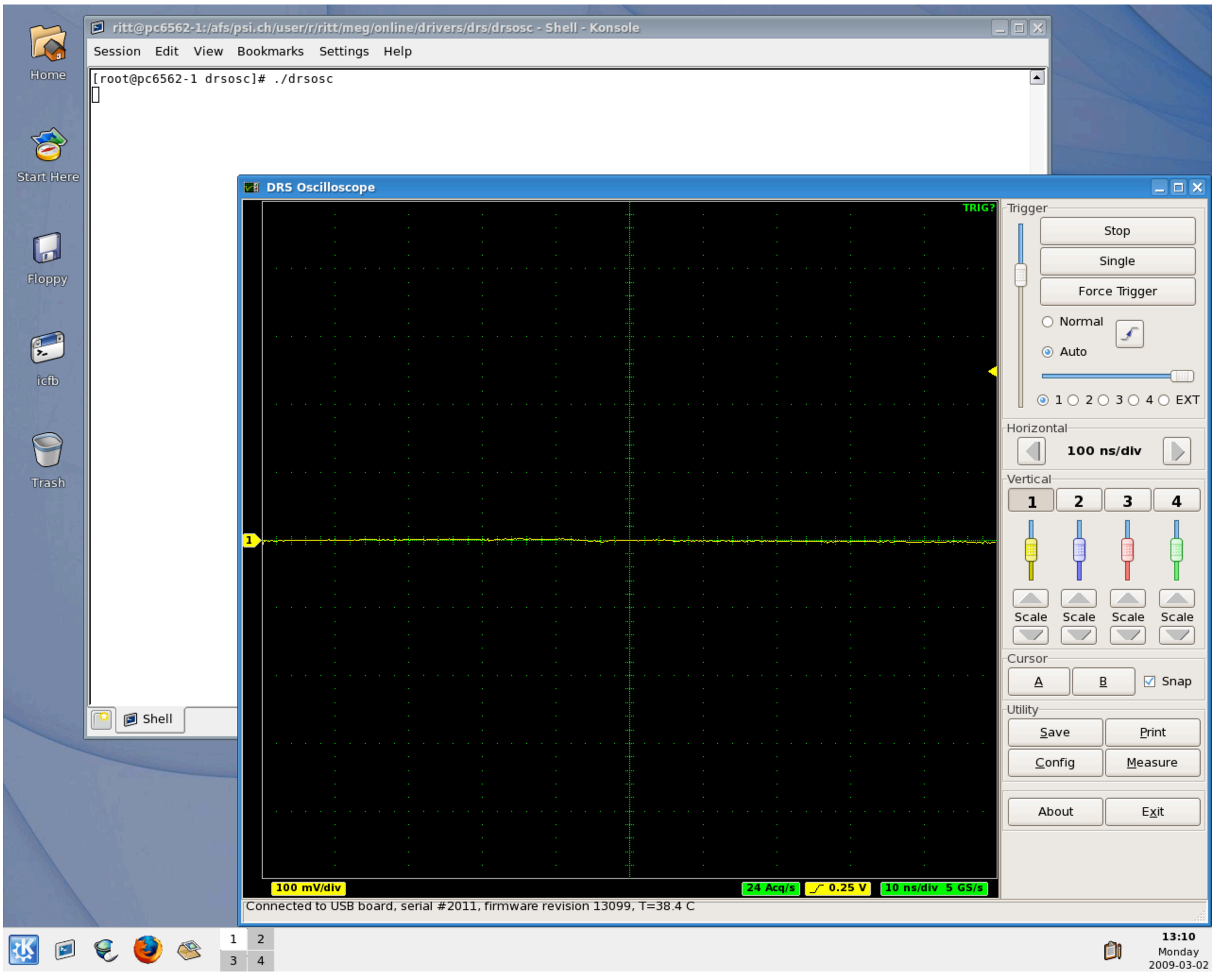
Now you can connect the DRS4 board to the PC. On systems where the "lsusb" tool is installed, one should be able to find the DRS4 evaluation board after connecting it with following command:

```
[/usr/local/drs-1.0]$ /sbin/lsusb -d 04b4:1175 -v

Bus 005 Device 005: ID 04b4:1175 Cypress Semiconductor Corp.
Device Descriptor:
  bLength                18
  bDescriptorType         1
  bcdUSB               2.00
  bDeviceClass            0 (Defined at Interface level)
  bDeviceSubClass         0
  bDeviceProtocol         1
  bMaxPacketSize0        64
  idVendor           0x04b4 Cypress Semiconductor Corp.
  idProduct          0x1175
  bcdDevice            0.01
  iManufacturer           1 S. Ritt PSI
  iProduct                2 DRS4 Evaluation Board
  iSerial                 3 REV1
  bNumConfigurations      1
  Configuration Descriptor:
    bLength                 9
    bDescriptorType         2
    wTotalLength           46
    bNumInterfaces          1
    bConfigurationValue     1
    iConfiguration          0
    bmAttributes         0x80
    MaxPower              500mA
...
```

If the board is correctly recognized, one can access it with the command line program. Under most Linux distributions however, only the "root" user can directly access USB devices. Some systems can be configured to allow non-root access via the "udev" system, but the exact instructions vary from distribution to distribution and can therefore not be given here.

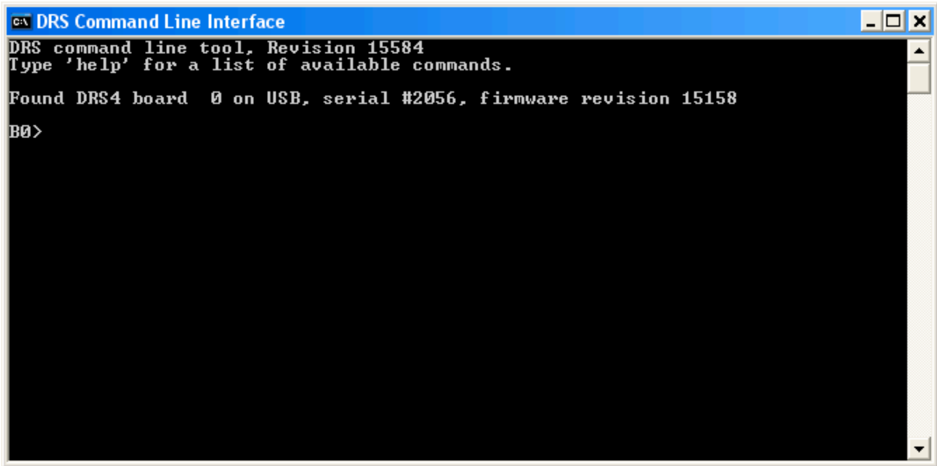
If the command line program works, the oscilloscope application "drsosc" can be started. It will open a X window and show exactly the same functionality as its Windows counterpart:



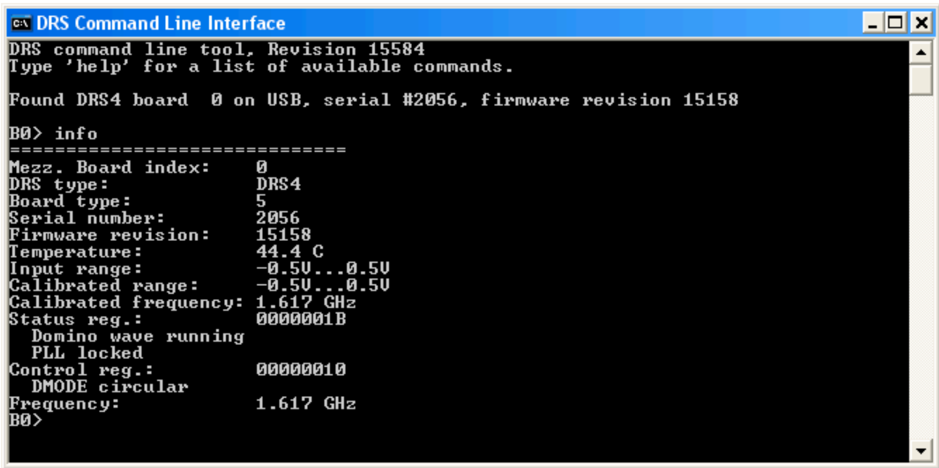
3. Running the Board

3.1. Command line Interface "drscl"

Clicking on „DRS Command Line Interface“ (Windows) or entering "drscl" (Linux) will start a simple application which connects to the DRS4 Evaluation Board. If it finds the board, it displays the board serial number and the firmware revision as on the following screen shot:

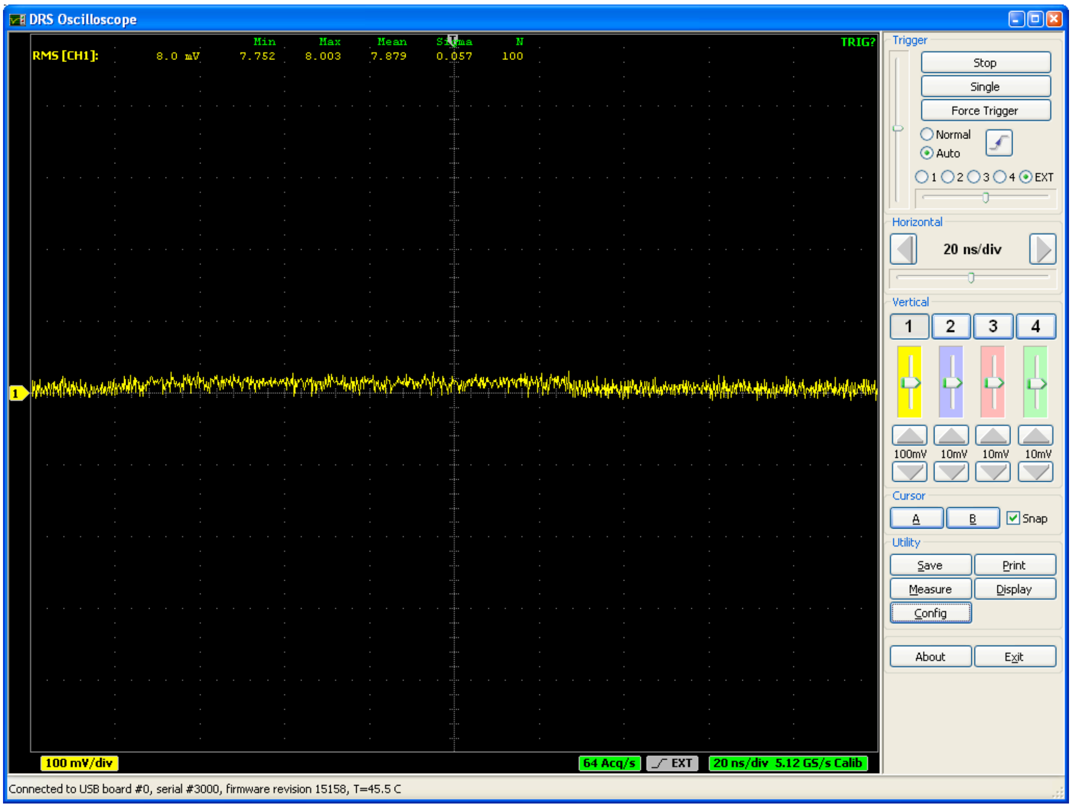


Now you are ready to issue your first command "info" which shows some more information, like the current board temperature. The temperature sensor is on the bottom side just below the DRS4 chip. If you keep issuing "info" commands and touch that sensor with your finger, you should see the temperature increase.

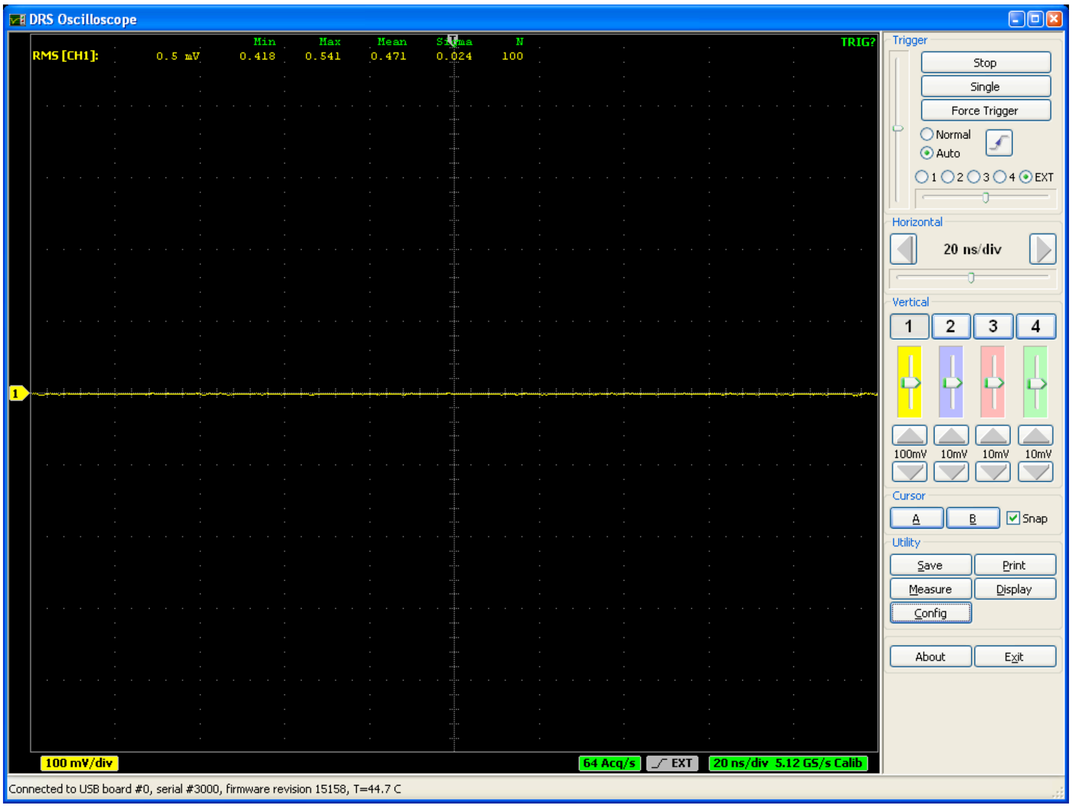


3.2. Oscilloscope application "drsosc"

The second application is an oscilloscope-like program, which connects to the DRS4 board and works pretty much like a normal oscilloscope. You can select the trigger mode, trigger level and trigger source. On Rev. 1.1 of the DRS4 evaluation board, only CH1 can be selected as trigger source. You enable a channel by clicking on the number "1" to "4". There are two cursors and a few utilities.

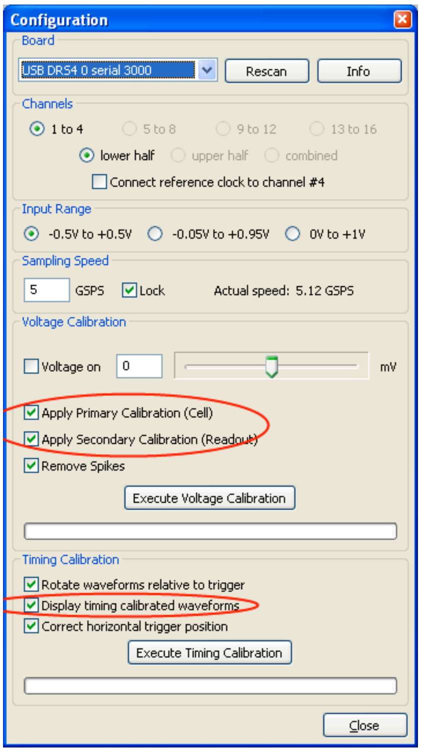


The picture above shows an un-calibrated evaluation board, which shows a noise level of about 8 mV RMS. After offset and gain calibrations, the noise level is reduced significantly:

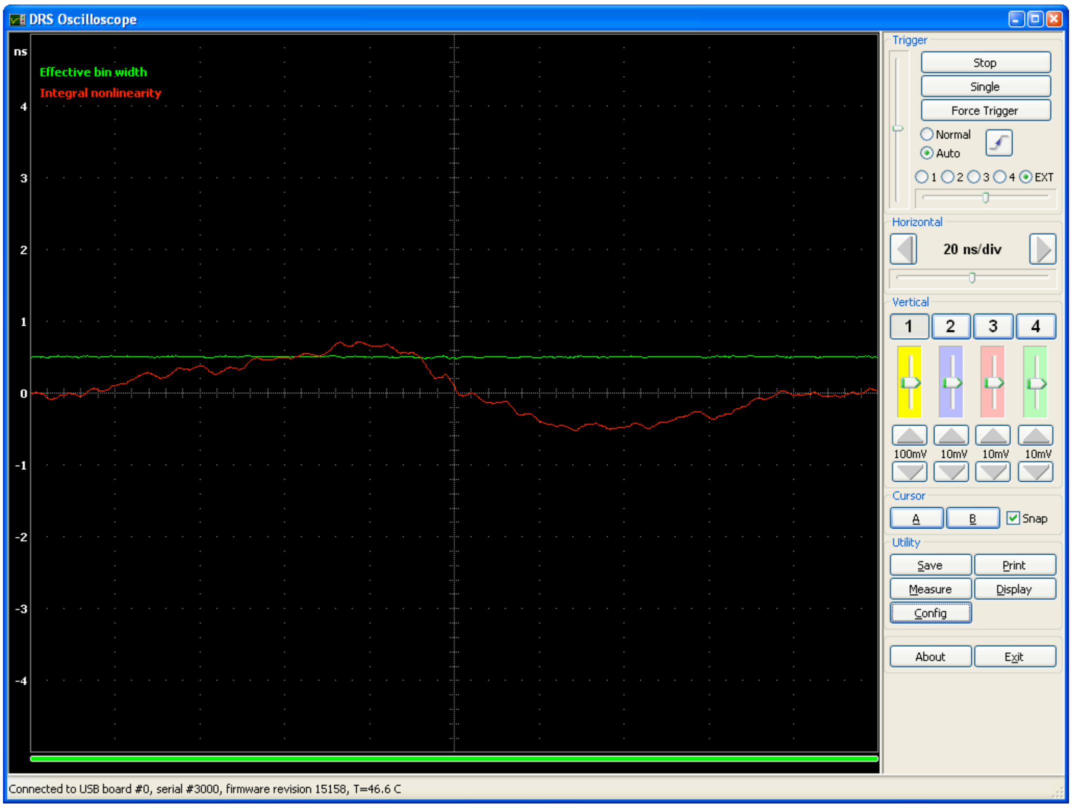


The evaluation board Rev. 3 still shows some small random spikes. It is expected that future versions will improve this and reduce the noise level further.

The DRS4 evaluation board is shipped pre-calibrated in amplitude and time. This calibration can be turned on or off using the check boxes "Display calibrated waveforms" and "Display timing calibrated waveforms" in the "Config" Dialog:

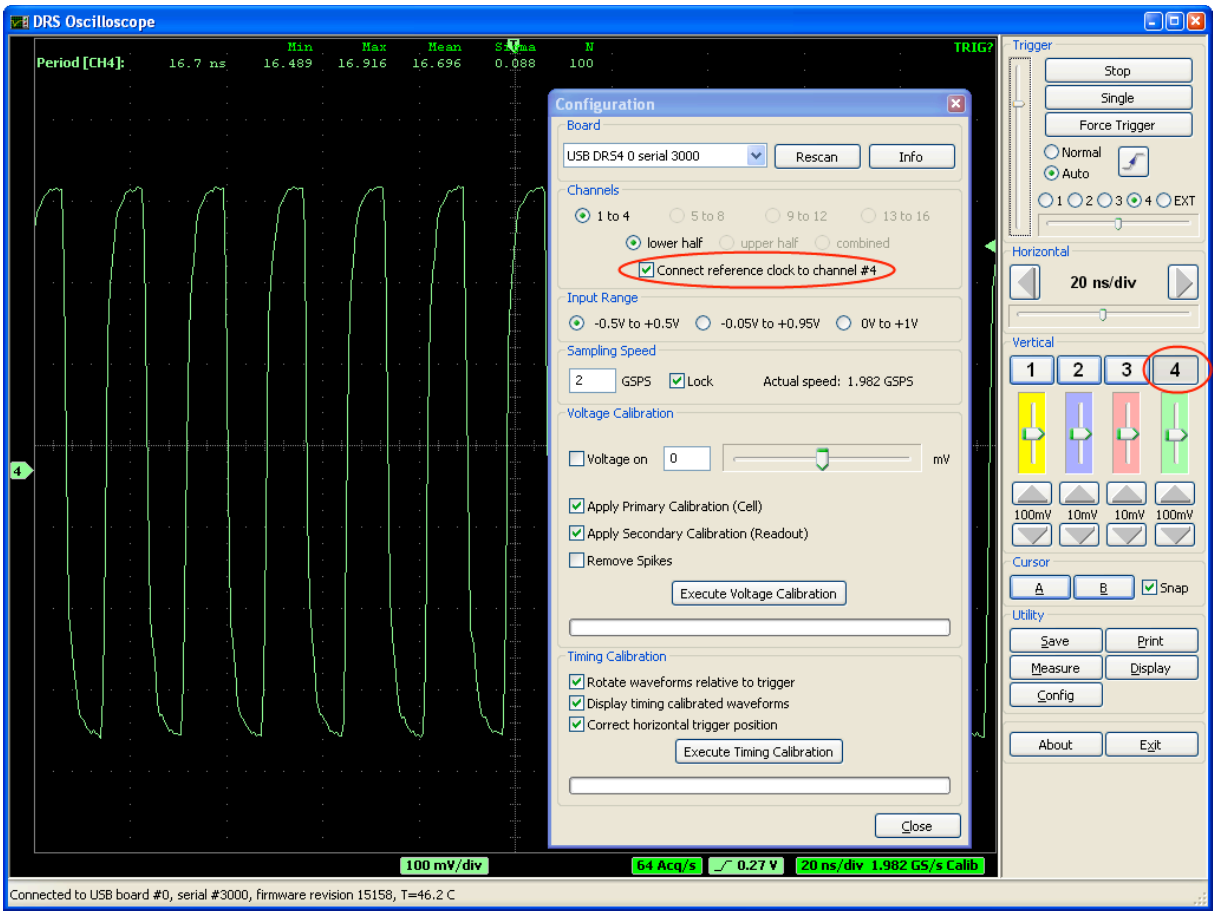


The calibration can be re-done any time by clicking on the "Execute Voltage Calibration" and "Execute Timing Calibration" buttons. For the voltage calibration, the inputs are switched to a calibration voltage generated by a DAC. Three calibration points (-0.4V, 0V, +0.4V) are taken and an offset and gain is evaluation. For the timing calibration, an internal 240 MHz clock is sampled in one channel and the deviation from the expected period to the measured period is used to determine the effective width of each cell. Following picture shows the result of such a timing calibration done at 2 GSPS. The effective bin width deviates only slightly from the nominal value of 0.5 ns, but the integral timing nonlinearity adds up to almost 1 ns, which is typical for the DRS4 chip. Since transistor parameters have normally gradients over the chip wafer, SCA chips are usually "faster" on one side compared to the other.



This calibration data both for voltage and timing is then stored in the EEPROM on the evaluation board, from where it is obtained each time the oscilloscope gets started. This assures that a board is calibrated even when used on different computers. Note however that the timing calibration is only valid for some sampling speed. So if you want to run the board at a different speed, you have to redo the timing calibration at that speed. The voltage calibration is a bit less dependent on the sampling speed, there is however some dependence on temperature. It is advised to keep the board running for a few minutes until the temperature shown in the status bar stabilizes before doing a voltage calibration.

For test purposes, an internal 60 MHz reference clock signal can be connected to channel #4 via the "Config" menu. To do so, activate channel #4, then select the "Config" menu and click on "Connect reference clock to channel #4":



The effect of the timing calibration can be tested by turning the timing calibration on and off via the "Display timing calibrated waveforms" check box.

You can save a waveform in an ASCII and a binary format by pressing the "Save" button. After you open a file, each trigger will write the waveform of the active channel(s) to that file. When you are continuously running, the file will grow very quickly. If the file has the extension ".xml" it will be written in ASCII form using XML encoding, otherwise a raw binary file will be written. Here is a snipped of such an XML file:

```
<?xml version="1.0" encoding="ISO-8859-1"?>
<!-- created by MXML on Tue Feb 15 13:05:04 2011 -->
<DRSOSC>
  <Event>
    <Serial>1</Serial>
    <Time>2011/02/15 13:05:04.758</Time>
    <HUnit>ns</HUnit>
    <VUnit>mV</VUnit>
    <CHN1>
      <Data>20.7,-63.7</Data>
      <Data>21.7,-62.3</Data>
      ...
      <Data>1033.4,424.9</Data>
      <Data>1034.4,423.3</Data>
    </CHN1>
    <CHN2>
      <Data>20.7,-8.5</Data>
      <Data>21.7,-7.0</Data>
      ...
      <Data>1033.4,-8.3</Data>
      <Data>1034.4,-8.2</Data>
    </CHN2>
  </Event>
  <Event>
    <Serial>2</Serial>
    <Time>2011/02/15 13:05:04.883</Time>
    <HUnit>ns</HUnit>
    <VUnit>mV</VUnit>
    <CHN1>
      <Data>20.6,-63.0</Data>
      <Data>21.6,-63.8</Data>
      ...
```

Each individual event contains a header with the serial number of that event (starting with 1), and the date/time it was recorded. Then there is the channel data with pairs of time (in ns) and voltage (in mV). The number of channels depend on which channel was on when the data was recorded. It might be a single channel (CHN1) or all four channels (CHN1-CHN4). Please note that the XML format requires more space on your storage and takes also more CPU power to be written, so the maximum data rate is limited.

The binary format requires less space and can be written faster, but it requires a special program to read and analyze the data.

Word	Byte 0	Byte 1	Byte 2	Byte 3	Contents
0	'E'	'H'	'D'	'R'	Event Header
1	Serial number				Serial number starting with 1
2	Year		Month		Event date/time 16-bit values
3	Day		Hour		
4	Minute		Second		
5	Millisecond		*reserved*		
6	Time Bin #0				Time of sample bins in ns encoded in 4-Byte floating point format
7	Time Bin #1				
…	…				
1029	Time Bin 1023				
1030	'C'	'0'	'0'	'1'	Channel 1 header
1031	Voltage Bin #0		Voltage Bin #1		Channel 1 waveform data encoded in 2-Byte integers. 0=-0.5V and 65535=+0.5V
1032	Voltage Bin #2		Voltage Bin #3		
…	…		…		
1542	Voltage Bin #1022		Voltage Bin #1023		
1543	'C'	'0'	'0'	'2'	Channel 2 header
1544	Voltage Bin #0		Voltage Bin #1		Channel 2 waveform data encoded in 2-Byte integers. 0=-0.5V and 65535=+0.5V
1545	Voltage Bin #2		Voltage Bin #3		
…	…		…		
2055	Voltage Bin #1022		Voltage Bin #1023		
2056	'E'	'H'	'D'	'R'	Next Event Header
…					

Depending on the number of channels which are "on" during data acquisition, the file contains up to four channels, which can be identified by their channel headers. Then the next event follows, which can be identified by the event header 'EHDR'. All multi-byte data is encoded with LSB first, as in all Intel PC systems.

4. Development Hints

The idea behind the evaluation board is to make first steps in using the DRS4 chip, but then develop your own custom electronics around the chip. The first thing to do there is to study carefully the DRS4 data sheet, which can be obtained from http://drs.web.psi.ch/datasheets. Then have a look at the DRS4 Evaluation Board Reference Design, which schematics is supplied at the end of this document. When you start to design your own electronics, there are however some important points, which are not necessarily obvious from the data sheet or from the reference design. These points together with some design tips are explained in this section.

4.1. Power Supply

As with any analog design, the quality of the power supply is very important, since it has an influence of the noise level measured by the DRS4 chip. Low noise linear regulators together with the usual decoupling capacitors are recommended for all power supplies. The analog power supply AV_{DD} powers only the domino circuit of the DRS4 chip and directly influences the jitter of the sampling frequency. Long term variations in this power supply (seconds…) are regulated by the on-chip PLL, but high frequency noise in the MHz region leads directly to an increase of the PLL jitter. Therefore the evaluation board contains two separate 2.5V linear regulators for the DRS4 chip, one for the AV_{DD} power and one for the DV_{DD} power. Although the DV_{DD} power is called "digital power", it powers also the analog output buffers of the DRS4 chip and needs the same good quality than the AV_{DD} power in order to minimize the noise of the board.

The DRS4 chip also contains two grounds AGND and DGND. They can be either routed separately on the board and be connected at the power source, or they can be directly connected to an overall dedicated ground plane of the PCB. Tests have been shown that the latter choice gives slightly less noise.

The bottom of the QFN76 package of the DRS4 has an exposed paddle connected to the internal DGND. It is recommended that this paddle is matched by a PCB pad of similar size connected to analog ground to achieve the best electrical and thermal performance of the DRS4. The copper plane should have several vias to achieve a good heat dissipation to flow through the PCB as shown in Figure 3:

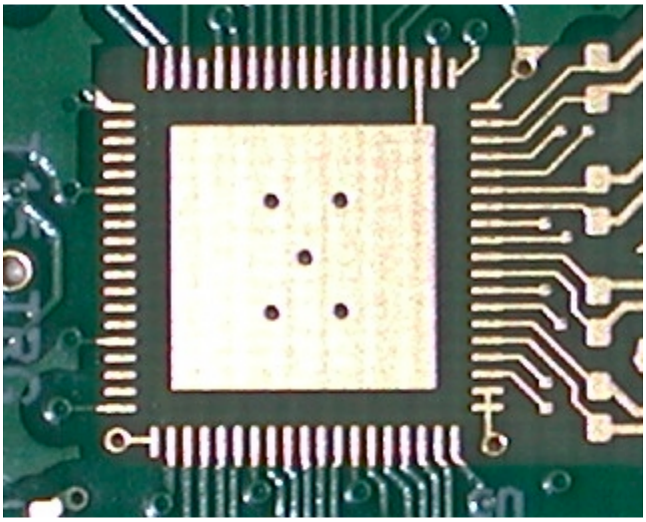


Figure 3: PCB pad under the DRS4 chip

These vias should be solder-filled or plugged. The maximum power dissipation of the DRS4 chip is not critical (350 mW), but an improved thermal stability helps the performance of any analog chip. To maximize the coverage and adhesion between the DRS4 and the PCB, the copper plane could be partitioned into several uniform sections, providing several tie points during the reflow process.

4.2. Analog Input

If non-differential signals should be digitized with the DRS4 chip, they must be converted into differential signals for the DRS4 inputs. The simplest solution is to connect the IN- inputs to AGND and to connect the signals directly to the IN+ inputs. This method has however the disadvantage that the crosstalk and noise immunity of the DRS4 chip are worsened. The evaluation board V3 uses differential drivers THS4508 from Texas Instruments® for this purpose. These drivers were carefully selected since they have to drive the relatively high DRS4 input current of almost 1 mA and capacitive load without compromising the analog bandwidth. The current design gives about 700 MHz (-3 dB) with moderate power consumption, so that the evaluation board can still be powered from the USB power (500 mA @ 5V). The linear regulator of the evaluation board V2 could however not be used, since the efficiency would be too low. Instead, a switching regulator LMZ10503 from National Semiconductor® is used on the board. It has an efficiency of more than 95% and a low output ripple. The output voltage of 3.3V is then converted using traditional linear regulators into two 2.5V low noise power supplies, which power the analog part of the board.

Other designs are possible which push the analog bandwidth to 800 or 900 MHz, close to the theoretical limit of 950 MHz of the DRS4 chip, but they require more power.

The usual design rules like proper termination, matched impedance PCB traces and separate power supply PCB planes apply as in any high frequency analog design.

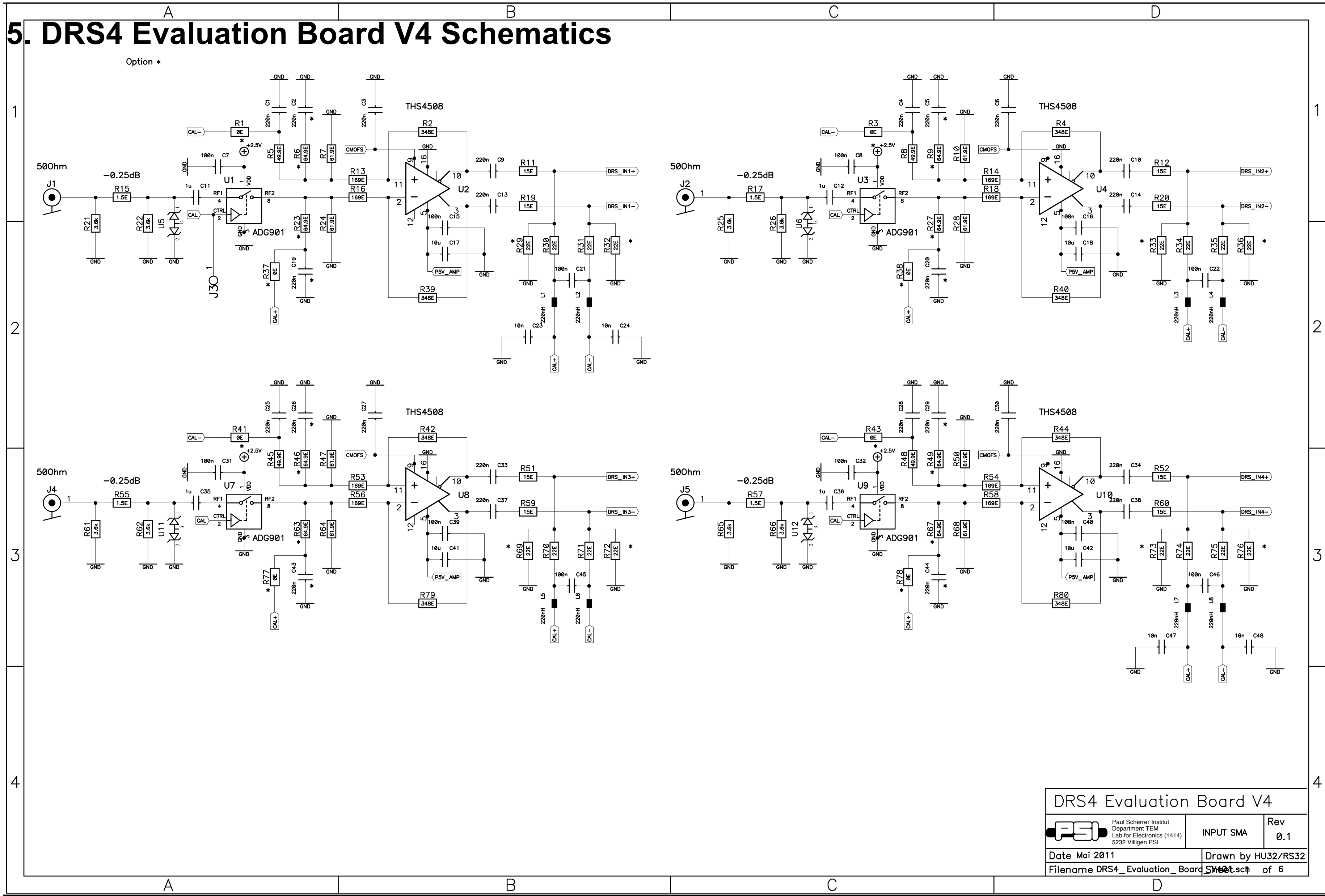
4.3. Control Voltages

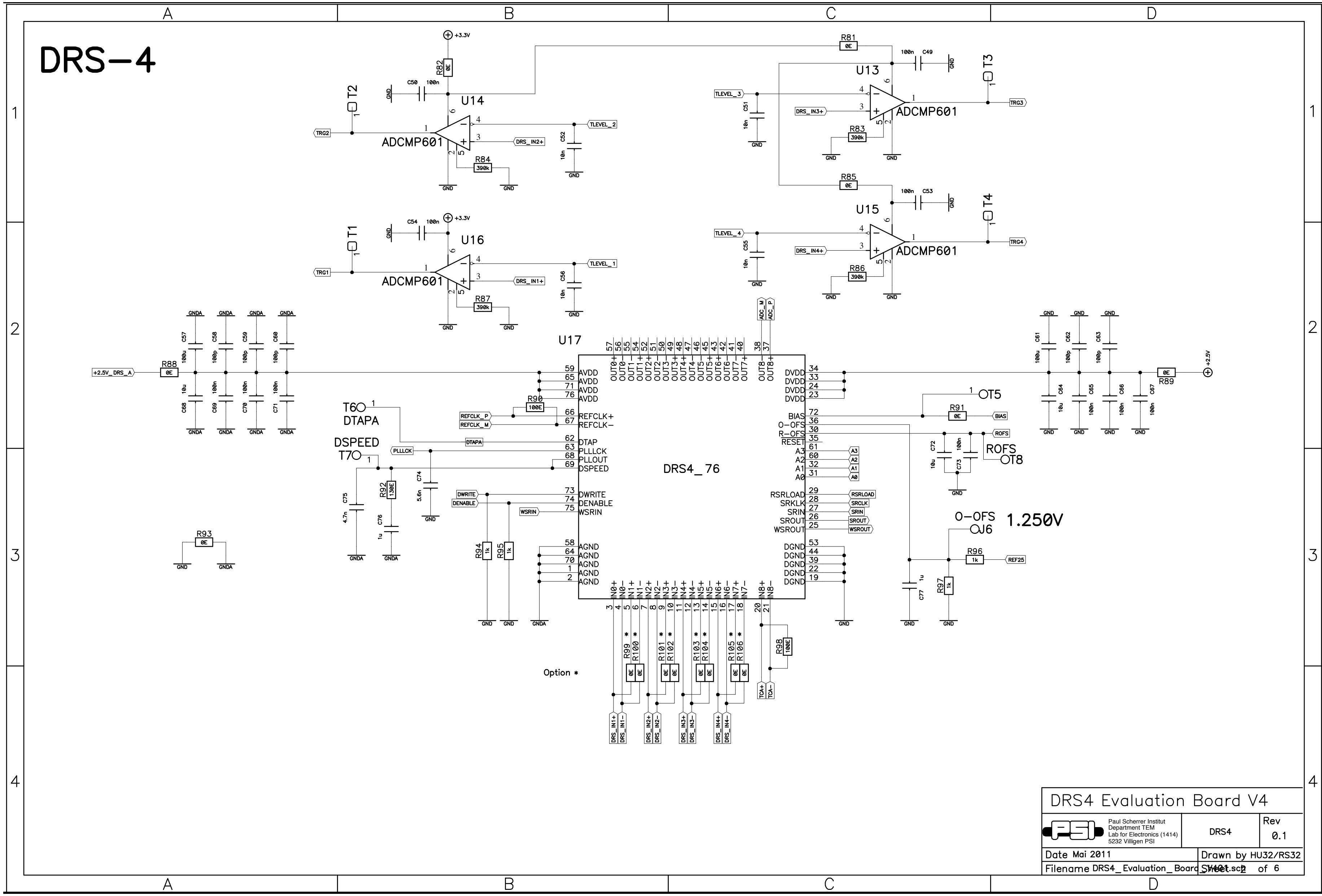
The DRS4 chip requires certain control voltages: ROFS, O-OFS and BIAS. The latter two are generated internally with some default voltage, but can be "overwritten" by an external low impedance source. It is recommended to connect these lines to an external 16-bit DAC, so that the DRS4 input range can be fine-tuned on a board-by-board basis, to compensate for chip variations. The ROFS signal should be driven by a high speed low noise buffer. If this signal would be directly connected to the DAC output, the signal height would change slightly during the chip readout and the measurement would show a varying baseline level.

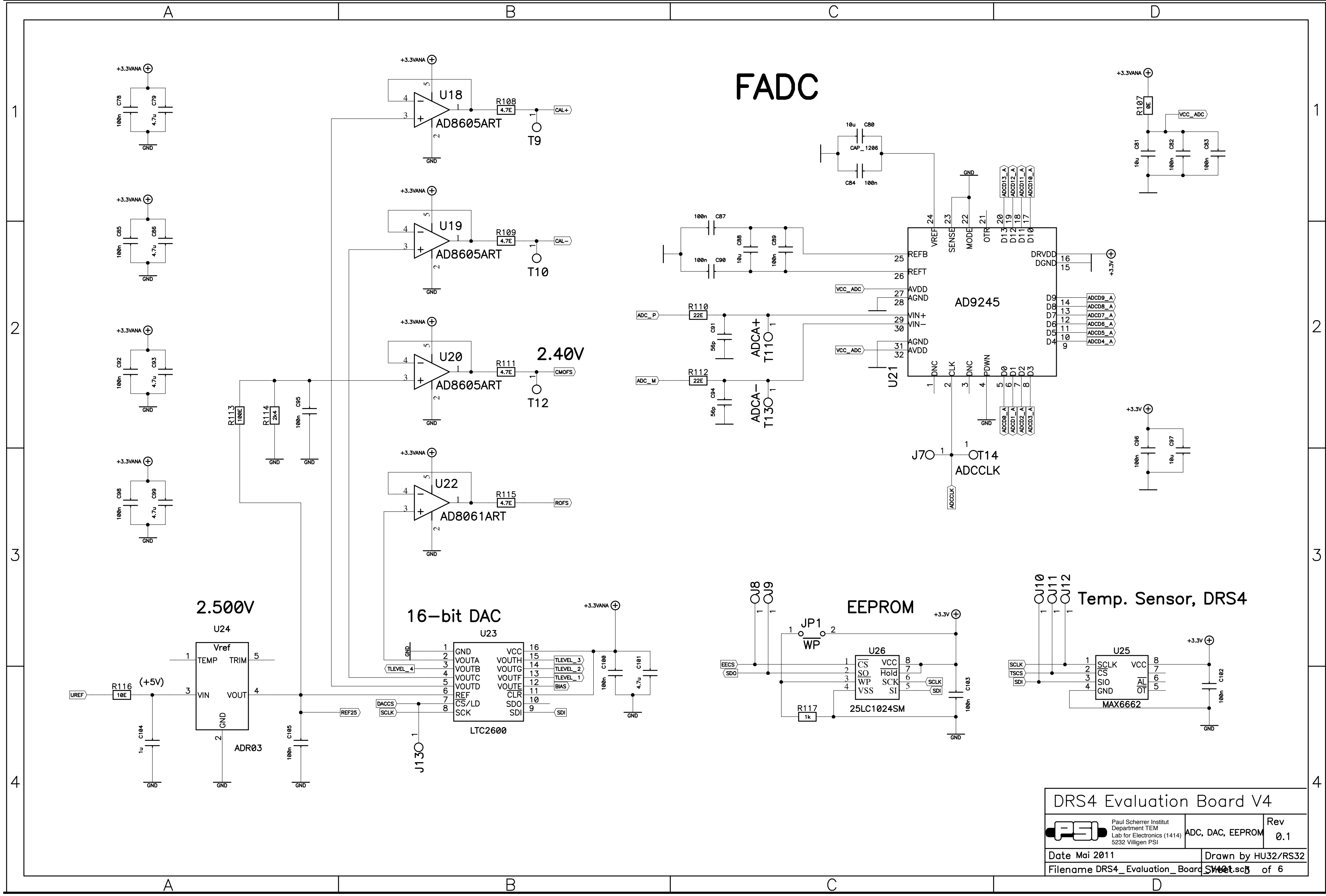
4.4. ADC Clock

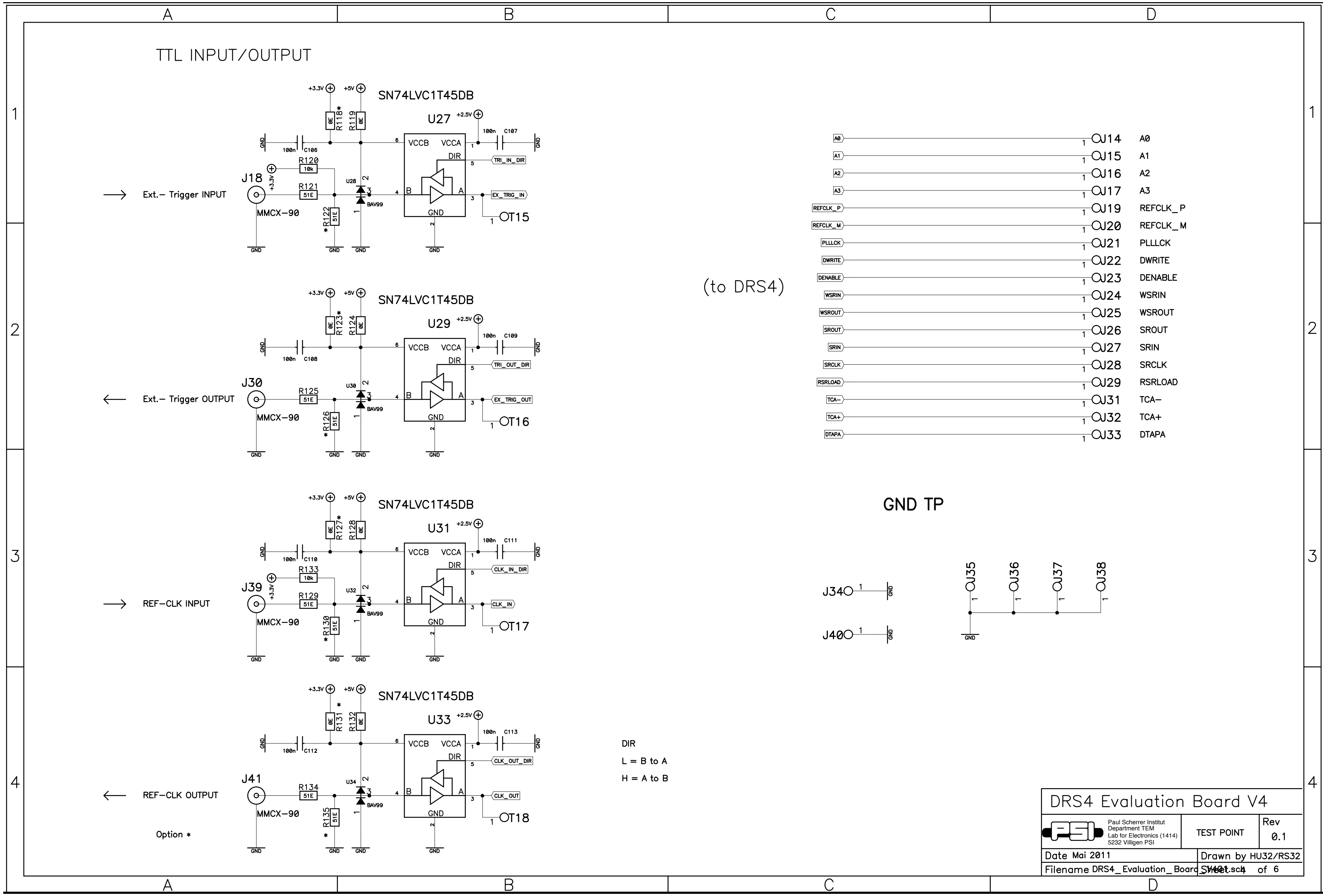
There is a very strict relation between the DRS4 output shift register clock SRCLK and the ADC clock (see DRS4 data sheet WAVEFORM READOUT). In order to reduce the noise due to aperture jitter, the phase shift between these two clocks must be fixed and contain very small jitter (~10ps). The easiest way to generate this phase shift is to use the digital clock managers (DCM) in the FPGA, as it is done on the evaluation board. Since the DCMs have however an inherent phase jitter of up to 150ps, this introduces some noise in form of a baseline variation when sampling a DC signal in the order of up to a few mV. If this becomes a problem, it is recommended to generate the phase shift between these two clocks with a low jitter delay circuit.

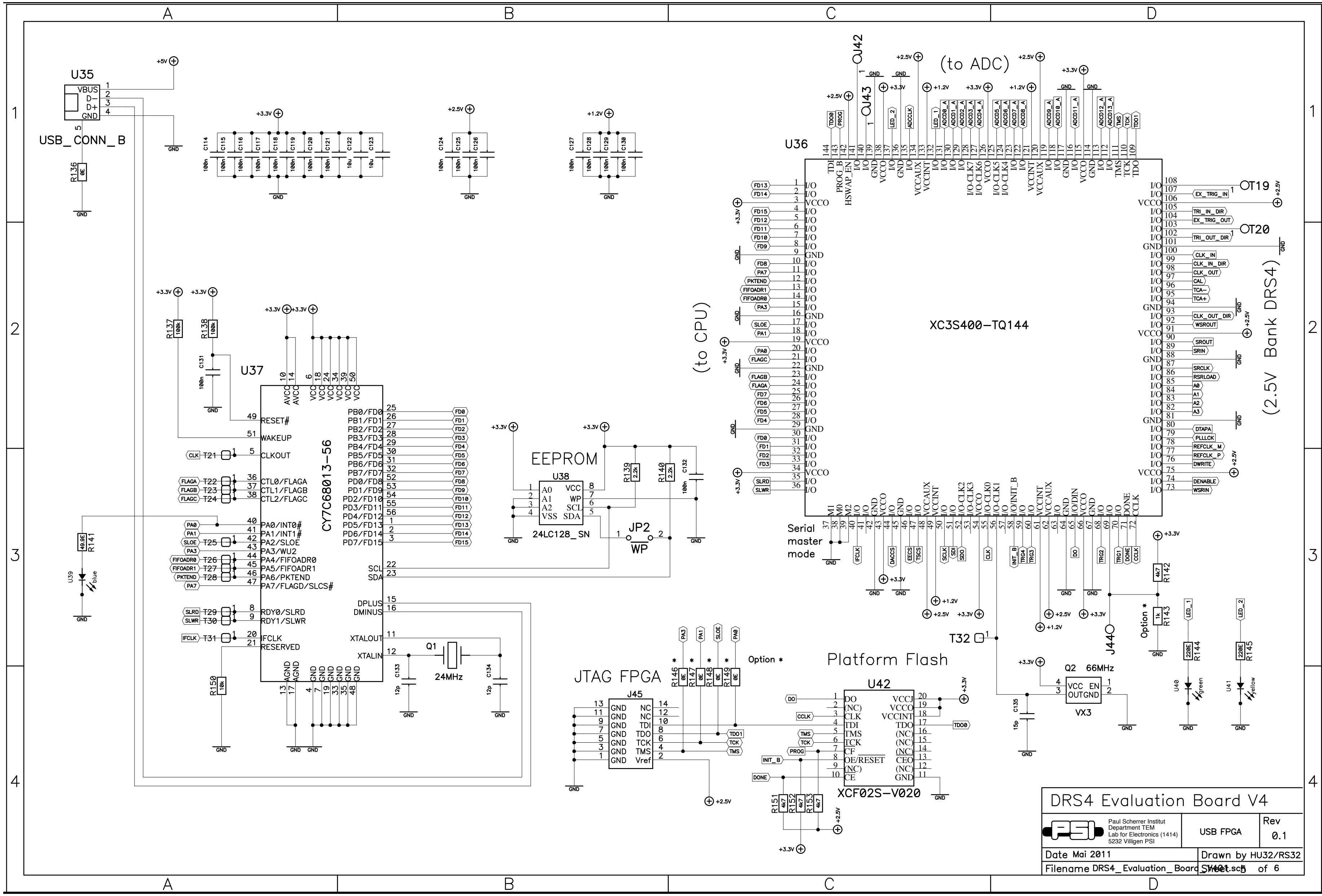
5. DRS4 Evaluation Board V4 Schematics

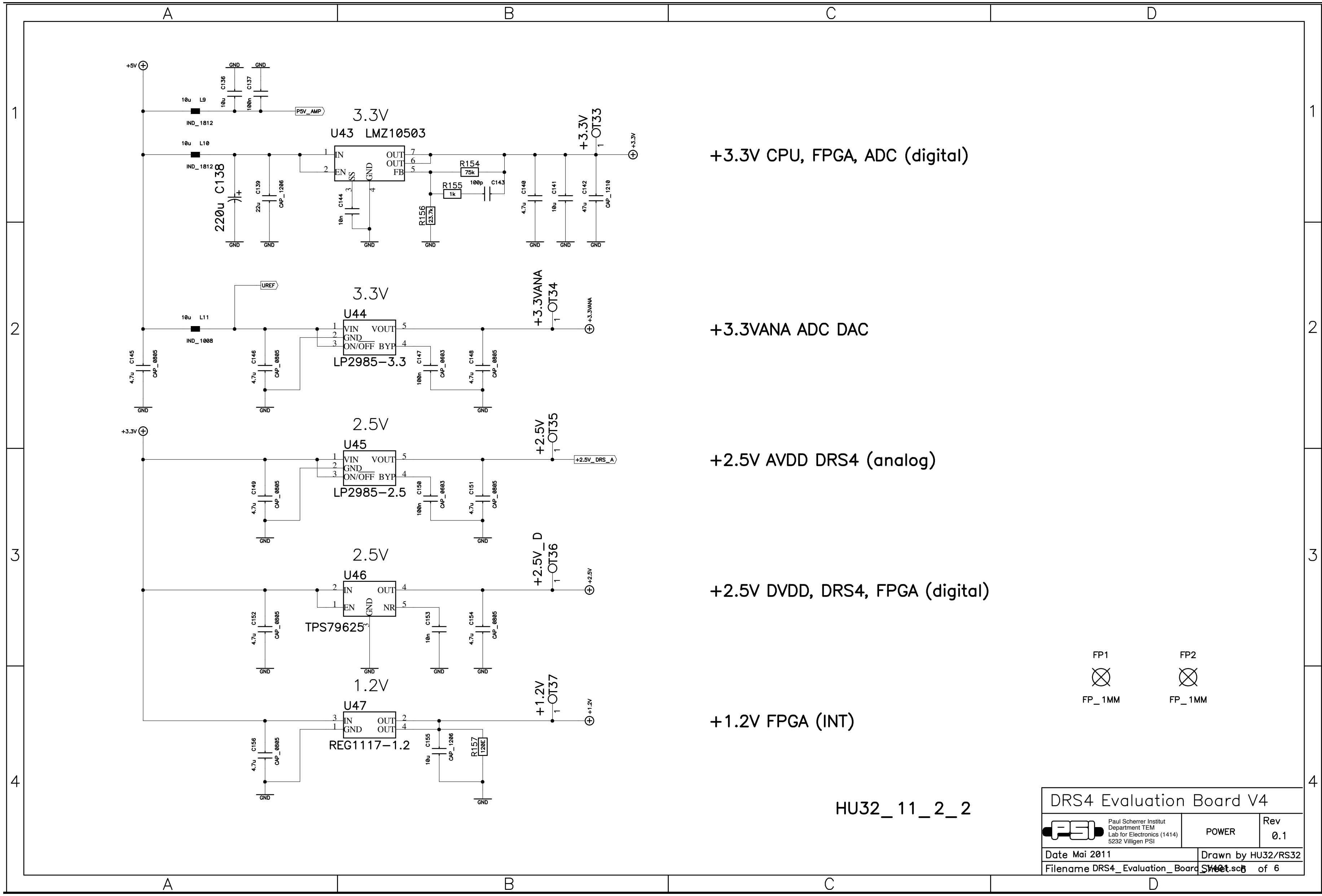



DRS-4
U14
ADCMP601
U16
ADCMP601
U13
ADCMP601
U15
ADCMP601
T1
T2
T3
T4
U17
DRS4_76
T6 DTAPA
DSPEED T7
T5
ROFS T8
O-OFS J6
1.250V
R81 0E
R82 0E
R83 390k
R84 390k
R85 0E
R86 390k
R87 390k
R88 0E
R89 0E
R90 100E
R91 0E
R92 130E
R93 0E
R94 1k
R95 1k
R96 1k
R97 1k
R98 100E
TRG1
TRG2
TRG3
TRG4
TLEVEL_1
TLEVEL_2
TLEVEL_3
TLEVEL_4
DRS_IN1+
DRS_IN2+
DRS_IN3+
DRS_IN4+
+2.5V_DRS_A
+3.3V
+2.5V
AVDD
REFCLK+
REFCLK-
DTAP
PLLLCK
PLLOUT
DSPEED
DWRITE
DENABLE
WSRIN
AGND
DVDD
BIAS
O-OFS
R-OFS
RESET
A3
A2
A1
A0
RSRLOAD
SRCLK
SRIN
SROUT
WSROUT
DGND
REF25
Option *
DRS4 Evaluation Board V4
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
DRS4
Rev
0.1
Date Mai 2011
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V4.sch
Sheet 2 of 6


FADC
AD9245
U21
U18
U19
U20
U22
AD8605ART
AD8061ART
2.40V
2.500V
U24
ADR03
16-bit DAC
U23
LTC2600
EEPROM
U26
25LC1024SM
Temp. Sensor, DRS4
U25
MAX6662
ADCCLK
DRS4 Evaluation Board V4
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
ADC, DAC, EEPROM
Rev 0.1
Date Mai 2011
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V4.sch
Sheet 5 of 6


TTL INPUT/OUTPUT
SN74LVC1T45DB
U27
Ext.– Trigger INPUT
J18
MMCX–90
TRI_IN_DIR
EX_TRIG_IN
T15
SN74LVC1T45DB
U29
Ext.– Trigger OUTPUT
J30
MMCX–90
TRI_OUT_DIR
EX_TRIG_OUT
T16
SN74LVC1T45DB
U31
REF–CLK INPUT
J39
MMCX–90
CLK_IN_DIR
CLK_IN
T17
SN74LVC1T45DB
U33
REF–CLK OUTPUT
J41
MMCX–90
CLK_OUT_DIR
CLK_OUT
T18
Option *
(to DRS4)
J14 A0
J15 A1
J16 A2
J17 A3
J19 REFCLK_P
J20 REFCLK_M
J21 PLLLCK
J22 DWRITE
J23 DENABLE
J24 WSRIN
J25 WSROUT
J26 SROUT
J27 SRIN
J28 SRCLK
J29 RSRLOAD
J31 TCA–
J32 TCA+
J33 DTAPA
GND TP
J34
J40
J35
J36
J37
J38
DIR
L = B to A
H = A to B
DRS4 Evaluation Board V4
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
TEST POINT
Rev
0.1
Date Mai 2011
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V4.sch
Sheet 4 of 6


U35
USB_CONN_B
U37
CY7C68013-56
EEPROM
U38
24LC128_SN
JP2
WP
Q1
24MHz
JTAG FPGA
J45
Platform Flash
U42
XCF02S-V020
Option *
U36
XC3S400-TQ144
(to ADC)
(to CPU)
(2.5V Bank DRS4)
Serial master mode
Q2 66MHz
VX3
DRS4 Evaluation Board V4
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
USB FPGA
Rev 0.1
Date Mai 2011
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V4.sch
Sheet 5 of 6


+5V
P5V_AMP
3.3V
U43 LMZ10503
+3.3V
OT33
220u C138
R154
R155
R156
+3.3V CPU, FPGA, ADC (digital)
UREF
3.3V
U44
LP2985-3.3
+3.3VANA
OT34
+3.3VANA ADC DAC
+3.3V
2.5V
U45
LP2985-2.5
+2.5V
OT35
+2.5V_DRS_A
+2.5V AVDD DRS4 (analog)
2.5V
U46
TPS79625
+2.5V_D
OT36
+2.5V DVDD, DRS4, FPGA (digital)
FP1
FP2
FP_1MM
FP_1MM
1.2V
U47
REG1117-1.2
+1.2V
OT37
R157
+1.2V FPGA (INT)
HU32_11_2_2
DRS4 Evaluation Board V4
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
POWER
Rev
0.1
Date Mai 2011
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V4.sch
Sheet 6 of 6

6. DRS4 Evaluation Board V3 Bill of Materials

Count	ComponentName	RefDes	Value	Description
1	24LC128_SN	U38		EEPROM 16k x 8
1	25LC1024SM	U26		EEPROM
1	AD8061ART	U22		Amplifier
3	AD8605ART	U18		Amplifier
	AD8605ART	U19		Amplifier
	AD8605ART	U20		Amplifier
1	AD9245	U21		ADC
4	ADCMP601	U13		Comparator
	ADCMP601	U14		Comparator
	ADCMP601	U15		Comparator
	ADCMP601	U16		Comparator
4	ADG901	U1		Wideband SPST Switches
	ADG901	U3		Wideband SPST Switches
	ADG901	U7		Wideband SPST Switches
	ADG901	U9		Wideband SPST Switches
1	ADR03	U24	2.5V	Ref.
4	BAV99	U28		Diode
	BAV99	U30		Diode
	BAV99	U32		Diode
	BAV99	U34		Diode
1	CAPP	C138	220u	Tantal, >=10V
4	CAP_0402	C51	10n	Capacitor >=10V
	CAP_0402	C52	10n	Capacitor >=10V
	CAP_0402	C55	10n	Capacitor >=10V
	CAP_0402	C56	10n	Capacitor >=10V
15	CAP_0402	C7	100n	Capacitor >=10V
	CAP_0402	C8	100n	Capacitor >=10V
	CAP_0402	C15	100n	Capacitor >=10V
	CAP_0402	C16	100n	Capacitor >=10V
	CAP_0402	C21	100n	Capacitor >=10V
	CAP_0402	C22	100n	Capacitor >=10V
	CAP_0402	C31	100n	Capacitor >=10V
	CAP_0402	C32	100n	Capacitor >=10V
	CAP_0402	C39	100n	Capacitor >=10V
	CAP_0402	C40	100n	Capacitor >=10V
	CAP_0402	C45	100n	Capacitor >=10V
	CAP_0402	C46	100n	Capacitor >=10V
	CAP_0402	C49	100n	Capacitor >=10V
	CAP_0402	C50	100n	Capacitor >=10V
	CAP_0402	C53	100n	Capacitor >=10V
5	CAP_0402	C58	100p	Capacitor >=10V
	CAP_0402	C59	100p	Capacitor >=10V
	CAP_0402	C60	100p	Capacitor >=10V
	CAP_0402	C62	100p	Capacitor >=10V
	CAP_0402	C63	100p	Capacitor >=10V
24	CAP_0402	C1	220n	Capacitor >=10V
	CAP_0402	C3	220n	Capacitor >=10V
	CAP_0402	C4	220n	Capacitor >=10V
	CAP_0402	C6	220n	Capacitor >=10V
	CAP_0402	C9	220n	Capacitor >=10V
	CAP_0402	C10	220n	Capacitor >=10V
	CAP_0402	C13	220n	Capacitor >=10V

	CAP_0402	C14	220n	Capacitor	>=10V
	CAP_0402	C25	220n	Capacitor	>=10V
	CAP_0402	C27	220n	Capacitor	>=10V
	CAP_0402	C28	220n	Capacitor	>=10V
	CAP_0402	C30	220n	Capacitor	>=10V
	CAP_0402	C33	220n	Capacitor	>=10V
	CAP_0402	C34	220n	Capacitor	>=10V
	CAP_0402	C37	220n	Capacitor	>=10V
	CAP_0402	C38	220n	Capacitor	>=10V
7	CAP_0603	C11	1u	Capacitor	>=10V
	CAP_0603	C12	1u	Capacitor	>=10V
	CAP_0603	C35	1u	Capacitor	>=10V
	CAP_0603	C36	1u	Capacitor	>=10V
	CAP_0603	C76	1u	Capacitor	>=10V
	CAP_0603	C77	1u	Capacitor	>=10V
	CAP_0603	C104	1u	Capacitor	>=10V
1	CAP_0603	C75	4.7n	Capacitor	>=10V
1	CAP_0603	C74	5.6n	Capacitor	>=10V
6	CAP_0603	C23	10n	Capacitor	>=10V
	CAP_0603	C24	10n	Capacitor	>=10V
	CAP_0603	C47	10n	Capacitor	>=10V
	CAP_0603	C48	10n	Capacitor	>=10V
	CAP_0603	C144	10n	Capacitor	>=10V
	CAP_0603	C153	10n	Capacitor	>=10V
2	CAP_0603	C133	12p	Capacitor	>=10V
	CAP_0603	C134	12p	Capacitor	>=10V
1	CAP_0603	C135	15p	Capacitor	>=10V
2	CAP_0603	C91	56p	Capacitor	>=10V
	CAP_0603	C94	56p	Capacitor	>=10V
51	CAP_0603	C54	100n	Capacitor	>=10V
	CAP_0603	C65	100n	Capacitor	>=10V
	CAP_0603	C66	100n	Capacitor	>=10V
	CAP_0603	C67	100n	Capacitor	>=10V
	CAP_0603	C69	100n	Capacitor	>=10V
	CAP_0603	C70	100n	Capacitor	>=10V
	CAP_0603	C71	100n	Capacitor	>=10V
	CAP_0603	C73	100n	Capacitor	>=10V
	CAP_0603	C78	100n	Capacitor	>=10V
	CAP_0603	C82	100n	Capacitor	>=10V
	CAP_0603	C83	100n	Capacitor	>=10V
	CAP_0603	C84	100n	Capacitor	>=10V
	CAP_0603	C85	100n	Capacitor	>=10V
	CAP_0603	C87	100n	Capacitor	>=10V
	CAP_0603	C89	100n	Capacitor	>=10V
	CAP_0603	C90	100n	Capacitor	>=10V
	CAP_0603	C92	100n	Capacitor	>=10V
	CAP_0603	C95	100n	Capacitor	>=10V
	CAP_0603	C96	100n	Capacitor	>=10V
	CAP_0603	C98	100n	Capacitor	>=10V
	CAP_0603	C100	100n	Capacitor	>=10V
	CAP_0603	C102	100n	Capacitor	>=10V
	CAP_0603	C103	100n	Capacitor	>=10V
	CAP_0603	C105	100n	Capacitor	>=10V
	CAP_0603	C106	100n	Capacitor	>=10V
	CAP_0603	C107	100n	Capacitor	>=10V
	CAP_0603	C108	100n	Capacitor	>=10V
	CAP_0603	C109	100n	Capacitor	>=10V
	CAP_0603	C110	100n	Capacitor	>=10V

	CAP_0603	C111	100n	Capacitor	>=10V
	CAP_0603	C112	100n	Capacitor	>=10V
	CAP_0603	C113	100n	Capacitor	>=10V
	CAP_0603	C114	100n	Capacitor	>=10V
	CAP_0603	C115	100n	Capacitor	>=10V
	CAP_0603	C116	100n	Capacitor	>=10V
	CAP_0603	C117	100n	Capacitor	>=10V
	CAP_0603	C118	100n	Capacitor	>=10V
	CAP_0603	C119	100n	Capacitor	>=10V
	CAP_0603	C120	100n	Capacitor	>=10V
	CAP_0603	C121	100n	Capacitor	>=10V
	CAP_0603	C124	100n	Capacitor	>=10V
	CAP_0603	C125	100n	Capacitor	>=10V
	CAP_0603	C126	100n	Capacitor	>=10V
	CAP_0603	C127	100n	Capacitor	>=10V
	CAP_0603	C128	100n	Capacitor	>=10V
	CAP_0603	C129	100n	Capacitor	>=10V
	CAP_0603	C130	100n	Capacitor	>=10V
	CAP_0603	C132	100n	Capacitor	>=10V
	CAP_0603	C137	100n	Capacitor	>=10V
	CAP_0603	C147	100n	Capacitor	>=10V
	CAP_0603	C150	100n	Capacitor	>=10V
1	CAP_0603	C143	100p	Capacitor	>=10V
14	CAP_0805	C79	4.7u	Capacitor	>=10V
	CAP_0805	C86	4.7u	Capacitor	>=10V
	CAP_0805	C93	4.7u	Capacitor	>=10V
	CAP_0805	C99	4.7u	Capacitor	>=10V
	CAP_0805	C101	4.7u	Capacitor	>=10V
	CAP_0805	C140	4.7u	Capacitor	>=10V
	CAP_0805	C145	4.7u	Capacitor	>=10V
	CAP_0805	C146	4.7u	Capacitor	>=10V
	CAP_0805	C148	4.7u	Capacitor	>=10V
	CAP_0805	C149	4.7u	Capacitor	>=10V
	CAP_0805	C151	4.7u	Capacitor	>=10V
	CAP_0805	C152	4.7u	Capacitor	>=10V
	CAP_0805	C154	4.7u	Capacitor	>=10V
	CAP_0805	C156	4.7u	Capacitor	>=10V
16	CAP_1206	C17	10u	Capacitor	>=10V
	CAP_1206	C18	10u	Capacitor	>=10V
	CAP_1206	C41	10u	Capacitor	>=10V
	CAP_1206	C42	10u	Capacitor	>=10V
	CAP_1206	C64	10u	Capacitor	>=10V
	CAP_1206	C68	10u	Capacitor	>=10V
	CAP_1206	C72	10u	Capacitor	>=10V
	CAP_1206	C80	10u	Capacitor	>=10V
	CAP_1206	C81	10u	Capacitor	>=10V
	CAP_1206	C88	10u	Capacitor	>=10V
	CAP_1206	C97	10u	Capacitor	>=10V
	CAP_1206	C122	10u	Capacitor	>=10V
	CAP_1206	C123	10u	Capacitor	>=10V
	CAP_1206	C136	10u	Capacitor	>=10V
	CAP_1206	C141	10u	Capacitor	>=10V
	CAP_1206	C155	10u	Capacitor	>=10V
1	CAP_1206	C139	22u	Capacitor	>=10V
1	CAP_1206	C131	100n	Capacitor	>=10V
1	CAP_1210	C142	47u	Capacitor	>=10V
2	CAP_1210	C57	100u	Capacitor	>=10V
	CAP_1210	C61	100u	Capacitor	>=10V

1	CONN_MOLEX_JTAG_FPGA	J45	JTAG	
1	CY7C68013-56	U37		Microcontroller
1	DRS4_76	U17		DRS4
8	IND_0603	L1		
	IND_0603	L2		
	IND_0603	L3	220nH	Inductor
	IND_0603	L4	220nH	Inductor
	IND_0603	L5	220nH	Inductor
	IND_0603	L6	220nH	Inductor
	IND_0603	L7	220nH	Inductor
	IND_0603	L8	220nH	Inductor
1	IND_1008	L11	10u	Inductor
2	IND_1812	L9	10u	Inductor
	IND_1812	L10	10u	Inductor
2	JMP2MM	JP1	~WP	Jumper
	JMP2MM	JP2	~WP	Jumper
1	LED_PLCC-4	U39		HSMN-A400-S8PM2
1	LED_PLCC-4	U40	green	HSMM-A400-U4QM2
1	LED_PLCC-4	U41	yellow	HSMA-A401-U45M1
1	LMZ10503	U43		Power Module 3A
1	LP2985-2.5	U45		150mA Low Dropout
1	LP2985-3.3	U44		150mA Low Dropout
1	LTC2600	U23		DAC
1	MAX6662	U25		Temp. Sensor
4	MMCX-90	J18		
	MMCX-90	J30		
	MMCX-90	J39		
	MMCX-90	J41		
1	QUARZ_NKS7	Q1	24MHz	24MHz, MQ/30/30/40/12pf
4	RCLAMP0502B	U5		ESD Protection
	RCLAMP0502B	U6		ESD Protection
	RCLAMP0502B	U11		ESD Protection
	RCLAMP0502B	U12		ESD Protection
1	REG1117-1.2	U47		REG 1117A Low Dropout
19	RES_0402	R1	0E	Resistor
	RES_0402	R3	0E	Resistor
	RES_0402	R37	0E	Resistor
	RES_0402	R38	0E	Resistor
	RES_0402	R41	0E	Resistor
	RES_0402	R43	0E	Resistor
	RES_0402	R77	0E	Resistor
	RES_0402	R78	0E	Resistor
	RES_0402	R99	0E	Resistor
	RES_0402	R100	0E	Resistor
	RES_0402	R101	0E	Resistor
	RES_0402	R102	0E	Resistor
	RES_0402	R103	0E	Resistor
	RES_0402	R104	0E	Resistor
	RES_0402	R105	0E	Resistor
	RES_0402	R106	0E	Resistor
	RES_0402	R146	0E	Resistor
	RES_0402	R147	0E	Resistor
	RES_0402	R148	0E	Resistor
8	RES_0402	R11	15E	Resistor
	RES_0402	R12	15E	Resistor
	RES_0402	R19	15E	Resistor
	RES_0402	R20	15E	Resistor
	RES_0402	R51	15E	Resistor

	RES_0402	R52	15E	Resistor
	RES_0402	R59	15E	Resistor
	RES_0402	R60	15E	Resistor
16	RES_0402	R29	22E	Resistor
	RES_0402	R30	22E	Resistor
	RES_0402	R31	22E	Resistor
	RES_0402	R32	22E	Resistor
	RES_0402	R33	22E	Resistor
	RES_0402	R34	22E	Resistor
	RES_0402	R35	22E	Resistor
	RES_0402	R36	22E	Resistor
	RES_0402	R69	22E	Resistor
	RES_0402	R70	22E	Resistor
	RES_0402	R71	22E	Resistor
	RES_0402	R72	22E	Resistor
	RES_0402	R73	22E	Resistor
	RES_0402	R74	22E	Resistor
	RES_0402	R75	22E	Resistor
	RES_0402	R76	22E	Resistor
4	RES_0402	R5	49.9E	Resistor
	RES_0402	R8	49.9E	Resistor
	RES_0402	R45	49.9E	Resistor
	RES_0402	R48	49.9E	Resistor
8	RES_0402	R7	61.9E	Resistor
	RES_0402	R10	61.9E	Resistor
	RES_0402	R24	61.9E	Resistor
	RES_0402	R28	61.9E	Resistor
	RES_0402	R47	61.9E	Resistor
	RES_0402	R50	61.9E	Resistor
	RES_0402	R64	61.9E	Resistor
	RES_0402	R68	61.9E	Resistor
8	RES_0402	R6	64.9E	Resistor
	RES_0402	R9	64.9E	Resistor
	RES_0402	R23	64.9E	Resistor
	RES_0402	R27	64.9E	Resistor
	RES_0402	R46	64.9E	Resistor
	RES_0402	R49	64.9E	Resistor
	RES_0402	R63	64.9E	Resistor
	RES_0402	R67	64.9E	Resistor
8	RES_0402	R13	169E	Resistor
	RES_0402	R14	169E	Resistor
	RES_0402	R16	169E	Resistor
	RES_0402	R18	169E	Resistor
	RES_0402	R53	169E	Resistor
	RES_0402	R54	169E	Resistor
	RES_0402	R56	169E	Resistor
	RES_0402	R58	169E	Resistor
8	RES_0402	R2	348E	Resistor
	RES_0402	R4	348E	Resistor
	RES_0402	R39	348E	Resistor
	RES_0402	R40	348E	Resistor
	RES_0402	R42	348E	Resistor
	RES_0402	R44	348E	Resistor
	RES_0402	R79	348E	Resistor
	RES_0402	R80	348E	Resistor
3	RES_0402	R83	390k	Resistor
	RES_0402	R84	390k	Resistor
	RES_0402	R86	390k	Resistor

13	RES_0603	R81	0E	Resistor
	RES_0603	R82	0E	Resistor
	RES_0603	R85	0E	Resistor
	RES_0603	R91	0E	Resistor
	RES_0603	R118	0E	Resistor
	RES_0603	R119	0E	Resistor
	RES_0603	R123	0E	Resistor
	RES_0603	R124	0E	Resistor
	RES_0603	R127	0E	Resistor
	RES_0603	R128	0E	Resistor
	RES_0603	R131	0E	Resistor
	RES_0603	R132	0E	Resistor
	RES_0603	R149	0E	Resistor
6	RES_0603	R94	1k	Resistor
	RES_0603	R95	1k	Resistor
	RES_0603	R97	1k	Resistor
	RES_0603	R117	1k	Resistor
	RES_0603	R143	1k	Resistor
	RES_0603	R155	1k	Resistor
4	RES_0603	R15	1.5E	Resistor
	RES_0603	R17	1.5E	Resistor
	RES_0603	R55	1.5E	Resistor
	RES_0603	R57	1.5E	Resistor
1	RES_0603	R114	2k4	Resistor
2	RES_0603	R139	2.2k	Resistor
	RES_0603	R140	2.2k	Resistor
8	RES_0603	R21	3.6k	Resistor
	RES_0603	R22	3.6k	Resistor
	RES_0603	R25	3.6k	Resistor
	RES_0603	R26	3.6k	Resistor
	RES_0603	R61	3.6k	Resistor
	RES_0603	R62	3.6k	Resistor
	RES_0603	R65	3.6k	Resistor
	RES_0603	R66	3.6k	Resistor
3	RES_0603	R151	4k7	Resistor
	RES_0603	R152	4k7	Resistor
	RES_0603	R153	4k7	Resistor
1	RES_0603	R142	4k7	Resistor
4	RES_0603	R108	4.7E	Resistor
	RES_0603	R109	4.7E	Resistor
	RES_0603	R111	4.7E	Resistor
	RES_0603	R115	4.7E	Resistor
1	RES_0603	R116	10E	Resistor
3	RES_0603	R120	10k	Resistor
	RES_0603	R133	10k	Resistor
	RES_0603	R150	10k	Resistor
2	RES_0603	R110	22E	Resistor
	RES_0603	R112	22E	Resistor
1	RES_0603	R156	23.7k	Resistor
1	RES_0603	R141	49.9E	Resistor
1	RES_0603	R154	75k	Resistor
3	RES_0603	R90	100E	Resistor
	RES_0603	R98	100E	Resistor
	RES_0603	R113	100E	Resistor
2	RES_0603	R137	100k	Resistor
	RES_0603	R138	100k	Resistor
1	RES_0603	R92	130E	Resistor
2	RES_0603	R144	220E	Resistor

	RES_0603	R145	220E	Resistor
1	RES_0603	R87	390k	Resistor
2	RES_0805	R88	0E	Resistor
	RES_0805	R89	0E	Resistor
3	RES_0805	R93	0E	Resistor
	RES_0805	R107	0E	Resistor
	RES_0805	R136	0E	Resistor
1	RES_0805	R96	1k	Resistor
8	RES_1206	R121	51E	Resistor
	RES_1206	R122	51E	Resistor
	RES_1206	R125	51E	Resistor
	RES_1206	R126	51E	Resistor
	RES_1206	R129	51E	Resistor
	RES_1206	R130	51E	Resistor
	RES_1206	R134	51E	Resistor
	RES_1206	R135	51E	Resistor
1	RES_1206	R157	120E	Resistor
4	SMA_SMD_S	J1		SMA Connector
	SMA_SMD_S	J2		SMA Connector
	SMA_SMD_S	J4		SMA Connector
	SMA_SMD_S	J5		SMA Connector
4	SN74LVC1T45DB	U27	Transceiver	Bus Transceiver
	SN74LVC1T45DB	U29	Transceiver	Bus Transceiver
	SN74LVC1T45DB	U31	Transceiver	Bus Transceiver
	SN74LVC1T45DB	U33	Transceiver	Bus Transceiver
4	THS4508	U2		Amplifier
	THS4508	U4		Amplifier
	THS4508	U8		Amplifier
	THS4508	U10		Amplifier
1	TPS79625	U46		Low Dropout
1	USB_CONN_B	U35		
1	VX3	Q2	66MHz	Oszillator VX3, 3.3V
1	XC3S400-TQ144	U36		FPGA
1	XCF02S-V020	U42		EEPROM