NA61 Readout Upgrade Using the DRS Digitizer

Alessandro Bravar
University of Geneva

Abstract

A proposal to replace aging NA61 readout electronics using the DRS digitizer is presented. This upgrade is motivated by the overall poor stability and reliability of the NA61 Time of Flight system electronics (discriminators, TDCs, and ADCs). The readout of other sub-systems (BPD, PSD, trigger) can be upgraded using the same DRS electronics yielding to an improved performance of these systems. This upgrade will add multi-hit capabilities to the ToF, which at present are missing, and timing information to the BPDs and the PSD.

Contents

1 Motivation

The NA61 readout electronics was inherited from the NA49 experiment. In particular, the readout of the Time of Flight (ToF) systems is based on FASTBUS TDC and ADC modules, while the readout of the beam detectors and trigger counters is based on CAMAC modules. Both systems are interfaced to the central NA61 DAQ via VME micro-controllers. This system, consisting of elements produced by various manufacturers, is obsolete, difficult to operate reliably and maintain. Moreover due to aging it shows a rising falling rate of its components, which cannot be replaced or fixed.

A major upgrade of the TPC readout was undertaken in 2008, rendering this system much more stable and reliable. It allows us to read the TPCs at a rate close to 100 Hz (10 fold improvement w.r.t. NA49). In 2009 the trigger system was replaced with an FPGA based logic allowing for simultaneous multi-trigger data taking.

The most critical element for the successful operation of the NA61 experiment is the readout of the ToF systems (ToF-L/R and ToF-F), which must be replaced before the next NA61 data taking period planned for the fall of 2014. The ToF systems consist of about 2000 photomultipliers coupled to fast plastic scintillators. Fast analog signals from the ToF PMTs are split in two parts before being fed into the readout electronics. One signal is fed into constant fraction discriminators (CFD) followed by FASTBUS TDC modules for time measurement. The other part of the analog signals is fed in FASTBUS ADC modules for energy measurement. The time resolution of the ToF-L/R system is about 60 ns and that of the ToF-F about 110 ns. Replacing this readout electronics (i.e. CFDs, TDCs, and ADCs) with commercially available modules would represent a prohibitive cost for NA61 (estimated around 1k CHF per channel for a total of about 2M CHF).

At the same time it would be also desirable to replace the CAMAC readout system of the trigger beam counters and BPDs with more modern and reliable electronics. The performance of the PSD could be further improved with an upgrade of the PSD readout electronics.

After carefully examining various possibilities, NA61 decided to replace the ToF readout system (CFDs, TDCs, and ADCs) with custom made electronics based on the use of well-established waveform digitizing technology [1]. All operations (CFD, optimal filtering, integration, etc.) can be done digitally. The advantage of this technology compared to traditional constant fraction discrimination and TDCs is that pile-up can be effectively recognized and corrected for. Moreover it could offer equivalent or better timing performance compared to the traditional approaches [2, 3]. In addition pulse height information becomes available (no need for additional ADC channels), which can be used to discriminate signals.

2 Overview

The chosen waveform digitizing technology is based on the switched capacitor array chip, the Domino Ring Sampler (DRS) digitizer developed at PSI [1]. The DRS has been designed for maximum flexibility and use in many different applications, in particular for very fast analog signals from photomultipliers and photodiodes. For the sake of completeness let me mention that several chips with similar have been developed by other groups [4, 5]. These chips are targeted for specific application. One of the main reason for choosing the DRS chip is the proximity with PSI and the involvement of UniGE in the Mu3e experiment, which will heavily rely on the DRS chip for the readout of the time of flight system (SciFi

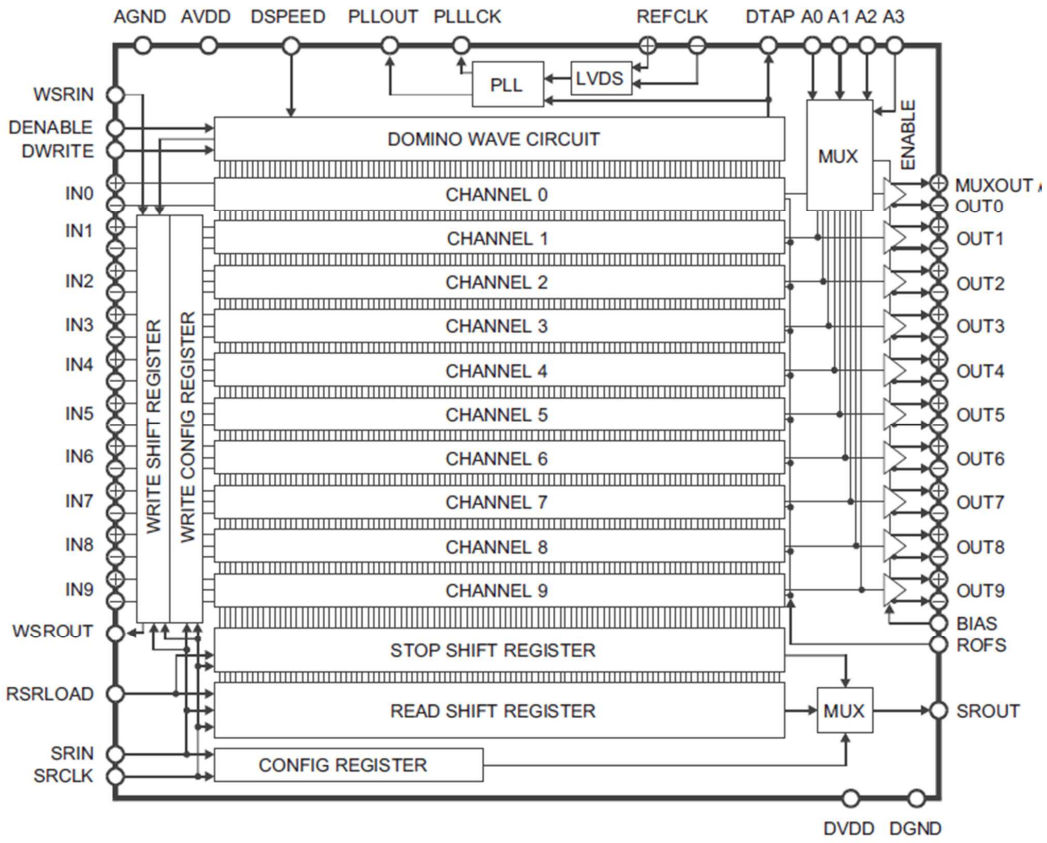

Figure 1: Functional block diagram of the DRS4 chip.

tracker and scintillating tiles).

The DRS4 chip is based on a circular switched capacitor array, consisting of an array of 1024 capacitors per channe (see figure 1), and samples input analog signals at a rate up to 5 GHz with a resolution close to 12 bits and a 200 ns deep circular buffer. Each chip comprises 8 independent channels. The signals are then digitized with commercial ADCs at a much lower rate (around 50 MHz). In other words, the DRS is a *waveform stretcher* ADC running at a very high sampling rate, which allows one to extract both the time and charge information from the recorded waveforms. The DRS combines in a single element the functions of a CFD, TDC, and ADC. The whole system is controlled by FPGAs, which also control the calibration of the system.

The use of the DRS digitizer will allow us to match the timing requirements of the NA61 ToF systems (intrinsic time resolution better than 25 ps) offering excellent performance at an estimated cost of 100 CHF per channel. Moreover, it will add multi-hit capabilities to the ToF systems. Indeed, during the 2009 run the ToF-F suffered from pileup in the central region (at the level of few %) because of high beam intensities.

The DRS readout will be interfaced to the central NA61 DAQ using the DDL link [6] already used for the readout of the TPCs. This should facilitate the inclusion of the DRS in the DAQ. It is expected that it will have moderate impact on the overall functioning of the NA61 DAQ.

The same electronics developed for replacing the ToF readout is very flexible and can be used to upgrade the readout of other sub-systems (BPDs, PSD, trigger) at an incremental cost proportional to

the number of channels only.

In the following each sub-system is briefly examined one at a time.

ToF

As discussed above, the ToF system consist of about 2000 channels. Typical rise times of the analog signals from the ToF PMTs are around 2 to 3 ns. Each channel will be digitized at the highest sampling frequency of 5 GHz, which is adequate for this kind of signals. No particular conditioning of the signals from the ToF PMTs is required. The DRS will replace obsolete CFD, TDC, and ADC modules.

Beam Counters and Trigger

Presently the beam counters are read out with CAMAC ADCs and the time information is recorded only for few channels. All beam counters will be read out like the ToF elements with the DRS sampling the signals from the PMTs at the highest sampling frequency of 5 GHz. Moreover to monitor the beam activity in a wide window of ± 4 μs around the trigger time, the same signals will be sampled at a lower frequency of 500 MHz and 4 consecutive DRS channels will be cascaded to increase the buffer depth of the sampled waveform to 8 μs. This will allow us to reject events with beam particles too close to each other.

Commercial VME electronics will be used to replace the CAMAC scalers and registers used to monitor the functioning of the trigger.

BPDs

The BPDs are proportional chambers with cathode strip readout. They generate *charge* signals that with proper conditioning, much slower (FWHM around 120 ns) compared to those from the ToF PMTs. Therefore there is no need to run the DRS at the highest possible sampling frequency, and a sampling rate of 500 MHz is appropriate, giving a buffer depth of 2 μs for the digitized signals. To monitor the beam activity around the trigger time over a wider window of ± 4 μs as for the beam counters 4 consecutive DRS channels will be cascaded. The signals from the BPD FE amplifiers can be fed directly into the DRS without additional conditioning. The new readout electronics will add the timing information to the reconstructed beam tracks, with a resolution sufficient to reconstruct correctly and separate multiple beam tracks when NA61 is taking data at high beam intensities. At present this feature is missing.

As a side benefit, the upgrade of the BPDs readout and of the beam counters would allow us to remove completely all CAMAC electronics from the NA61 DAQ chain.

PSD

The PSD is the most recent detector that has been added to NA61 in 2010. Reading out the PSD with the DRS electronics would allow us to analyze the waveforms of the signals generated by the calorimeter Si-PMs, thus improving its performance. In particular we would add the timing information which is at present missing without degrading the energy measurements. Given that the analog signals are not that fast for this detector, we envisage to run the DRS at a lower sampling frequency of 1 GHz. The signals will be thus sampled over a window of ± 500 ns around the trigger time. To monitor the beam activity

sub-system	# of ch.	# DRS ch.	# DRS boards	sampling frequency (MHz)	buffer depth (ns)
ToF-R	891	891	56	5000	200
ToF-L	891	891	56	5000	200
ToF-F	160	160	10	5000	200
beam	16	16	1	5000	200
	16	64	4	500	8000
BPD	144	576	36	500	8000
PSD	440	440	28	1000	400
	16	64	4	500	8000

Table 1: Number of DRS readout channels required for each sub-system, including the sampling frequencies and acquisition windows for each sub-system. Each DRS boards comprises 2 DRS4 chips and has 16 channels.

around the trigger time also with this detector, the central part of the calorimeter will be also sampled at lower frequency of 500 MHz cascading 4 consecutive DRS channels as for the BPDs and beam counters. In the case of the PSD, however, the FE electronics needs to be rebuilt.

Table 1 summarizes the number of DRS channels required for the upgrade of the NA61 readout. It also shows the various sampling frequencies at which the DRS will be operated and the corresponding acquisition windows for each sub-system. Around 500 DRS4 chips, including spares, will be required to upgrade the NA61 readout.

3 Conceptual Design

Figure 2 illustrates the modular design of the DRS readout electronics. It consists of the major parts: the DRS mezzanine boards with 2 DRS4 digitizer chips, the motherboards which host 4 DRS mezzanine boards, and the data concentrator (DC) box which receives the data from the DRS motherboards and sends them to the central DAQ via the DDL link. This modularity increases the flexibility of the system at a very limited cost increment and also allows us to divide the project in various tasks carried out by different groups. In particular UniGE will develop the DRS boards while KFKI-Budapest will develop the DRS motherboards. The DC and DDL links are already used in NA61 for the readout of the TPC.

The DRS boards are connected to the DRS motherboards via 2 high frequency high density multipin connector. The analog input signals are actually received on the motherboards and fed to the DRS board via one of the above connectors. Each DRS boards contains 2 DRS chips and can digitize up to 16 input signals. Each single ended input signal is first conditioned with a differential amplifier (THS4508) before being fed into the DRS4 chips. During calibration of the DRS4, each circuit can be decoupled from the input with a GHz switch. Each DRS4 chip is read out by an 8 channel 12 bit ADC (AD9222) running at 33 MHz. The digital data are fed into a Spartan6 or a Kintex7 FPGA from Xilinx. One FPGA is used for both DRS4 chips and ADCs. The DRS board comprises also memory chips to store the calibration data and several full events. UniGE will fully develop the DRS boards.

The FPGA synchronizes the readout of the DRS4 with the ADC, distributes triggers and control signals to the DRS4, oversees the calibration of the DRS4 chip, and transfers the digital data from the

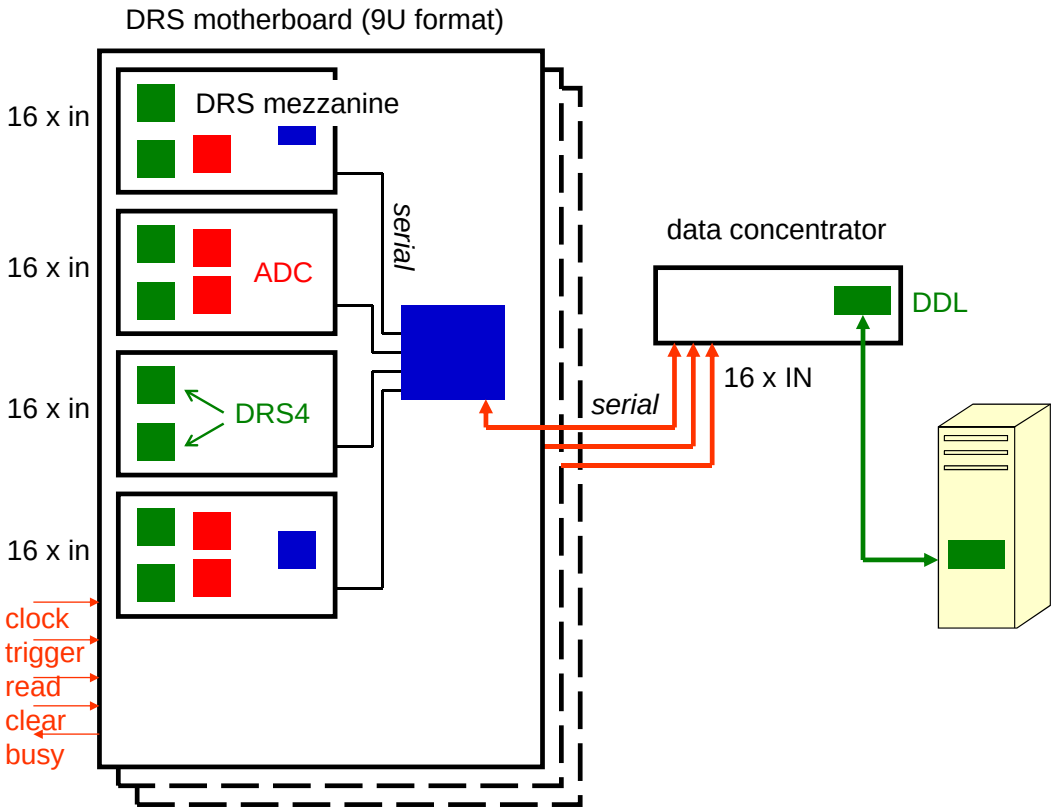

Figure 2: Layout of the DRS readout system.

ADCs to the motherboard through a serial link using the second multipin connector mentioned above. Before transferring the data, however, the zero suppression is performed using calibration data stored in an on board memory and only interesting segments of the waveforms are actually transfered in order to reduce the amount of the data. UniGE will also develop the firmware which controls the functioning of the DRS board and transfers the data, while the part relative to the waveform processing will be developed by USA groups ? under the supervision of a UniGE physicist.

Each motherboard hosts up to 4 DRS boards. In addition to receiving the data from the DRS mezzanine boards and sending them to the DC box via a 1 Gb serial link, the DRS motherboard receives clock and trigger signals an distributes them the DRS boards, it comprises also a USB microcontroller for communication and data transfer independently of the main NA61 DAQ system. Each input analog signal is split on the DRS motherboard and also sent to a comparator, which allows one to trigger the system on a single channel basis. The DRS motherboards and firmware will be developed by KFKI-Budapest in close collaboration with UniGE. ??? will develop the part relative to the USB readout and single channel triggering.

The DC boxes and DDL links are already used for the readout of the NA61 TPCs and were developed by KFKI-Budapest. Each DC box can receive data from up to 32 DRS motherboards via 1 Gbit serial links. KFKI-Budapest will modify the DC boxes firmware for use with the DRS boards.

component	# of boards	cost (1 pc.)	cost (total)
DRS mezzanine	200	1000	200k CHF
DRS motherboard	50	1500	75k CHF
DC and DDL links	5	5000	25k CHF
crates and PS	5	4000	20k CHF
cabling			30k CHF
total			350k CHF

Table 2: Estimated cost of major components for 3200 channels in CHF.

4 Implementation Plan

5 Implications for DAQ

6 Implications for the Offline Analysis

7 Costing

The current cost estimate is of about 100 CHF per channel, for a total of about 350k CHF (3500 channels). That includes the DRS boards and the DRS motherboards including 20 % spare channels, the data concentrators and DDL links, crates and power supplies, cables, etc. Table 2 summarizes the estimated cost of major components, while table 3 lists the prices of major electronics components (chips).

component	part	# of parts	cost (1 pc.)	cost (total)
digitizer	DRS4	400	57.5	23000
ADC	AD9222	400	47.5	19000
amplifier	THS4508	3200	5.7	18240
Xilinx FPGA	XC6LTX100T	200	165.0	33000
Xilinx FPGA	XC6LTX45T	50	75.0	3750
flash memory	XCF04S	250		
RAM memory		500		
clock conditioner	LMK03000	200	11.0	2200
DAC	LTC2600	800	15.0	12000
microcontroller	CY7C68013	50		
PCB DRS		200	150.0	30000
PCB DRS M		50	500.0	25000

Table 3: List of some major components and prices for 3200 channels in CHF (1 euro = 1.25 CHF, 1 $ = 1 CHF).

The cost will be covered by UniGE (150k CHF), US groups (150k CHF) and NA61 common fund (50k CHF). An additional 20k CHF are required for the development of this readout system. This additional cost will be covered by UniGE from other funds.

8 Available Resources

9 Schedule and Milestones

In this section the plan for developing and implementing the DRS upgrade is presented. The schedule and various milestones are outlined in table 4. It also presents the plan for the DAQ, offline, and online software modifications to cope with the new system. A review of the whole project by external experts is planned by the end of the Summer 2013, when also NA61 will take the formal decision concerning this upgrade. Construction will start soon after. The aim is to have the new system fully deployed and debugged by the end of Summer 2014, before the restart of SPS operation and beams in the North Area planned for Q4 2014.

10 DRS Performance Test Results

11 Backup Plan

References

[1] S. Ritt, R. Dinapoli, and U. Hartmann. Application of the DRS chip for fast waveform digitizing. *Nucl.Instrum.Meth.*, A623:486, 2010.

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[5] E. Delagnes et al. *Nucl.Instrum.Meth.*, A567:21, 2006.

[6] DDL .....

December 2012	**study DRS performance**, in particular the time resolution complete specifications (incl. detector interfaces and cabling) start building first prototype (full chain: DRS → DDL → PC) → Q2 2013 full implementation plan explore implications for DAQ explore implications for analysis **full proposal**
June 2013	complete first prototype (full chain: DRS → DDL → PC) debug prototype(s) → Q4 2013 finalize design develop basic firmware (data transfer, DRS and ADC controls, calibrations) start developing data encoding and filtering (firmware) → Q3 2014 start developing real time calibration algorithms → Q3 2014 start developing waveform analysis (offline) → Q3 2014 start developing online monitoring → Q3 2014 plan DAQ modifications
June 2013	**external review**
December 2013	**NA61 final decision** **full funding available** complete DRS boards debugging and design full working system with several DDL links basic (complete) firmware ready **ready for mass production** all components in hand start DAQ implementation → Q3 2014 start preparing for installation
June 2014	all DRS boards procured all DRS boards tested complete preparations for installation backward compatibility basic DAQ ready basic online monitoring ready
September 2014	system fully installed **system fully operational and debugged w/o beam** DAQ ready analysis (offline) ready online monitoring ready
October 2014	**system fully debugged w/ beam** **ready for physics**

Table 4: Schedule and milestones. The various milestones are in bold. The various tasks are expected to be completed by the end of the indicated month.